Data Converter Fundamentals

- Fundamental aspects are discussed only
  - without regard for the internal architecture or circuit design
  - converters are treated as black boxes
  - input-output relationships
  - two main types of data converters, Nyquist-rate and oversampling
- Nyquist-rate converters
  - Nyquist-rate analog-to-digital converters (ADCs)

    Nyquist-rate digital-to analog converters (DACs)
  - seldom used at Nyquist-rate due to the difficult in realizing practical anti-aliasing and reconstruction filters.

    In most cases, Nyquist-rate converters operate at 1.5 to 10 times the Nyquist rate (i.e,3 to 20 times the input signal's bandwidth).

Data Converter Fundamentals (Cont.)

- Oversampling converter
  - oversampling ADCs and

    oversampling DACs
  - operate much faster than the input signal's Nyquist rate (typical 8 to 512 times faster)
  - Noise shaping is used to place much of the quantizaition noise outside the input signal's bandwidth
  - increase the output's signal-to-noise ratio(SNR) by filtering out quantization noise that is not in the signal bandwidth .

    In A/D converters, this filtering is performed digitally, whereas in D/A converters, analog filtering is used.

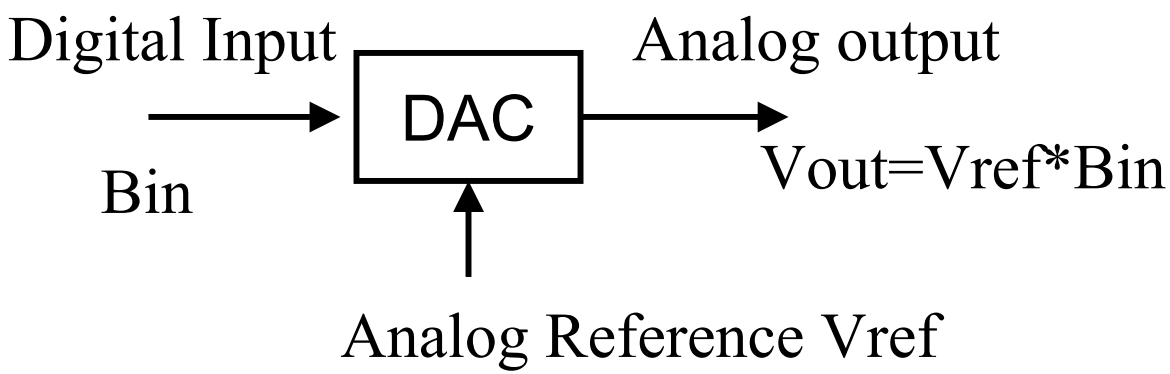
Idea D/A Converter

- Ideal N-bit DAC
  - digital input Bin=$b_1 2^{-1} + b_2 2^{-2} + \cdots + b_N 2^{-N}$

    where b_i is 1 or 0,i.e. binary

    b_1 is most significant bit (MSB)

    b_N is the last significant bit (LSB)



Ideal D/A Converter (Cont.)

1. A unipolar DAC produces an output signal of only one polarity.
2. A signed (or bipolar) DAC produce an output signal of either positive or negative polarity, depending on a sign bit, usually b1.
3. Other digital (or analog) representation may be used (e.g. sign magnitude, offset binary, or 2's complement, ...etc.)
4. We assumed here that DAC is unipolar (for simplicity).

Ideal D/A Converter (Cont.)

– Analog output, Vout, is related to Bin through an analog reference, Vref.

1. Vout and Vref may be voltage, current, or charge.
2. We assume here that they are voltage (for simplicity)
3. definitions:

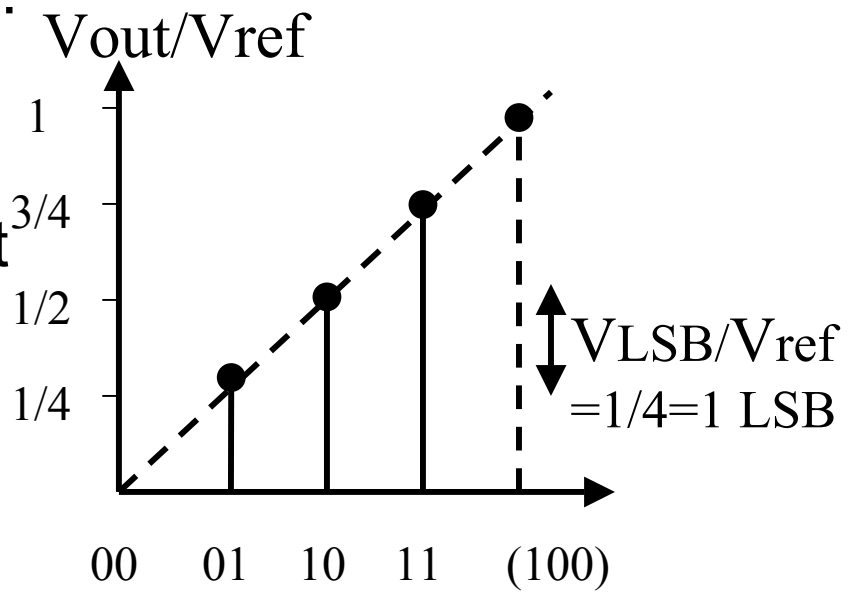
   Vout =Vref($b_1 2^{-1} + b_2 2^{-2} + \cdots + b_N 2^{-N}$)=Vref*Bin

   V_{LSB}=Vref/2^N where V_{LSB} is defined as the voltage changes when one LSB changes

   1LSB= $1/2^N$ unitless definition

Ideal D/A Converter (Cont.)

4. An ideal 2-bit DAC example:
   Input-output transfer curve.
   In general, the maximum value of Vout is not Vref but rather Vref(1- 2^{-N}), or equivalently, Vref-VLSB.



5. A multiplying DAC(MDAC) is realized by simply allowing the reference signal, Vref, to be a varying input signal along with Bin. Such an arrangement results in Vout being proportional to the multiplication of the input signals, Bin and Vref.

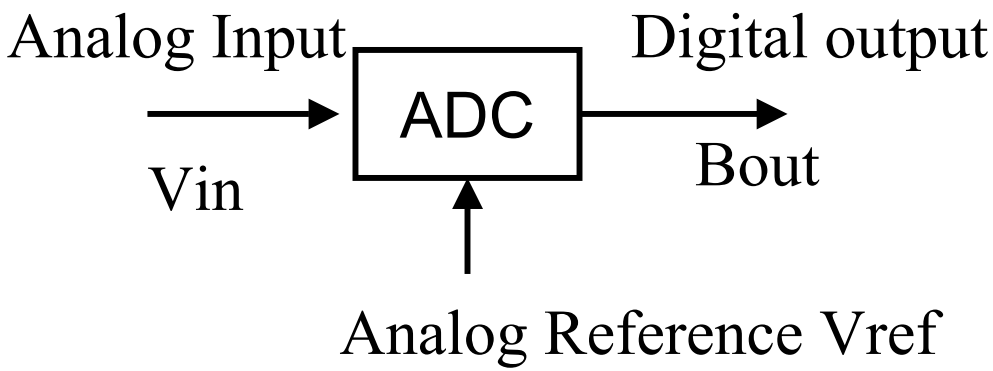
Ideal A/D Converter

- Ideal N-bit ADC
  - relations between external signals

$$Vref(b1*2^{-1}+b2*2^{-2}+.....+bN*2^{-N})=Vin \pm Vx$$

where $b1*2^{-1}+b2*2^{-2}+.....+bN*2^{-N}$=Bout is the digital output. Vin and Vref are the analog input and analog reference signals. Vx is quantization error and

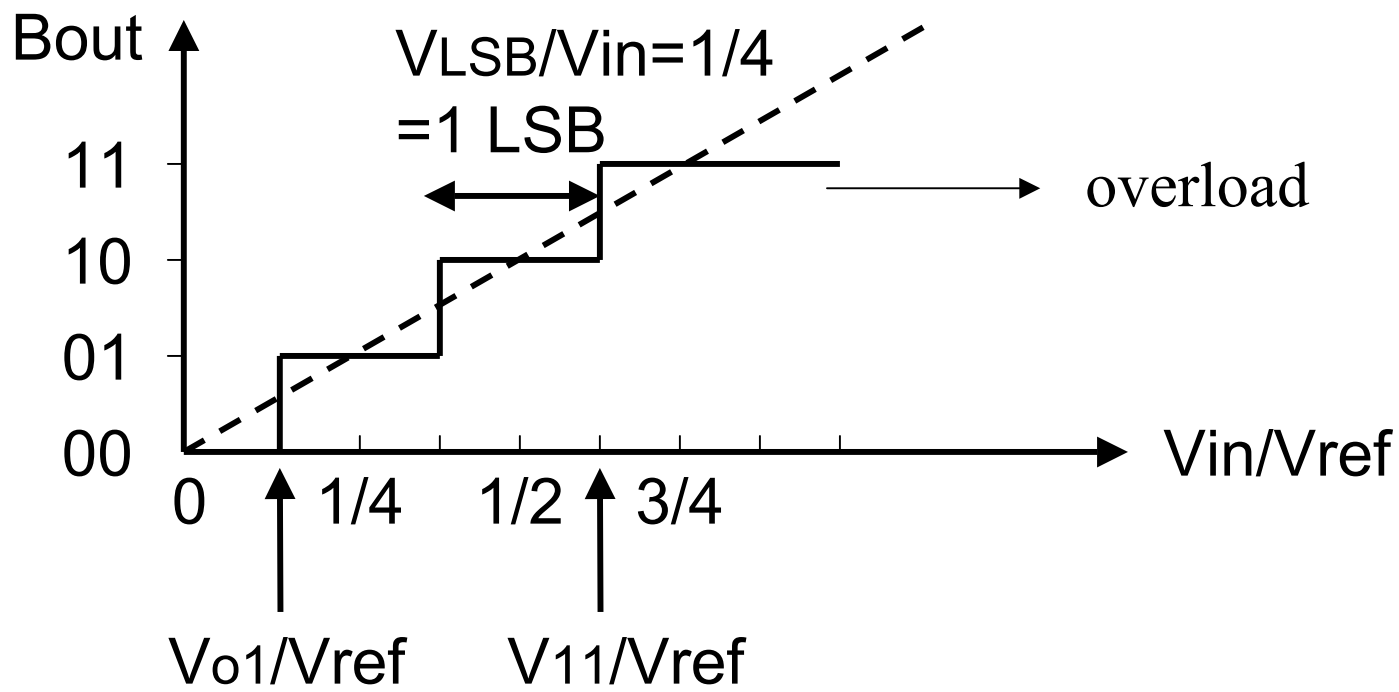
$-1/2V_{LSB} \leq V_X \leq 1/2V_{LSB}$



Ideal A/D Converter (Cont.)

– Input-output transfer curve of an ideal 2-bit ADC

1. Transitions along the Vin axis are offset by 1/2V_{LSB} so that the midpoints of the staircase curve fall precisely on the equivalent D/A transfer curve.



Ideal A/D Converter (Cont.)

2. Transition voltages at Vij where the subscript ij indicates the upper Bout value of the transition, e.g. V_{01} is the transition from 00 to 01.
3. The above equation holds only if Vin remains within 1LSB of the two last transition voltages. i.e. in this

   2-bit example -1/8<Vin<7/8Vref.

   Otherwise, the quantizer is said to be overloaded since the magnitude of the quantization error would be larger than 1/2LSB.

Quantization Error in Ideal ADCs and DACs

- Ideal ADC

  in the range of [-1/2LSB,1/2LSB].
- Ideal DAC
  - N-bit input for N-bit DAC

    No quantization error occurs
  - M-bit input for N-bit DAC(N>M)

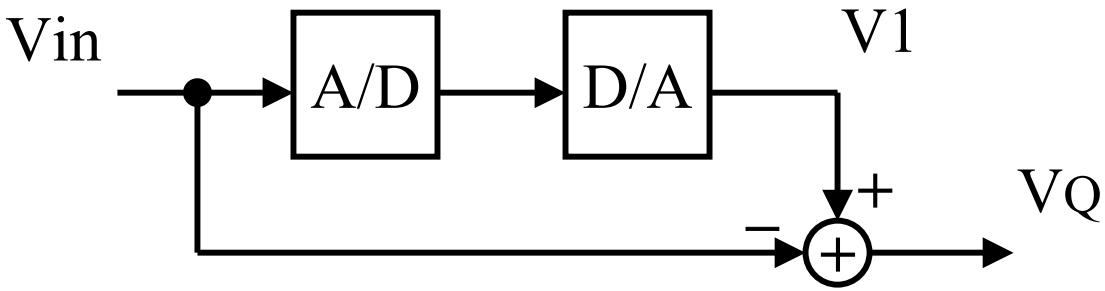
    No quatization error
  - M-bit input for N-bit DAC(N<M)

    in the range of [-(1-1/2^{M-N})LSB, (1-1/2^{M-N})LSB]

    Quantization errors occurs in the conversion from a M-bit digital to a N-bit digital signal.

Quantization Noise in Ideal ADCs

- Circuit to investigate quantization noise behavior:



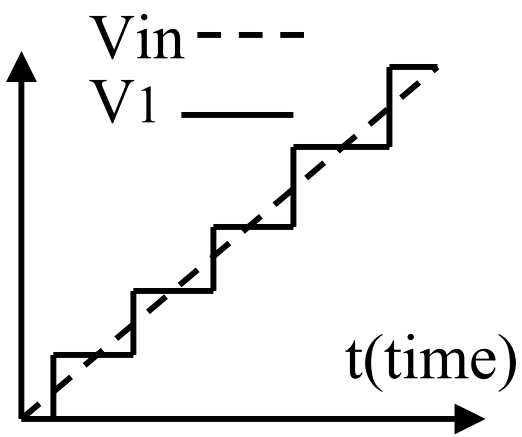
$V_Q = V1 - Vin$

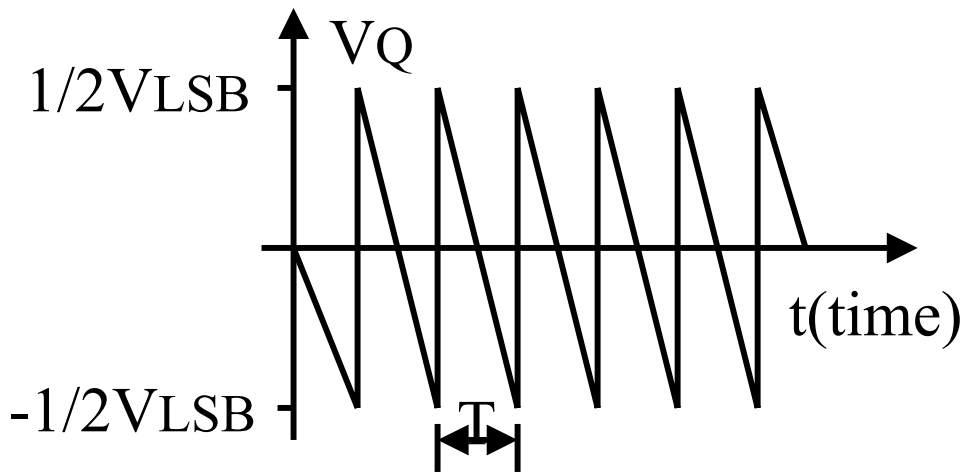
or $V1 = Vin + V_Q$

⇨ Quantization noise can be modeled as the input signal, Vin, plus some additional quantization noise signal, V_Q .

Quantization Noise in Ideal ADCs (Cont.)

- Calculation of quantization noise
  - deterministic approach
    1. assume the Vin is an ramp and such an input signal results in the output V1 appearing as a staircase (no overloading is assumed). Taking the difference between Vin and V1 gives us V_Q, which is quatization error V_Q is limited to $\pm$ 1/2LSB.





Quantization Noise in Ideal ADCs (Cont.)

2. The average of VQ is zero

   root mean square (rms) value VQ(rms)

$$V_{Q(rms)} = [\frac{1}{T}\int_{-T/2}^{T/2} V_Q^2 dt]^{1/2} = [\frac{1}{T}\int_{-T/2}^{T/2} V_{LSB}^2 (-t/T)^2 dt]^{1/2}$$

$$= [\frac{V_{LSB}^2}{T^3}](\frac{t^3}{3})\Big|_{-T/2}^{T/2}]^{1/2} = V_{LSB}/\sqrt{12}$$

$\Rightarrow$ VQ is proportional to the size of VLSB, which is determined by bit number N.

– Stochastic approach

To deal with more general input case, a stochastic approach is typically used.

1. Assume that the input signal is varying rapidly such that VQ is a random variable uniformly distributed between ±1/2VLSB.

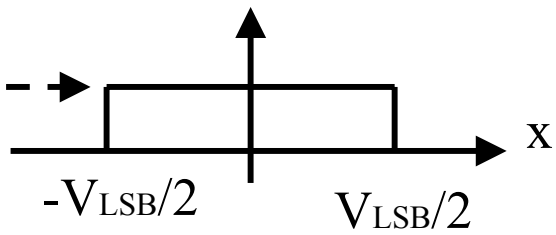
Quantization Noise in Ideal ADC (Cont.)

The probability density function fQ(x)

$$f_Q(x) = 1/V_{LSB}$$ where -1/2VLSB<x<1/2VLSB

Height=$1/V_{LSB}$

$$\int_{-\infty}^{\infty} f_Q(x)dx = 1$$



2. The average value of VQ is zero

$$V_{Q(avg)} = \int_{-\infty}^{\infty} xfQ(x)dx = 1/V_{LSB}\int_{-V_{LSB}/2}^{V_{LSB}/2} xdx = 0$$

$$V_{Q(rms)} = [\int_{-\infty}^{\infty} x^2 fQ(x)dx]^{1/2}$$

$$= [1/VLSB(\int_{-V_{LSB}/2}^{V_{LSB}/2} x^2 dx)]^{1/2} = VLSB/\sqrt{12}$$

which are the same as those found using the deterministic ramp input .

Quantization Noise in Ideal ADCs (Cont.)

3. (i) Assume Vin is a sawtooth of height Vref(or a random signal uniformly distributed between 0 and Vref, the SNR is

$$SNR = 20\log(\frac{V_{in(rms)}}{V_{Q(rms)}}) = 20\log(\frac{V_{ref}/\sqrt{12}}{V_{LSB}/\sqrt{12}}) = 20\log(2^N) = 6.02NdB$$

(ii) A more common SNR formula is to assume Vin is a sinusoidal waveform between 0 and Vref.

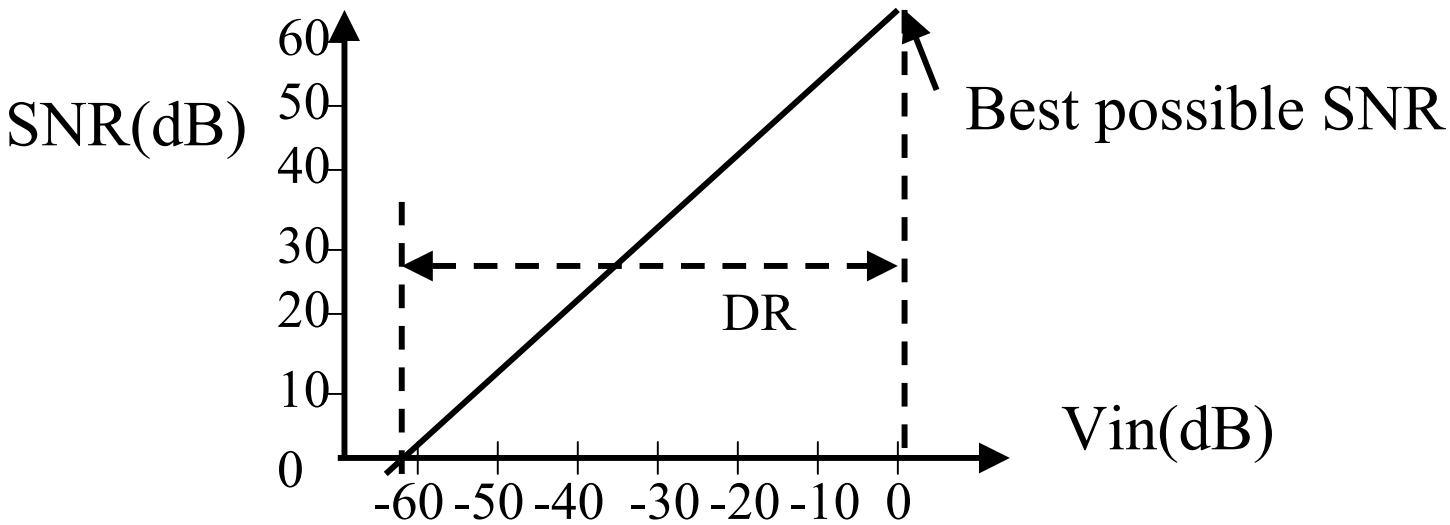
$$SNR = 20\log(\frac{V_{in(rms)}}{V_{Q(rms)}}) = 20\log(\frac{V_{ref}/2\sqrt{2}}{V_{LSB}/2\sqrt{2}}) = 20\log(\sqrt{\frac{3}{2}}2^N)$$

$$= 6.02N + 1.76dB$$

In other words, a sinusoidal signal has 1.76dB more ac power than a random signal uniformly distributed between the same peak levels. This equation gives the best possible SNR for an N-bit ADC. The maximum SNR can be achieved is also called peak signal-to-noise ratio (PSNR).

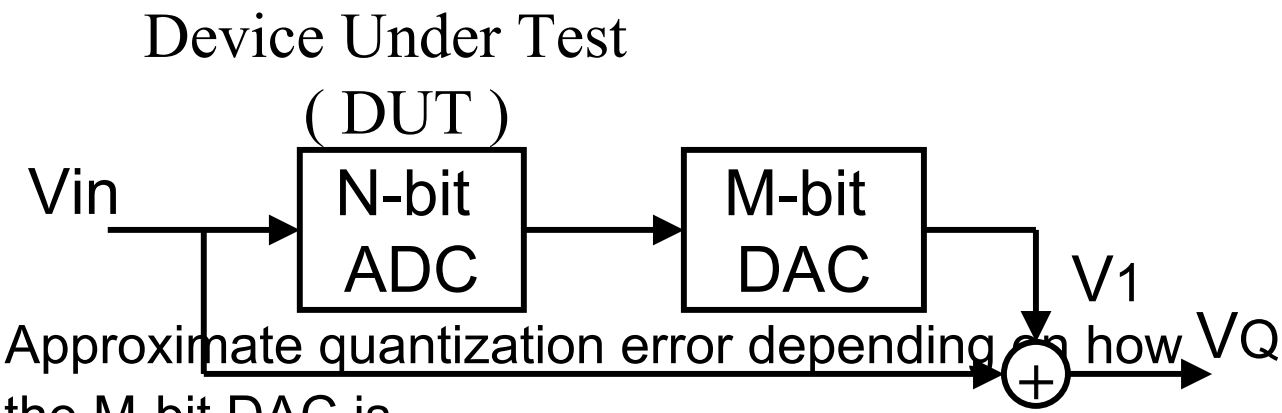
Quantization Noise in Ideal ADCs (Cont.)

(iii) SNR VS. Vin plot (sine input and ideal 10-bit input for this example)



Practical Method for Measuring Errors in real ADCs

- ADC and DAC both are not ideal.
  ADC is the device under test.



1. Approximate quantization error depending on how the M-bit DAC is.
2. M-bit DAC has accuracy higher than N-bit.
3. VQ can be further corrected
   pipelined ADC.

⇨

Signed Codes

- Sign magnitude
- 1's complement
- Offset binary
- 2's complement
  - If many numbers are being added using 2's complement codes, no overflow hardwire is required as long as the final result is within the digital range (even if the intermediate results go well out of range.)
  - A+B and A-B can be easily realized (refer to the textbook)

Signed Codes (Cont.)

- Gray code
  - often used for high speed communication systems.

    Some 4 bits signed digital representations:

Number	Normalized Number	Sign Magnitude	1's Complement	Offset Binary	2's Complement
+7	+7/8	0111	0111	1111	0111
+6	+6/8	0110	0110	1110	0110
+5	+5/8	0101	0101	1101	0101
+4	+4/8	0100	0100	1100	0100
+3	+3/8	0011	0011	1011	0011
+2	+2/8	0010	0010	1010	010
+1	+1/8	0001	0001	1001	0001
+	+0	0000	0000	1000	0000
(-0)	(0)	(1000	(1111)		
-1	-1/8	1001	1110	0111	1111
-2	-2/8	1010	1101	0110	1110
-3	-3/8	1011	1100	0101	1101
-4	-4/8	1100	1011	0100	1100
-5	-5/8	1101	1010	0011	1011
-6	-6/8	1110	1001	0010	1010
-7	-7/8	1111	1000	0001	1001
-8	-8/8			0000	1000

Performance Limitation

- Definitions for determining the transfer responses for both DACs and ADCs.
  - DAC

    The transfer response of a DAC is defined to be the analog levels that occur for each of the digital word.

  - ADC

    The transfer response of an ADC can be defined as the analog transition point values, Vij, we use the approach here.

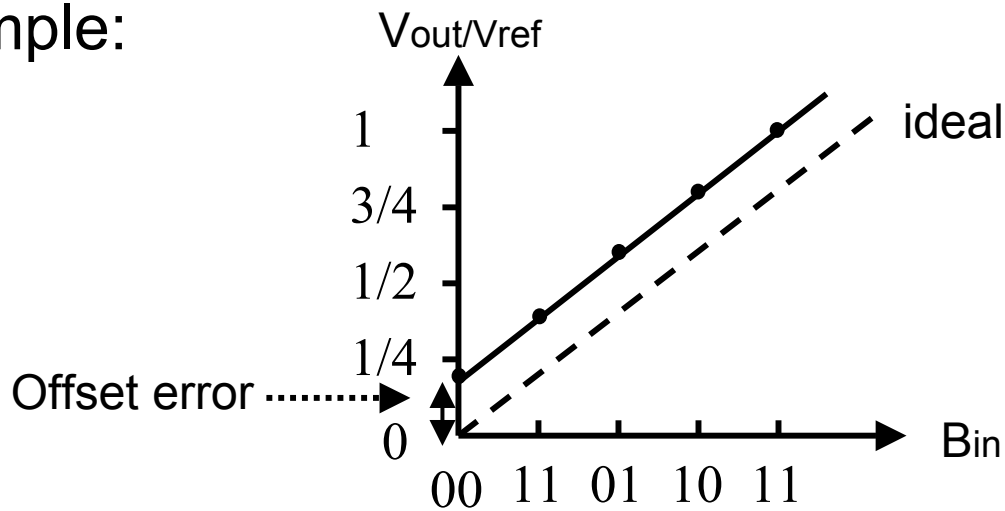
Performance Limitation (Cont.)

- Resolution
  - the number of distinct analog levels corresponding to different digital words. Thus, an N-bit resolution implies that the converter can resolve 2^N distinct analog levels.
  - Resolution is not necessarily an indication of the accuracy of the converter, but instead it usually refers to the number of digital input or output bits.

Offset Error

- Offset error is in units of LSBs.
- DAC
  - Offset error is the output that occurs for the input code that should produce zero output .

    $E_{off(DAC)} = V_{out}/V_{LSB}\big|_{0\ldots0}$
  - 2-bit example:

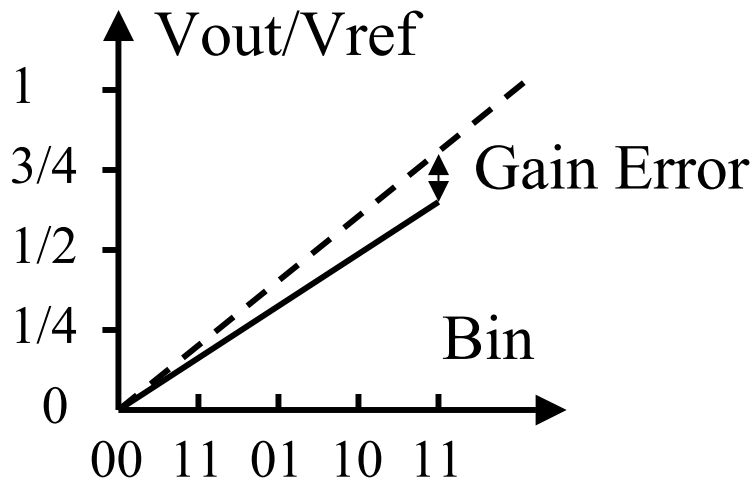


- ADC
  - Offset error is the deviation of $V_{0\ldots01}$ from 1/2LSB

$$E_{off(ADC)} = \frac{V_{0\cdots1}}{V_{LSB}} - 1/2LSB$$

Gain Error

- Gain error is the difference at the full-scale value between the ideal and actual when the offset error has been reduced to zero.
- Gain error is in units of LSBs.
- DACs
  - Egain(DAC)=($\left.\frac{Vout}{VLSB}\right|_{1\ldots1}$ - $\left.\frac{Vout}{VLSB}\right|_{0\ldots0}$)-(2^N-1)
  - 2-bit example



- ADC

$$E_{gain}(ADC) = (\frac{V_{1...1}}{V_{LSB}} - \frac{V_{0...01}}{V_{LSB}}) - (2^N - 2)$$

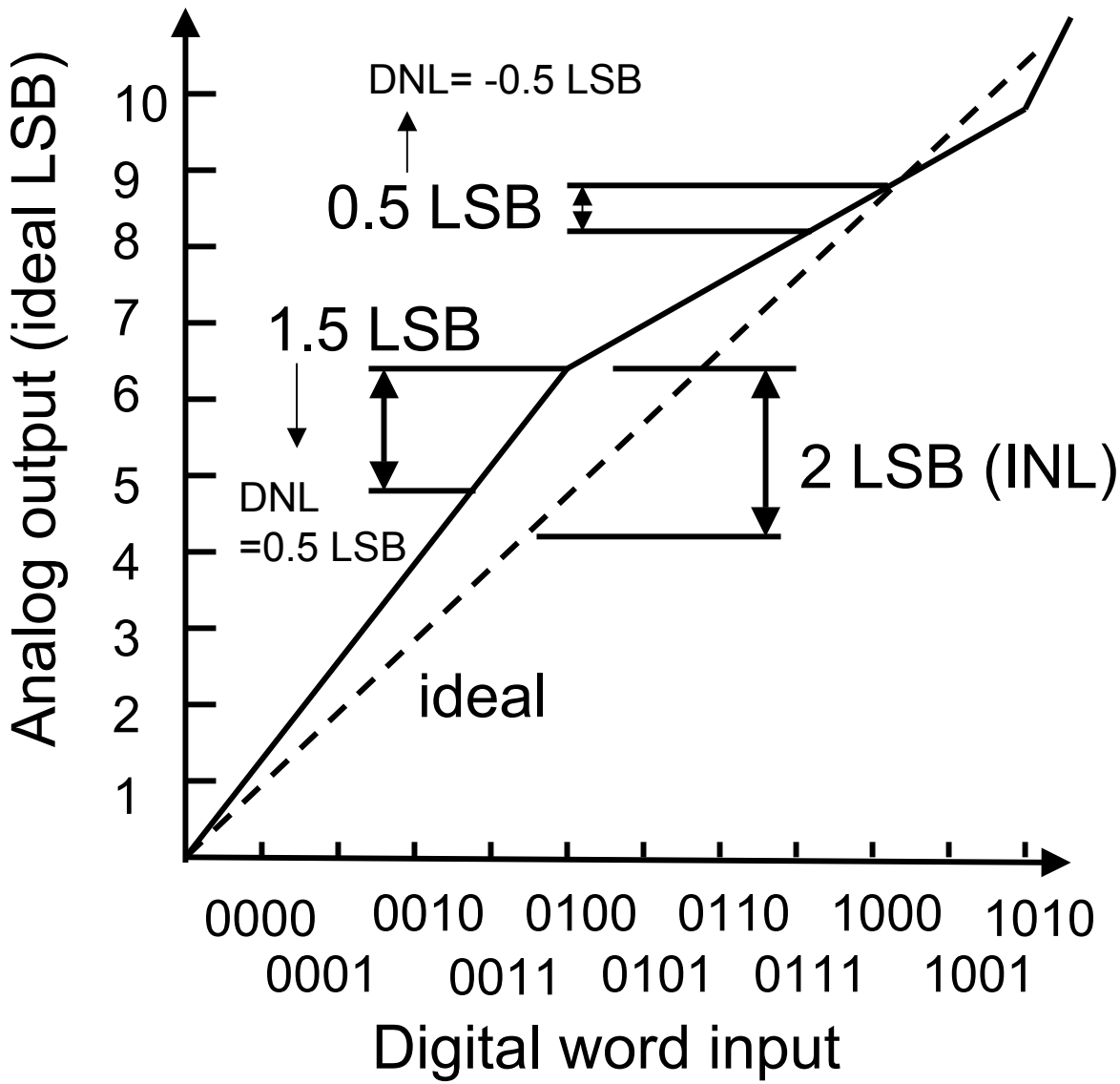
Accuracy

- Absolute accuracy
  - the difference between the expected and actual and transfer responses.
  - Includes 1. offset error, 2. gain error, and 3. linearity error
- Relative accuracy
  - the accuracy of offset and gain errors have been removed
- Accuracy can be expressed as a percentage error of full-scale value, as the effective number of bit, or as a fraction of an LSB.
  - For example, a 12-bit accuracy implies that the converter's error is less than the full-scale divided by 2^{12}.
  - A converter may have 12-bit resolution with only 10-bit accuracy, or 10-bit resolution with 12-bit accuracy.
  - An accuracy greater than the resolution means that the converter's transfer response is very precisely controlled. (better than the number of bits of resolution).

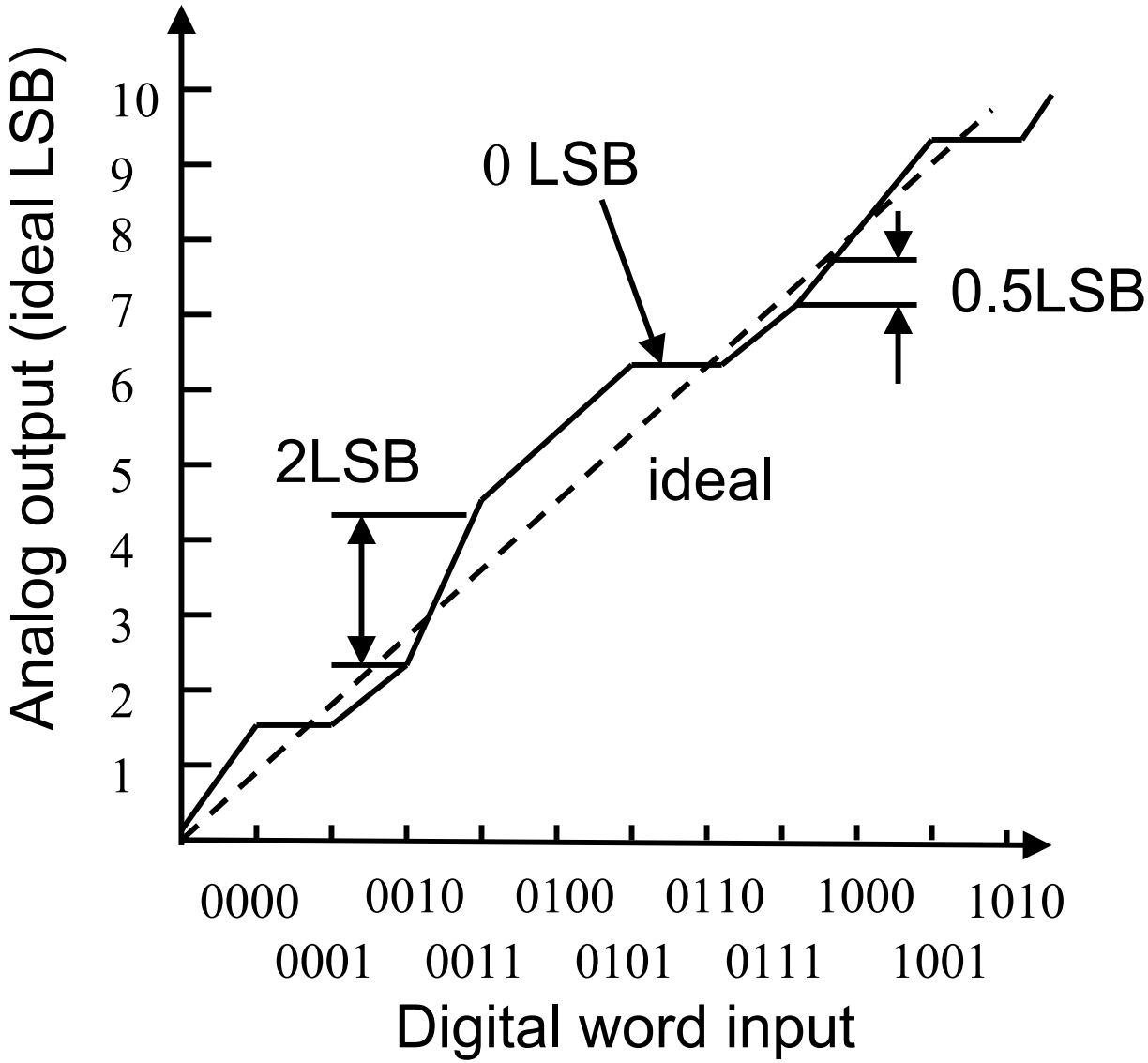
Accuracy (Cont.)

- Integral Nonlinearity (INL)Error:
  - After both the offset and gain error have been removed, the integral nonlinearity (INL) error is defined to be the deviation from a straight line. However, what straight line should be used?
  - A conservative measure of nonlinearity is to use the endpoints of the converter's transfer response to define the straight. An alternate definition is to find the best -fit straight line such that the maximum difference (or perhaps the mean squared error) is minimized.
  - In general, the INL values are defined for each digital word.
    Sometimes, "INL" is defined as the maximum magnitude of INL values.

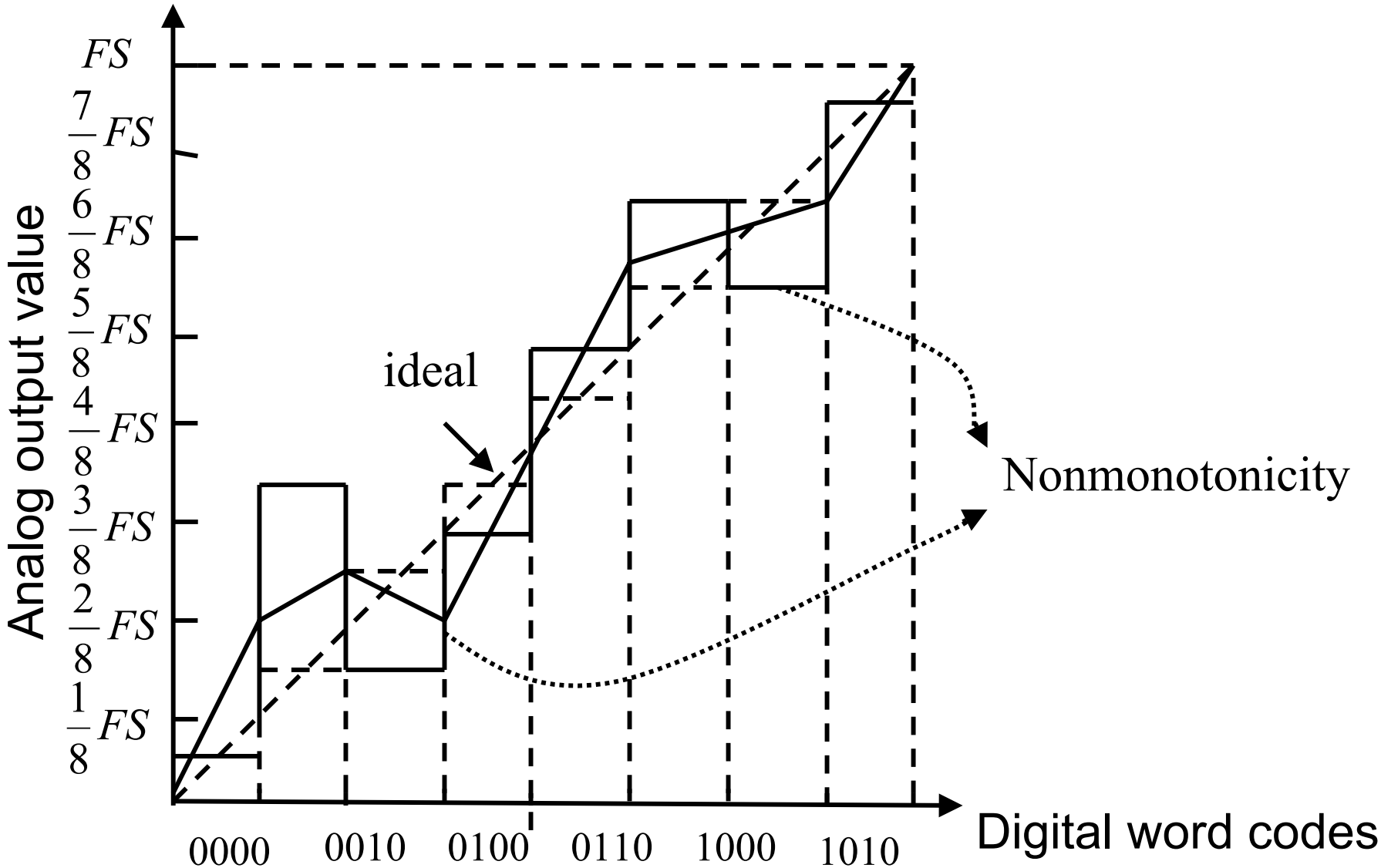
Accuracy (Cont.)



Accuracy (Cont.)



Accuracy (Cont.)



Accuracy (Cont.)

- Differential Nonlinearilty (DNL)Error:
  - In an ideal converter, each analog step size is equal to LSB. In other words, in a D/A converter, each output level is 1 LSB from adjacent levels, whereas in A/D, the transition values are precisely 1 LSB apart.
  - Differential nonlinearity (DNL) is defined as the variation in analog step sizes away from 1LSB (typically, offset error have been removed).
  - Thus, an ideal converter has it's maximum differential nonlinearity of 0 for all digital values, where as a converter with a maximum differential nonlinearity of 0.5 LSB has its step size varying from 0.5LSB to 1.5LSB.
  - In general, as in the INL case, DNL values are defined for each digital word, whereas sometimes DNL is defined as the maximum magnitude of the DNL values.

Accuracy (Cont.)

- Monotonicity:
  - A monotonic D/A is one in which the output always increase as the input increases. In other words, the slope of the D/A converter's transfer response is of only one sign.
  - If the maximum DNL error is less than 1LSB, then a D/A converter is guaranteed to be monotonic. However, many monotonic converter may have a maximum DNL greater than 1 LSB.
    Similarly,a converter is guaranteed to be monotonic if the maximum INL is less than 0.5LSB.
- Missing Codes:
  - Although monotonicity is appropriate for D/A converters, the equation term for A/D converter is missing codes. An A/D converter is guaranteed not to have any missing codes if the maximum DNL error is less than 1LSB or if the maximum INL error is less than 0.5LSB.

Accuracy (Cont.)

- A/D Conversion Time and Sampling Rate:
  - In A/D converter, the conversion time is the time taken for the converter to complete a single measurement including acquisition time for the input signal.
  - On the other hand, the sampling rate is the speed at which sampling can be continuously converted and is typically the inverse of the conversion time.
  - However, one should be aware that some converter have a large latency between the input and the output due to pipelining or multiplexing, yet they still maintain a high sampling rate. For example, a pipelined 12-bit A/D converter may have a conversion time of 2us (i.e. a sampling rate of 500kHz) yet a latency from input to output of 24us.

Accuracy (Cont.)

- D/A Settling Time and Sampling Rate:
  In a D/A converter, the settling time is defined as the time it takes for the converter to within some specified amount of final value(usually 0.5LSB). The sampling rate is the rate at which samples can be continuously converted and is typically the inverse of the settling time.
- Sampling Time Uncertainty :
  - Both A/D and D/A converter have limited accuracy when their sampling instances are ill defined. To quantify this sampling time uncertainty, also known as aperture jitter, for sinusoidal waveform, consider a full-scale signal, Vin, applied to an N-bit, signed, A/D converter with frequency fin.

Accuracy (Cont.)

– Mathematically, $V_{in} = \frac{V_{ref}}{2}\sin(2\pi f_{in} t)$

Since the rate of change (or slope) of Vin at the peak of a sinusoidal waveform is small, sampling time uncertainty is less of a problem near the peak values. However, the maximum rate of change for this waveform occurs at the zero crossing and can be found by differentiating Vin with respect to time and setting t=0. At the zero crossing, we find that

$$\left.\frac{\Delta V}{\Delta t}\right|_{\max} = \pi f_{in} V_{ref}$$

– If Δt represents some sampling-time uncertainty, and if we want to keep ΔV less than 1 VLSB, we see that

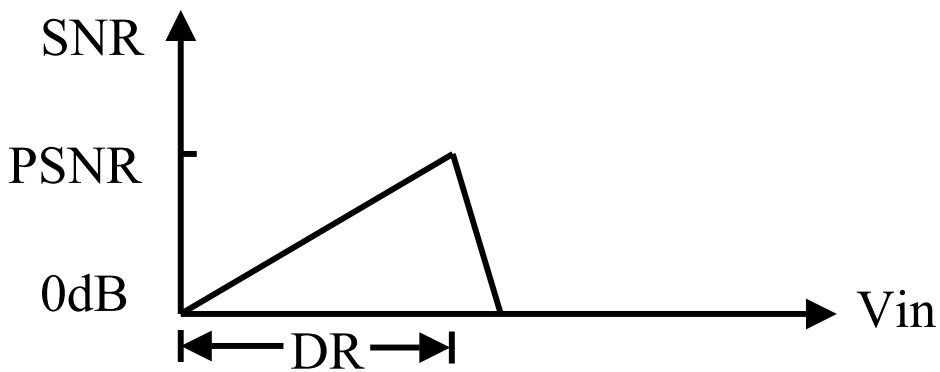
$$\Delta t < \frac{V_{LSB}}{\pi f_{in} V_{ref}} = \frac{1}{2^N \pi f_{in}}$$

For example, an 8-bit converter sampling a full-scale 250-MHz sinusoidal signal must keep its sampling-time uncertainty under 5 ps to maintain 8-bit accuracy. Also, the same 5 ps time accuracy is required for a 16-bit converter operating on a full-scale, 1-MHz signal.

Dynamic Range (DR)

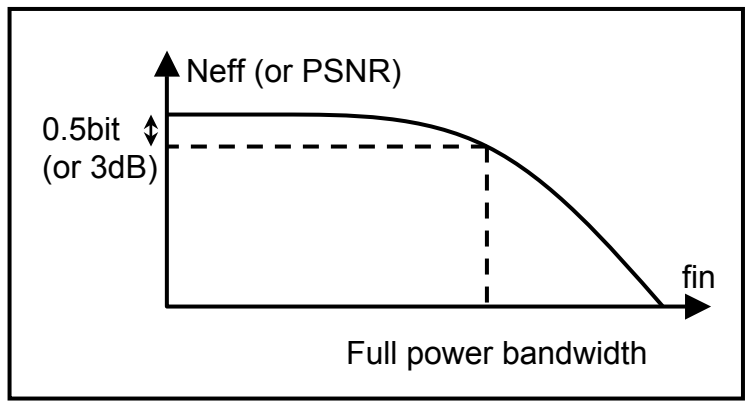
- Two different definitions:

  1. The ratio of maximum amplitude input sinusoidal to minimum amplitude input sinusoidal.
     - maximum input: input with PSNR or maximum allowable input.
     - minimum input: input with SNR=0.
  2. Effective number of bit using the equation
     PSNR=6.02Neff+1.76dB
     where 1 is commonly used.



Dynamic Range (Cont.)

- DAC
  analog output measured using spectrum analyzer
- ADC
  digital output analyzed using Fast Fourier Transform (FFT).
- Full-Power Bandwidth
- Dynamic range is function of the frequency of the sinusoidal input.



- For example, if an 8-bit, 200MHz A/D converter has a band-limited preamplifier or a slew rate limited sample and hold, dc input may show full 8-bit performance even at the maximum sample rate of 200M sample/s. However, a high-frequency sinusoidal input at, say, 40MHz, will require the input stage to track a rapidly varying signal and may result in only 6-bit performance.

Dynamic Range (Cont)

- Distortion level (or Nonlinearity performance) of many converters remains at a fixed level and is not a function of input signal level. Thus, as the input signal level is decreased, the signal-to-distortion ratio decreases. This behavior occurs because the distortion level is often determined by component matching and thus is fixed once the converter is realized.

  However, in some converters, the distortion level decreases as the input signal level is decreased, which is often a desirable property to have. For example, most 1-bit oversampling converters have this desirable property since they do not rely on component matching and their distortion level is often a result of weak nonlinear effect at the input stage.