Nyquist-Rate D/A Converts

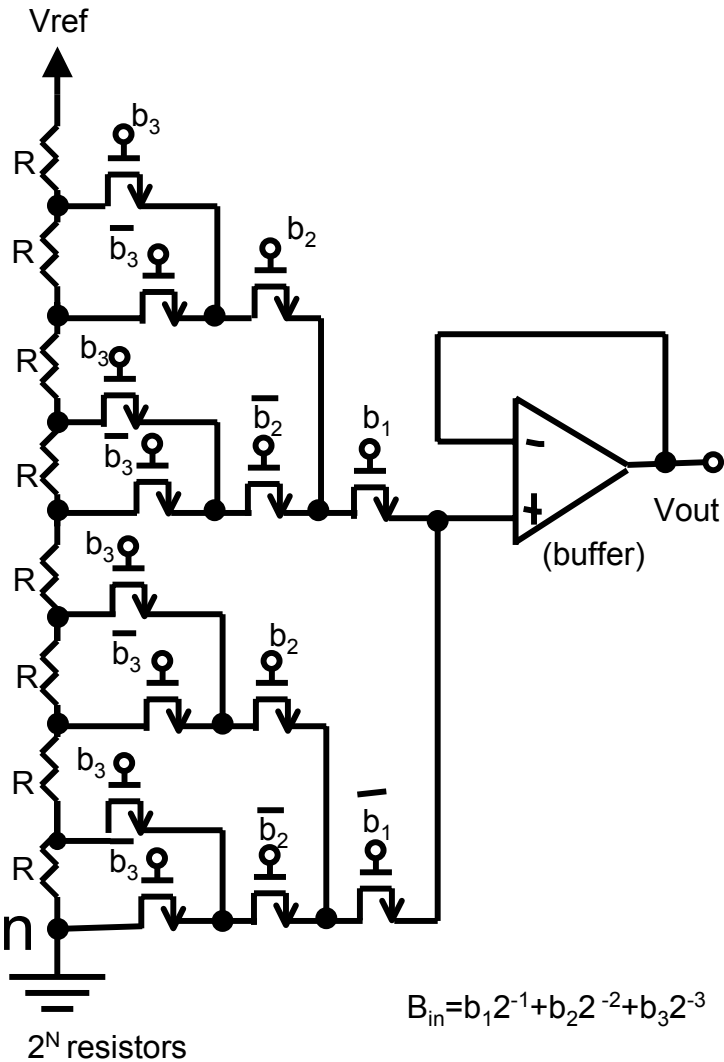
- Four main types
  - Decoder-based
  - Binary-weighted
  - Thermometer-code
  - Hybrid

Decoder-Based DAC

- Most straight forward approach
  - create 2^N reference signals and pass the appropriate signal to the output
- Three main types
  - Resistor string
  - Folded resistor-string
  - Multiple resistor-string

Resistor String DAC

- Example 1: a 3-bit DAC with transmission-gate, tree-like decoder
  - Transmission gates might be used rather than n-channel switches
    1. extra drain and source capacitance(to GND) is offset by the reduced switch resistance
    2. larger layout
    3. can operate closer to positive supply voltage
  - Only n-channel switches are used
    1. about the same speed as the transmission gate implementation
    2. compact layout(no contacts are required in the tree)



Resistor String DAC (Cont.)

- Monotonicity is guaranteed (if the buffer's offset does not depend on its input voltage)
- The accuracy of this DAC depends on the type of resistor used. Polysilicon(20-30 Ω/square) can have up to 10 bits of accuracy
- Speed:

  can be estimated using open-circuit time-constant approach (refer to microelectronics textbook written by Sedra and Smith)

  Time-constant $\approx 3 R_{tr}C_{tr} + 2 \bullet 3 R_{tr}C_{tr} + \ldots\ldots + N \bullet 3R_{tr}C_{tr}$

  $= N(N+1)/2 * 3 R_{tr}C_{tr}$

  where R_{tr} is on resistance of switches

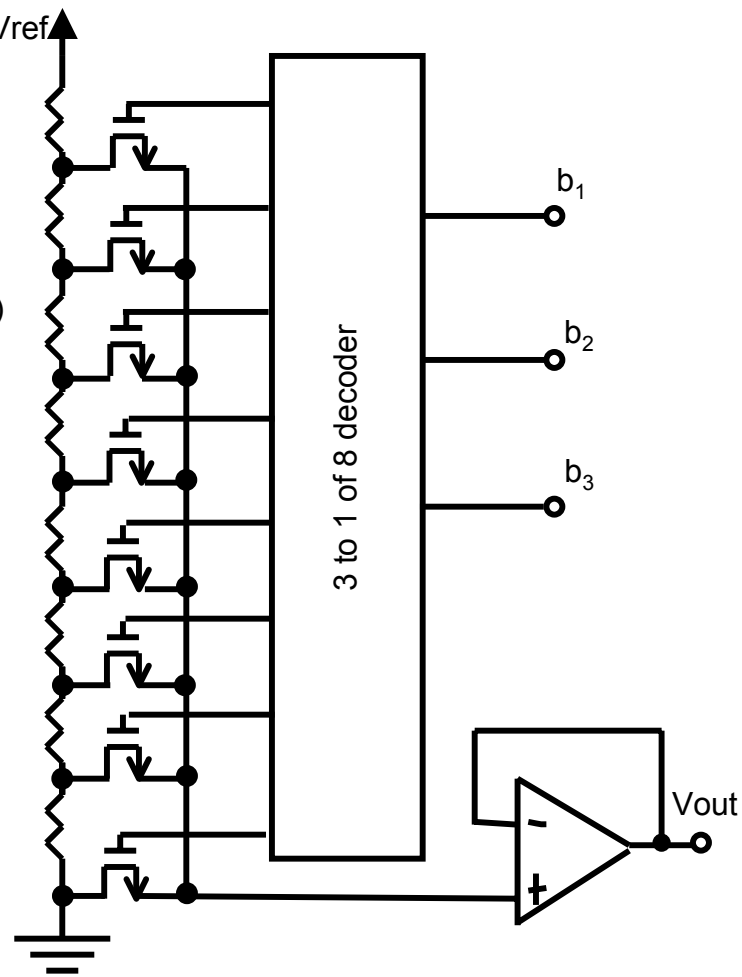
  C_{tr} is drain or source capacitance of switches

  N is bit number

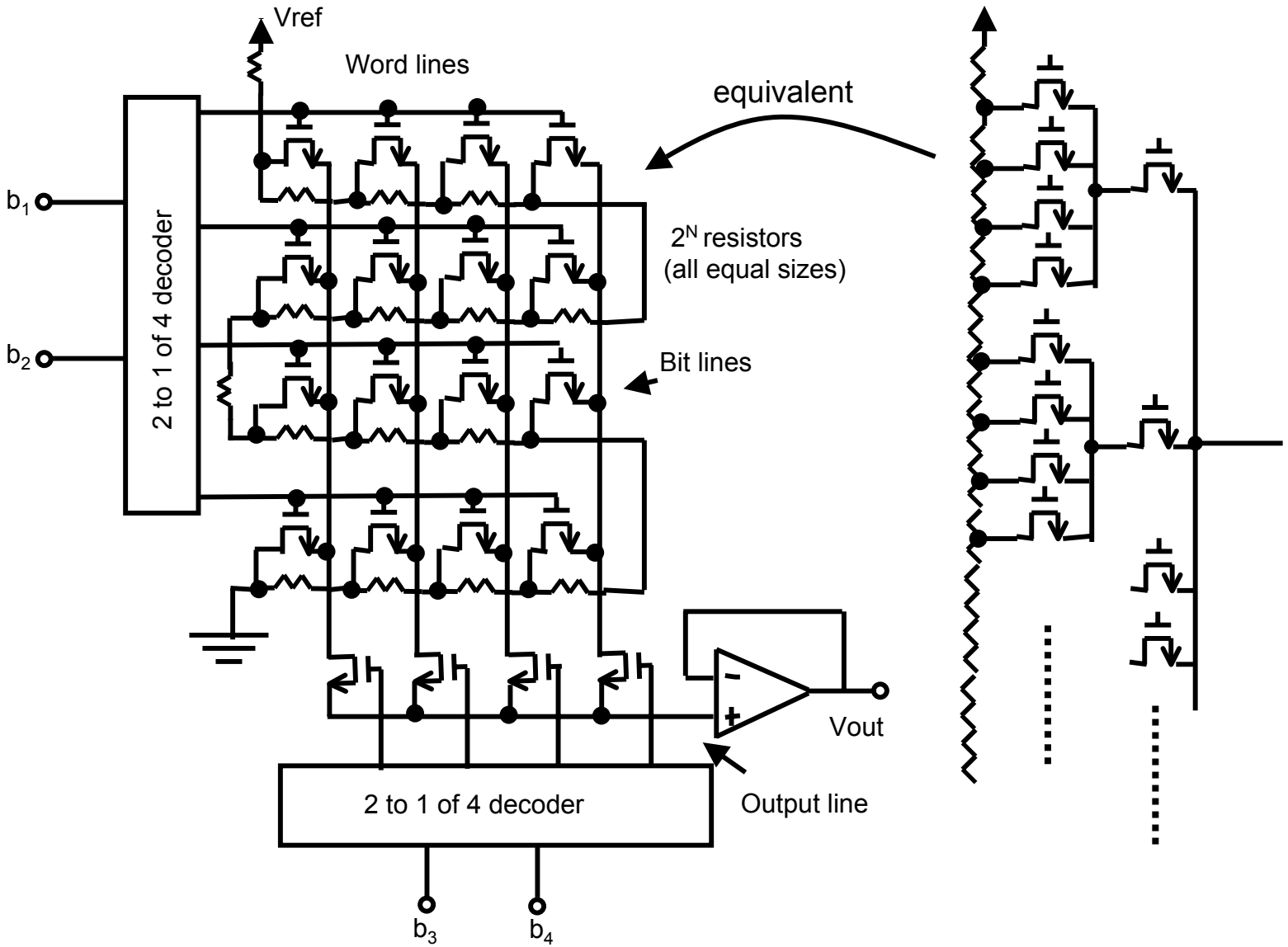
Resistor String DAC (cont.)

- Example 2: a 3-bit DAC with digital decoding
  - compared to Example1
    1. higher speed
    2. more area for decoding circuit
  - speed:
    Time-constant $\approx R_{tr} \cdot 2^N C_{tr}$
    For $N \leq 6$ Example 2 is faster
    For $N > 7$ Example 1 is faster
- compromis between Examples 1 and 2

  =>Folded resistor-string DAC



Folded Resistor-String DAC



Folded Resistor-String DAC (Cont.)

- Reduce the amount of digital decoding
- Reduce large capacitive loading
- Decoding is very similar to that for a digital memory
- Example:

  4 bit (=2 bit+2 bit) DAC

  Time constant $\approx R_{tr}(2^2 C_{tr})+2 R_{tr}(2^2 C_{tr})$
- other design examples

  12 bit=6 bit+6 bit, or 4 bit+4 bit+4 bit, or…..

  10 bit=5 bit+5 bit, or 3 bit+3 bit+4 bit, or…...

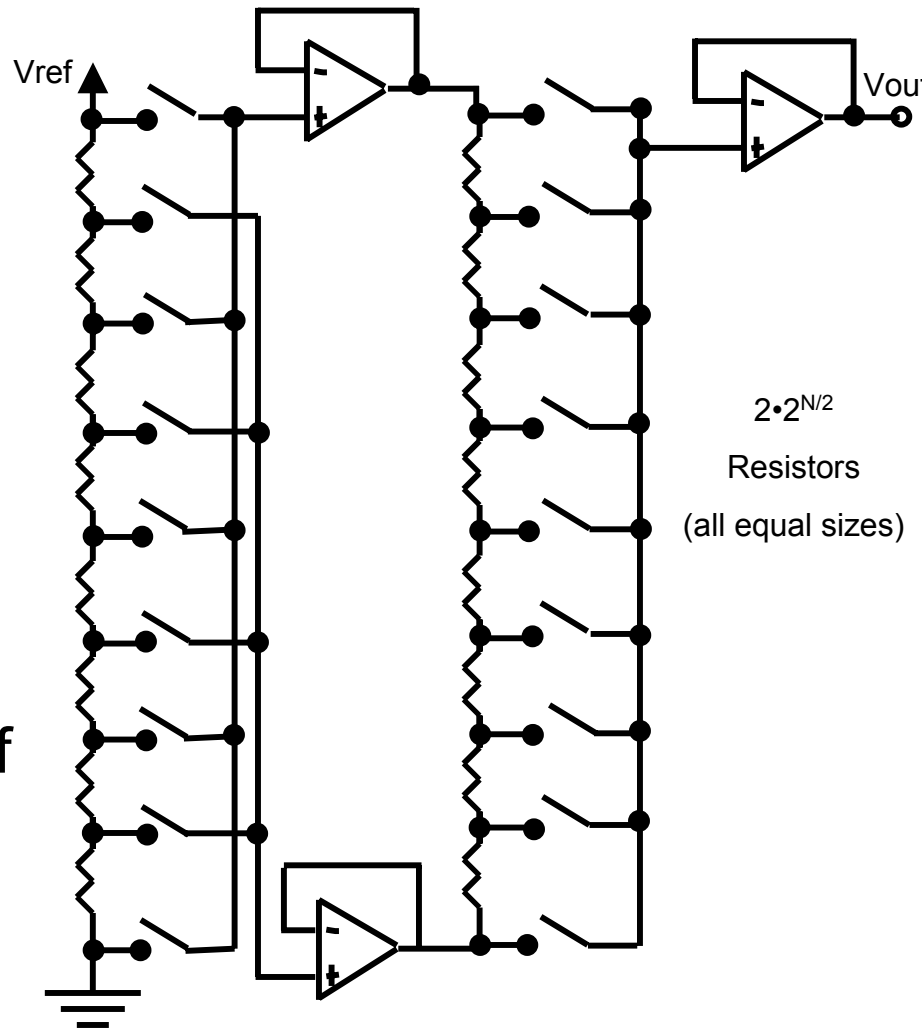
  ⋮

  etc.

Multiple Resistor-string DAC

- 6-bit example
- Requires only $2 \cdot 2^{N/2}$ resistors
- Monotonic if OPAMPS have matched, voltage-insensitive offset voltages.
- For high speed, OPAMPS must be fast.

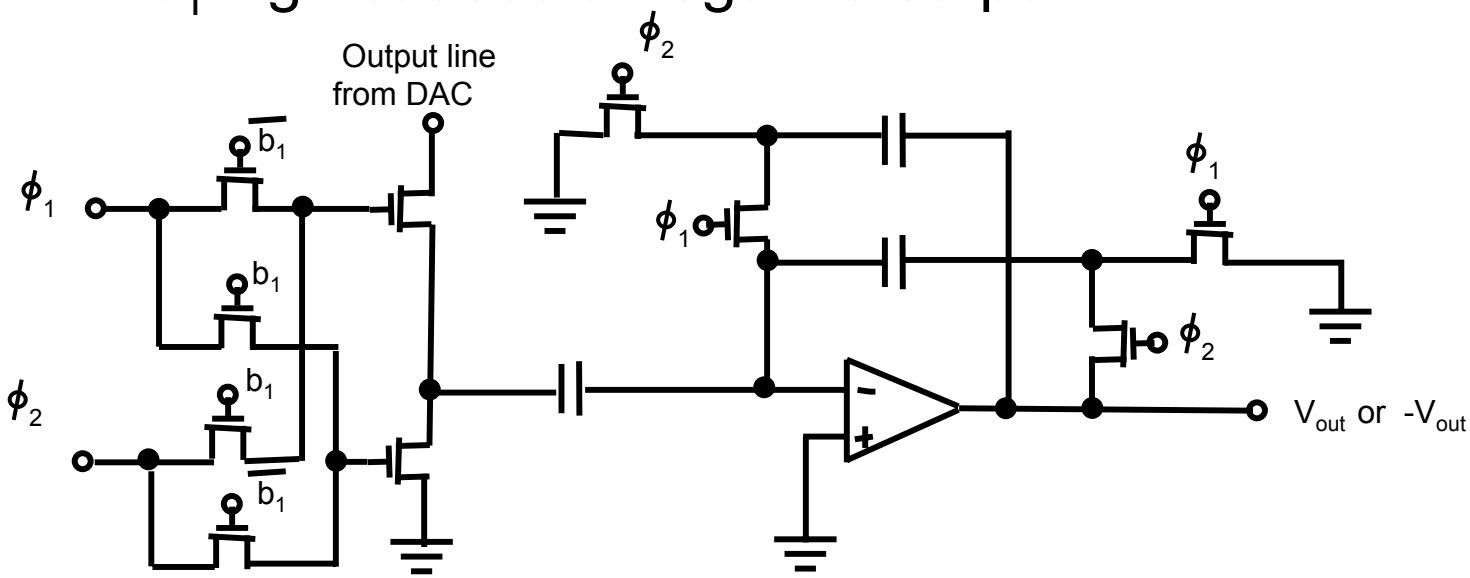
  For high resolution, OPAMPS must be low noise.
- The matching requirements of the second resistor string are not nearly as severe as those for the first string.



  - The second resistor string is used to decode only lower-order bits

Signed Outputs

- Negative output voltages are required. Two popular methods
  1. The bottom of the resistor string can be connected to -Vref
     - requires a negative power supply
     - circuits are needed to realize a dual power supply
     - high cost if the negative supply is obtained off chip
  2. Using SC inverting amplifier
     - realizes a signed output from a unipolar (positive) DAC output
     - b_1 high causes a negative output



Binary-Weighted (or Binary-Scaled) Converters

- An appropriate set of signals that are all related in a binary fashion

  The binary array of signals might be voltages, charges, or currents
- Binary-weighted resistor DAC

  Reduced-resistance-ratio ladders

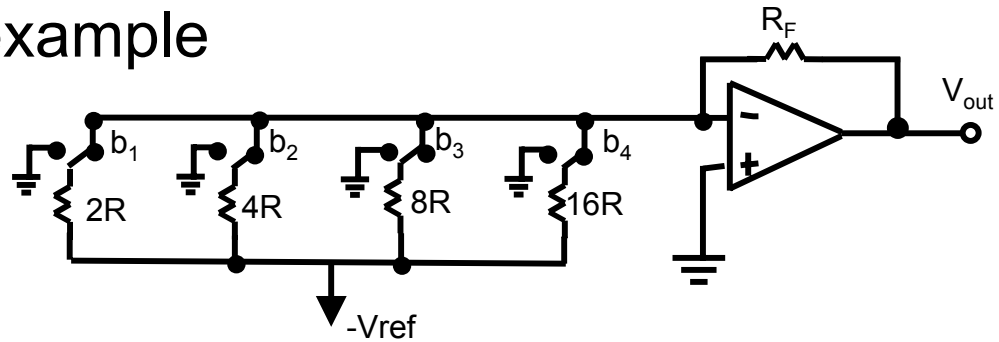
  R-2R-based DAC

  Charge-redistribution switched-capacitor DAC

  Current-mode DAC

Binary-Weighted Resistor DAC

- 4-bit example



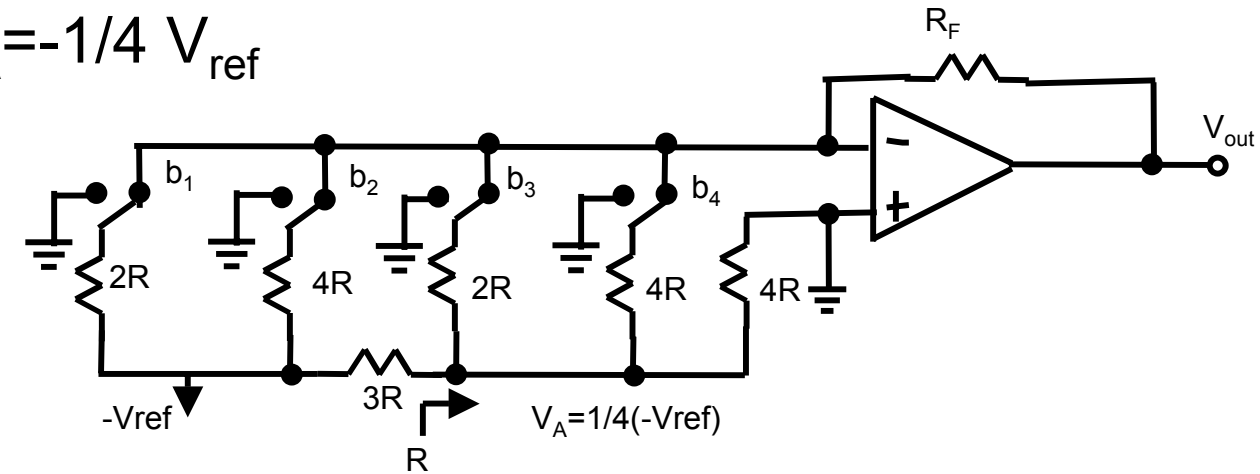
$$V_{out} = -R_F V_{ref}\left(-\frac{b_1}{2R} - \frac{b_2}{4R} - \frac{b_3}{8R}\cdots\right) = \left(\frac{R_F}{R}V_{ref}\right)B_{in}$$

$$where \quad B_{in} = b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \cdots$$

- Does not require many resistors or switches
- Disadvantages
  1. Resistor ratio and current ratio are on the order of 2^N. If N is large, this large current ratio requires that the switches also be scaled so that equal voltage drops appear across them.
  2. monotonicity is not guaranteed
  3. prone to glitches

Reduced-Resistance-Ratio Ladders

- Reduce the large resistor ratios in a binary-weighted array
- Introduce a series resistor to scale signals in portions of the array V_A=-1/4 V_{ref}



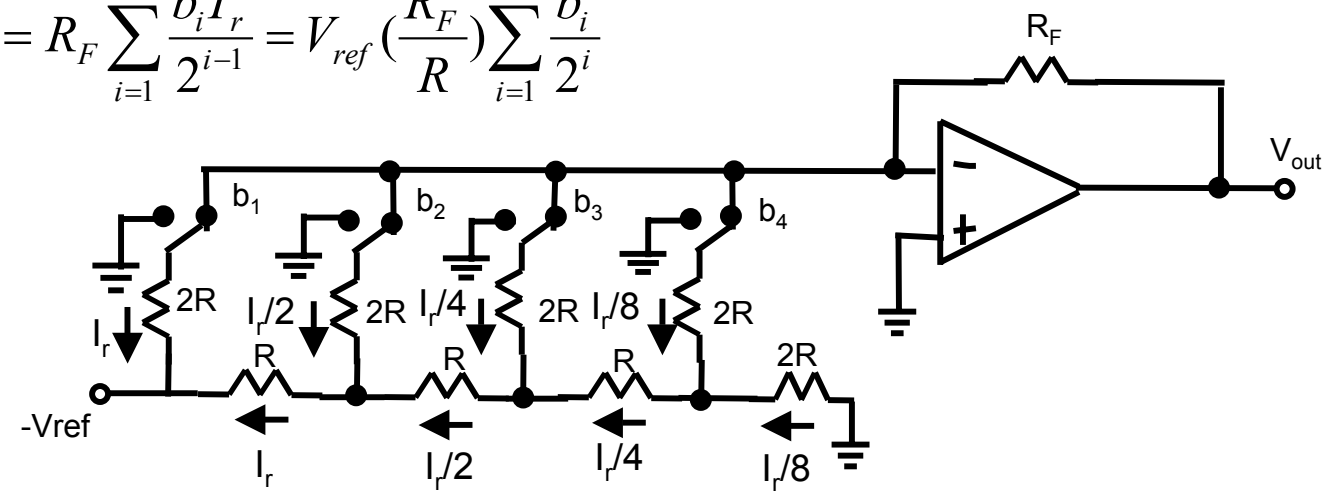
- An additional 4R was added such that resistance seen to the right of the 3R equals R.
- One-fourth the resistance ratio compared to the binary-weighted case
- Current ratio has remained unchanged
  =>Switches must be scaled in size
- Repeating this procedure recursively, one can obtain an R-2R ladder

R-2R-Based DAC

- Smaller size and better accuracy than a binary-sized approach
  1. small number of components
  2. resistance ratio of only 2
- 4-bit example

$$I_r = \frac{V_{ref}}{2R}$$

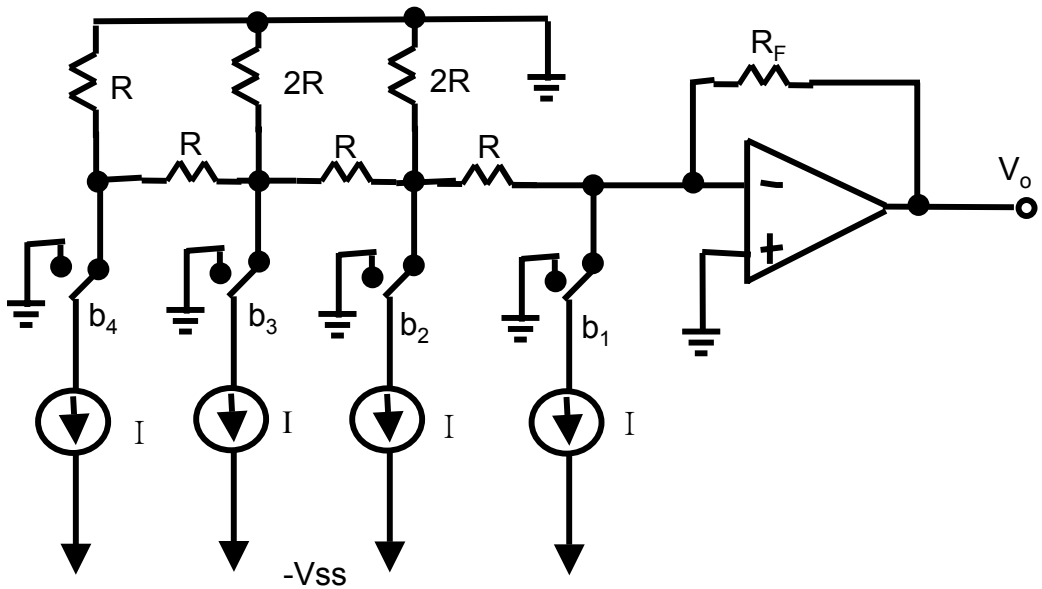
$$V_{out} = R_F \sum_{i=1}^{N} \frac{b_i I_r}{2^{i-1}} = V_{ref}\left(\frac{R_F}{R}\right)\sum_{i=1}^{N} \frac{b_i}{2^i}$$



- Current ratio is still large
  =>large ratio of switch sizes

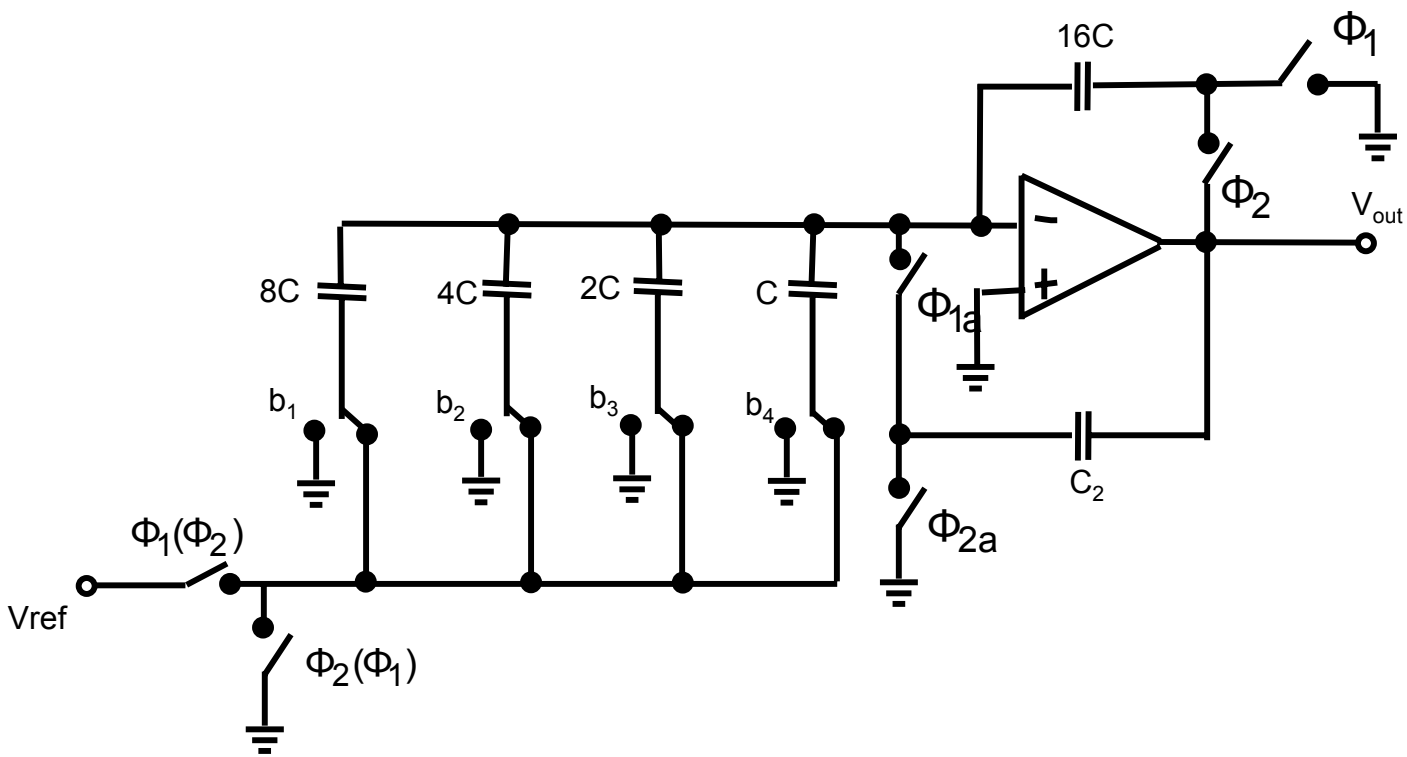
R-2R-Based DAC (Cont.)

- R-2R ladder DAC with equal currents through switches
  - slower since the internal nodes exhibit some voltage swings(as opposed to the previous configuration where internal nodes all remain at fixed voltage)



Charge-Redistribution Switched-Capacitor DAC

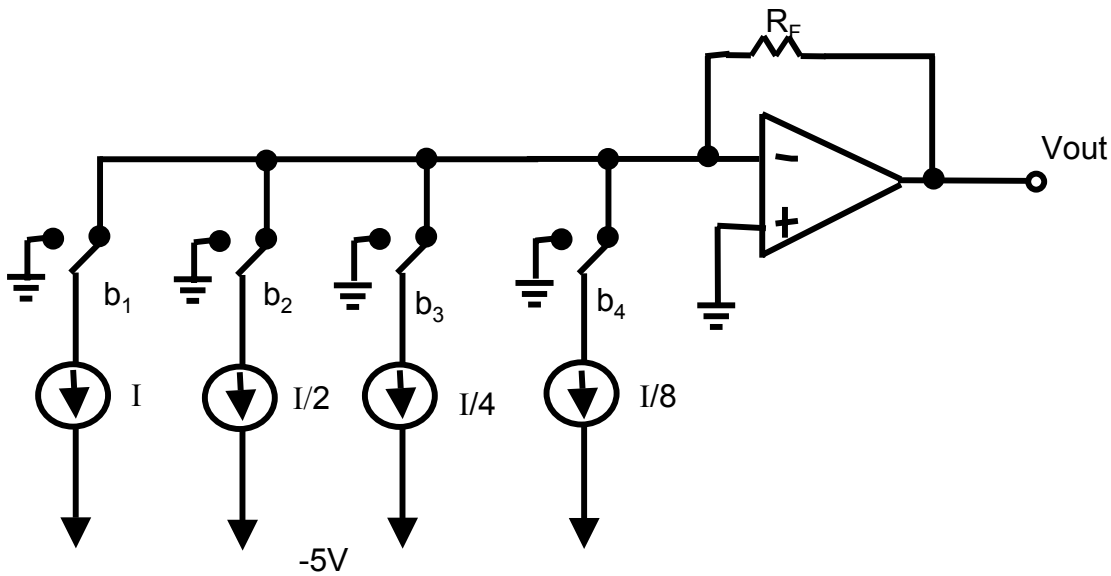
- Insensitive to OPAMP input-offset voltage, 1/f noise, and finite amplifier gain
- An additional sign bit can be realized by interchanging the clock phases(shown in parentheses)



Current-Mode DAC

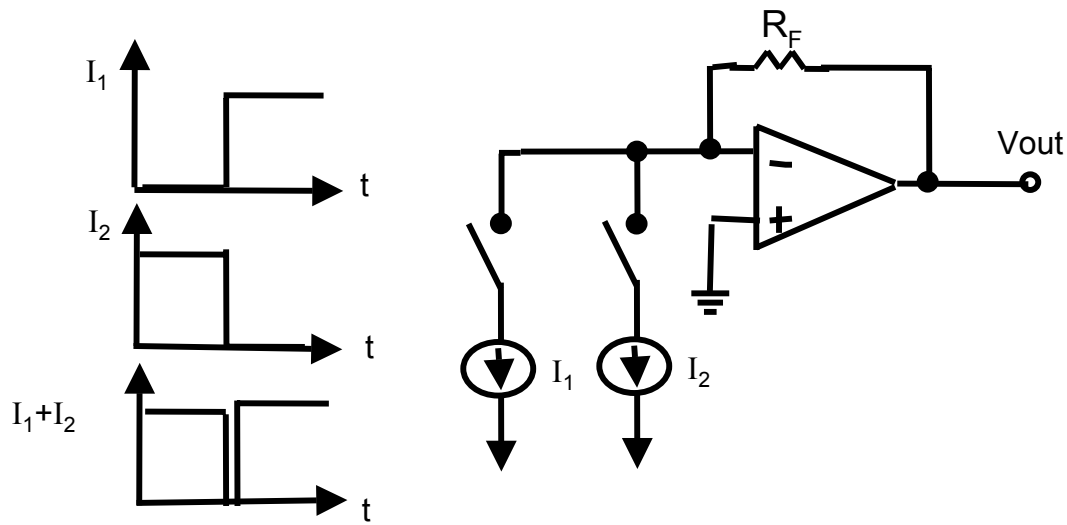
- High-speed
- Switch current to output or to ground

  The output current is converted to a voltage through R_F
- The upper portion of current source always remains at ground potential.



Glitches

- A major limitation during high-speed operation
- Mainly the result of different delays occuring when switching different signals
- Example: 01111……1--->1000 ……0
  1. I_1represents the MSB current, and I_2 represents the sum of (N-1) LSB currents.
  2. The MSB current turns off slightly early, causing a glitch of zero current



Glitches (Cont.)

- Glitch disturbance can be reduced by

  1. limiting the bandwidth (placing a capacitor across R_F)

     This method slows down the circuit.

  2. using a sample and hold on the output signal.

  3. modifying some or all of the digital word from a binary code to a thermometer code.

  (3. is the most popular method.)

Thermometer-Code DACs

- Digitally recode the input to a thermometer-code equivalent

Thermometer-code representations for 3-bit binary values

Decimal	Binary			Thermometer Code						
	b1	b2	b3	d1	d2	d3	d4	d5	d6	d7
0	0	0	0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0	0	0	1
2	0	1	0	0	0	0	0	0	1	1
3	0	1	1	0	0	0	0	1	1	1
4	1	0	0	0	0	0	1	1	1	1
5	1	0	1	0	0	1	1	1	1	1
6	1	1	0	0	1	1	1	1	1	1
7	1	1	1	1	1	1	1	1	1	1

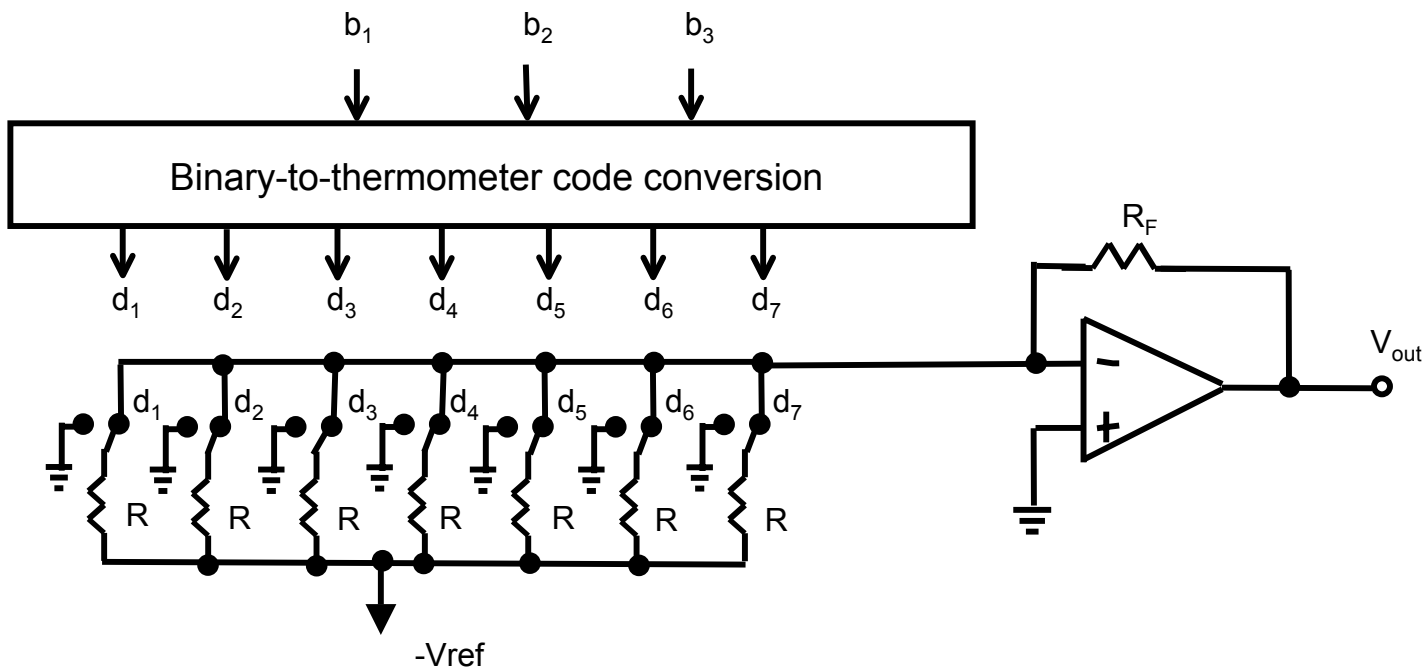
- Advantages over its binary-weighted counterpart
  1. low DNL errors
  2. guaranteed monotonicity
  3. reduced glitching noise
- Does not increase the size of the analog circuitry compared to a binary-weighted approach

Thermometer-Code DACs (Cont.)

- Total area required by the transistor switches is the same (compared to binary-weighted)

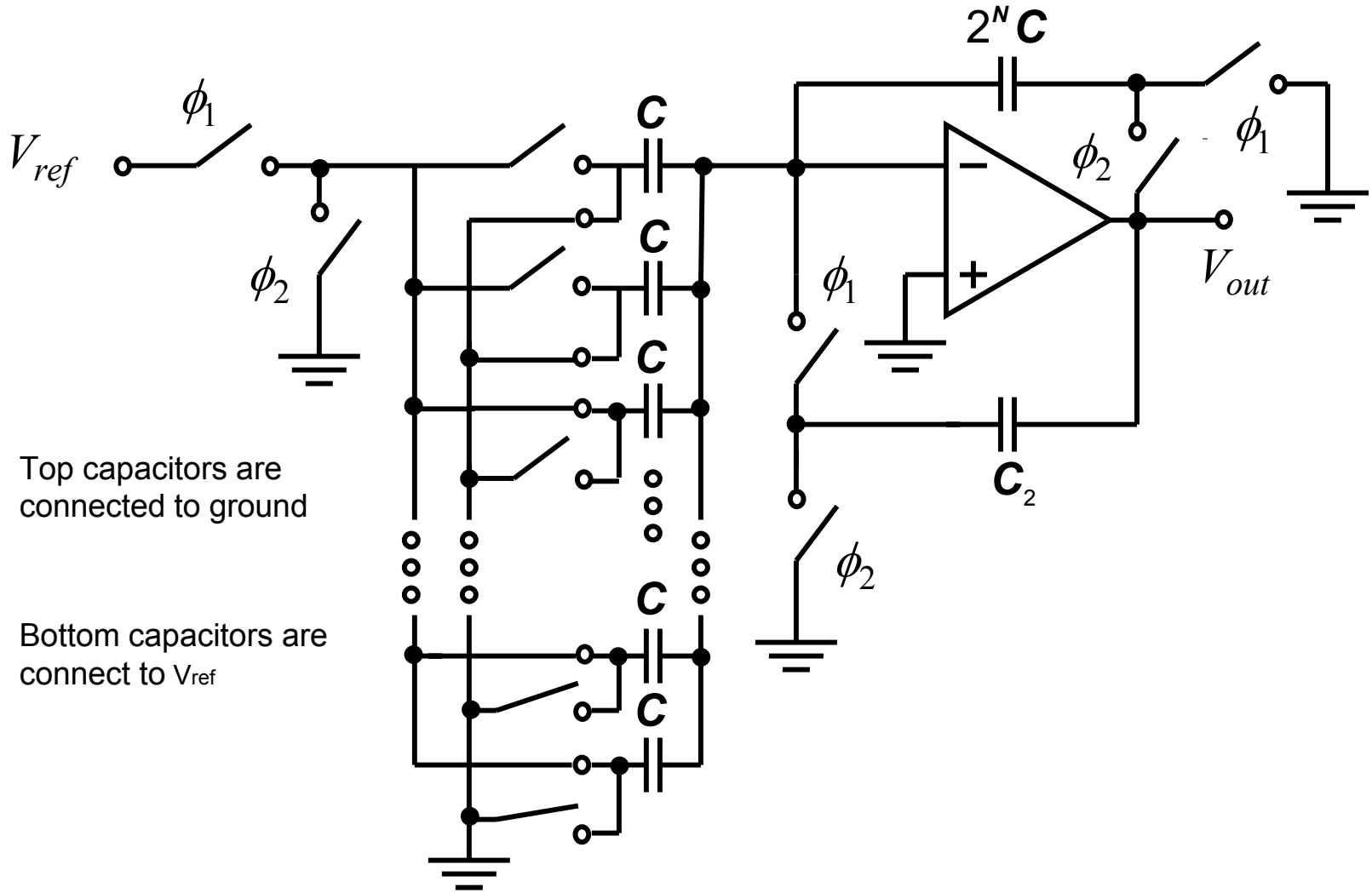
  All transistor switches are of equal sizes since they all pass equal currents
- Examples

  1. thermometer-code resistor DAC



Thermometer-Code DACs (Cont.)

2. thermalmeter-code charge-redistribution DAC

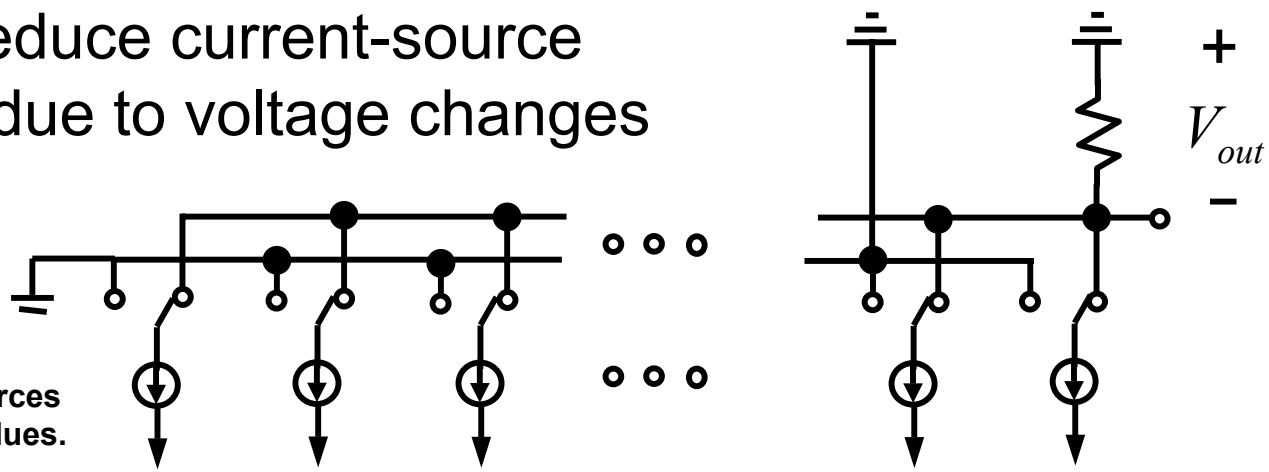


Thermometer-Code Current-Mode DAC

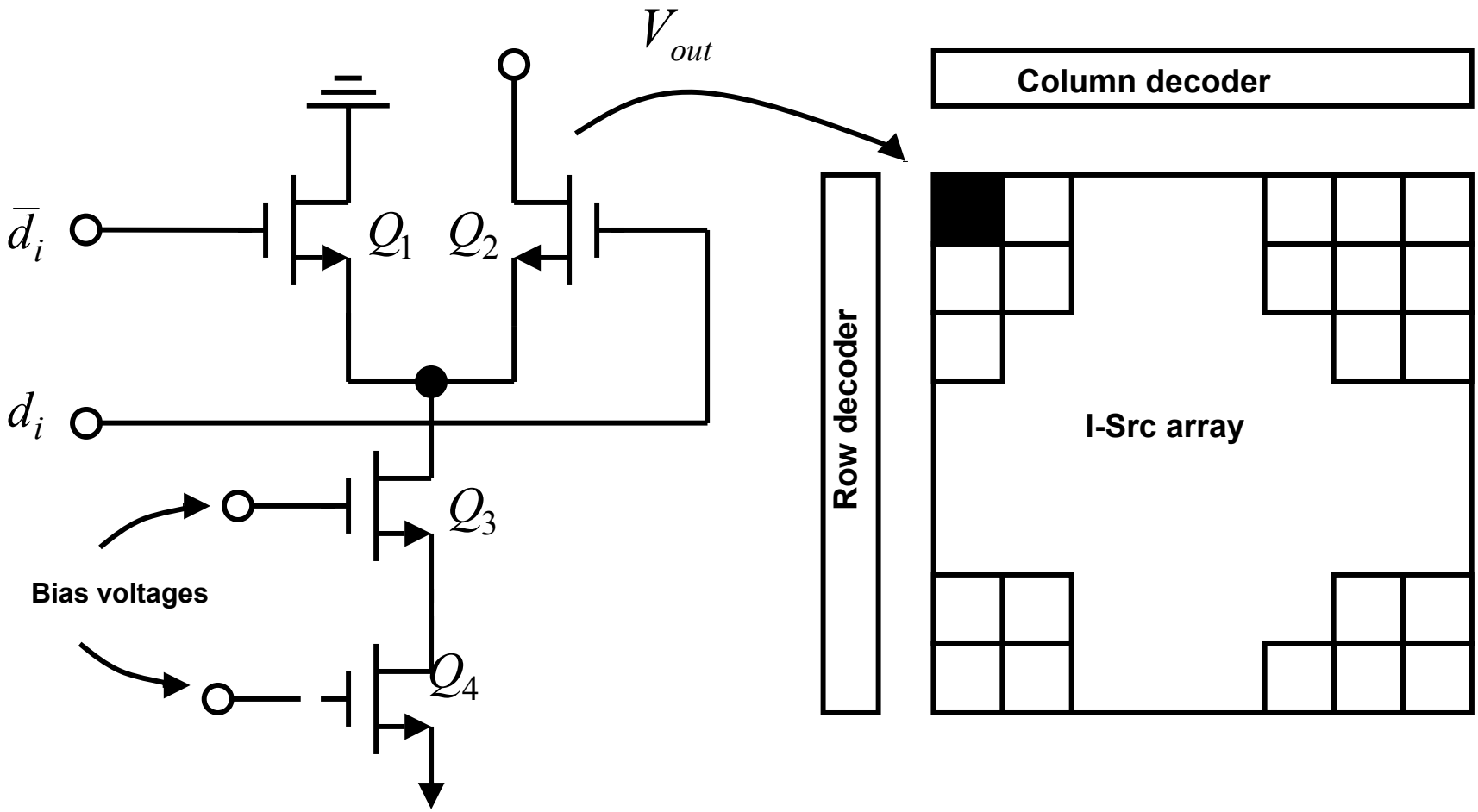
- Row and column decoders
- Inherent monotonicity
- Good DNL errors

  INL errors depend on the placement of the current sources
- In high-speed applications

  1. The output current feeds directly into an off-chip 50 Ω or 75 Ω resistor, rather than an output OPAMP.
  2. Cascode current sources are used to reduce current-source variation due to voltage changes in V_{out}



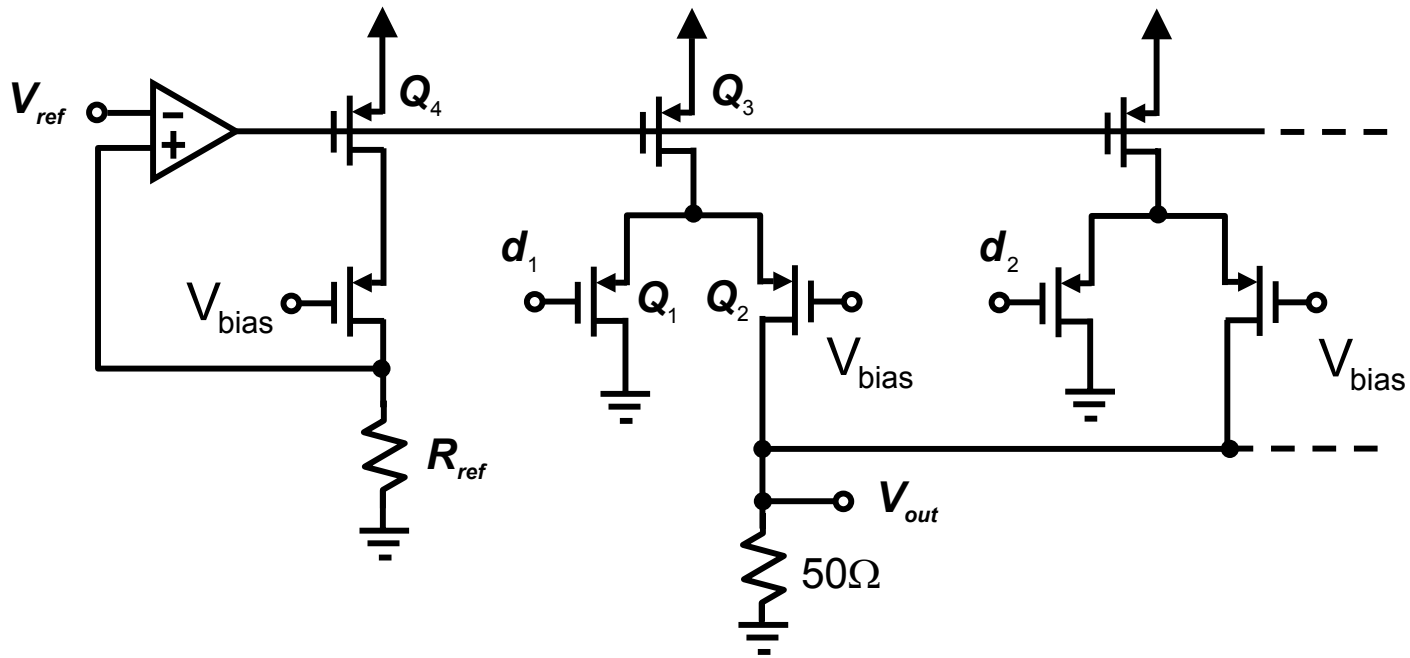
Thermometer-Code Current-Mode DAC (Cont.)



Thermometer-Code Current-Mode DAC (Cont.)

- Precisely timed edges are needed
  1. If both $\overline{d}_i$ and d_i are low simultaneously, the drain of Q_3 is pulled low and the circuit takes longer time to respond.
  2. If both $\overline{d_i}$ and d_i are high simultaneously, V_{out} is shorted to ground.
- To avoid the use of the two logic levels, the gate of Q_2 should be connected to a dc bias voltage

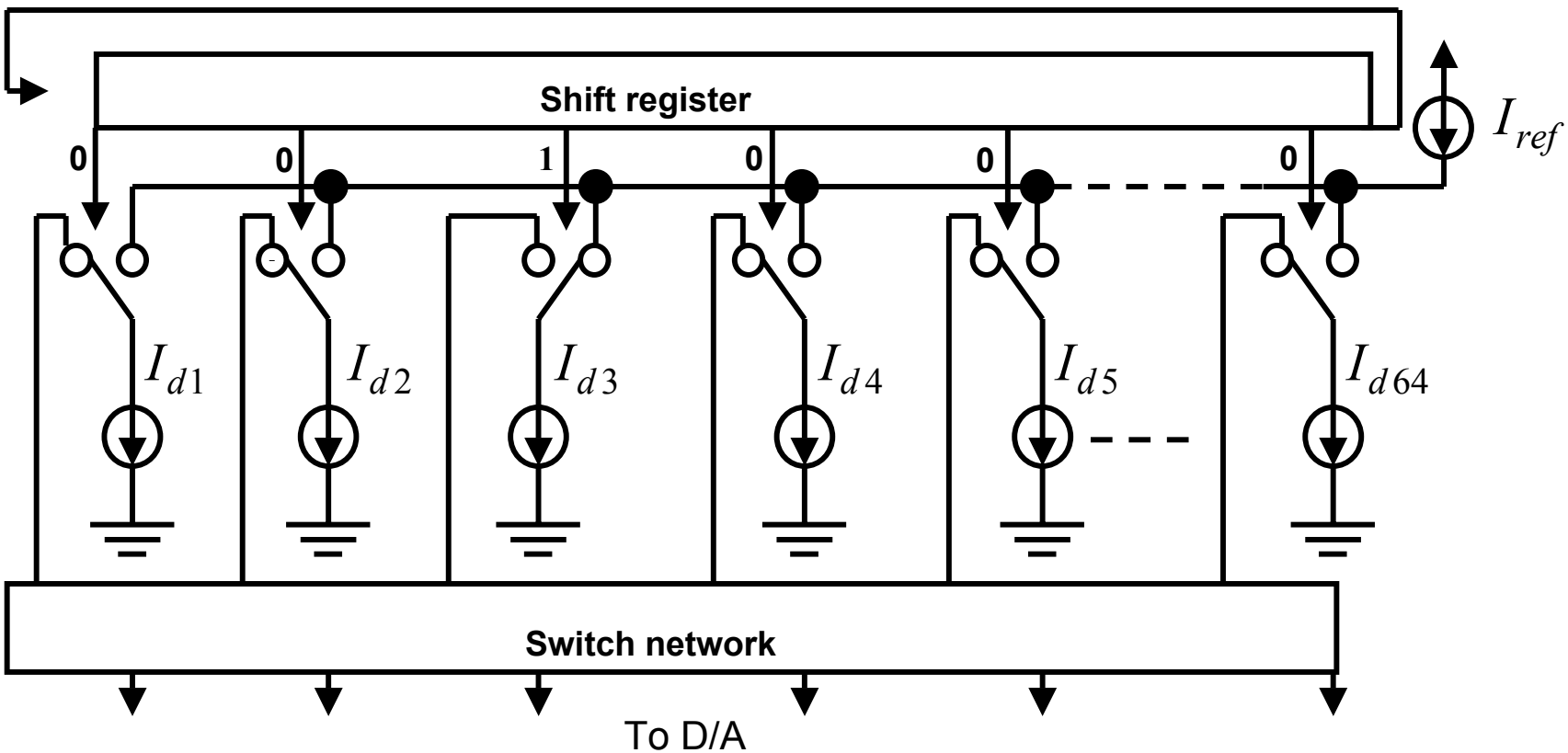
Thermometer-Code Current-Mode DAC (Cont.)



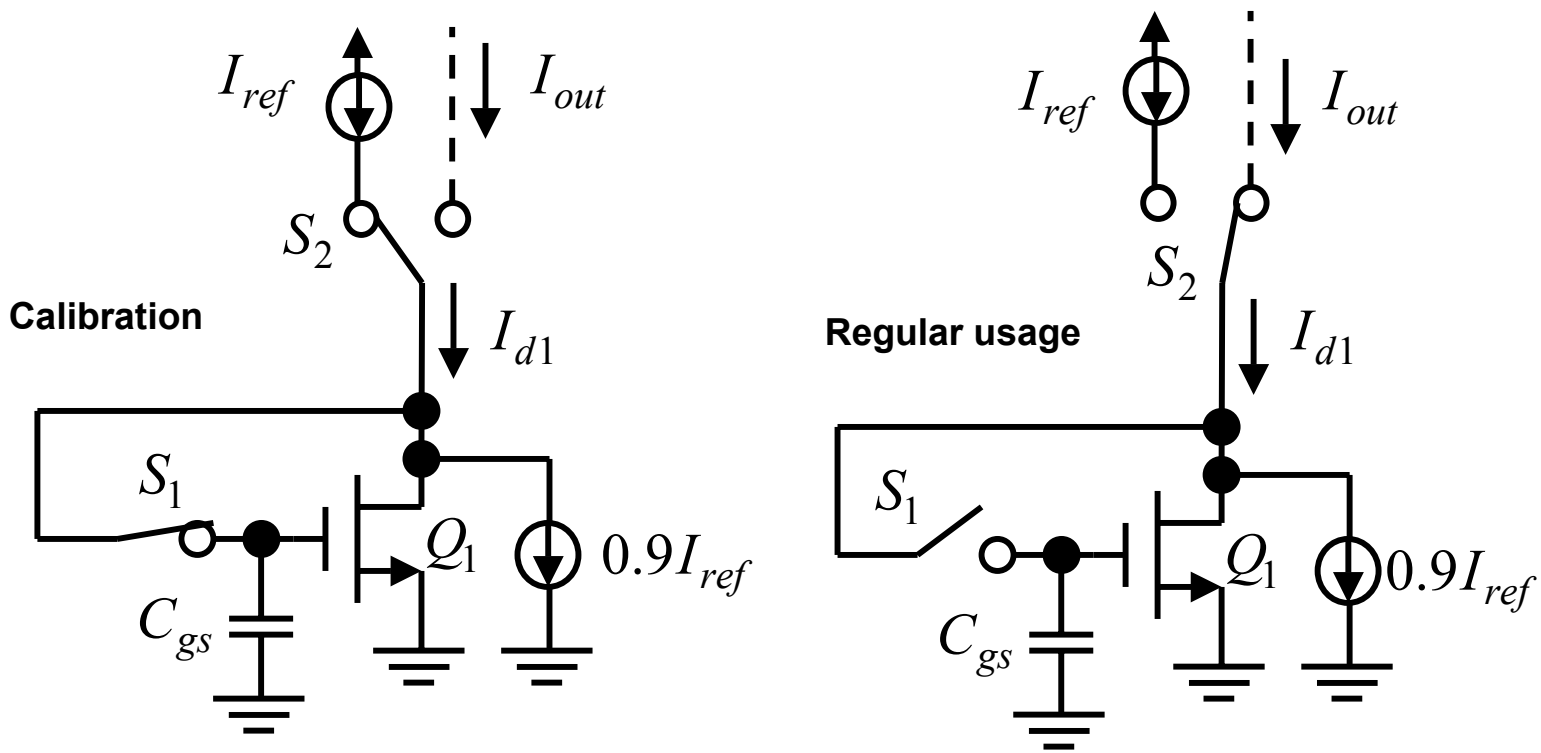
- Can be clocked at the maximum rate without the need for precisely timed edges
- Q_2 and Q_3 effectively form a cascode current source when they drive current to the output.
- To maximize speed, the voltage swing at the common connection (e.g. Q_1 , Q_2 and Q_3) of the current switches should be small.

Dynamically Matched Current Sources

- A method for realizing very well-matched current sources (up to 10-bit accuracy) for audio DACs
- Continuously and cyclically calibrate MSB portions
- 16 - bit example



Dynamically Matched Current Sources (Cont.)



1. 6MSBs were realized using a thermometer code
2. Since the accuracy requirements are reduced for the remaining bits, a binary array was used in their implementation.

Dynamically Matched Current Sources (Cont.)

3. 64 accurately matched current sources for the 6 MSBs
   - current sources are calibrated
   - dynamically setting current sources
   - even though only 63 are required, the extra one is needed so that DAC can continuously operate when one of them is being calibrated
4. major limitation in matching 64 current sources is due to the differences in clock feedthrough and charge injection switches S_i
   - the best way is to minimize them
     - ⇨ large C_{gs} and large V_{gs} of Q_1
     - ⇨ Q_1 only source a small current
     - ⇨ W_{small}/L_{large} can be used for Q_1

Dynamically Matched Current Sources (Cont.)

- large C_{gs} to minimize leakage current effect before current sources are recalibrated
- dummy transistor can be added to S_i
- other methods to minimize these errors are referred to switched-current (SI) papers

Hybrid Converters

- Combine the advantages of different approaches
- It's quite common to use a thermometer-code approach for the top few MSBs while using a binary-scaled technique for the lower LSBs
  - glitching is significantly reduced and accuracy is high
  - circuit area is saved with a binary-scaled approach for LSBs
- Examples

  1. Resistor-capacitor hybrid DAC
  2. Segmented DAC