High-Resolution Sigma-Delta Oversampling Converters

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OUTLINE

- Introduction
- Relaxed anti-alias filtering
- Quantization noise
- Oversampling
- Noise shaping
- SDM structures
- Stability
- Idle tone and dither
- High-order sigma-delta modulator synthesis tool (HOST)
- Data weighted averaging (DWA)
- VLSI implementation
- Simulation
- Bandpass oversampling converters
- Summary

Introduction

- Delta-sigma ADC/DAC
  = Sigma-delta ADC /DAC
  = Oversampling ADC /DAC
- Developed three decades ago
- Achieved commercial implementation due to recent advances in mixed-mode analog-digital VLSI technology
- Recently very popular for high-resolution medium-to-low speed applications
- Relax the requirements placed on the analog circuitry at the expense of more complicated digital circuitry
  – This tradeoff becomes more desirable for modern submicron technologies with 3.3V power supplies. (even lower voltage for deep submicron)
    1. Complicated high-speed digital circuitry is more easily realized in less area

Introduction (Cont.)

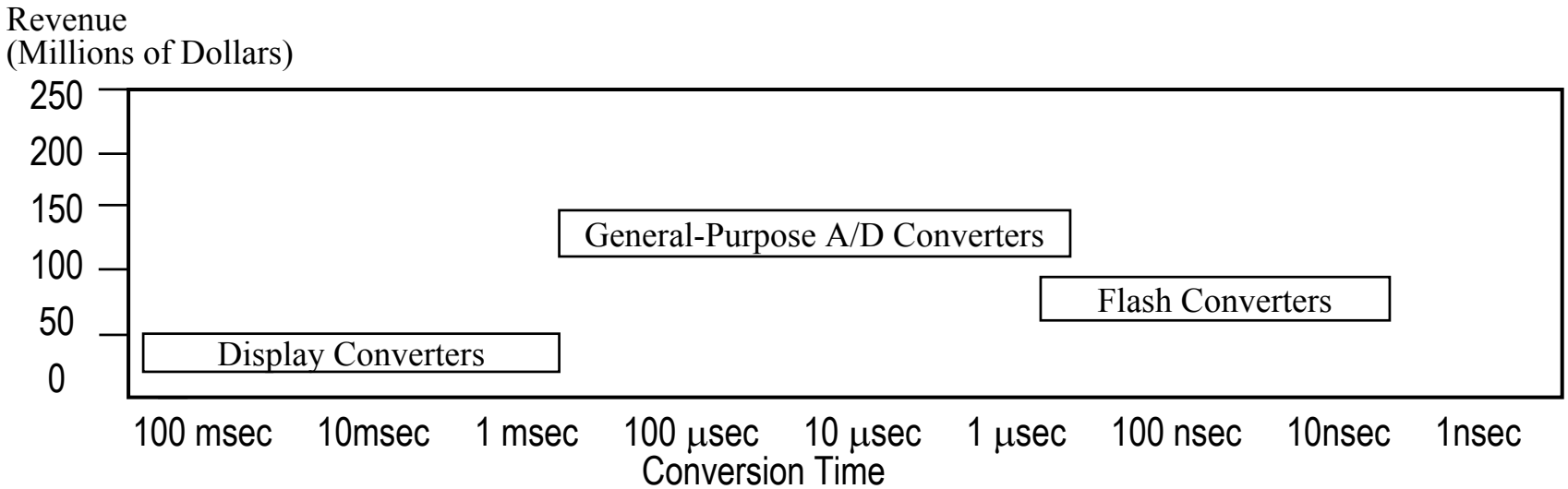
2. High-resolution analog circuitry is complicated by
   (i) low power supply voltages
   (ii) poor output impedance, caused by short-channel effects
3. Reduced requirements on matching tolerances and amplifier gain

– Simplify the requirements of analog anti-aliasing filters for ADCs and smoothing filters for DACs (on chip or off chip)
– S/H is usually not required at the input of an oversampling ADC (internal integrators have the function)

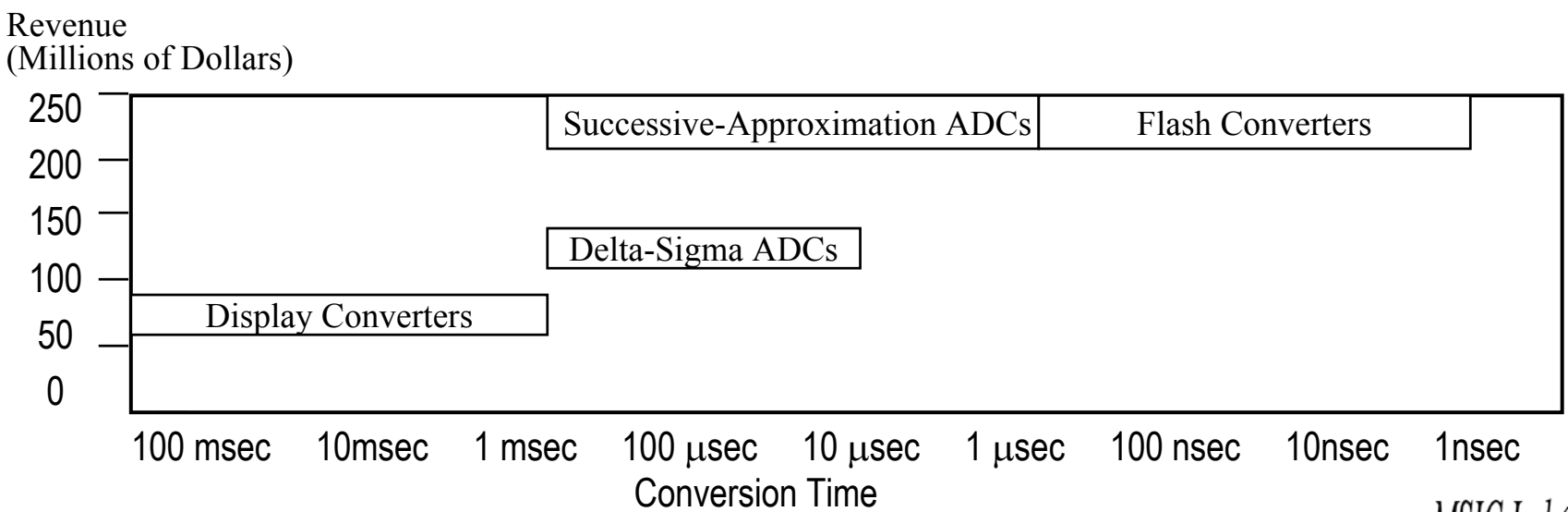
- Extra bits of resolution can be extracted from converters that sample much faster than the Nyquist rates by spectrally shaping the quantization noise through the use of feedback.

Delta-Sigma Market Potential

- ADC revenue & conversion rate - 1989



- Estimated ADC revenue & conversion rate - 1994



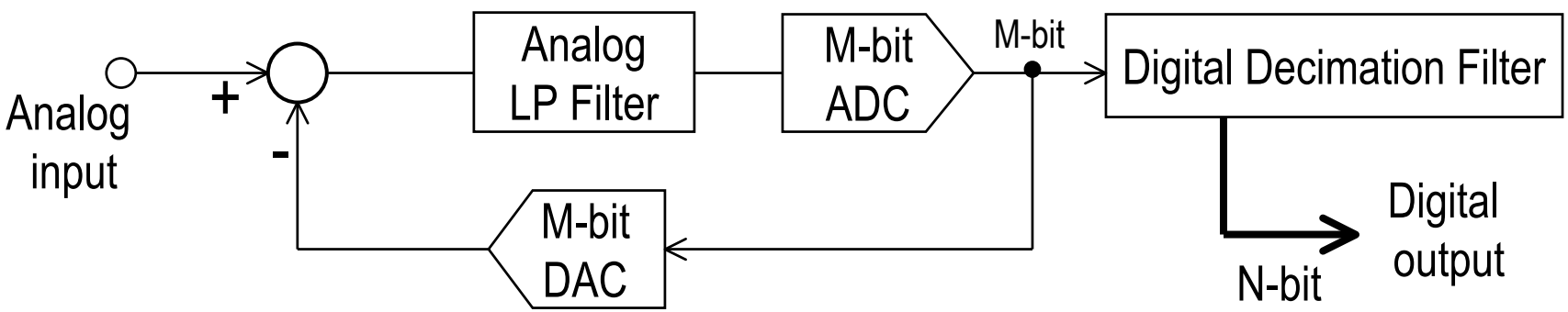
Applications

- Audio/Voice codec
- DVD
- High precision measurement
- ISDN
- ADSL
- Mobile (Cellular) phone
- Many others

Brief Overview of Sigma-Delta A/D Structure

- Sigma-delta ADC consists of two basic blocks
  - Analog negative feedback loop
    Oversamples & processes analog input
  - Digital decimation filter
    Perform system-level filtering with performance unachievable in analog form

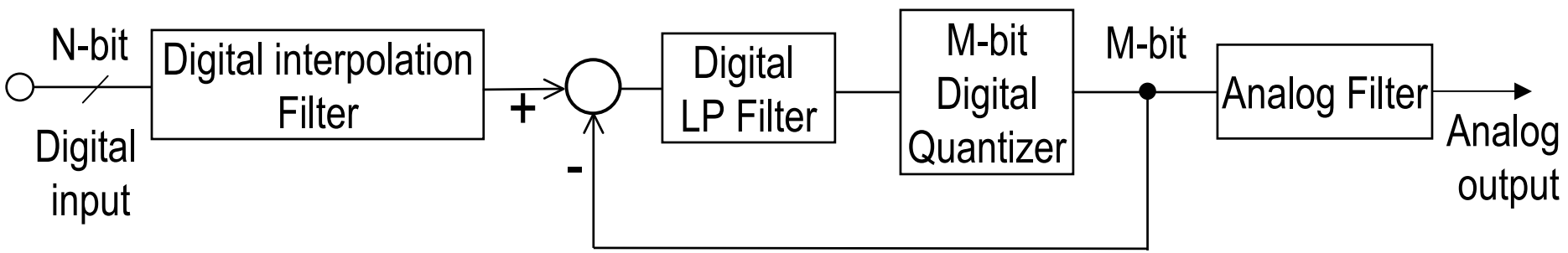
- Structure of an N-bit ADC with an M-bit internal ADC and DAC



Brief Overview of Sigma-Delta D/A Structure

- Sigma-delta DAC consists of three blocks
  - Digital interpolation filter
  - Digital negative feedback loop
  - Analog filter including digital-to-analog interface

- Structure of an N-bit DAC with an M-bit internal quantizer



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Signal Spectra of Zero-Width Samples

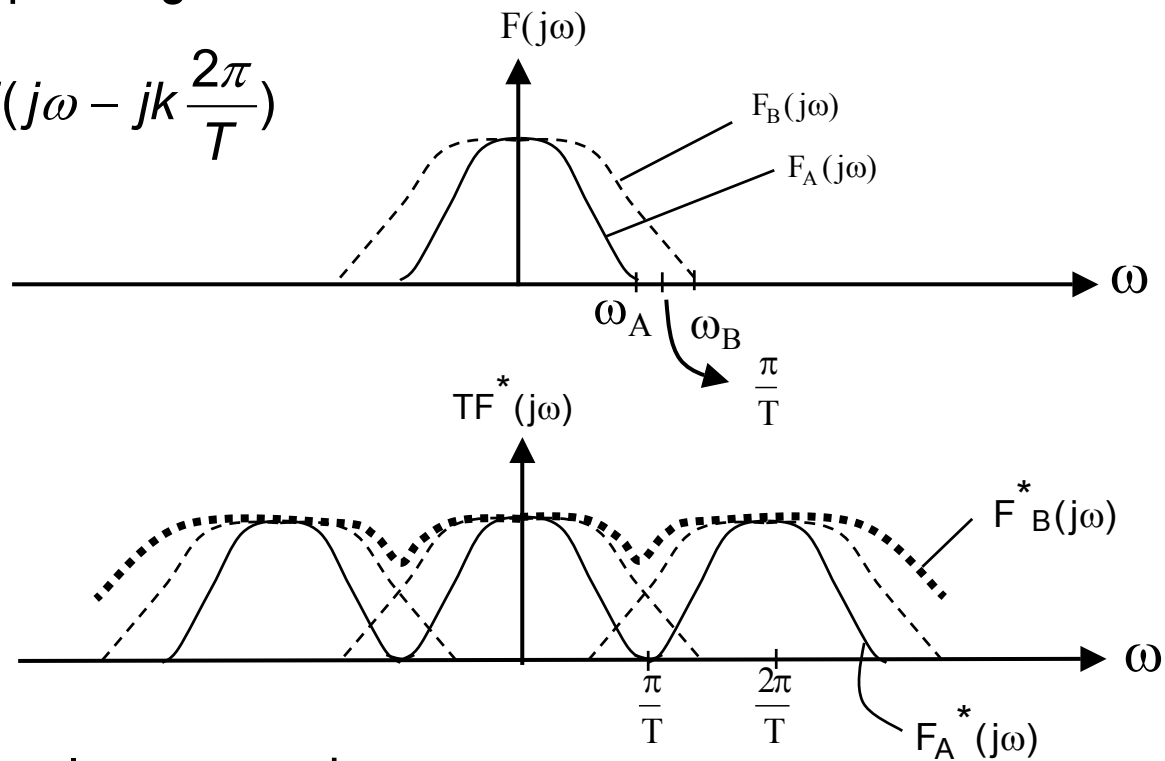
- For zero-width sampling

  $f(t) \rightarrow F(j\omega)$ ⋯⋯⋯⋯ Original signal

  $f^*(t) \rightarrow F^*(j\omega)$ ⋯⋯⋯ Sampled-data signal

  – Spectrum of sampled signal

$$F^*(j\omega) = \frac{1}{T}\sum_{k=-\infty}^{\infty} F(j\omega - jk\frac{2\pi}{T})$$



- Continuous-time signals $f_A(t)$ and $f_B(t)$
- Sample-data signals $f_A^*(t)$ and $f_B^*(t)$

Nyquist Theorem

- Replicas forming $F_B^*(j\omega)$ overlap

  This phenomenon is called aliasing or folding.

  It is a nonlinear distortion

- Low-pass filter

$$H(j\omega) = \begin{cases} 1 & ; \quad |\omega| \le \dfrac{\pi}{T} \\ 0 & ; \quad |\omega| > \dfrac{\pi}{T} \end{cases}$$

$$F_A^*(j\omega)H(j\omega) = F_A(j\omega)$$

  – The continuous-time signal $f_A(t)$ is recovered.

  But no such operation can regain $F_B(j\omega)$ from $F_B^*(j\omega)$

  – Nyquist first observed this phenomenon

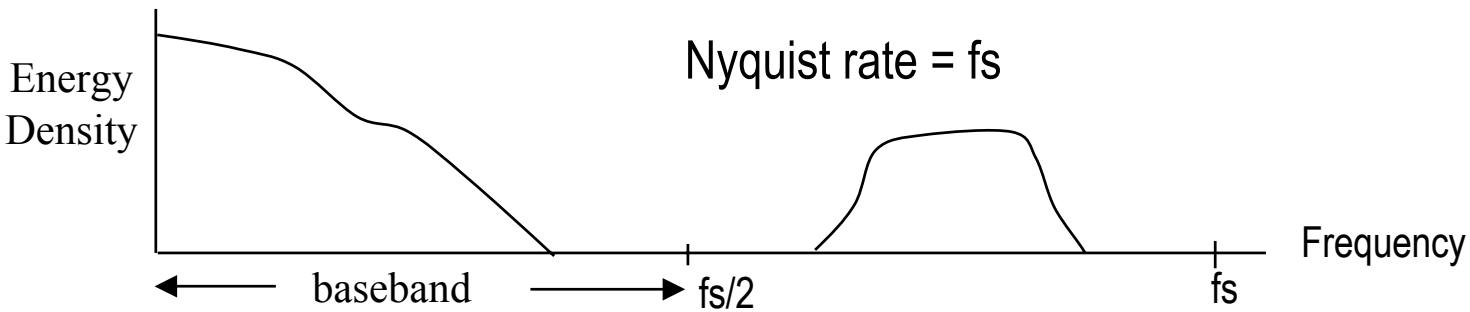
  ↑ Nyquist theorem

Sampling

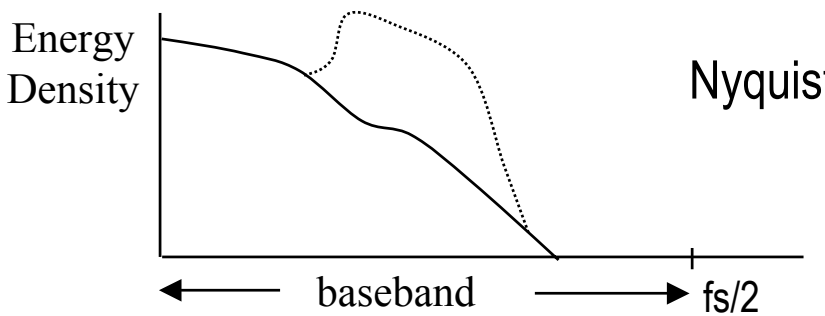
- Nyquist theorem :

  To avoid aliasing, sampling frequency must be at least twice of the signal to be sampled.

- Alias
  - Spectrum before sampling

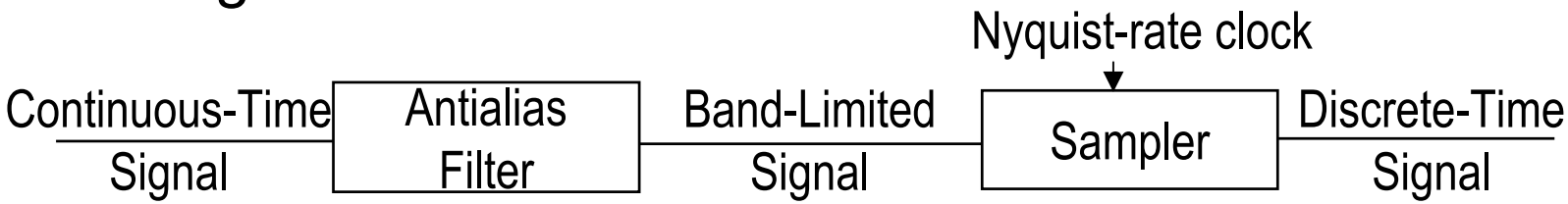


  - Spectrum after sampling

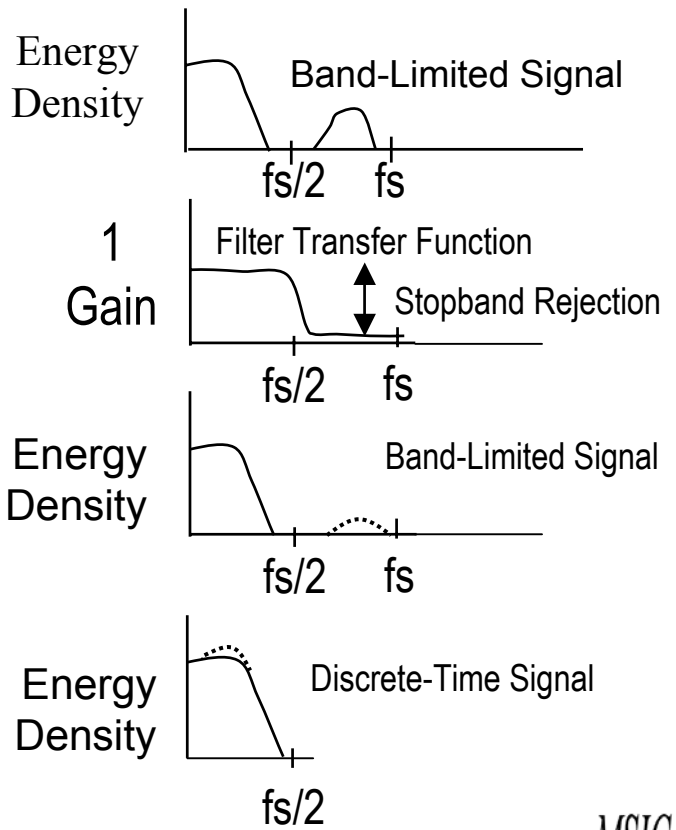


Anti-Alias Filtering for Nyquist-Rate Sampling

- Block diagram

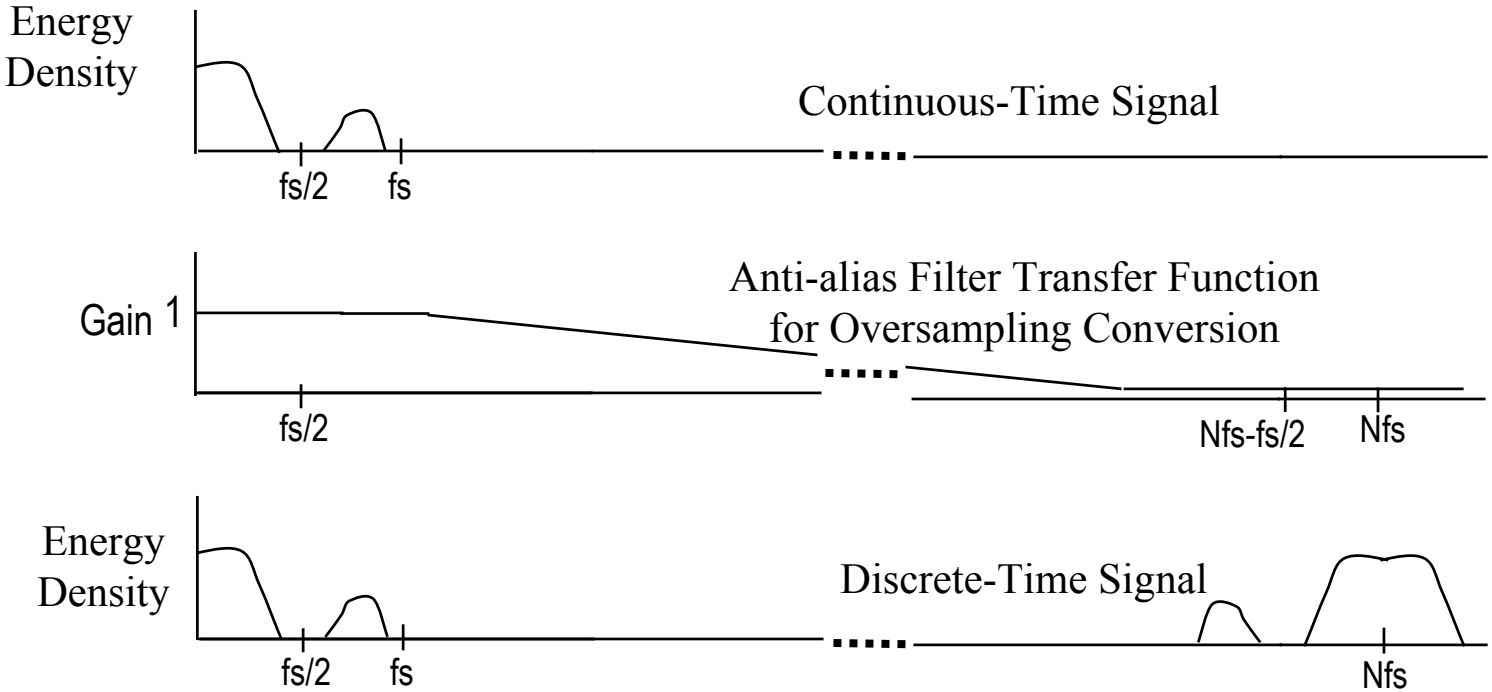


- Major Difficulties :
  - Brick wall anti-aliasing filters (AAF) required
  - Non-linear phase distortion in baseband caused by AAF
  - SIN(X)/X spectral droop in baseband due to sample/hold effect
  - All non-idealities (both quantization noise and circuit noise) of the A/D show up directly in baseband

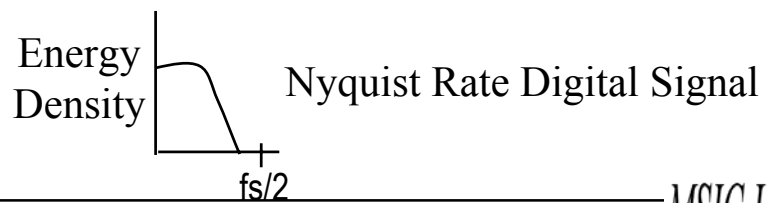


Relaxed Anti-Alias Filtering for Oversampling Technique

- Anti-aliasing

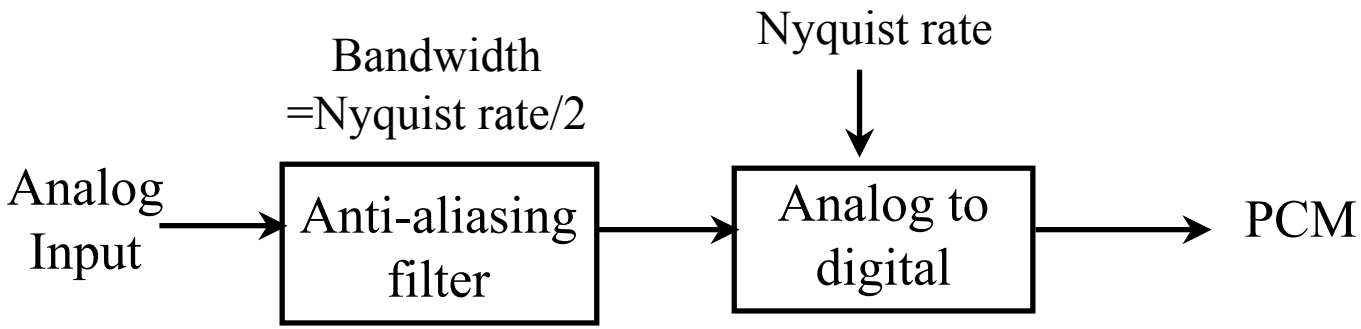


- Digital filtering/decimation
  - High performance digital filter is required

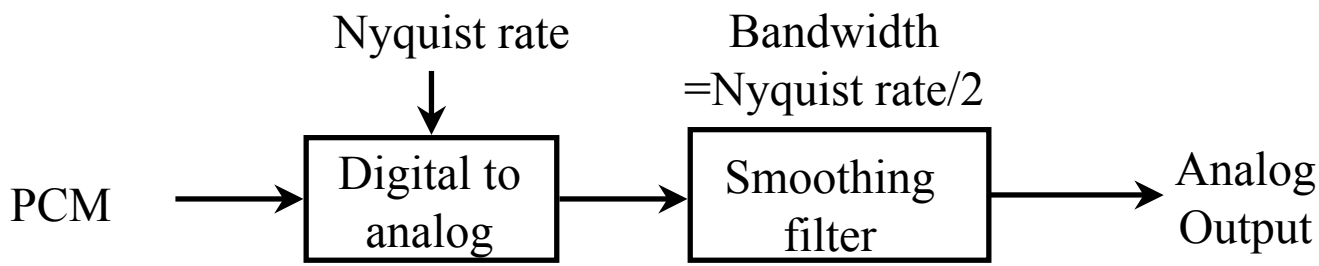


Conventional Conversion vs. Sigma-Delta Conversion

- Nyquist ADC (pules-code modulation, PCM)

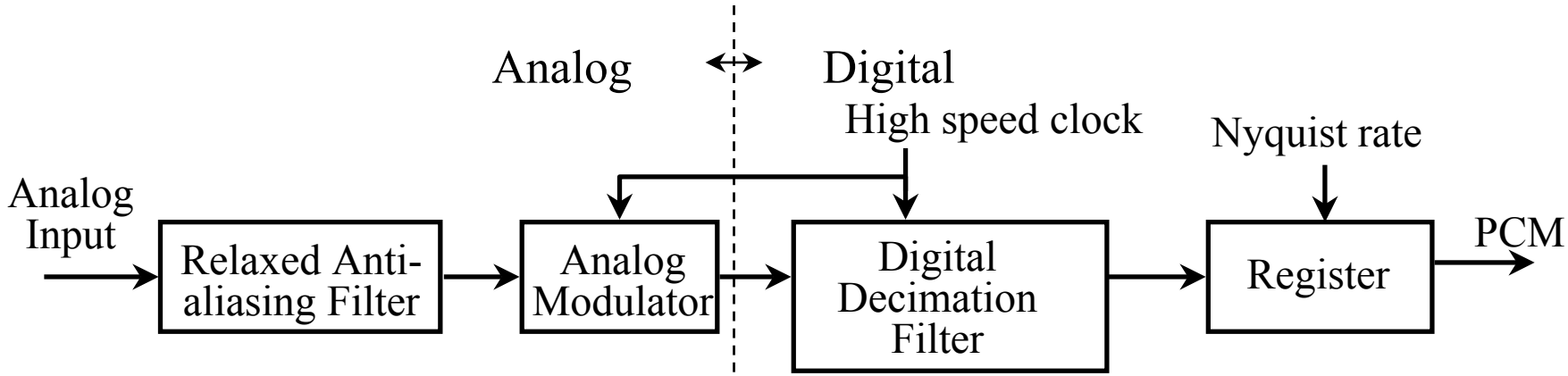


- Nyquist DAC

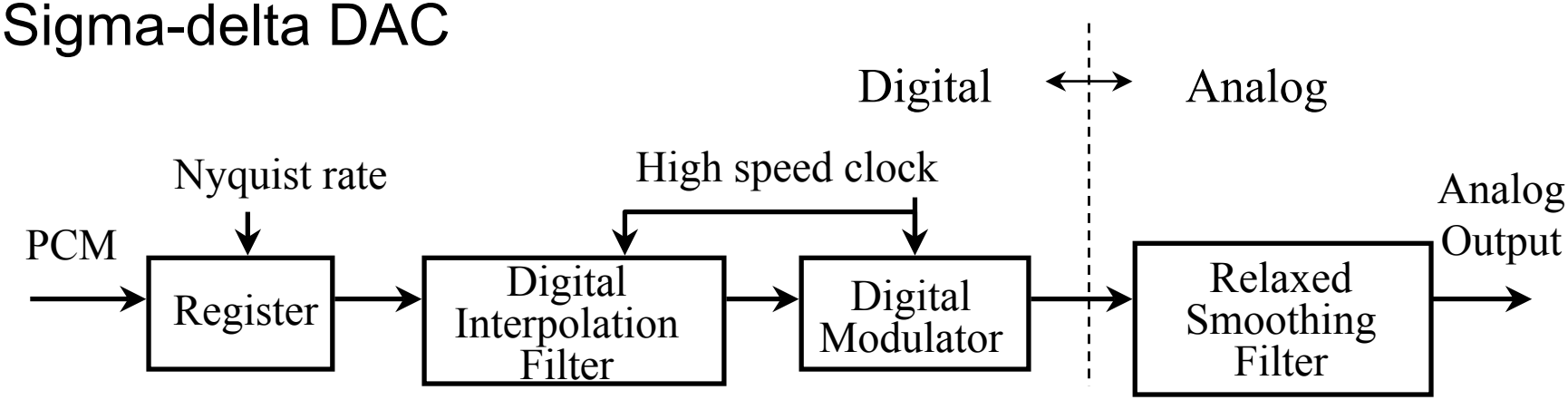


•Conventional Conversion vs. Sigma-Delta Conversion (Cont.)

- Sigma-delta ADC



- Sigma-delta DAC



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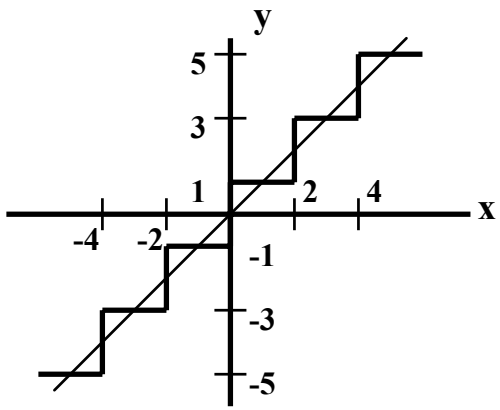
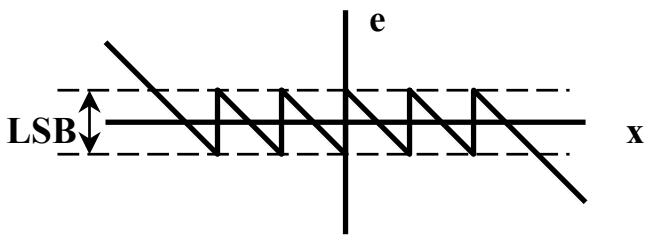
Quantization Noise

- Random signal assumption —— qantization error *e* is uniformly distributed between +LSB/2 and -LSB/2

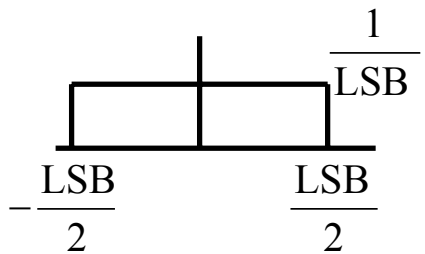
transfer curve



quantization error



probability density function



- Qantization noise power and signal-to-noise ratio (SNR)

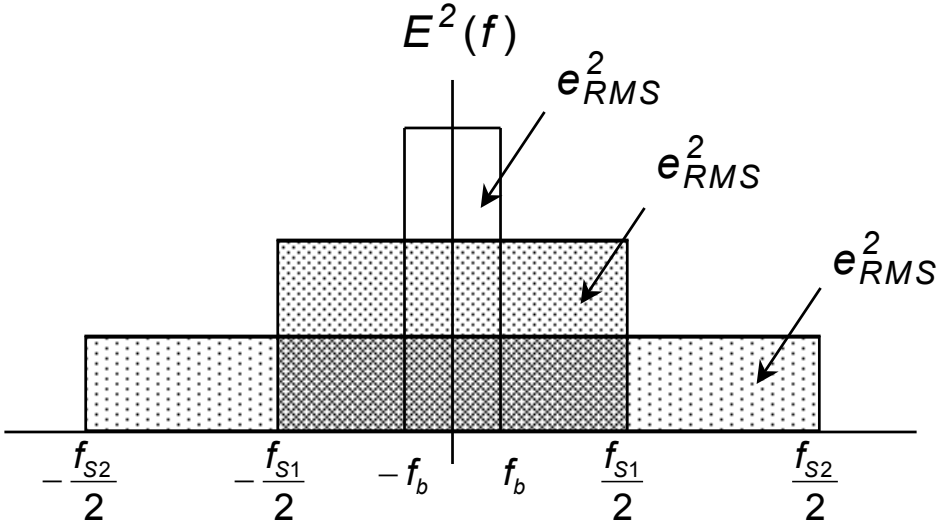
$$e_{RMS}^2 = \int_{-\infty}^{\infty} e^2 p(e)de = \frac{1}{LSB}\int_{-\frac{LSB}{2}}^{\frac{LSB}{2}} e^2 de = \frac{LSB^2}{12}$$

For a sinusoidal input, $x(t) = A\sin(\omega t)$, A is full scale magnitude, b is number of bit and $\mathrm{LSB} = 2\mathrm{A}/2^{\mathrm{b}}$, then peak SNR (PSNR)

$$PSNR = \frac{P_{SIGNAL}}{P_{NOISE}} = \frac{A^2/2}{e_{RMS}^2} = 10\log\left(\frac{A^2/2}{LSB^2/12}\right) = 6.02b + 1.76\ (dB)$$

Quantization Noise Spectrum

- White noise assumption ——power spectral density is constant



$$E^2(f) = \frac{LSB^2}{12}\frac{1}{fs}$$

– Quantization noise density is inversely proportional to the sampling rate

– If signal bandwidth is f_b and oversampling ratio OSR= $f_S / 2f_b$

total noise in signal band = $P_{NOISE} = \frac{LSB^2}{12}\frac{2f_b}{f_S} = \frac{LSB^2}{12}\frac{1}{OSR}$

$$PSNR = 6.02b + 1.76 + 10\log(OSR) \quad (dB)$$

⇨ Doubling OSR increases 3dB SNR

Limitation of Oversampling

- $P_{NOISE} = \frac{LSB^2}{12}\frac{1}{OSR}$
  - S/N is improved by *OSR*
  - LSB becomes $\sqrt{OSR}$ smaller
  - Resolution is increased by $\log_2(\sqrt{OSR})$
- The problem with 1-bit (or even multi-bit) converters is that the desired resolution and bandwidth requires unreasonable oversampling ratios

13 Bits,	4KHz	VOICE ⟺	1 Bit, 537GHz
			3 Bits, 134GHz
13 Bits,	144KHz	ISDN ⟺	1 Bit, 19.3THz
			3 Bits, 4.8THz
16 Bits,	20KHz	Digital HIFI ⟺	1 Bit, 172THz
			3 Bits, 43THz

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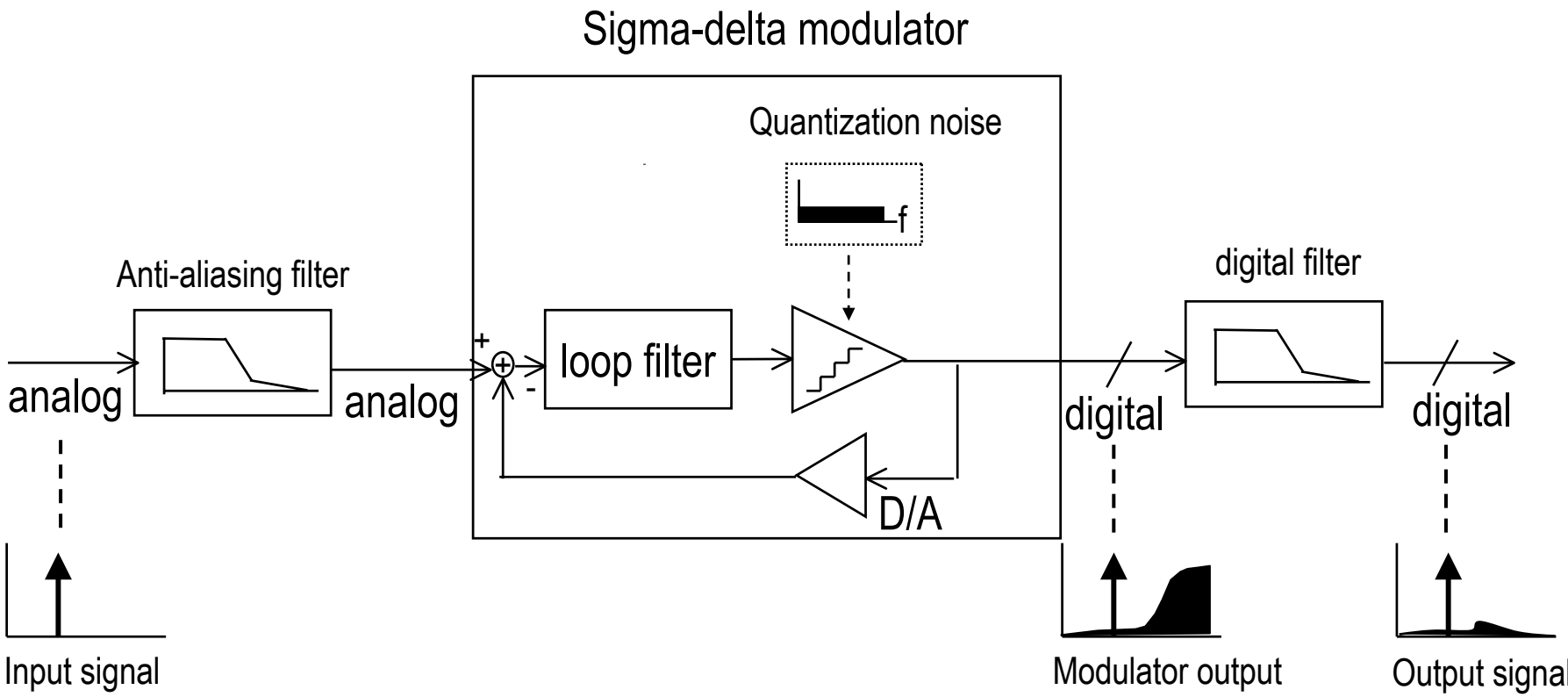
Sigma-Delta Modulation : Noise-Shaping + Oversampling

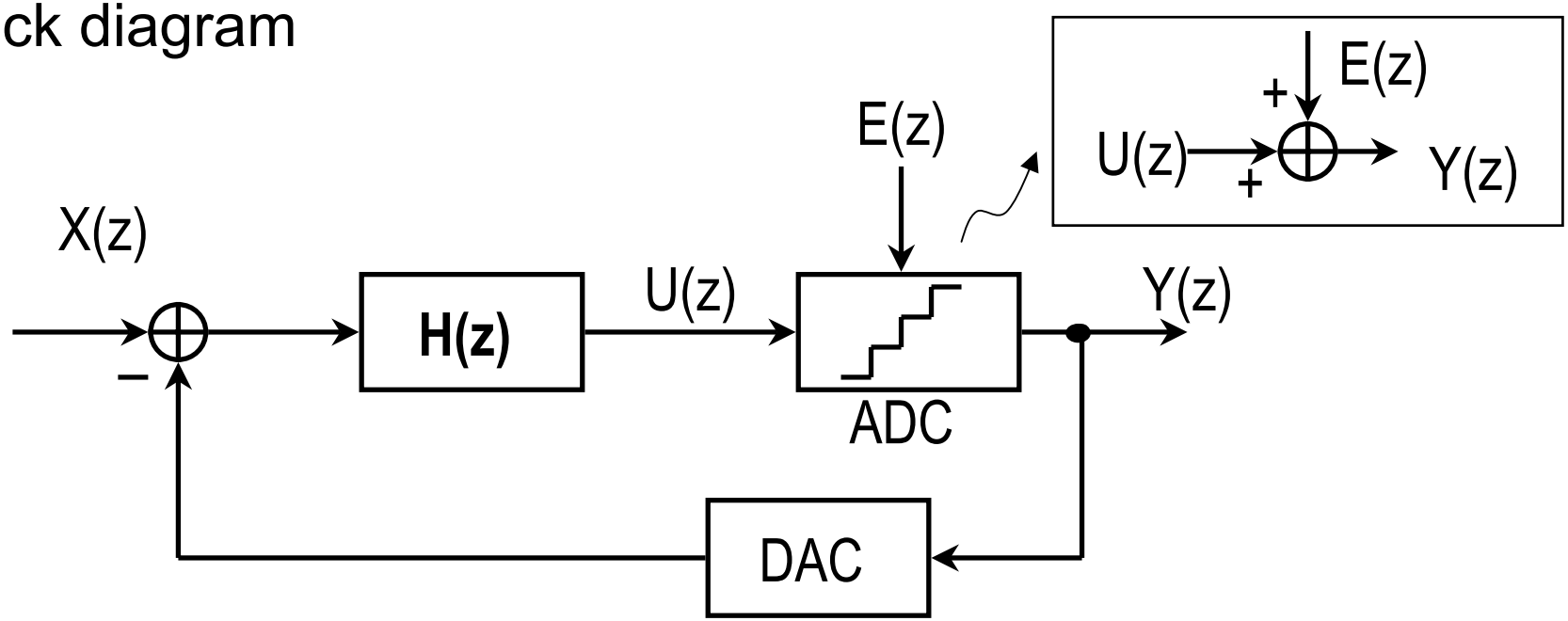
- Change the energy spectrum of quantization noise.

  Shift low frequency energy to high frequency stopband of decimation filter.
- Spectrum of sigma-delta ADC

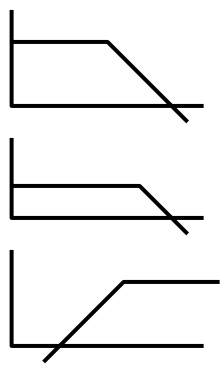


Sigma-Delta Modulators

- Block diagram



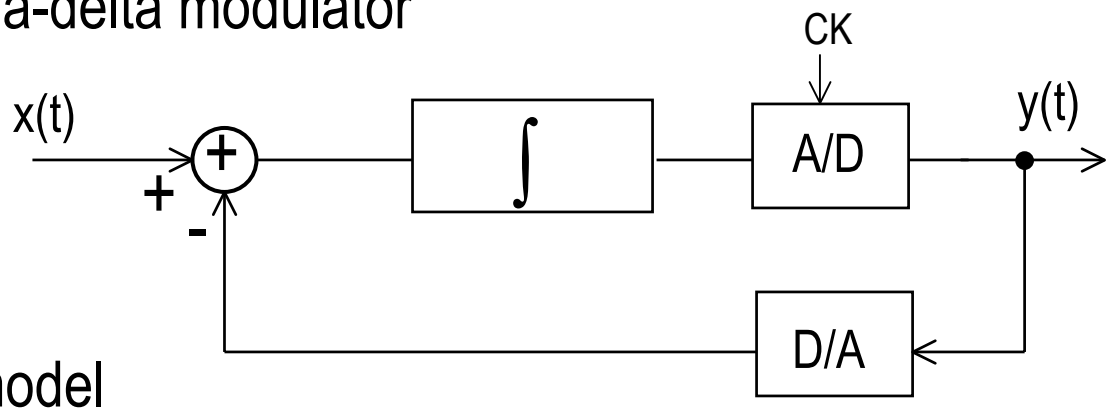
$$Y(z) = \frac{H(z)}{1+H(z)}X(z) + \frac{1}{1+H(z)}E(z) = STF(z)X(z) + NTF(z)E(z)$$



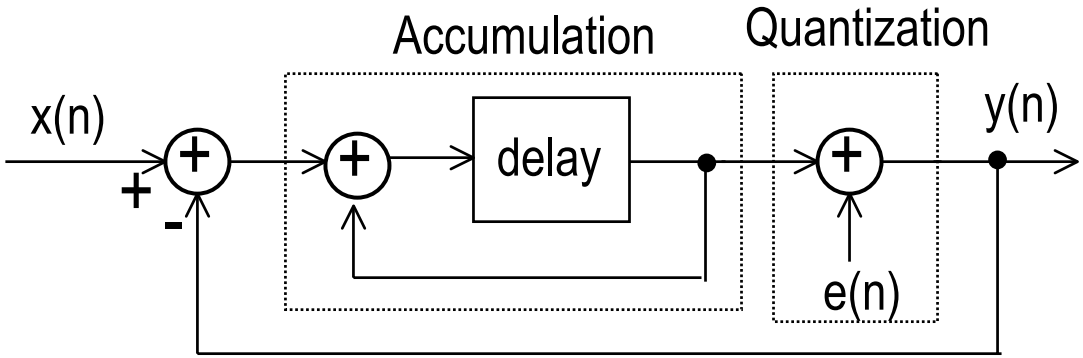
- H(z) : high-gain lowpass function
- STF : Signal Transfer Function (lowpass)
- NTF : Noise Transfer Fuction (highpass)

Noise Shaping

- First-order sigma-delta modulator



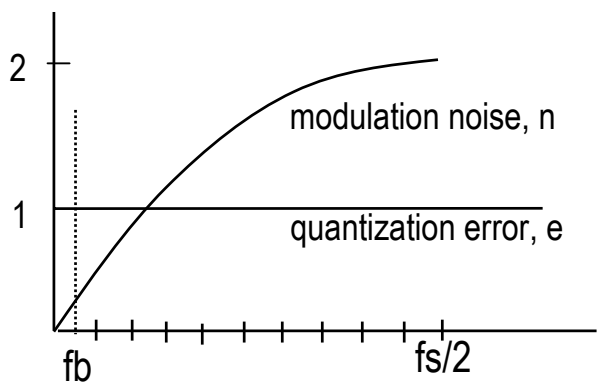
- Discrete-time model



$$y(n) = x(n-1) + e(n) - e(n-1)$$

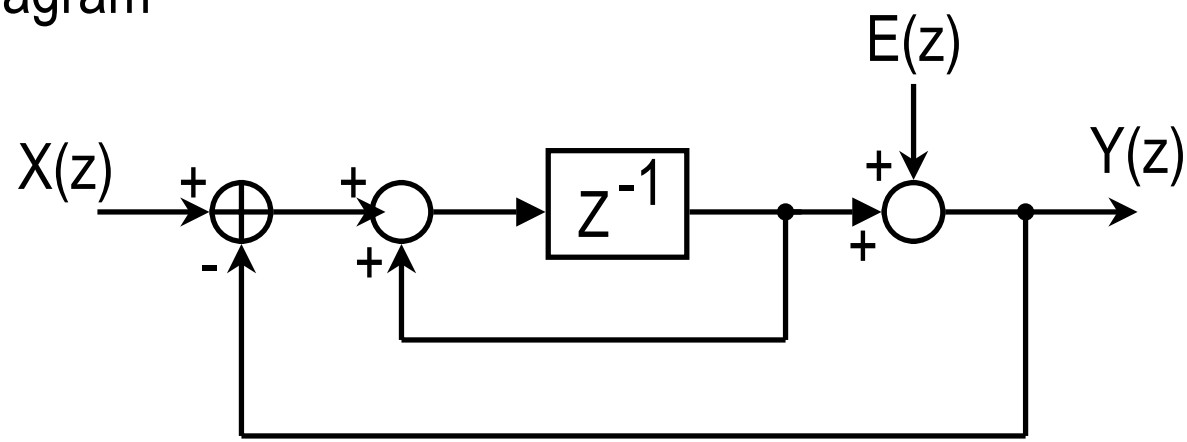
$$Y(z) = X(z)Z^{-1} + E(z)(1 - Z^{-1})$$

- Effect of feedback on noise
  - Frequency characteristic of $\left|1 - Z^{-1}\right|$



First-Order Sigma-Delta Modulator

- Block diagram



$$Y(z) = z^{-1}X(z) + (1 - z^{-1})E(z)$$

- Noise power in the baseband

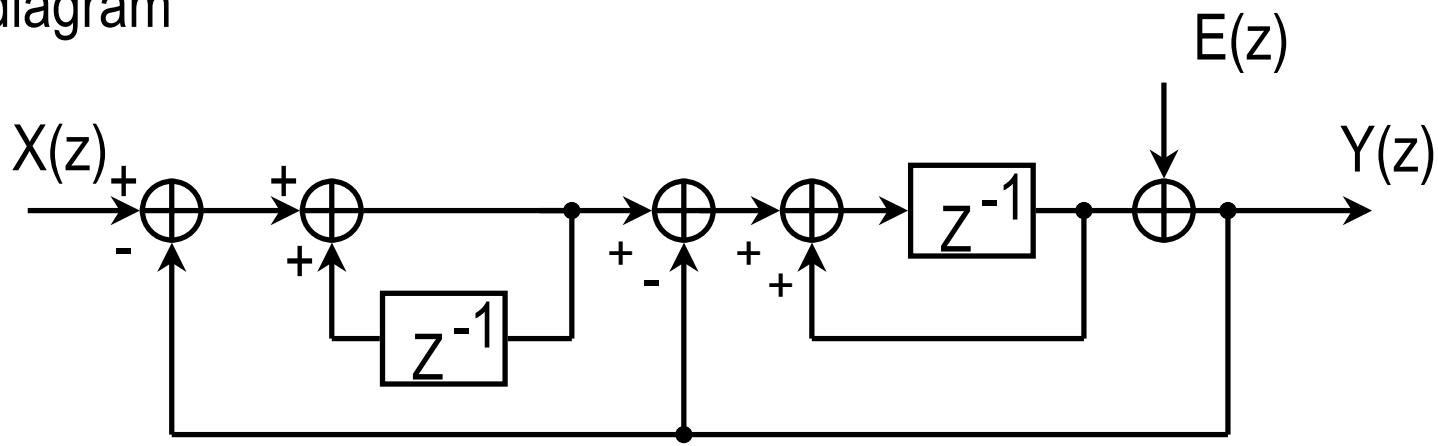
$$P_{NOISE} = \int_{-f_b}^{f_b} e_{RMS}^2 \left|(1 - z^{-1})\right| df = \frac{LSB^2}{12}\frac{\pi^2}{3}\left(\frac{2f_b}{f_S}\right)^3 = \frac{LSB^2}{12}\frac{\pi^2}{3}\left(\frac{1}{OSR}\right)^3$$

- Doubling the OSR increases 9dB SNR

$$PSNR = 6.02b + 1.76 - 5.17 + 30\log(OSR) \ \ (dB)$$

Second-Order Sigma-Delta Modulator

- Block diagram



$$Y(z) = z^{-1}X(z) + (1 - z^{-1})^2 E(z)$$

- Noise power in the baseband

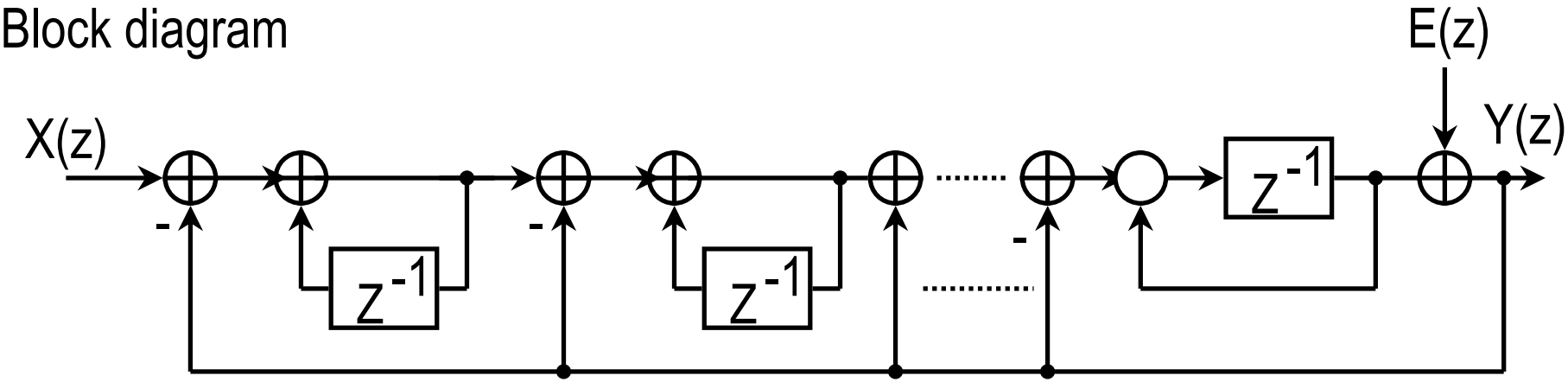
$$P_{NOISE} = \int_{-fb}^{fb} e_{RMS}^2 \left|(1 - z^{-1})^2\right| df = \frac{LSB^2}{12}\frac{\pi^4}{5}\left(\frac{2fb}{fs}\right)^5 = \frac{LSB^2}{12}\frac{\pi^2}{3}\left(\frac{1}{OSR}\right)^5$$

- Doubling the OSR increases 15dB SNR

$$PSNR = 6.02b + 1.76 - 12.9 + 50\log(OSR) \ \ (dB)$$

Nth-Order Sigma-Delta Modulator

- Block diagram



$$Y(z) = z^{-1}X(z) + (1 - z^{-1})^N E(z)$$

- Noise power in the baseband

$$P_{NOISE} = \int_{-fb}^{fb} e_{RMS}^2 \left|(1 - z^{-1})^N\right| df = \frac{LSB^2}{12} \frac{\pi^{2N}}{2N+1} \left(\frac{2fb}{fs}\right)^{2N+1}$$

$$= \frac{LSB^2}{12} \frac{\pi^{2N}}{2N+1} \left(\frac{1}{OSR}\right)^{2N+1}$$

- Doubling the OSR increases *3(2N+1)* dB SNR

$$PSNR = 6.02b + 1.76 - 10\log\left(\frac{\pi^{2N}}{2^{N+1}}\right) - 10(2N+1)\log(OSR) \quad (dB)$$

Noise-Shaping Characteristics of SDMs

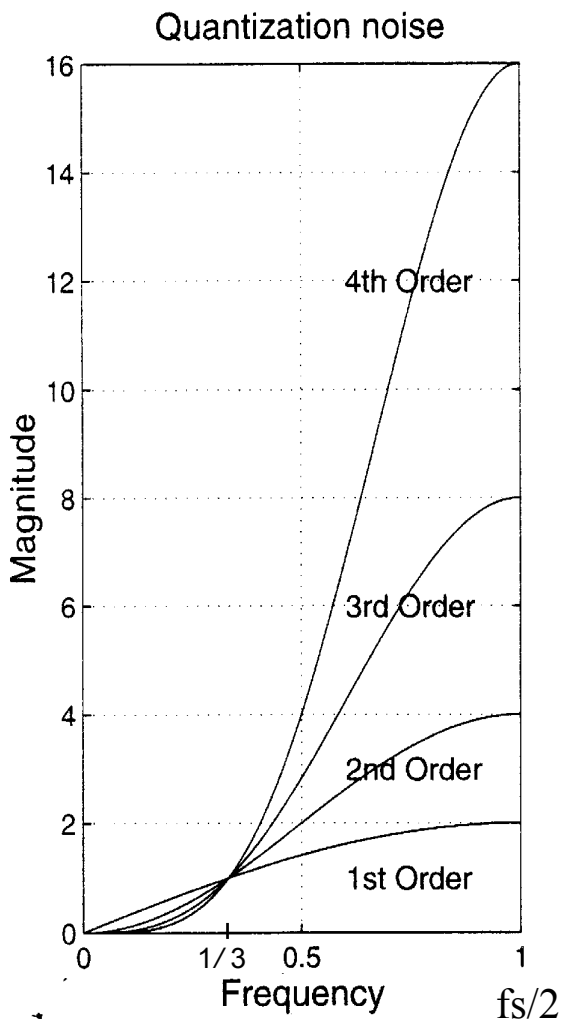
$$1\text{st}-\text{order}: \left|1-z^{-1}\right|$$

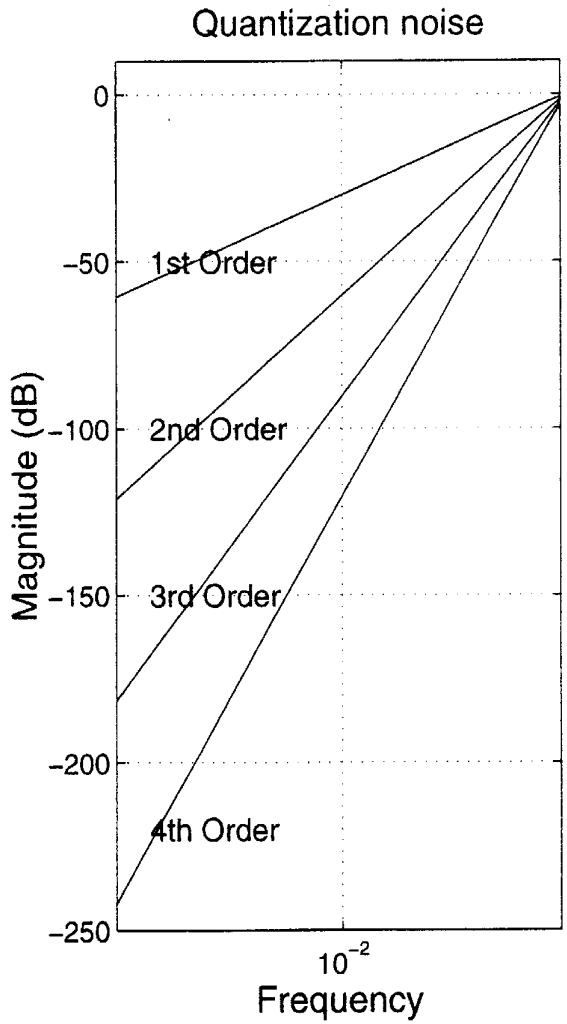
$$2\text{nd}-\text{order}: \left|(1-z^{-1})^2\right|$$

$$3\text{rd}-\text{order}: \left|(1-z^{-1})^3\right|$$

...

$$\text{Nth}-\text{order}: \left|(1-z^{-1})^N\right|$$





Quantization Noise Power of 1-bit Modulators

- 1-bit SDM output Y : ±1
  ⇨ Normalized power : 1 Watt
- Y(n) consists of signal and quantization noise
  ⇨ Signal power can never be greater than 1 Watt
- Example
  peak signal is within ±0.25
  ⇨ maximum signal power = 62.5mW
  ⇨ quantization noise power = 1W – 62.5mW = 937.5mW
  ⇨ signal power is 12 dB below the quantization noise power
- The quantization noise power is mostly in a different region than the signal power and can therefore be filtered out.
- The filter must have a dynamic range capable of accommodating the full power at its input.

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Low-Order vs. High-Order SDMs

- Low-order SDMs (1st and 2nd order)
  - Higher OSR ⇨ Signal bandwidth is limited
  - Serious tones in the baseband ⇨ dither is required
  - Stable
- High-order SDMs (≥3rd order)
  - Lower OSR required to achieve the same SNR
  - Less tones in baseband (quantization noise is more random)
  - Instability problems
    1. Complicated design for a stable modulator
    2. Smaller stable input range
  - High SNR and DR

High-Order SDM Structures

- Multi-stage noise shaping (MASH) structure
  - Cascaded first-order modulator

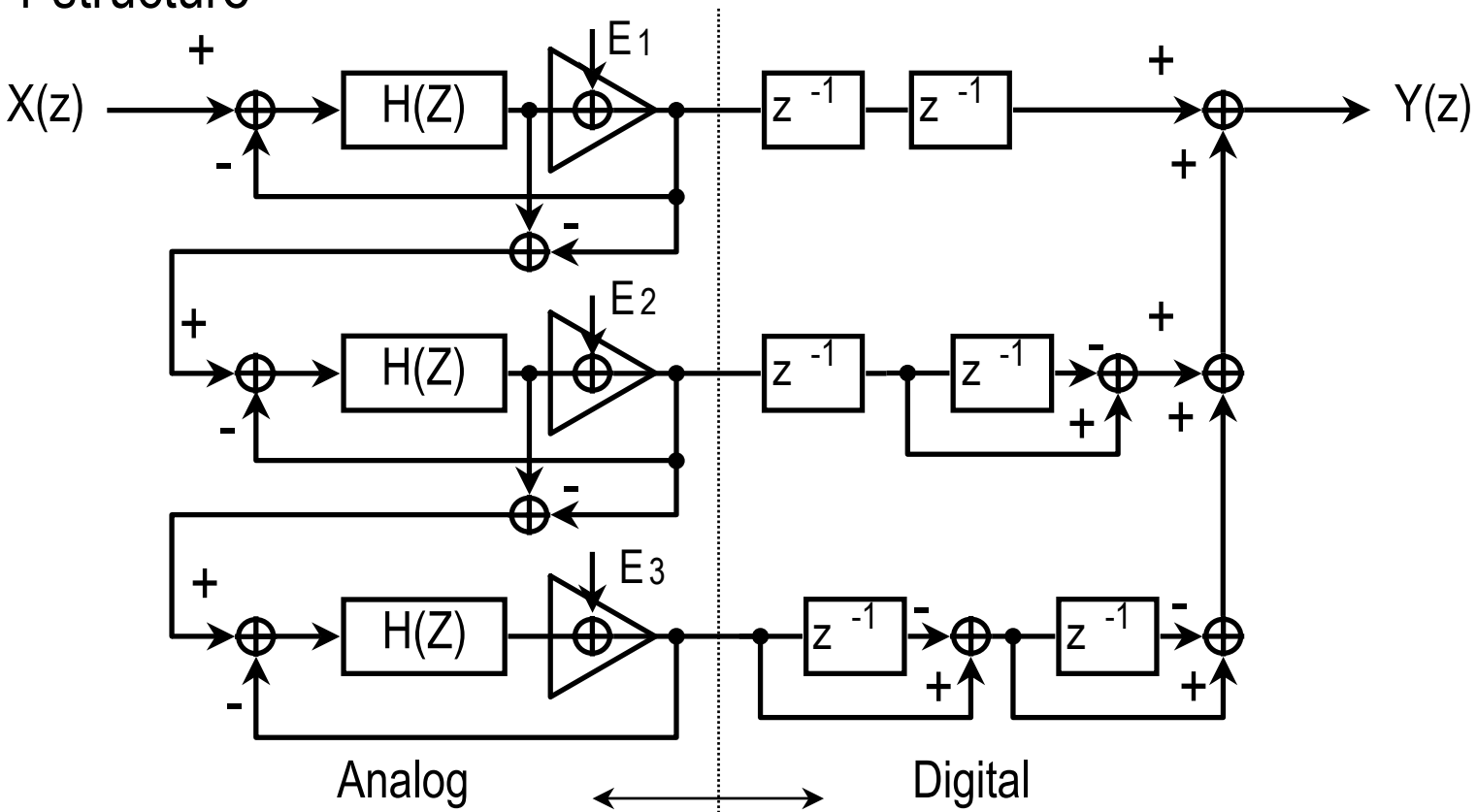
    1+1+1 SDM, 1+1+1+1 SDM
  - Cascaded first-order and/or second-order modulator

    2+1 SDM, 2+2 SDM

- Single-stage structure
  - Feedforward (FF) modulator
  - Multiple-feedback (MF) modulator
  - Others

MASH (Cont.)

- 1+1+1 structure

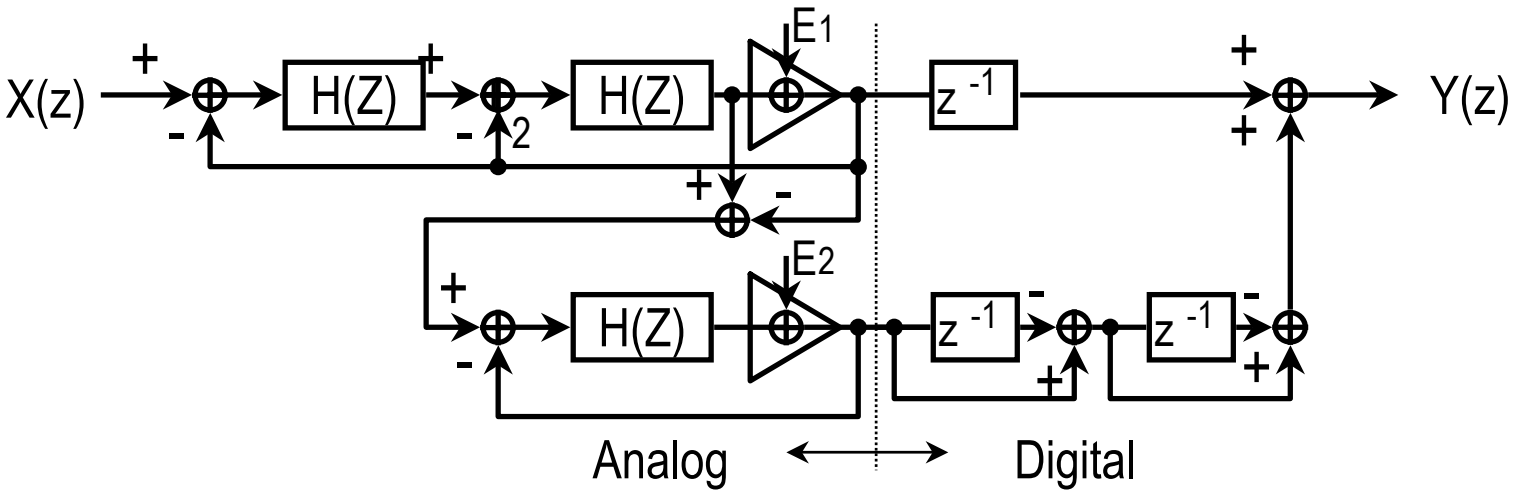


$$Y(z) = z^{-3}X(z) + (1 - z^{-1})^3 E_3(z)$$

where $H(z) = \dfrac{z^{-1}}{1 - z^{-1}}$

MASH (Cont.)

- 2+1 structure



$$Y(z) = z^{-3}X(z) + (1 - z^{-1})^3 E_2(z)$$

MASH (Cont.)

- Advantages
  - Stable (composed of low-order SDMs)
  - Structure design is easier (compared with single-stage)
- Disadvantages
  - Requirement of better components matching

    Sensitive to finite OPAMP gain and mismatches between the analog and digital circuitry.

    Such mismatches cause first-order noise to leak through from the first modulator and hence reduce dynamic range.

    To alleviate this mismatch problem, often the first stage is chosen to be a higher order modulator
  - Usually, order ≤ 4 (limited by mismatch) for ADC

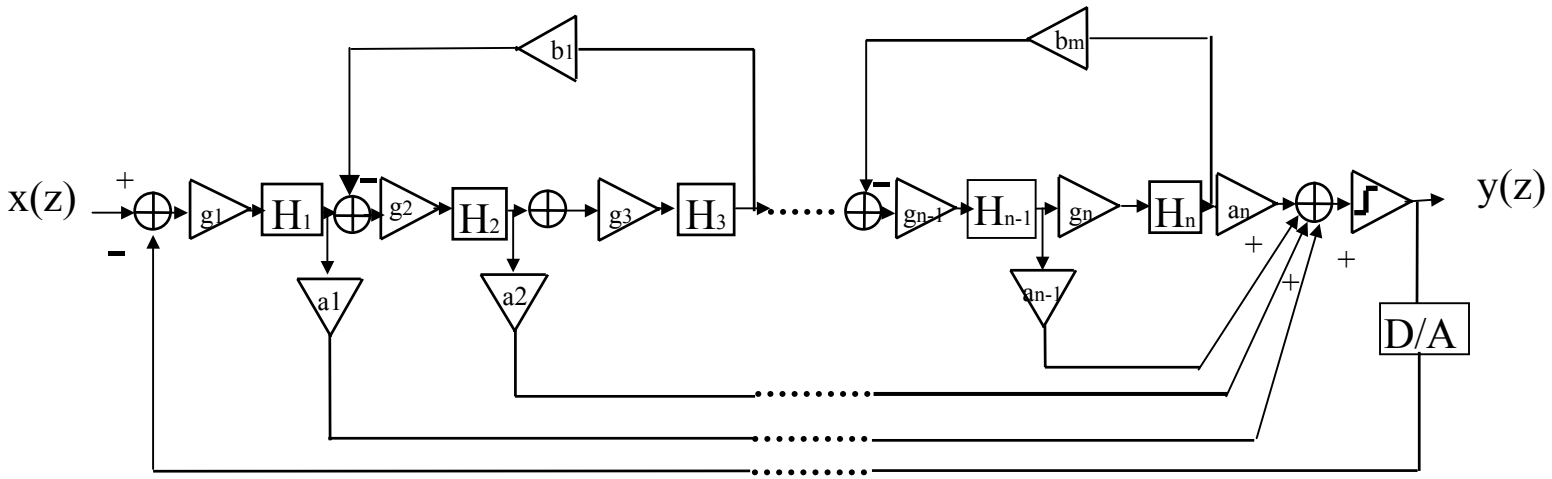
MASH (Cont.)

- It is very important to minimize errors due to input-offset voltages that might occur because of clock feedthrough or OPAMP input-offset voltages. In practical realizations, additional circuit design techniques will be employed to minimize those effects
- Digital output signal, Y(n) is a multi-level ($\geq$4 level) rather than two-level signal due to the combination of the original two-level signals. Such a multi-level signal would require a linear multi-level DAC in a D/A application

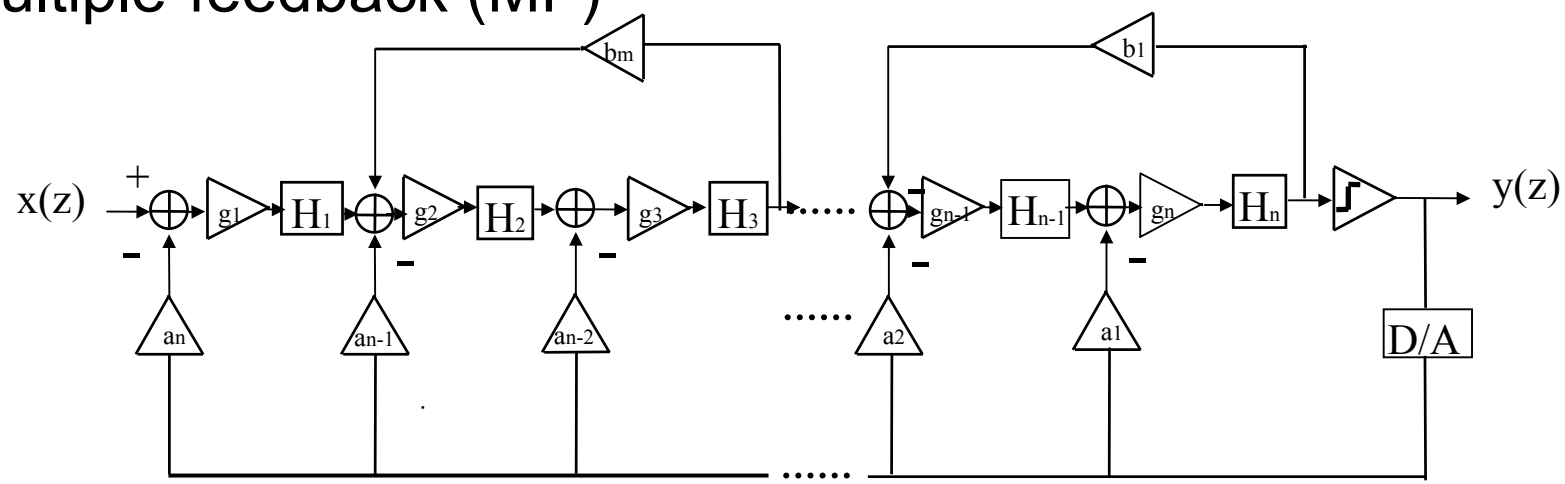
  For A/D application, it makes the FIR decimation filter slightly more complex.

Commonly Used Single-Stage SDM Structures

- Feedforward (FF)



- Multiple-feedback (MF)



Single-Stage SDMs

- Advantages
  - Less component matching requirement (compared with MASH architechures)
  - Very high resolution (very high order is achievable)
- Main problems
  - Instability of high-order SDMs
    - ↑ Instability recovery machanism is required
  - Complicated design for a stable high-order modulator
    - ↑ Efficient design tool for high-order SDMs is required

OUTLINE

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Stability Criteria

- A stable modulator is defined here, as one in which the input to the quantizer remains bounded such that the quantization does not become overloaded.

  Overloaded quantizer: quantization error greater than $\pm$LSB/2
- The stability of higher-order modulator is not well understood as they include a highly nonlinear element (especially low-bit quantizer).
- Stability criteria

  1. Rule of thumb for stable SDM

     $\left|NTF(e^{jw})\right| \le 1.5$ for $0 \le w \le \pi$

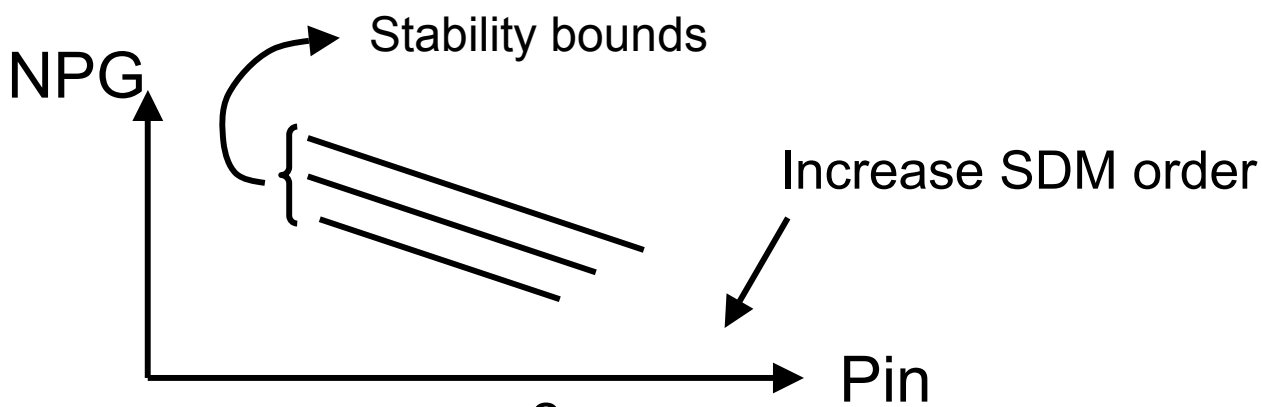
     This stability criterion has little rigorous justification.

  2. 1-norm stability criterion, $\|NTF\|_1 = \frac{2}{f_s}\int_0^{f_s/2} |NTF(f)|df < 3 - X_{in,max}$

     It's often too conservative, as it eliminates many stable modulators.

Stability Criteria(Cont.)

3. 2-norm stability criterion
   - Numerical simulation can be used to find stability bounds
   - Useful stability bounds for single-stage SDMs are first proposed by T.H. Kuo and K.D. Chen, EE, NCKU, Taiwan (IEEE Trans. CAS-II, Jan. 1999)



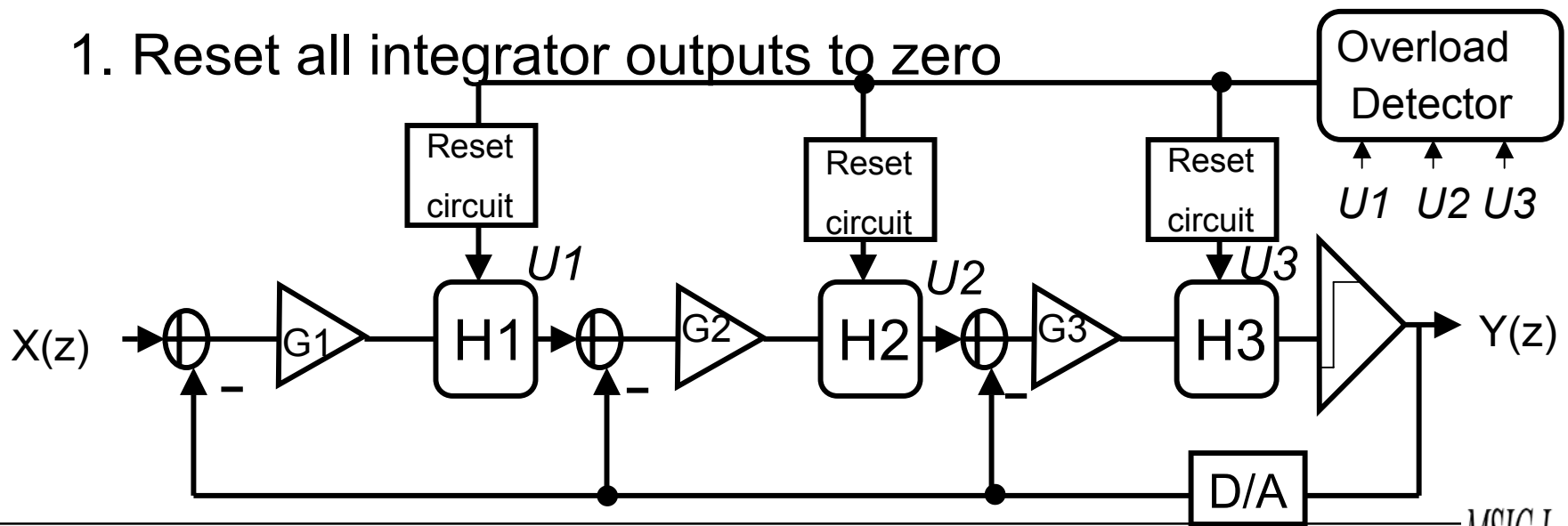
where $NPG = \|NTF(f)\|_2^2 = \frac{2}{f_S}\int_0^{f_s/2} |NTF(f)|^2 df$

$P_{in} = A^2/2$ for sinwaves with a amplitude of A

– Larger NPG $\Rightarrow$ { less stable; larger PSNR; smaller $P_{in(max)}$

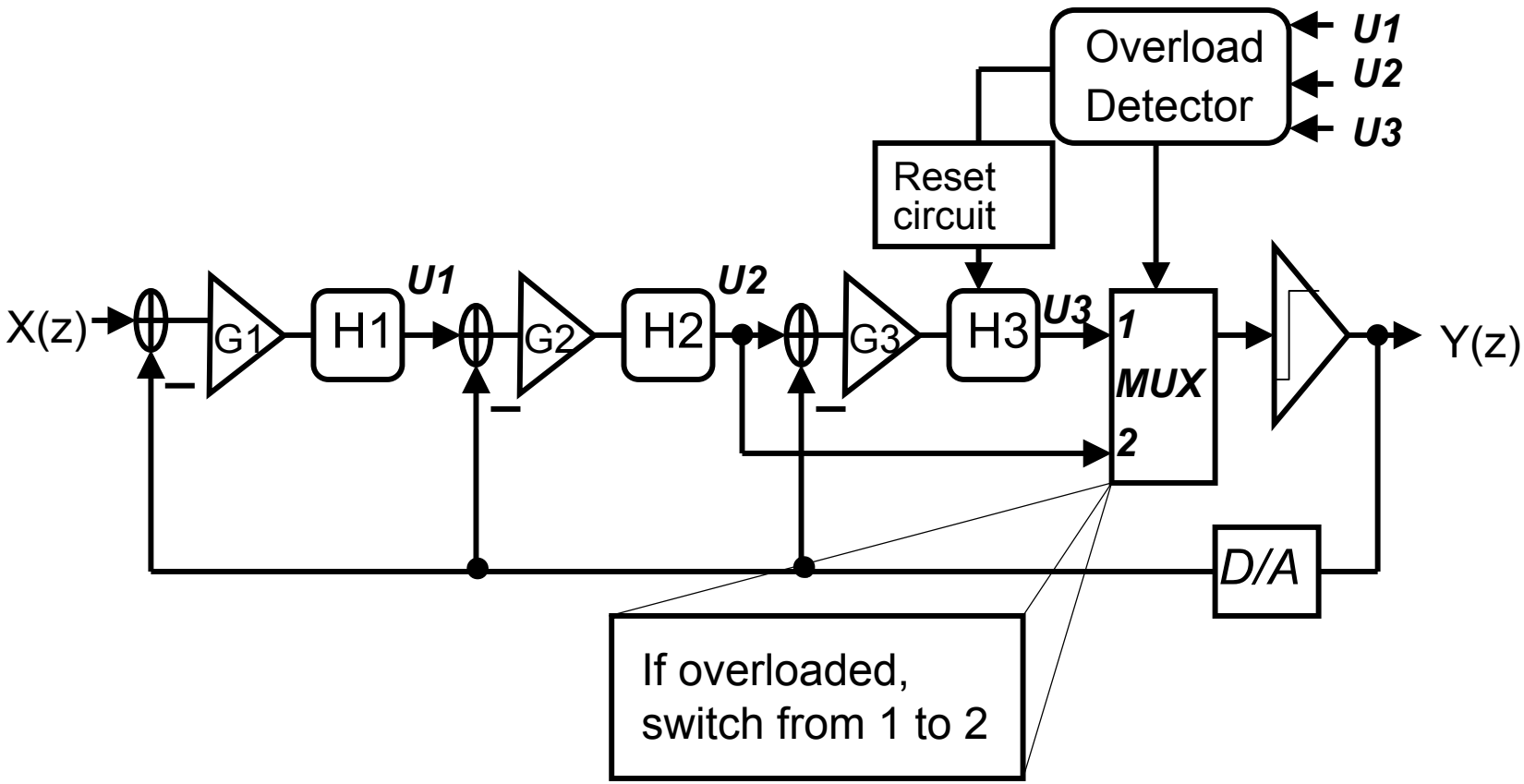
Instability Recovery

- Instability detection(two commonly used methods)
  1. Looking for long strings of 1s or 0s at the SDM output.
  2. Monitoring signal amplitude at the quantizer input to see if predetermined amplitude thresholds are exceeded for a specified number of consecutive clock cycles.
- Instability recovery (Circuit is changed to force an unstable SDM back to its stable state) Three methods:
  1. Reset all integrator outputs to zero



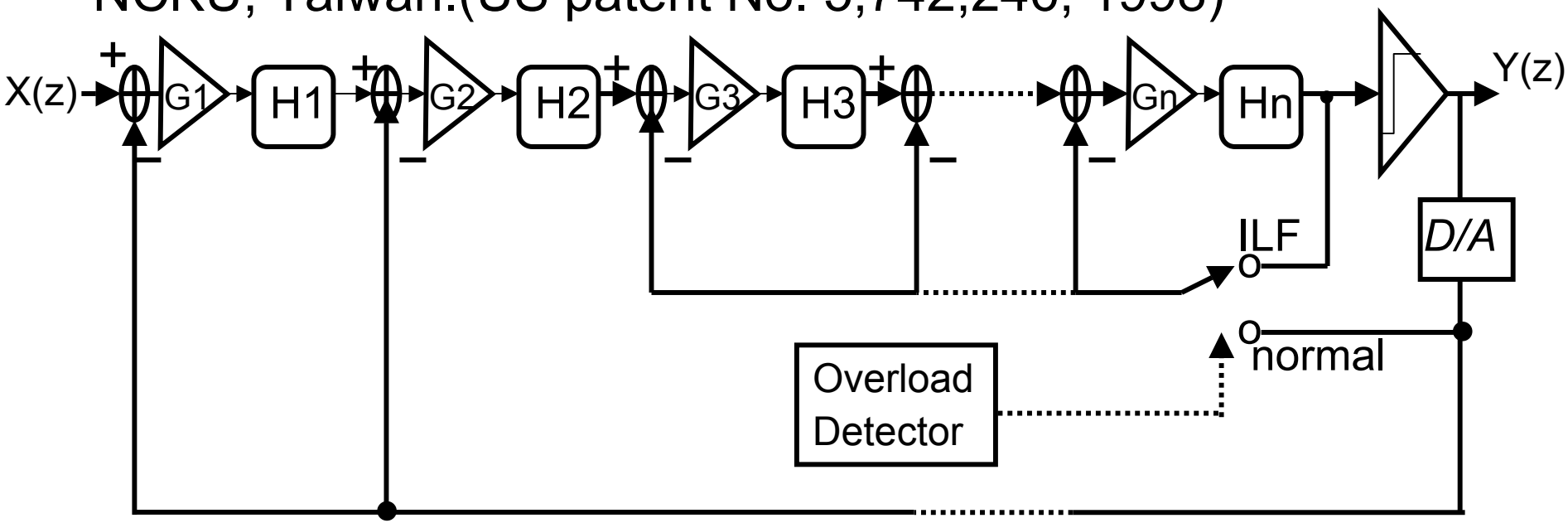
Instability Recovery

2. Change the SDM into a 2nd-order or even first-order SDM by using only the first two integrators and resetting others.



Instability Recovery(cont.)

3. Eliminate the comparator temporarily from the high-order integrators. This changes the modulator into a modulator-filter combined SDM. This technique is called internal linear feedback(ILF). Invented by T.H. Kuo and W.C.Wang, etc., EE, NCKU, Taiwan.(US patent No. 5,742,246, 1998)



– "3" is the best. "1" and "2" lose information due to reset.
– Multi-bit SDMs exhibit improved stability over their 1-bit counterpart.

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Idle Tone

- Examples:
  1. apply a dc level of 1/3 to a 1st-order SDM having a 1-bit quantizer with output levels of ± 1

     modulator output = $\{ 1,1,-1,1,1,-1,1,1-1,1,1..... \}$

     $\Rightarrow$ idle tone at $\frac{f_S}{3}$ — can be filtered by lowpass postfilter
  2. apply a dc level of 3/8 to the same modulator

     modulator output = $\{ 1,1,-1,1,1,-1,1,1,-1,1,1,1,-1,1,1,-1,.... \}$

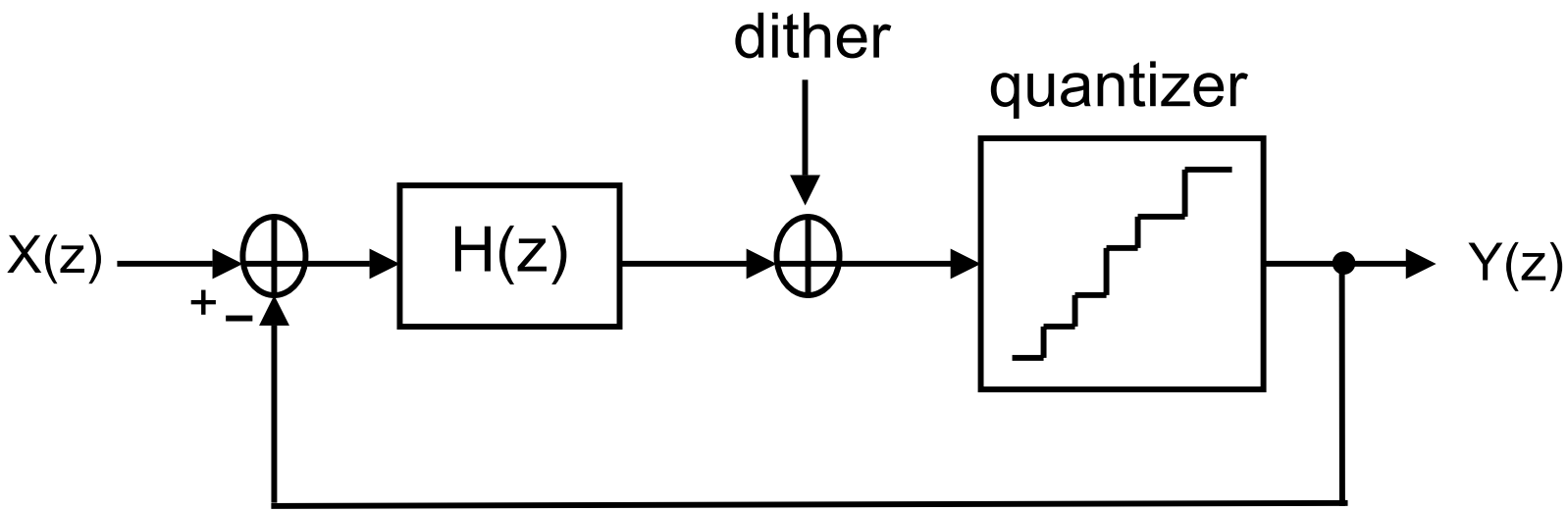
     $\Rightarrow$ idle tone at $\frac{f_S}{16}$ — may not be filtered by lowpass postfilter
- Higher-order SDM $\Rightarrow$ less idle tone
- Tones might not lie at a single frequency but instead be short-term periodic patterns. In other words, a tone appearing near 1KHz might actually be a signal varying between 900Hz and 1.1KHz in a random-like fashion.

Dithering

- One way to reduce the amount of idle tones in modulators through the use of dithering. The term dithering here refers to the act of introducing some random(or pseudo-random) signal into a modulator.
- The most suitable place to add the dithering signal is just before the quantizer. Thus, the dithering signal becomes noise shaped in the same manner as the quantization noise, and therefore a large amount of dithering can be added.
- Typically, the dithering signal is realized using some sort of pseudo-random number generator with only a few bits of resolution, but its total noise power is comparable to the quantization noise power.

Dithering(cont.)

- The use of dither to reduce idle tones is not an attempt to add noise to mask out the tones but instead breaks up the tones so that they never occur.
- Since the noise power of the dithering signal is similar to the quantization noise power, the use of dithering adds about 3dB extra inband noise and often requires rechecking the modulator's stability.



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HOST - **H**igh-**O**rder **S**DM **S**ynthesis **T**ool

- HOST was developed by T.H. Kuo, K.D. Chen and J.R. Chen, EE, NCKU, Taiwan.(Copyright No. 8702035,1998)

  HOST is the world first single-stage SDM synthesis tool.
- Automatic coefficient design of feedforward (FF) and multiple feedback (MF) SDMs
- Main features
  - Stable high-order SDMs with high tolerance coefficients
  - Optimization among SNR, OSR, order, coefficient sensitivity, quantization levels, and stability of a SDM
  - SDMs can be synthesized for various specifications.
  - Low baseband tones and harmonics

A Design Example Using HOST

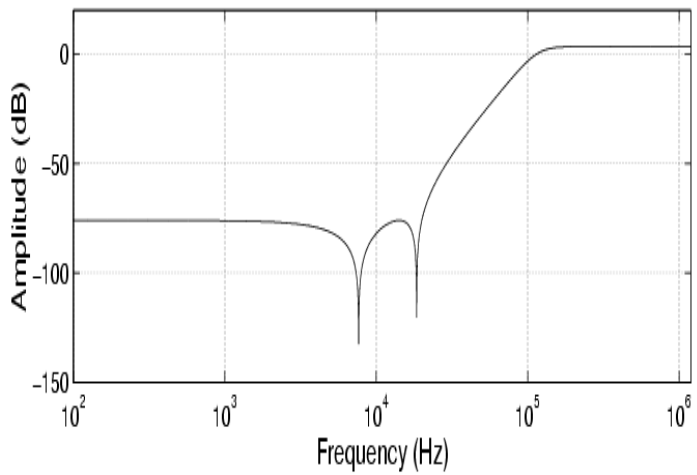
- Audio specifications
  - SNR (Dynamic Range) > 16 bit = 96dB
  - Oversampling ratio (OSR) =64
  - Baseband bandwith = 22.5kHz
  - Modulator order =4
  - Maximum stable input > -6dB
  - Bit number of internal quantizer = 1
  - Feedforward structure

- Synthesized modualtor coefficients

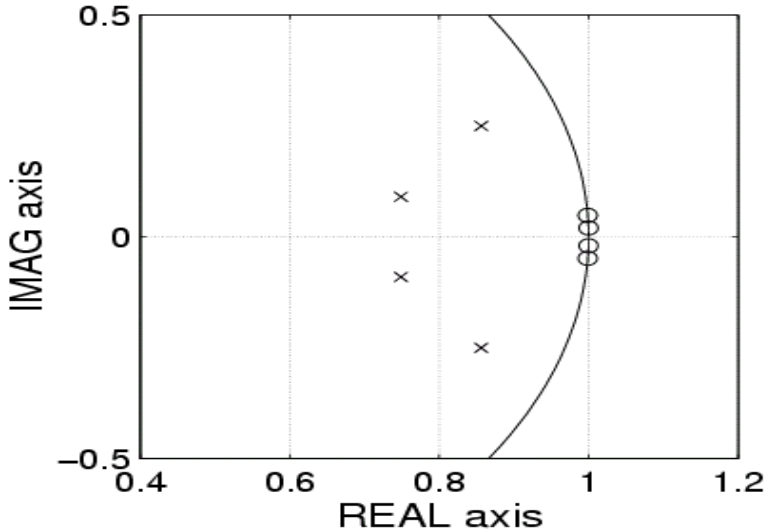
a1=1.276899	g1=0.575769	b1=0.083209
a2=0.710255	g2=0.629813	b2=0.013754
a3=0.452129	g3=0.308405	
a4=0.480403	g4=0.083209	

Simulation Results

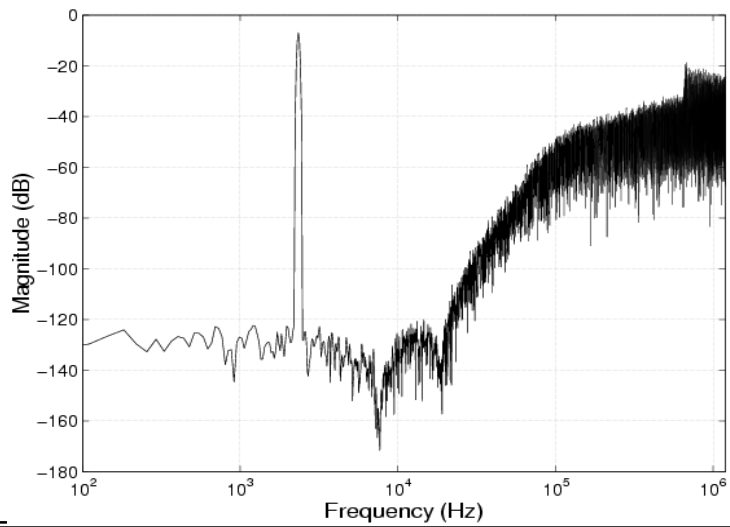
- Noise transfer function(NTF)



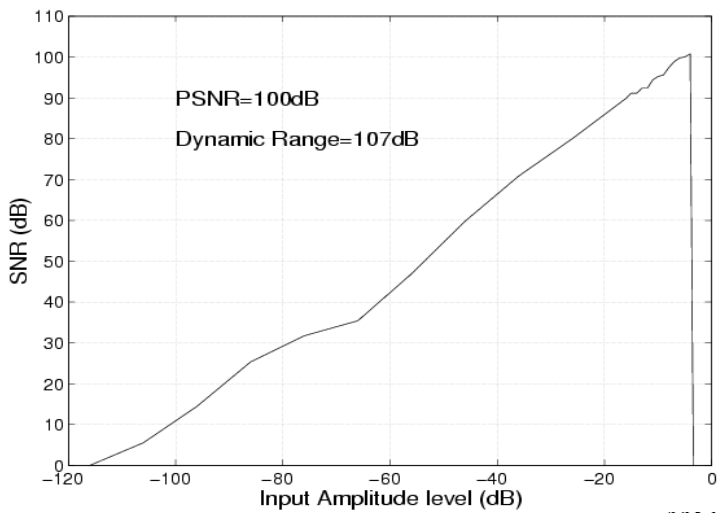
- Poles and zeros of NTF



- Output spectrum



- Dynamic range plot



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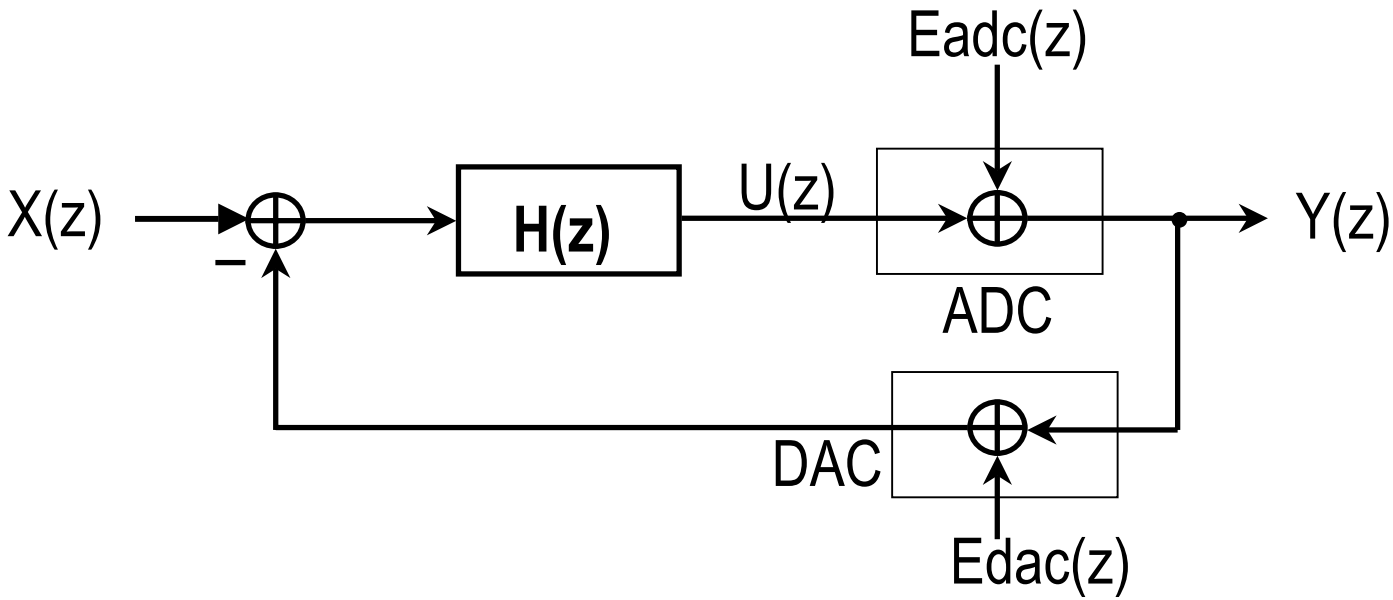
Conversion Errors of Internal ADC and DAC

- Block Diagram of analog SDM



$$Y = \frac{H(z)}{1+H(z)}[X(z)+Edac\ (z)]+\frac{1}{1+H(z)}Eadc\ (z)$$

- Internal A/D conversion errors can be attenuated by NTF at the baseband
- Internal D/A conversion errors are regarded as input signal (without any attenuation at the baseband)

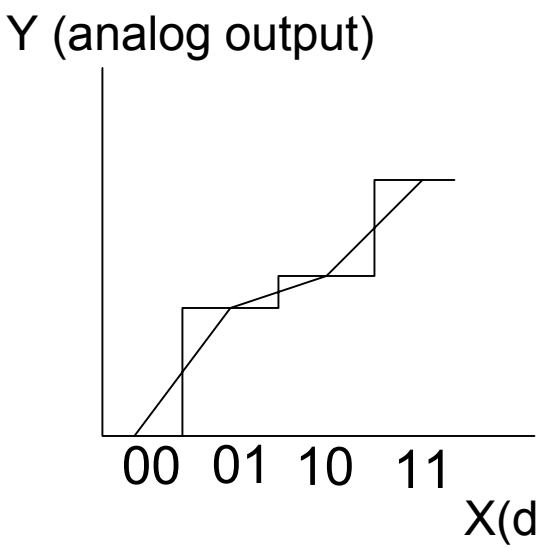
One-Bit vs. Multi-Bit Analog SDMs

- 1-bit DAC (only two level) is perfect linear
  - Major motivation for SDMs to use 1-bit internal DAC (and hence 1-bit internal ADC)
  - Many 16-18 bits audio converters presently use 1-bit internal DAC.
- Multi-bit DAC requires good component matching for high-resolution

  For a 16-bit resolution converter, components mismatch for internal DAC must be less than $1/2^{16} = 0.0015\%$

Multi-Bit Analog SDMs

- Multi-bit internal ADC or DAC
  - Quantization noise (smaller compared with 1-bit converters)
  - Offset error (can be ignored for SDM)
  - Gain error (can be ignored for SDM)
  - Nonlinearity error (introduces harmonic distortions)



Transfer curve

$$y = a + bx + cx^2 + dx^3 \cdots$$

Multi-Bit Analog SDMs

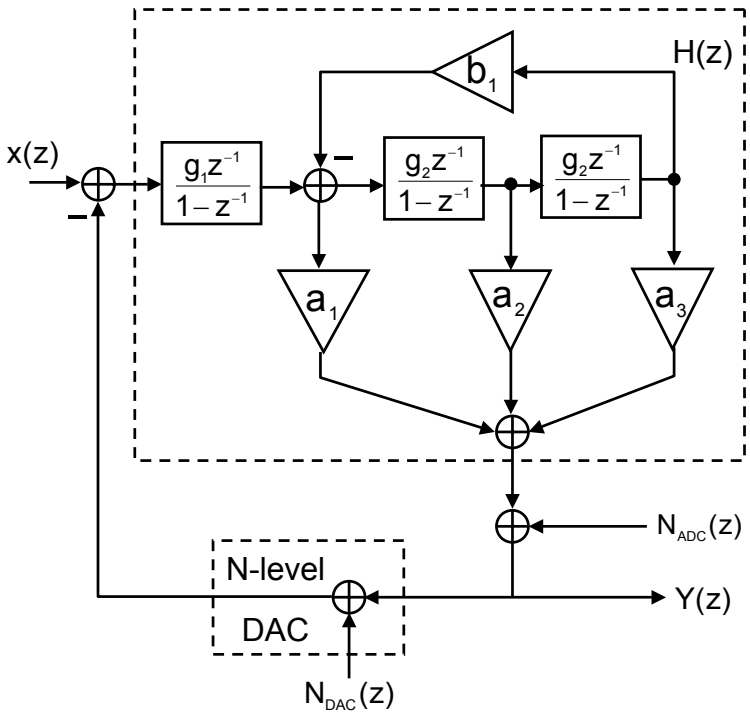
- Motivations of development for multibit sigma-delta converters
  - High speed applications (low OSR)
  - Enhancement of modulator stability
  - Relax post analog filter design of sigma-delta DACs.
- Multibit SDMs become popular due to the development of techniques for reducing DAC nonlinearity effect
  - Many methods (shown in the next page)
    IDWA is the best, up to now, among them
  - Improved Data weighted averaging (IDWA) algorithm
    1. First-order DAC-noise shaping (ideally)
    2. Most efficient on attenuation of DAC noise
    3. Lowest cost for implementation

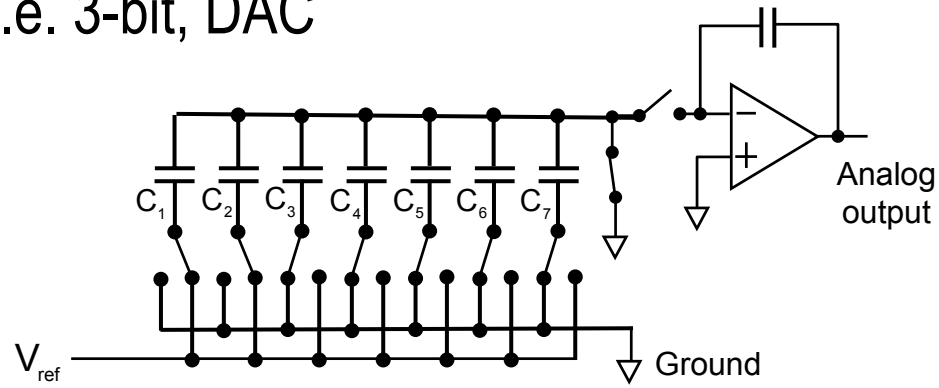
Techniques for Overcoming DAC Linearity Problem

- Changed SDM architectures (ISCAS'90,JSSC'91)
- Self-calibration technique (JSSC'91)
- Digital correction (JSSC'93)
- Dynamic element matching, DEM
  - Randomization (JSSC'89)
  - Clock averaging (TCAS-II'92)
  - Individual level averaging (TCAS-II'92)
  - Data weighted averaging ('93 patent : Motolora)
  - Data-directed scrambling ('95 patent : Analog Device)
  - Second-order data weighted averaging (ISCAS'96)
  - Grouped-level averaging (ISSCC'98)
  - Tree structure noise shaping dynamic element matching (ISSCC'98)

Data Weighted Averaging

- Using elements at maximum possible rate ensures that the DAC errors will quickly sum to zero, moving distortion to high frequencies
  - Example : 8 - level (7- element), i.e. 3-bit, DAC

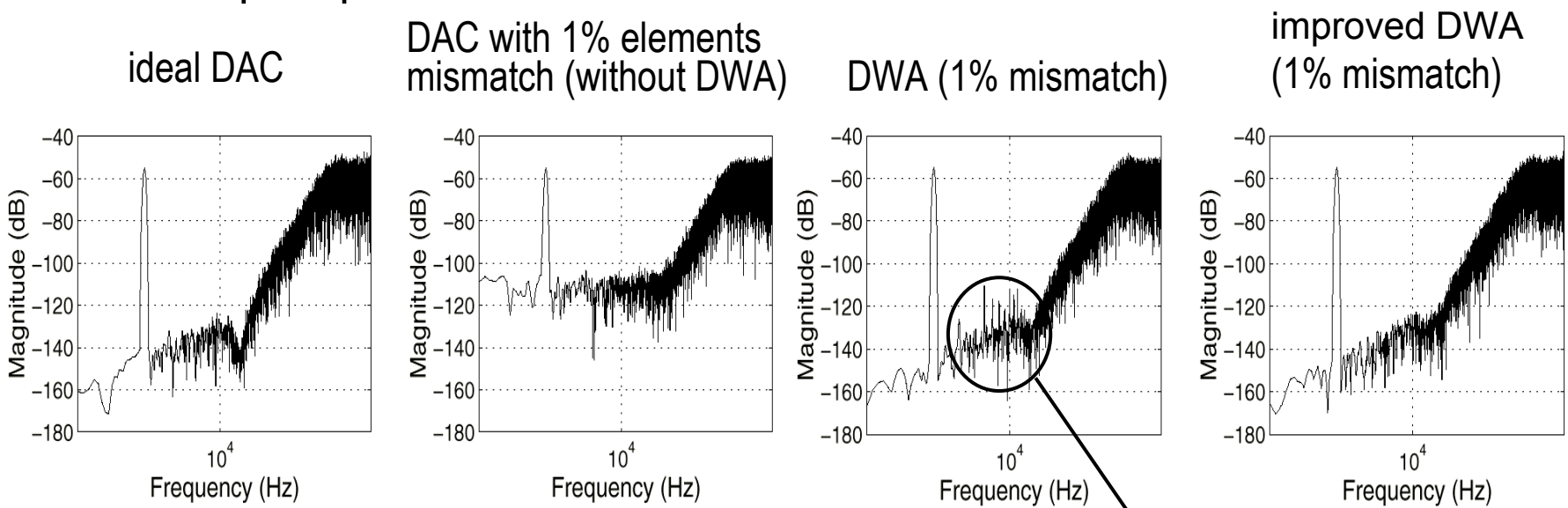




Time slot	n	n+1	n+2	n+3	n+4	n+5
DAC input code, y(n)	3	4	0	2	5	3
pointer position, ptr(n)	4	1	1	3	1	4
selected elements	C_1	C_4		C_1	C_3	C_1
	C_2	C_5		C_2	C_4	C_2
	C_3	C_6			C_5	C_3
		C_7			C_6	
					C_7	

Data Weighted Averaging (Cont.)

- Example : a third-order SDM with a 8 level DAC
  - SDM output spectrum



- Limitation of conventional DWA
  - Aliasing tones in the baseband
- This problem can be resolved by
  - Adding dither at the expense of noise level increase
  - Using an improved DWA proposed by K.D.Chen and T.H.Kuo, EE, NCKU,Taiwan (IEEE Trans. CAS-II, Jan. 1999, ROC patent approved, US patent pending)

Practical Considerations of Two-Level D/A Converters

- Nonidealities of two-level D/A converters

  (can also be applied to multi-level converters)

  1. power supply bounce
  2. switch feedthrough is signal dependent, e.g.

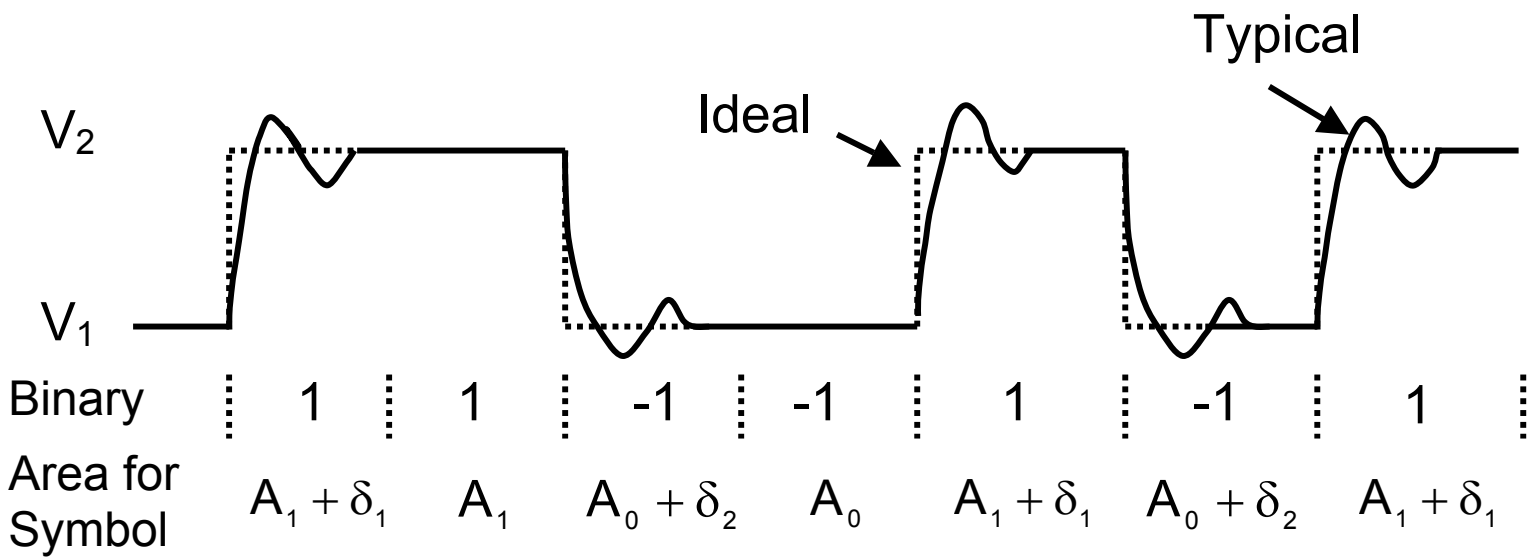
     when more 1s than 0s are being output by the D/A converter.

     $\Rightarrow$ Well-regulated power-supply voltages on the drivers for the input switches is very important.
  3. clock jitter

Practical Considerations of Two-Level Converters (Cont.)

4. memory between output levels

A nonreturn-to-zero(NRZ) 1-bit DAC typical output



Practical Considerations (Cont.)

Example: three periodic patterns corresponding to average voltages of 0,1/3,and -1/3 when V_1 and V_2 are $\pm$1V

$$0:\{1,-1,1,-1.....\}\cdot\cdot\overline{V_d(t)}=\frac{A_1+A_0+\delta_1+\delta_2}{2}=\overline{V_a(t)}+\frac{\delta_1+\delta_2}{2}$$

$$1/3:\{1,1,-1.....\}\rightarrow\overline{V_e(t)}=\frac{2A_1+A_0+\delta_1+\delta_2}{3}=\overline{V_b(t)}+\frac{\delta_1+\delta_2}{3}$$

$$-1/3:\{-1,-1,1.....\}\rightarrow\overline{V_f(t)}=\frac{A_1+2A_0+\delta_1+\delta_2}{3}=\overline{V_c(t)}+\frac{\delta_1+\delta_2}{3}$$

These three averages don't lie on a straight line except

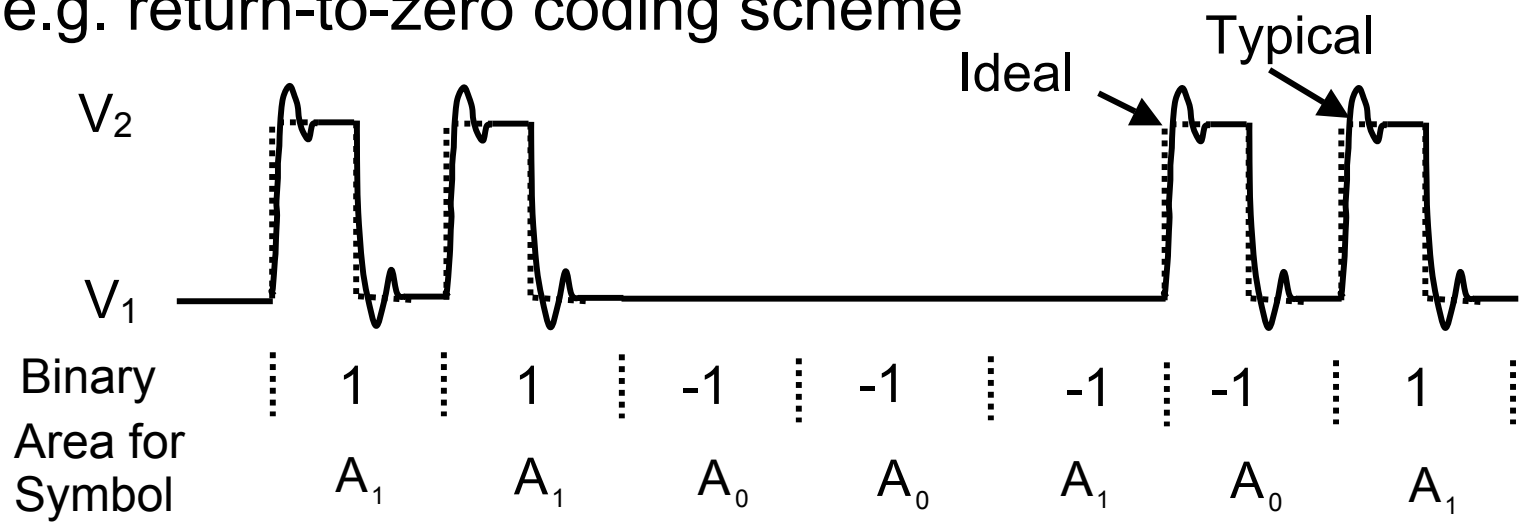
$$\delta_1=-\delta_2$$

Thus, one way to obtain high linearity is to match falling and rising signals. This is a very difficult task since they are typically realized with different types of devices.

Practical Considerations (Cont.)

– Memoryless coding scheme

e.g. return-to-zero coding scheme



- Switch capacitor circuits naturally realize memoryless levels as long as enough time is left for settling one each clock phase.

  Thus, the first stage of postfiltering in oversampling D/A converters is often realized using SCFs, which is followed by continuous-time filtering.

OUTLINE

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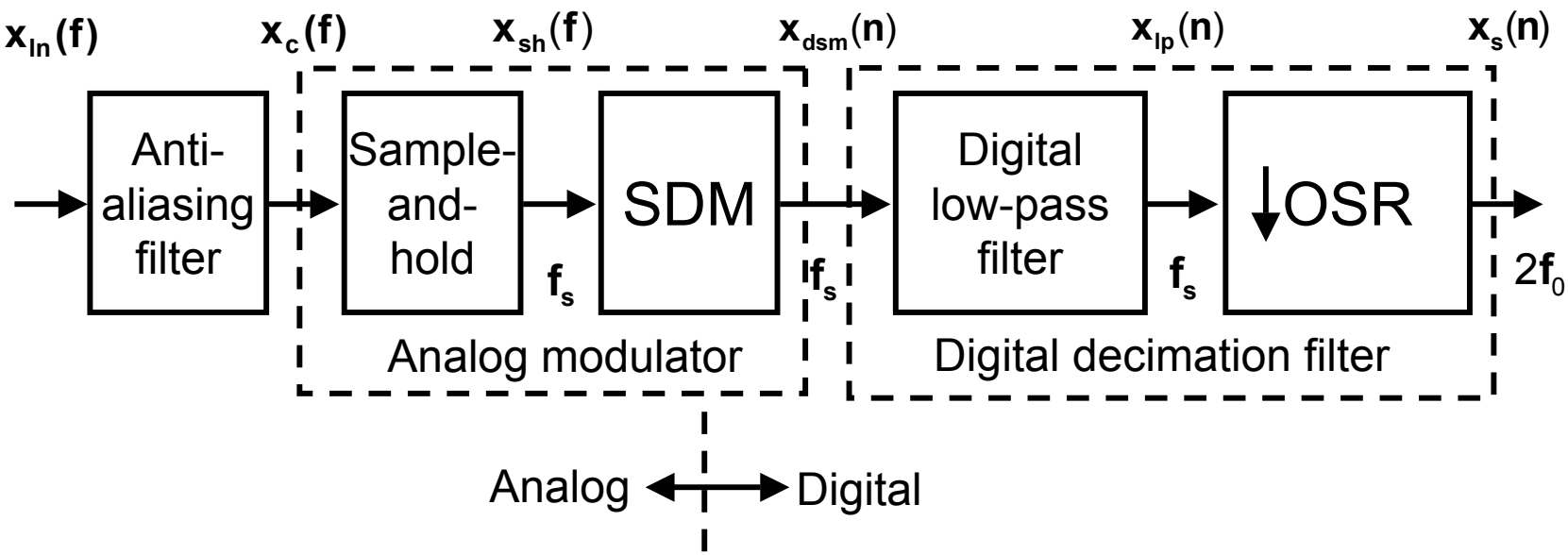
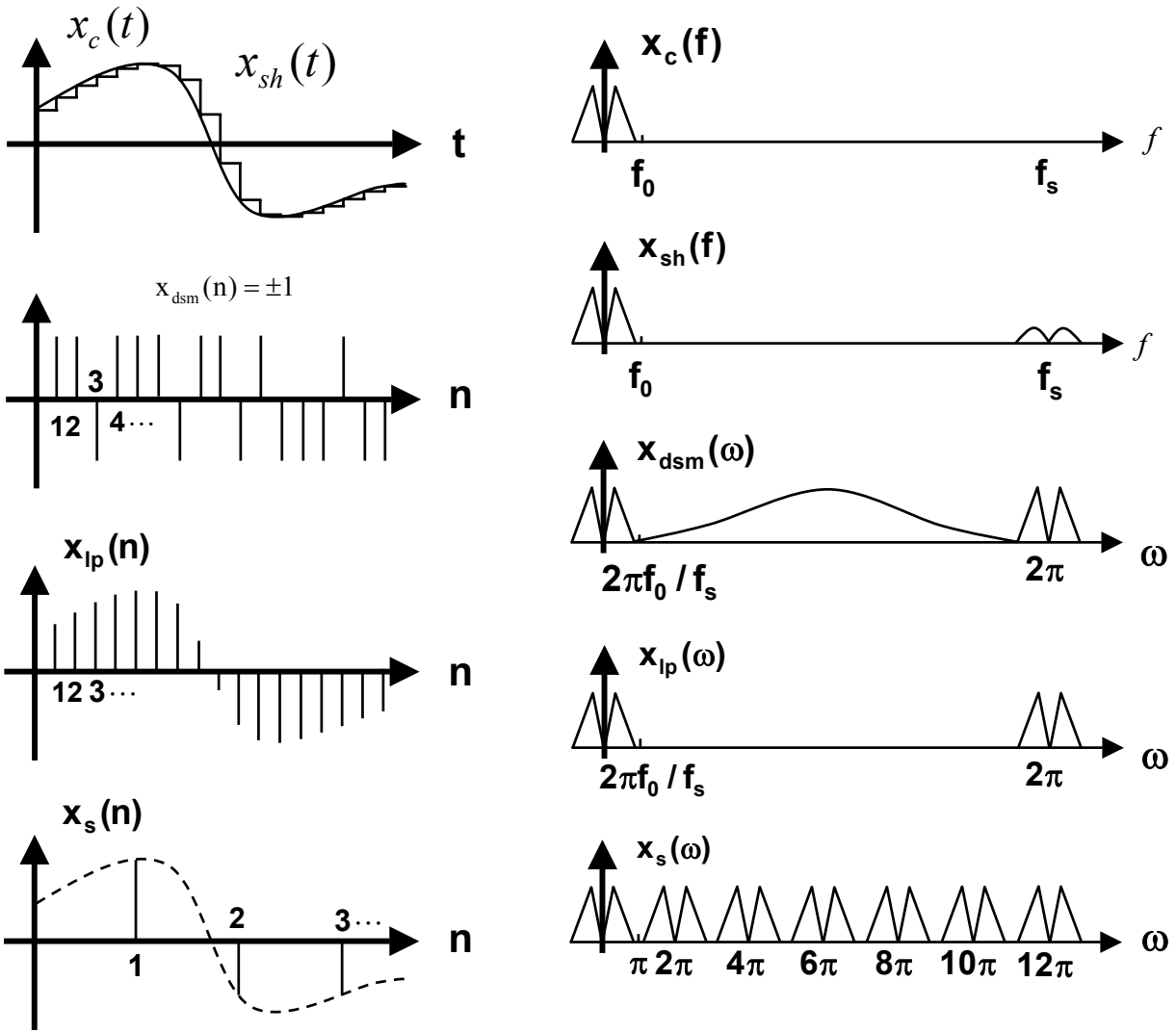
System Architectures of Sigma-Delta ADCs

- Block diagram
  - S/H is merged to SDM
  - Decimator (↓OSR) is merged to digital LPF



System Architectures of Sigma-Delta ADCs (Cont.)

- Signals and spectra



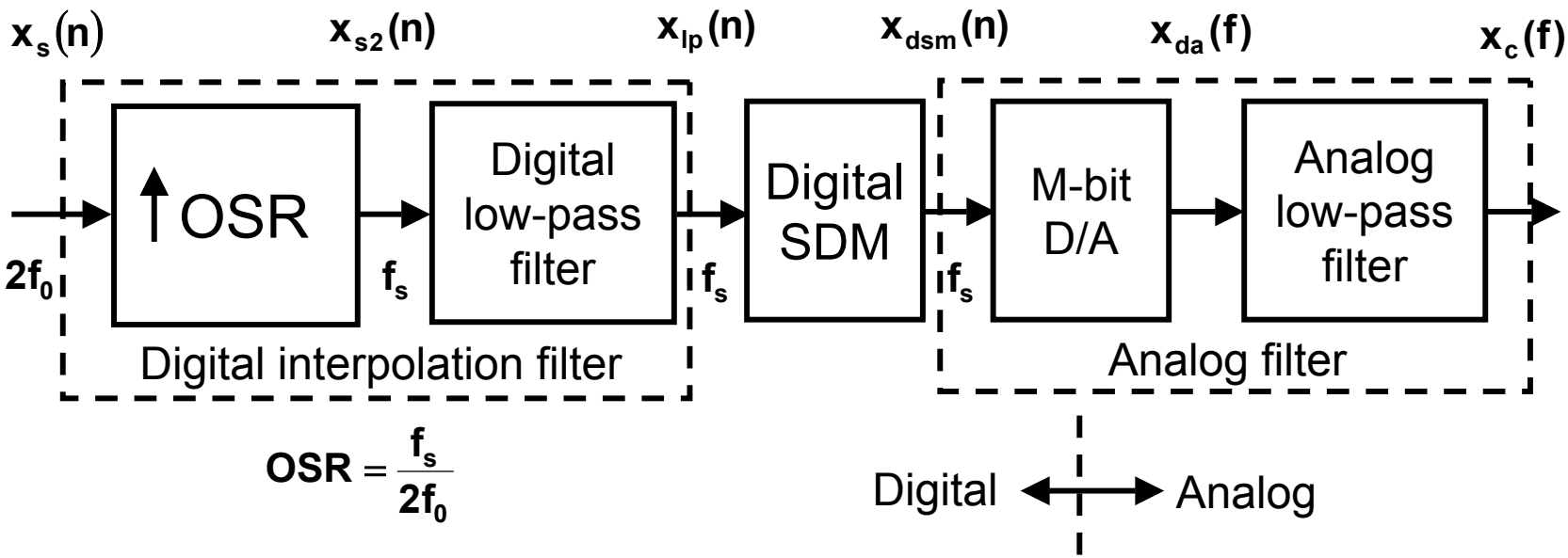
System Architectures of Sigma-Delta ADCs (Cont.)

- Since digital circuitry is linear, the overall linearity is most strongly dependent on realizing a linear DAC inside the sigma-delta modulator.

  Nonlinearity in the internal ADC have only a small effect on the linearity of the overall ADC, since the high gain in the feedback loop compensates for that nonlinearity

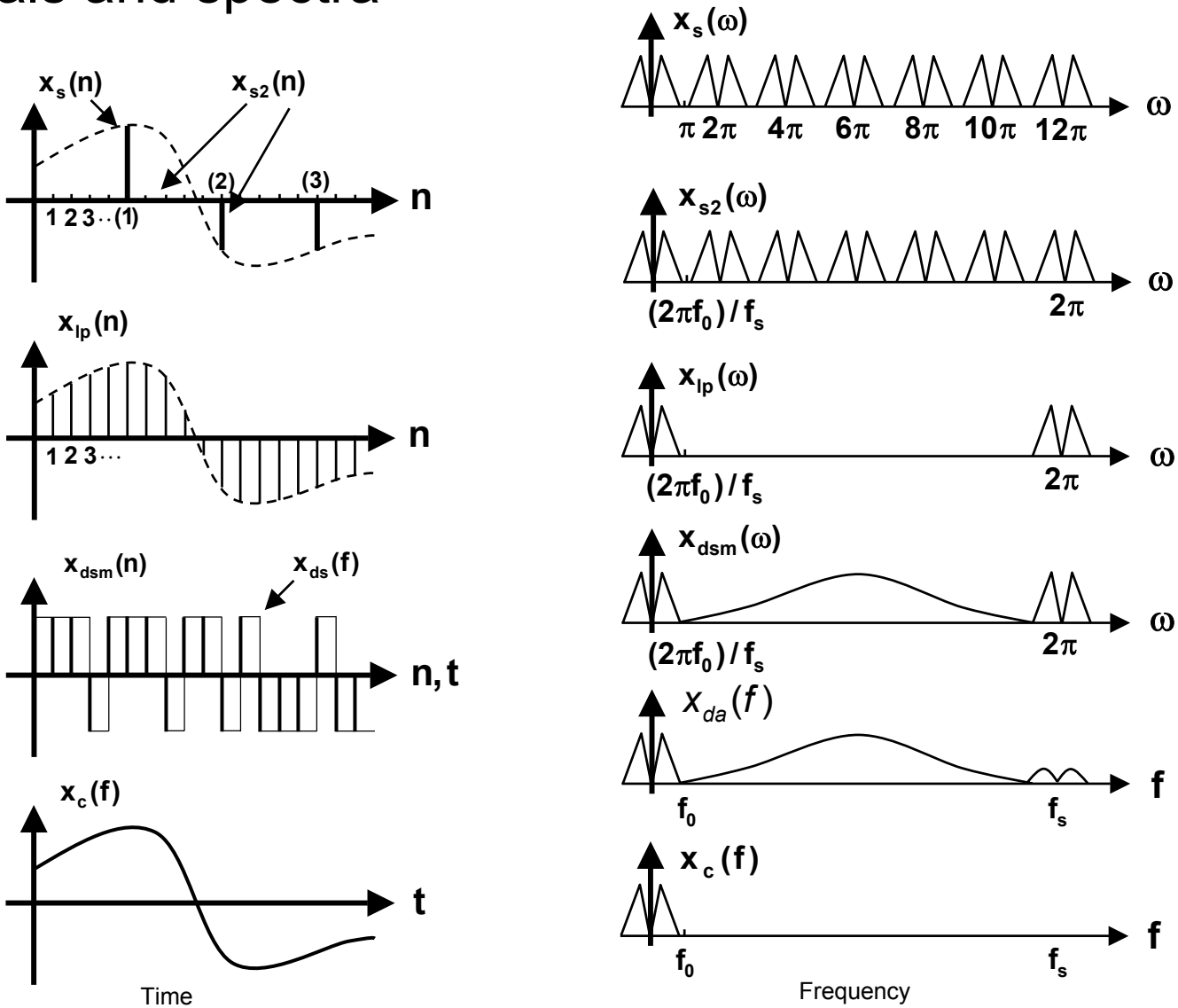
System Architectures of Sigma-Delta DACs

- Block diagram
  - Interpolator (↑OSR) is merged to digital LPF
  - M-bit D/A is usually merged to analog LPF



System Architectures of Sigma-Delta DACs (Cont.)

- Signals and spectra



System Architectures of Sigma-Delta DACs (Cont.)

- 1-bit internal D/A has excellent linearity.

  Multi-bit internal D/A can reduce analog filter's complexity. However, it's linearity problem must be resolved.

- The order of the analog filter should be at least one order higher than that of the SDM.

  This analog filter should be linear so it does not modulate the noise back to the frequency band of interest.

  In many applications, the realization of those filters, especially if they are integrated, is nontrivial.

Circuit Implementation of Sigma-Delta ADCs and DACs

- Simple anti-aliasing filter
- Analog modulator
  - Switched-capacitor circuits :
    1. Analog signal sampling, integration, delay, and scaling
    2. Feedback DAC
  - Cmparators : 1-bit or multi-bit analog quantizer
  - Realization for high-resolution is difficult
- Digital filters
  - Application specific architecture
  - FIR/IIR filter : decimation (ADC) and interplolation (DAC)
  - Fast logic circuits for operation of multiplication and addition

Circuit Implementation of Sigma-Delta ADCs and DACs (cont.)

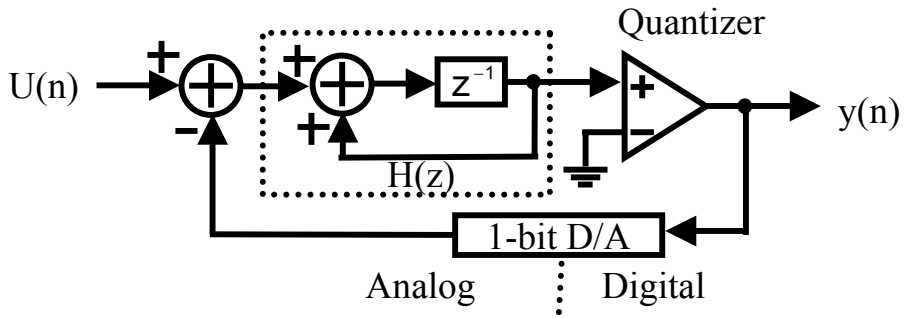
- Digital modulator
  - Simplification of multiplication and addition is required due to its high throughput rate.

    Power-of-two coefficients are usually used.
  - Digital quantization
  - Its function is similar to that of the analog SDM but it is implemented using digital circuits.
- Analog filter
  - At least one-order higher than that of the digital modulator
  - Realization for high performance, especially if it is integrated, is difficult.

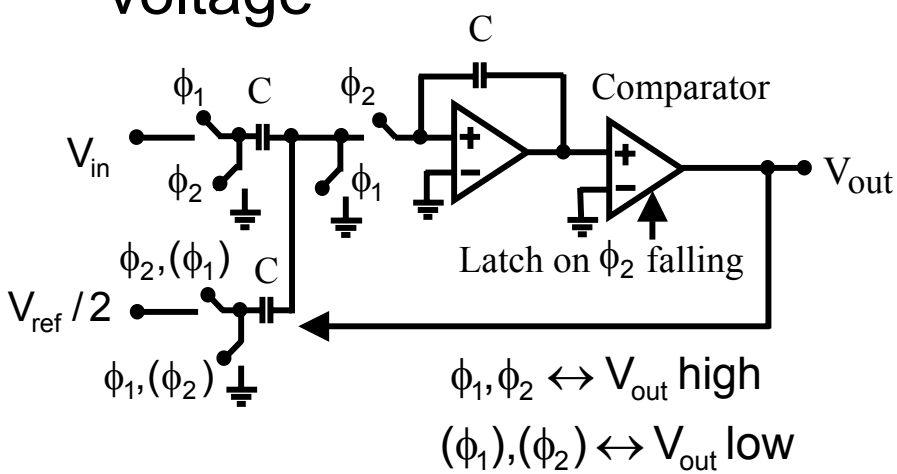
Example:SC Realization of a First-Order SDM for ADC

(Example with single-ended OPAMP and 1-bit internal DAC)

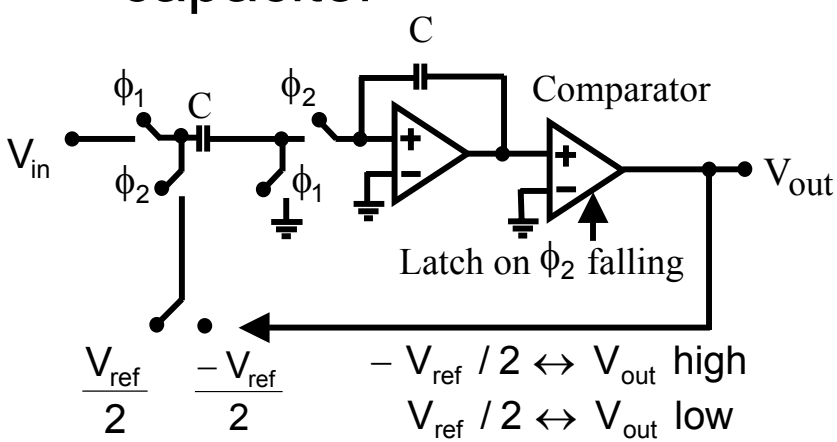
- Block diagram



- Switched-capacitor (SC) implementation
  - using only one reference voltage

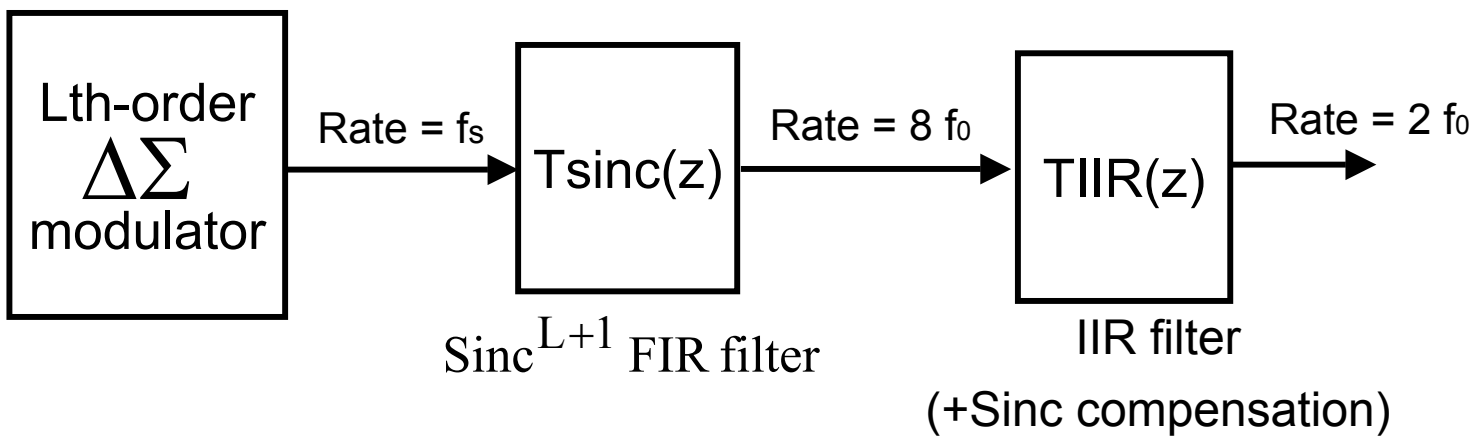


  - using only one input capacitor



Digital Decimation Filters for Sigma-Delta ADCs

- Two popular approaches : multi-stage and single-stage
- Multi-stage
  - a sinc FIR filter followed by an IIR filter
    1. sinc FIR filter : fast and simple
    2. IIR filter : low cost and large out-of-band attenuation, but nonlinear phase



Digital Decimation Filters for Sigma-Delta ADCs (Cont.)

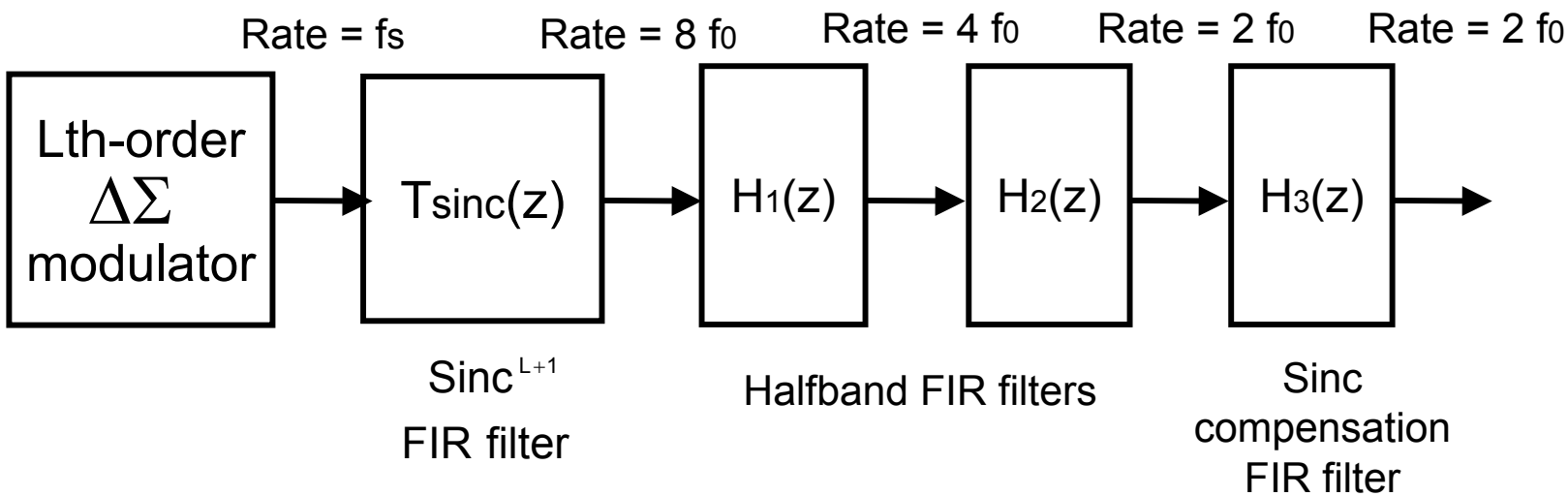
– a sinc FIR filter followed by half-band filters

half-band FIR :

(1) linear phase

(2) coefficients are symmetric

(3) every second coefficients are zero



Digital Decimation Filters for Sigma-Delta ADCs (Cont.)

- Realization of Sinc FIR

  Sinc filter : averaging filter

  Sinc^{L+1} for Lth-order SDM

  Example : average-of-M sinc filter

$$\mathrm{Sinc}(z) = \frac{1}{M}\sum_{i=0}^{M-1} z^{-i} = \frac{1}{M}\left(\frac{1-z^{-M}}{1-z^{-1}}\right)$$

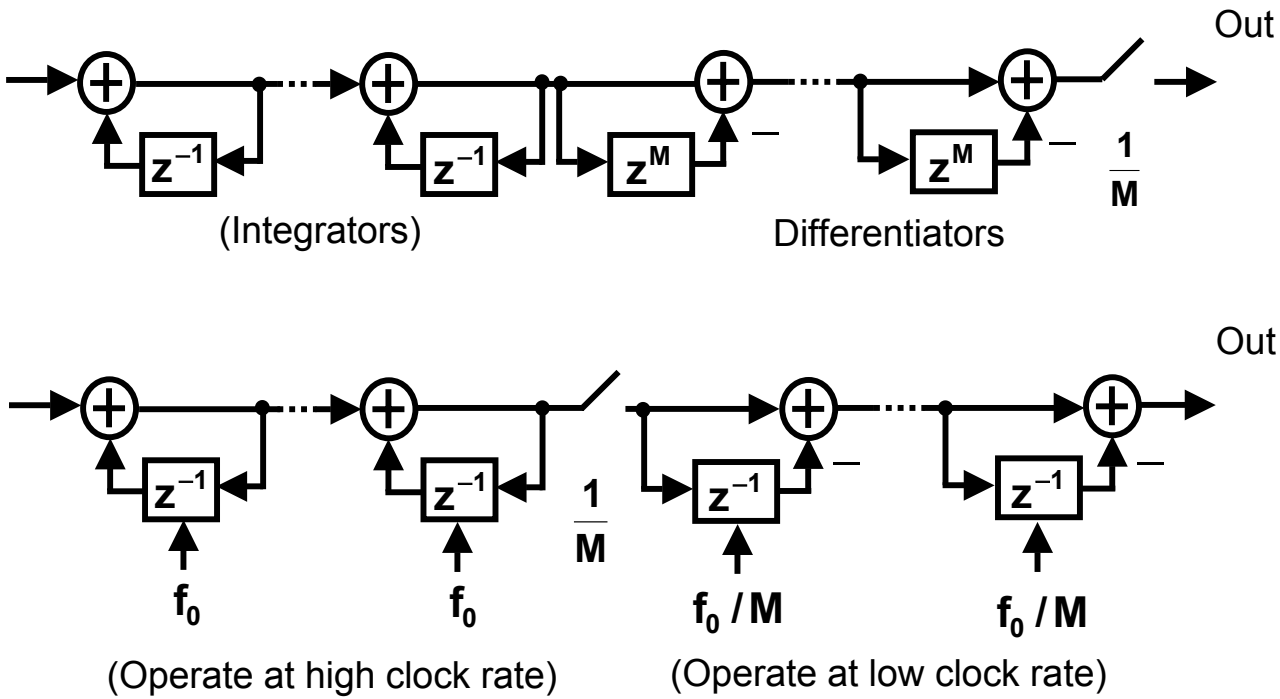
$$\mathrm{Sinc}^{L+1}(z) = \left(\frac{1}{1-z^{-1}}\right)^{L+1}(1-z^{M})^{L+1}\frac{1}{M^{L+1}}$$

Digital Decimation Filters for Sigma-Delta ADCs (Cont.)

Two approaches: (a) downsampling after filtering

(b) downsampling before differentiators

where (b) is more efficient (lower speed)



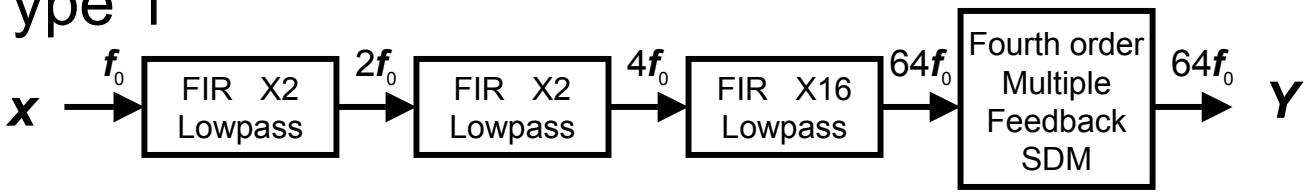
Digital Decimation Filters for Sigma-Delta ADCs (Cont.)

- Single-stage
  - Example: a 2048-tap FIR was used to decimate 1-bit outputs from SDMs
    1. No multi-bit multiplications are needed, since the input is simply 1-bit.
    2. 2048 additions are required during one clock cycle at the Nyquist rate.

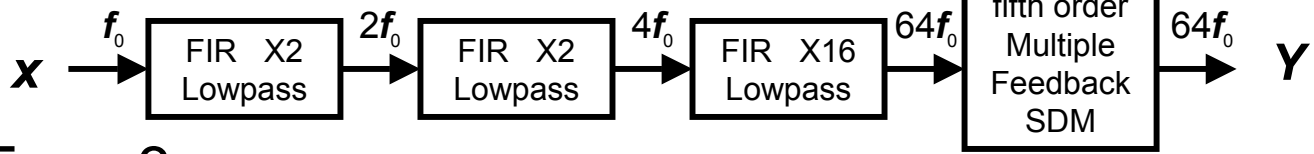
       If the Nyquist rate is 48KHz, a single accumulator would have to be clocked at 98.3MHz

Comparison Four Sigma-Delta DAC Structures

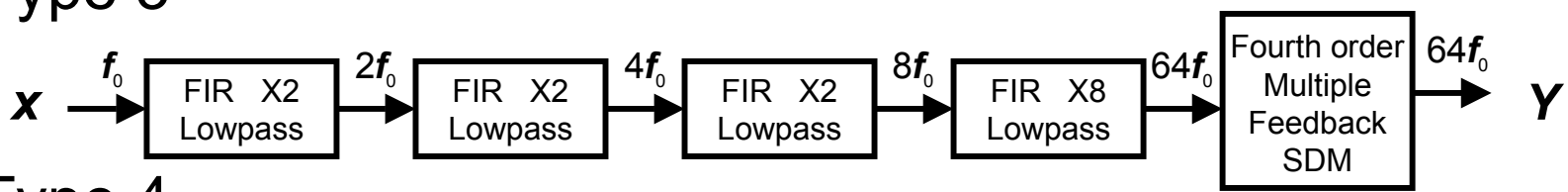
- Type 1



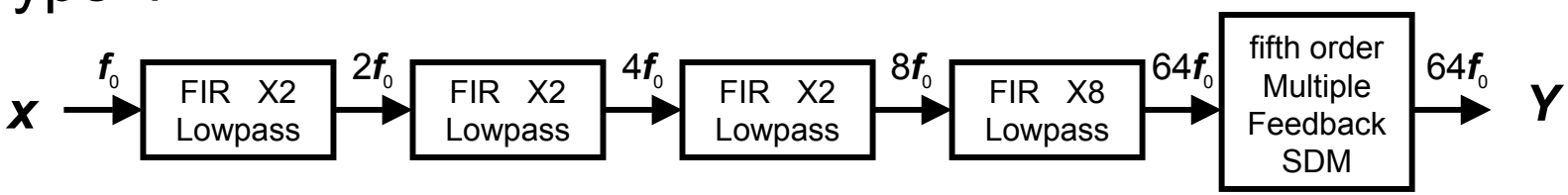
- Type 2



- Type 3



- Type 4



Structure Type	SNR(dB)	DR(dB)	Arithmetic complexity
Type 1	100	97	30
Type 2	108	105	30
Type 3	101	96	42
Type 4	111	105	42

OUTLINE

- Introduction
- Relaxed anti-alias filtering
- Quantization noise
- Oversampling
- Noise shaping
- SDM structures
- Stability
- Idle tone and dither
- High-order sigma-delta modulator synthesis tool (HOST)
- Data weighted averaging (DWA)
- VLSI implementation
- Simulation
- Bandpass oversampling Converters
- Summary

Simulation

- System simulation in frequency / Z domain
  - MATLAB/C/Fortran
  - ADC(analog modulator+digital decimation filter)
    DAC(digital interpolation filter+digital modulator+analog filter)
    1. Signal-to-noise ratio (SNR) and dynamic range (DR)
    2. Gain
    3. Phase or group delay
    4. Coefficient quantization => minimum wordlength required

Simulation(Cont.)

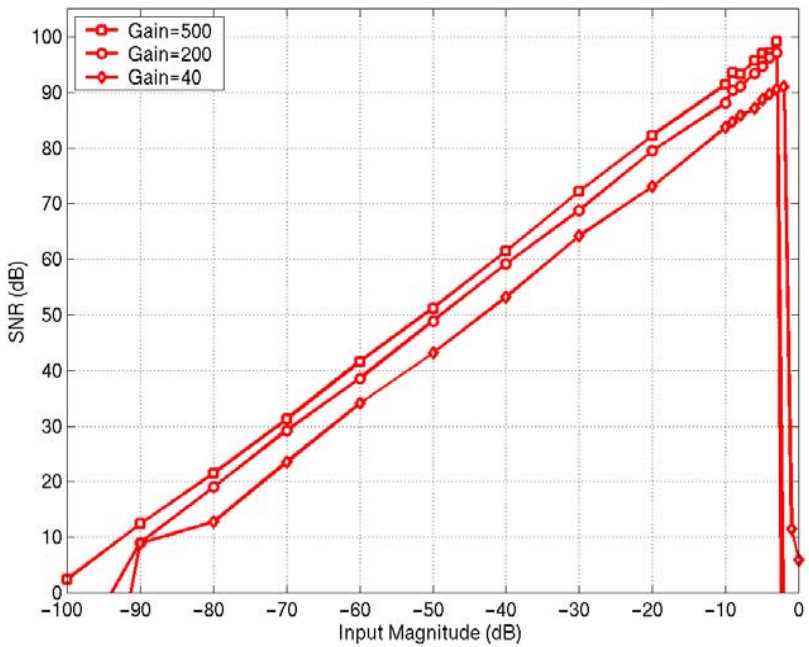
- Time-domain behavior simulation
  - MATLAB/C/Fortran
  - Modulator
    1. Stability
    2. Overload for analog SDM (overflow for digital SDM)
    3. Coefficient scaling
    4. Idle tone
    5. Effects of analog impairments for analog SDM
    6. Signal-to-(noise+distortion) ratio (SNDR) and DR
  - Digital filter
    1. Truncation/rounding : finite wordlength
    2. Transient response
    3. Overflow
- Circuit and logic simulation
  - Spice and logic simulator

Analog Impairments for Modulator Simulation

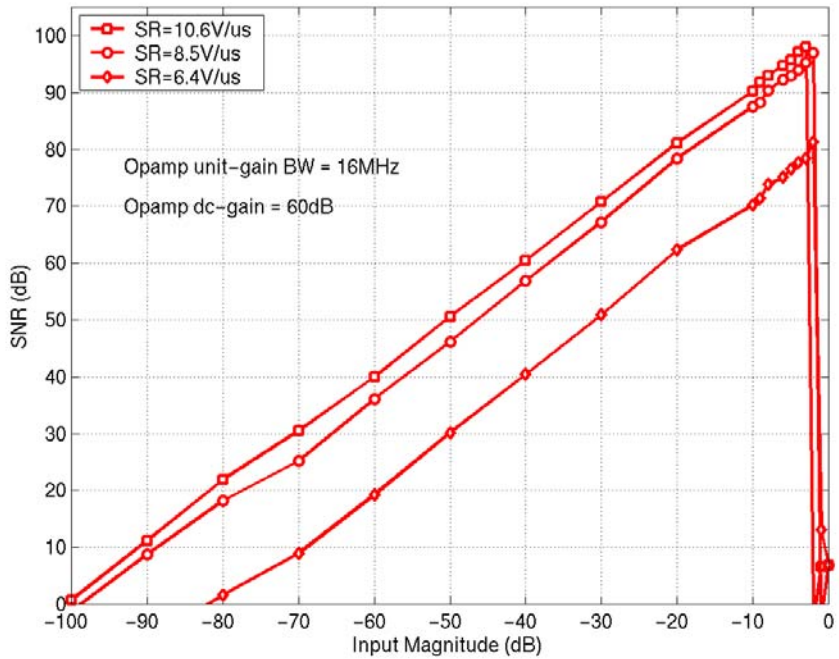
- Analog impairments
  - Operational amplifier: finite gain, finite bandwidth, slew rate limitation, limited swing, offset, nonlinearity, input-referred noise, output resistance
  - Comparator: offset, hysteresis, speed, gain
  - Capacitor: matching, voltage coefficient
  - Switch: nonlinear turn-on resistance, thermal noise, clock feedthrough, charge injection
  - Clock jitter
- Analysis and modeling of impairments
- Approximation and simulation
- Noise coupling (node-to-node, transistor-to-substrate-to-transistor)

Simulation Examples: Effects of Analog Impairments for Analog SDM

- Finite opamp gain



- Finite slew rate



- Many others

OUTLINE

- Introduction
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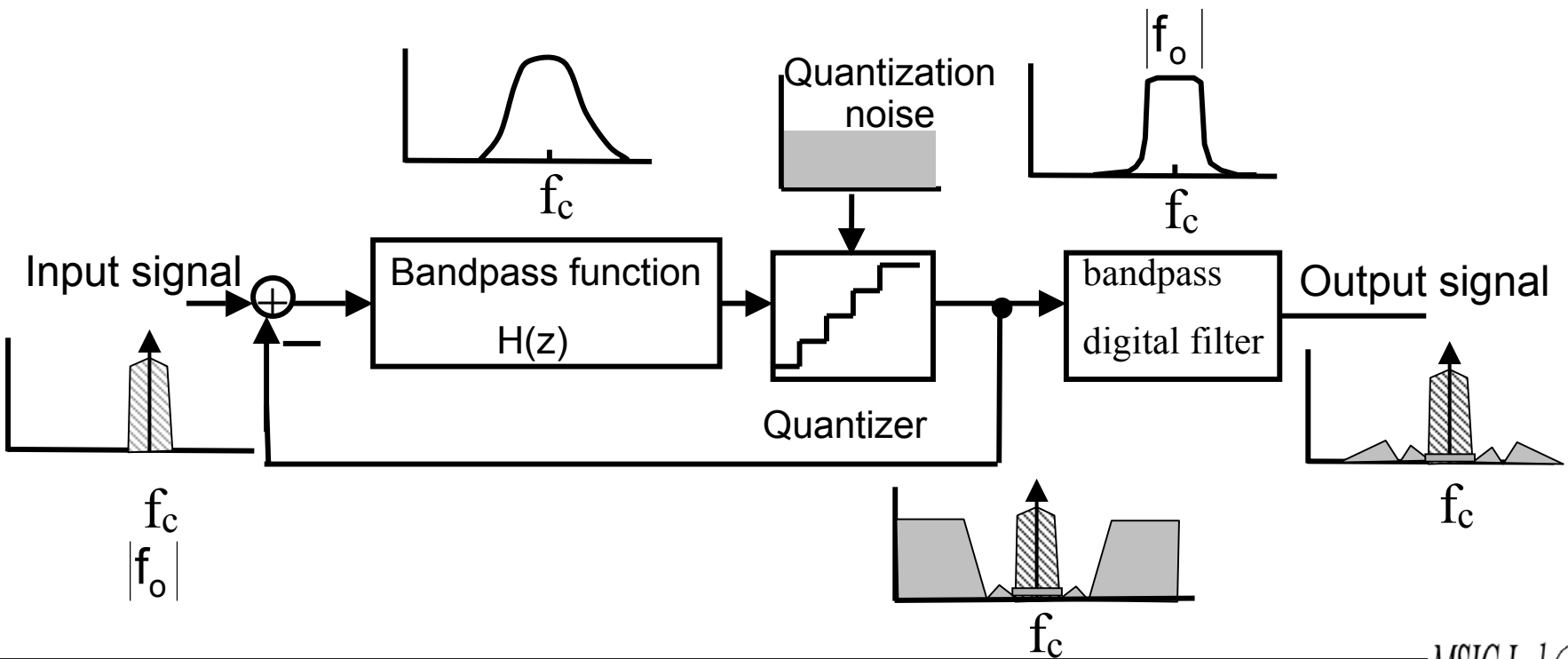
Bandpass Oversampling Converters

- For IF signal processing

  Signals are in a small amount of bandwidth, but have been modulated by higher-frequency carrier.

  – STF: bandpass

  – NTF: bandreject



Bandpass Oversampling Converters(Cont.)

- For lowpass SDMs, H(z) is lowpass and has a high gain near DC, thus quantization noise is small around DC.
- For bandpass SDMs, H(z) is bandpass and has a high gain near f_c, thus quantization noise is samll around f_c,

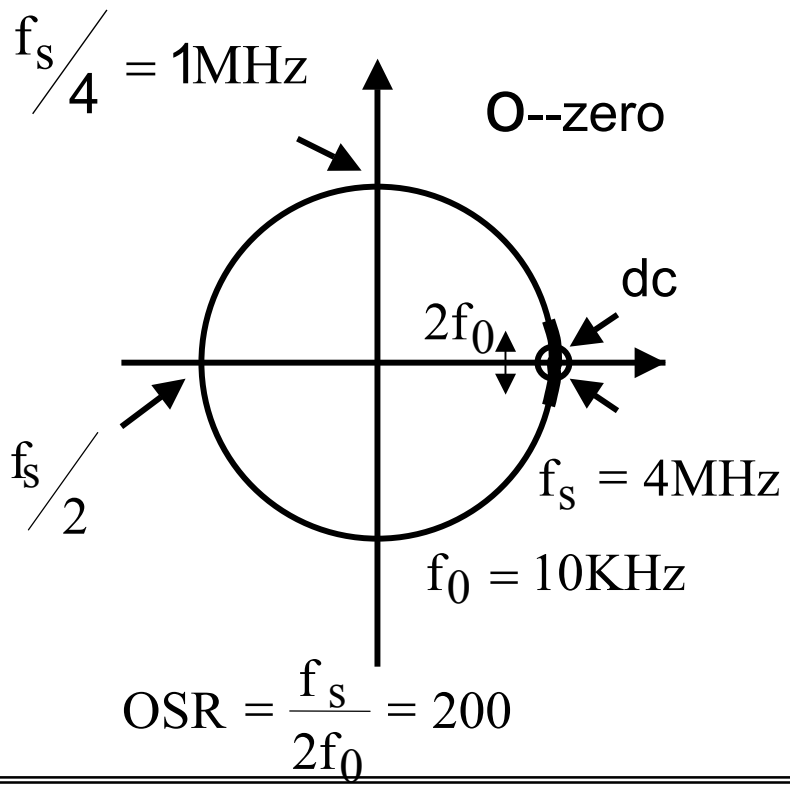
  and therefore most of the quantization noise can be removed through the use of a narrow bandpass filter of total width f_O following the modulator.
- In the case of a bandpass ADC intended for digital radio, post digital filtering would remove quantization noise as well as adjacent radio channels.
- The oversampling ratio for a bandpass converter is $f_s/(2f_o)$

  and does not depend on the value of f_c.

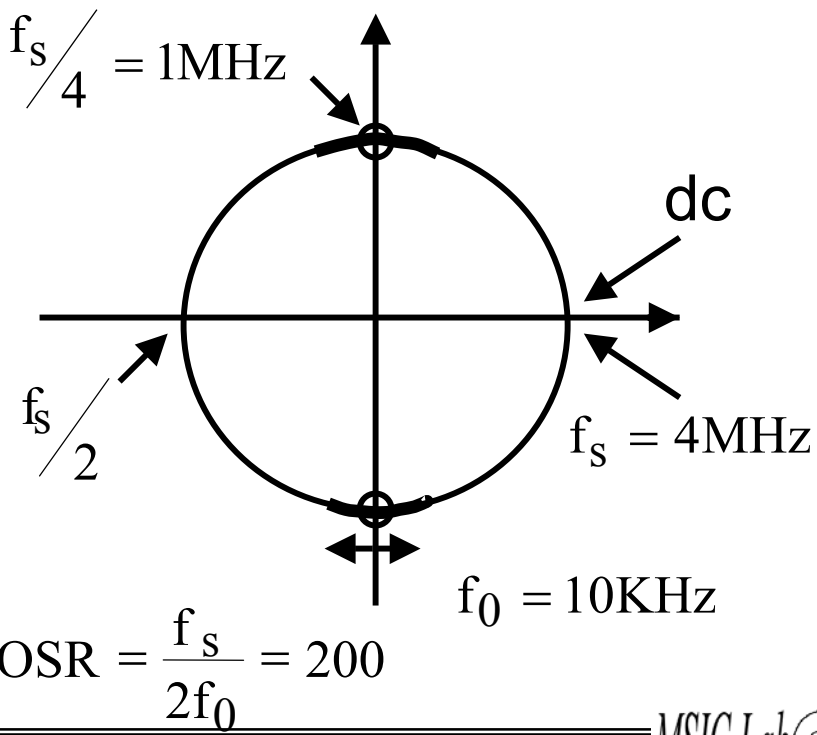
Bandpass Oversampling Converters(Cont.)

- Application example: a 2nd-order bandpass SDM with a sampling frequency $f_s=4f_c$
  - NTF zeros

1st-order lowpass SDM

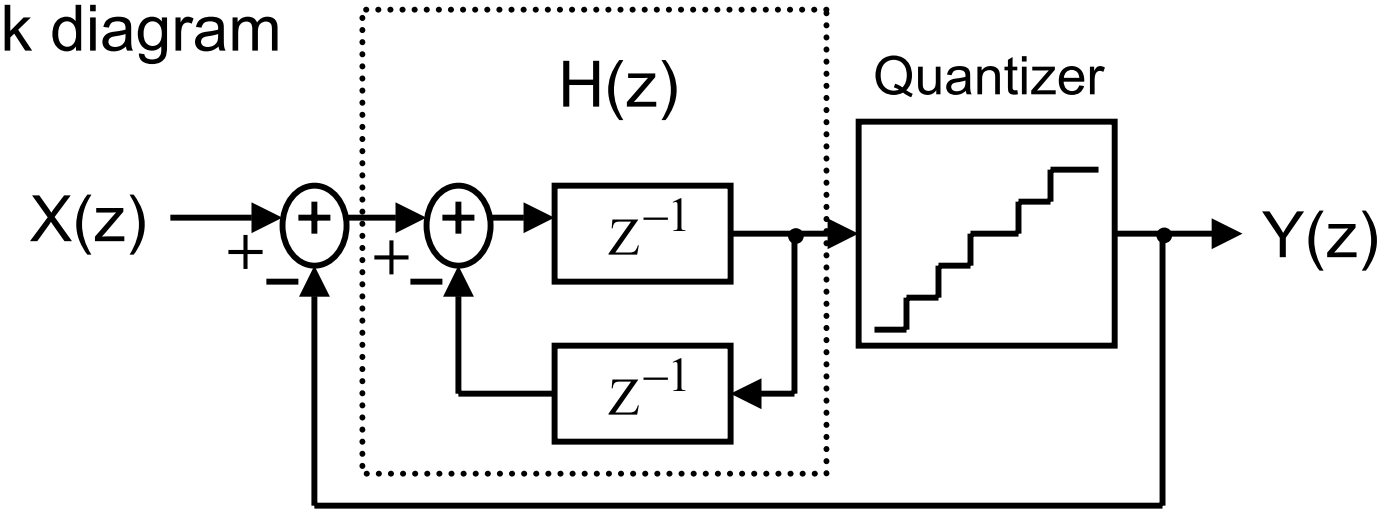


2nd-order bandpass SDM



Bandpass Oversampling Converters(Cont.)

- Block diagram



1. For a 1st-order lowpass SDM

   $H(z)=z^{-1}/(1- z^{-1})$

   NTF zero(i.e. H(z) pole)=1 (DC)

2. For a 2nd-order bandpass SDM

   $H(z)= z^{-1}/(1+ z^{-2})$

   NTF zeros(i.e. H(z) poles)=j, -j

Bandpass Oversampling Converters(cont.)

- Hence, the dynamic range increase of a 2nd-order bandpass converter equals that of a first-order lowpass converter that also has only one zero at DC.

  Specifically, the dynamic range increase of a 2nd-order bandpass converter is 1.5bits/octave or, equivalently, 9dB/octave.

  To obtain the equivalent dynamic range increase of a 2nd-order lowpass converter, a fourth-order bandpass converter would have to be used.

Summary

- The benefits from oversampling combined with noise shaping are substantial
- They are likely to continue to replace high-resolution Nyquist rate converters in many applications with signal bandwidth up to several MHz range, particularly telecom and audio
- Mixed Analog-Digital VLSI technology for implementation
- High resolution analog circuit design is complex and difficult
- Heavy loading on simulation

Summary (Cont.)

- Many challenges still exist:
  - Applications on video and RF
  - Analog circuits:
    1. Low circuit noise
    2. Low supply voltage
    3. High speed
  - Testing:

    Ultra high precision
  - Efficient circuit-level simulator