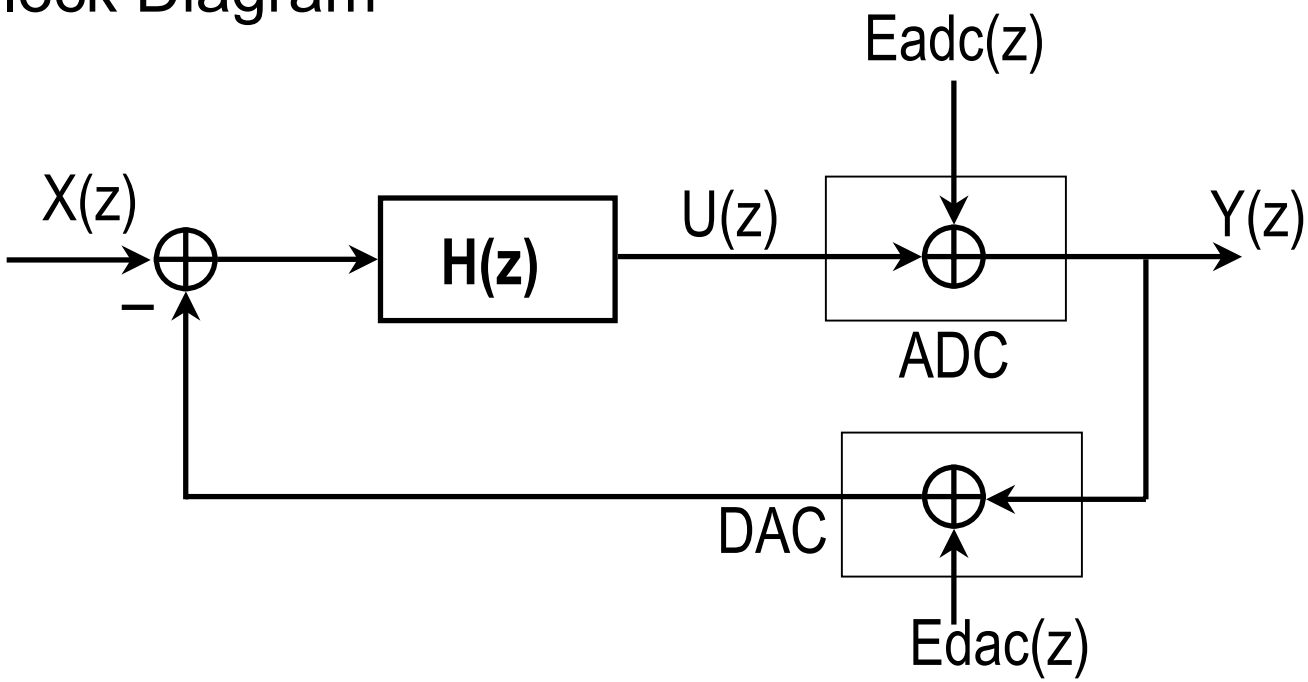
Appendix 4A
Techniques for Overcoming DAC Linearity Problem

- Changed SDM architectures (ISCAS'90,JSSC'91)
- Self-calibration technique (JSSC'91)
- Digital correction (JSSC'93)
- Dynamic element matching, DEM
  - Randomization (JSSC'89)
  - Clock averaging (TCAS-II'92)
  - Individual level averaging (TCAS-II'92)
  - Data weighted averaging ('93 patent : Motolora)
  - Data-directed scrambling ('95 patent : Analog Device)
  - Second-order data weighted averaging (ISCAS'96)
  - Grouped-level averaging (ISSCC'98)
  - Tree structure noise shaping dynamic element matching (ISSCC'98)

Multibit Sigma-Delta Modulator

- Block Diagram

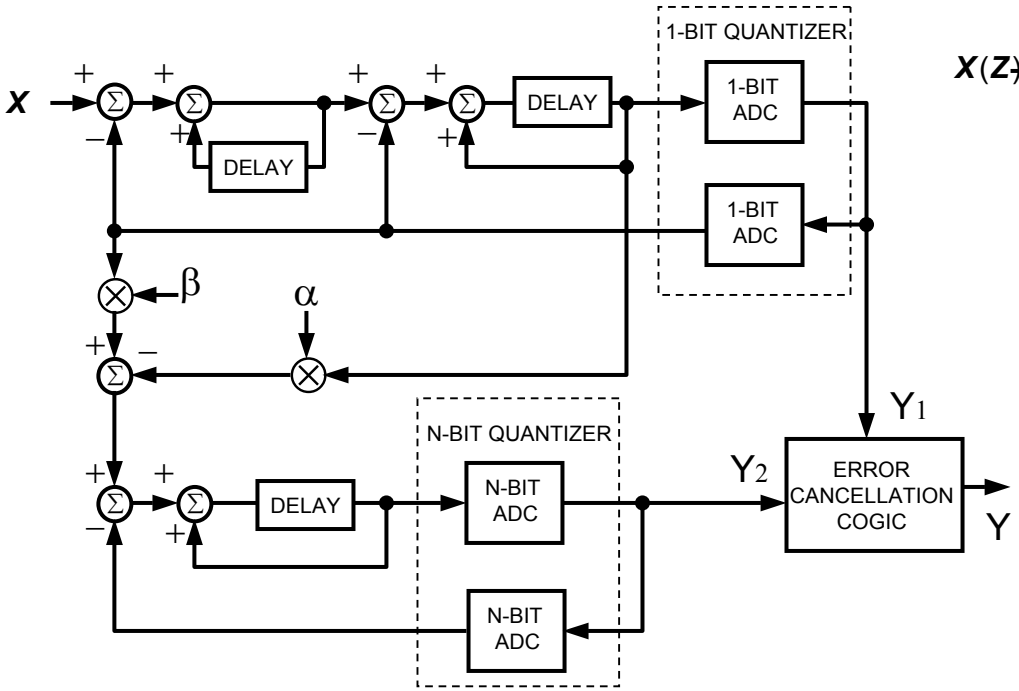


$$Y = \frac{H(z)}{1+H(z)}X(z) + \frac{H(z)}{1+H(z)}Edac(z) + \frac{1}{1+H(z)}Eadc(z)$$

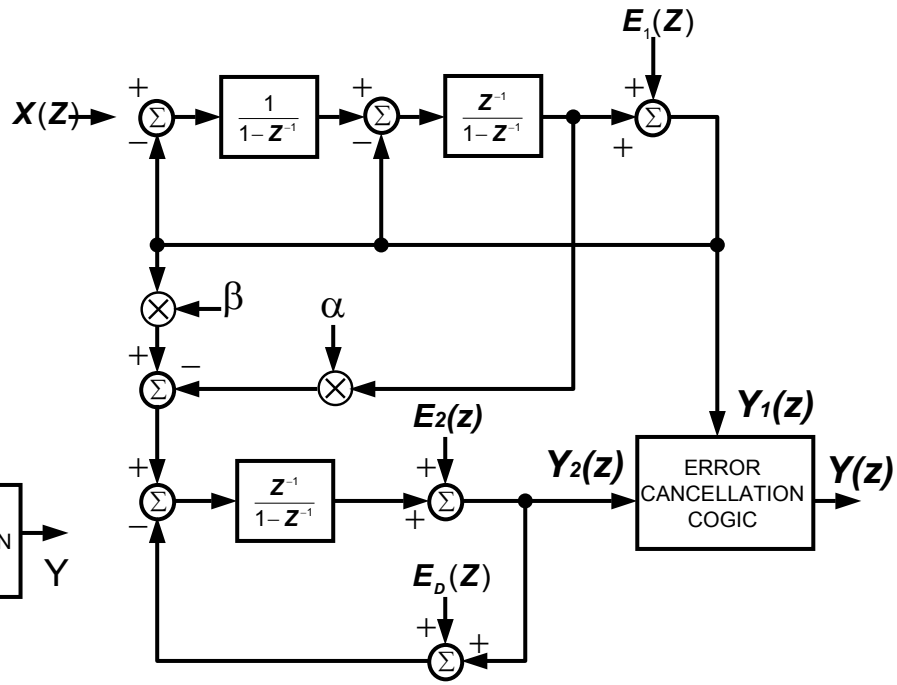
- DAC noise can not be shaped by loop filter

Cascaded Multibit SDM (JSSC'91)

- Block diagram



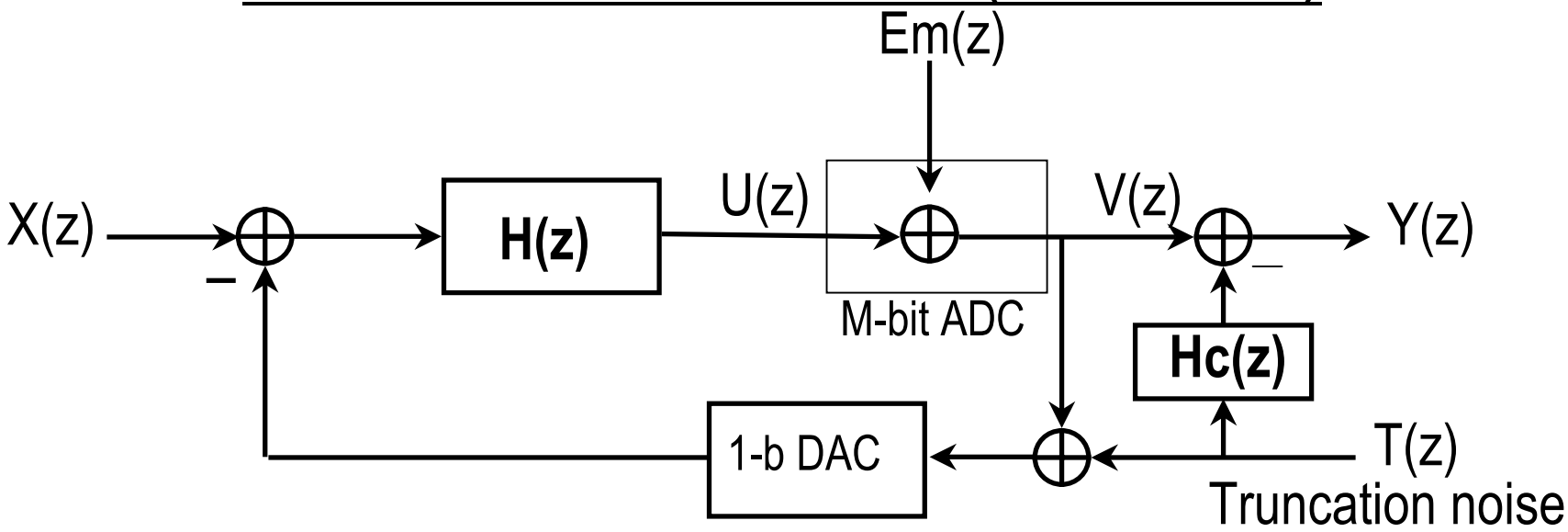
-Linear model



$$Y = z^{-2}X(z) + z^{-1}(1-z^{-1})^2 E_D(z) - (1-z^{-1})^3 E_2(z)$$

- DAC noise is attenuated by second-order noise shaping
- Requirement of better matching for modulator

Leslie's SDM Structure (ISCAS'90)

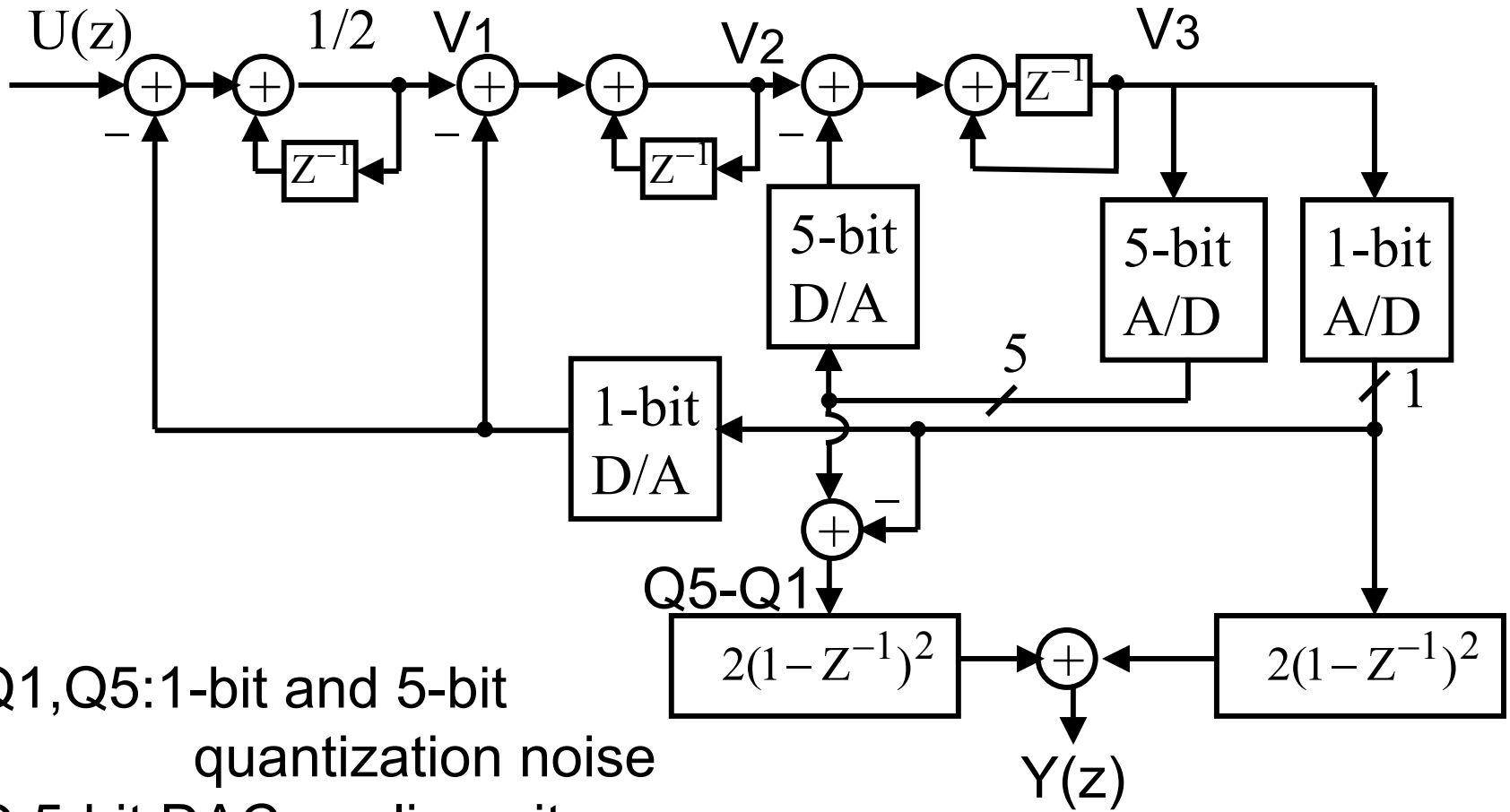


$$V(z) = \frac{H(z)}{1+H(z)}X(z) + \frac{H(z)}{1+H(z)}T(z) + \frac{1}{1+H(z)}Em(z)$$

$$Hc(z) = \frac{H(z)}{1+H(z)}$$

- Requirement of better matching for modulator

Dual Quantization SDM struture(Elctronic Let.'91)



Q1,Q5:1-bit and 5-bit quantization noise

Q:5-bit DAC nonlinearity

$$Us(z) = U(z)z^{-1} + Q1(z)\frac{(1-z^{-1})^2}{1-0.5z^{-1}} - Q5(z)\frac{z^{-1}(1-z^{-1})^{-2}}{1-0.5z^{-1}} - Qd(z)\frac{z^{-1}(1-z^{-1})^{-2}}{1-0.5z^{-1}}$$

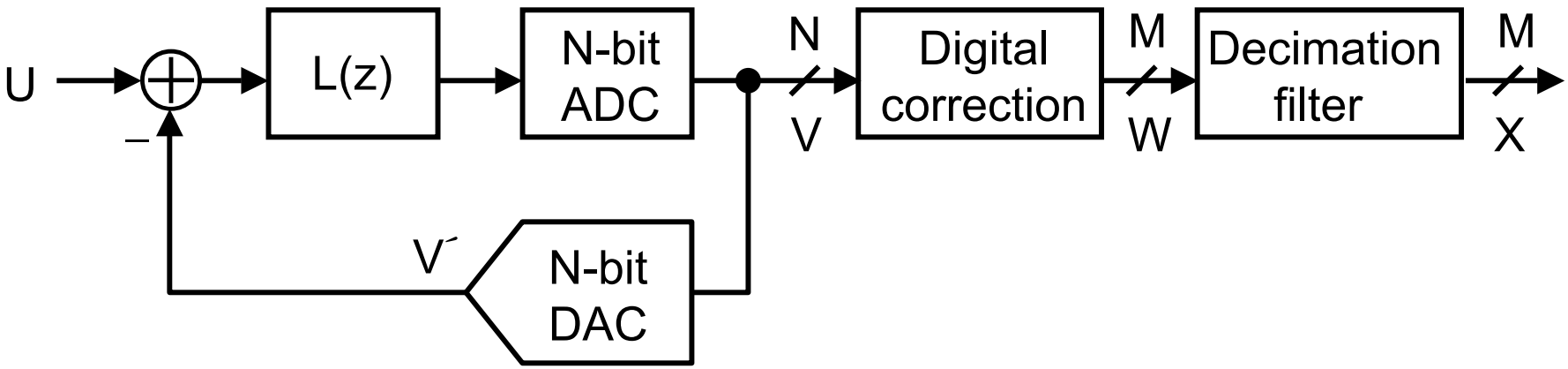
$$Y(z) = U(z)z^{-1} + 2Q5(z)(1-z^{-1})^3 - 2Qd(z)z^{-1}(1-z^{-1})^2$$

Dual Quantization SDM structure(Electronic Let.'91)

- Require better matching between analog and digital circuits.
- If not perfect cancellation => Q1:second-order noise shaping.
- No requirement of any multiplication.
- Complicated realization of the following decimator due to multibit signals.

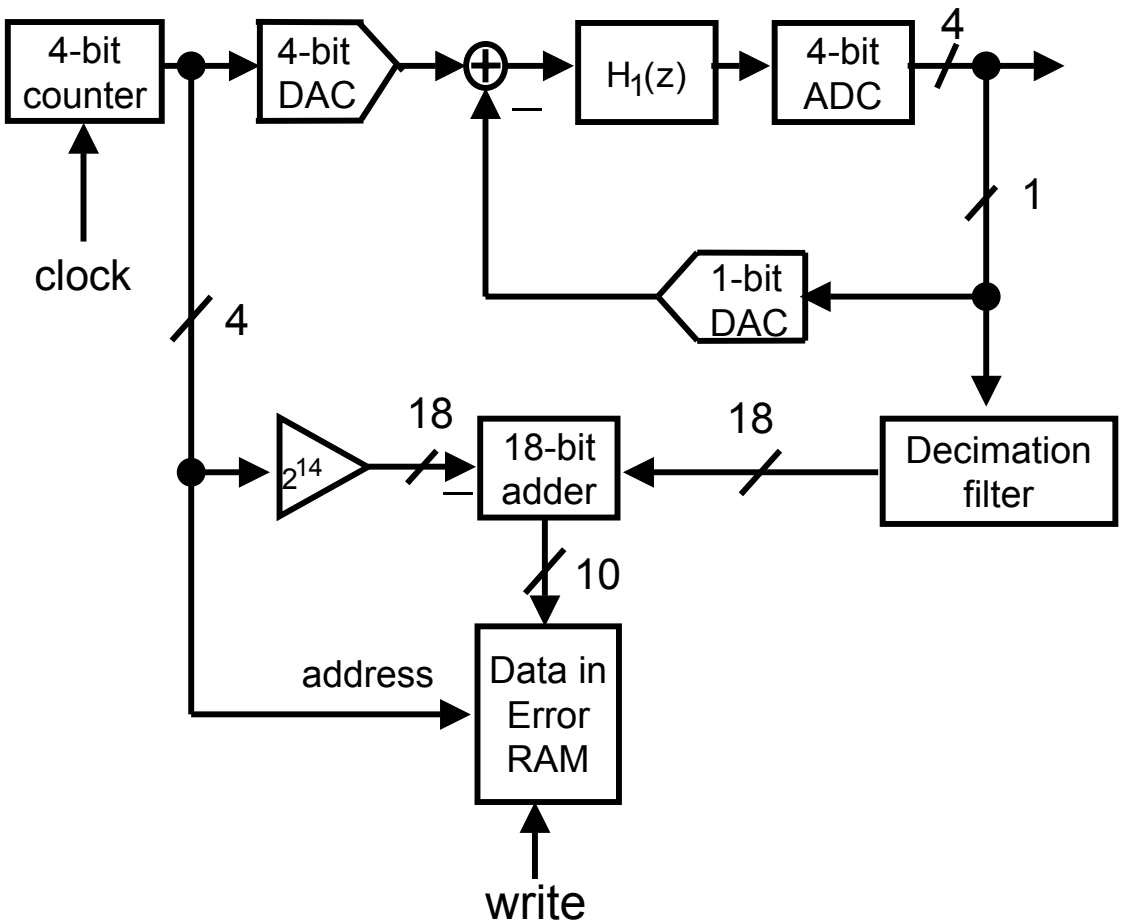
Digital Corrected multibit SDM (JSSC'93)

- Block diagram



Digital Corrected multibit SDM (JSSC'93) (cont.)

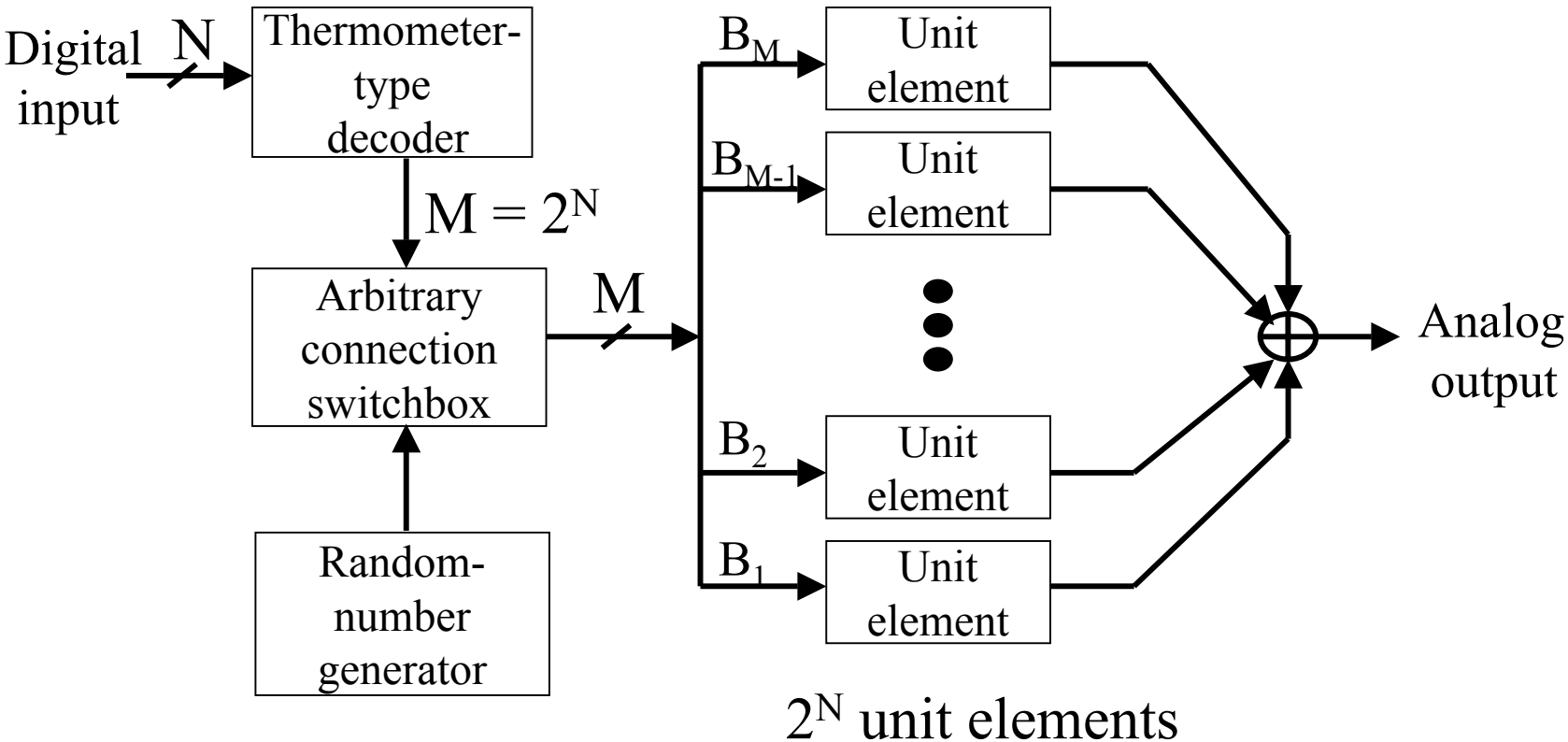
– Calibration technique



- Requirement of complex extra circuits

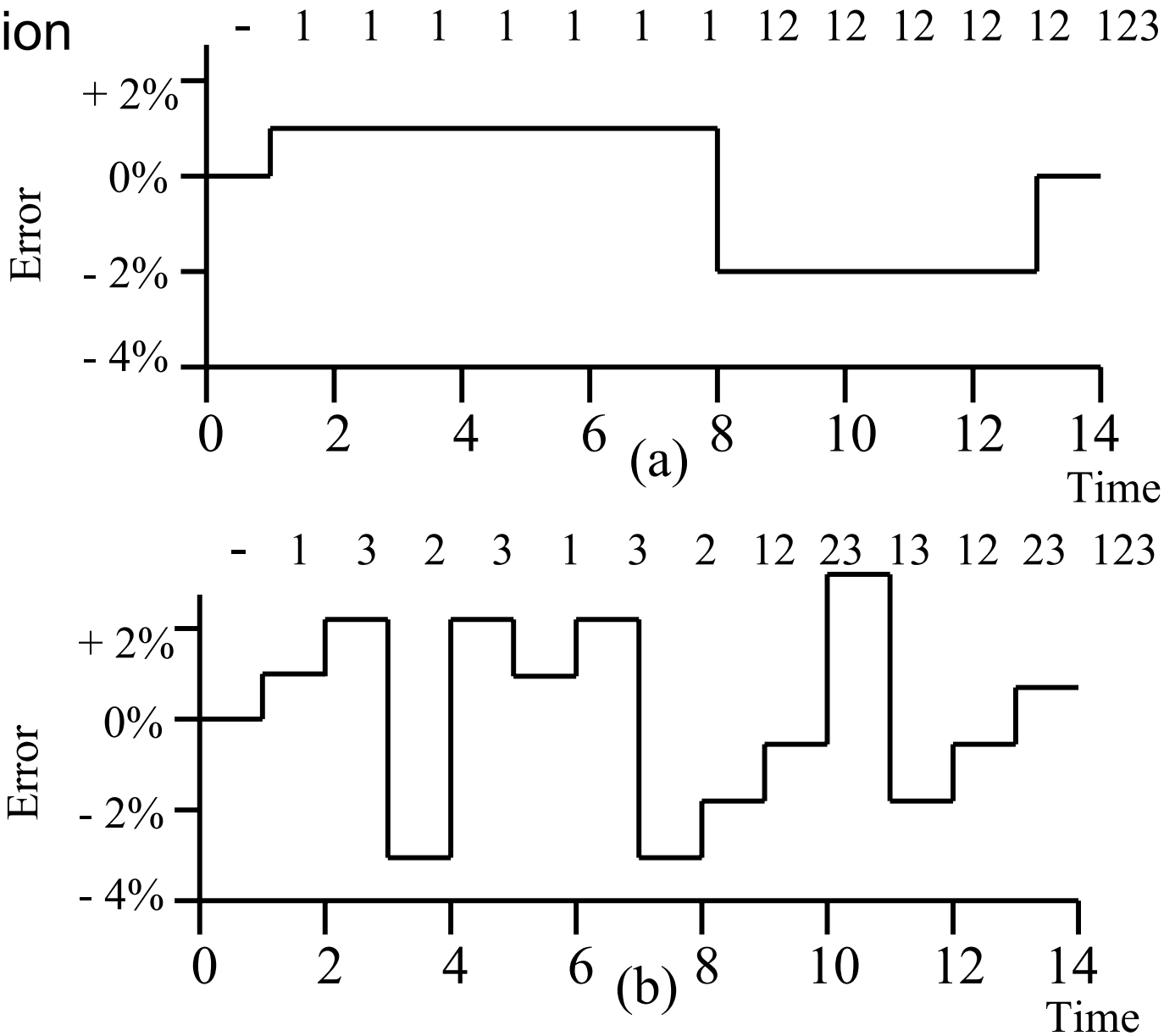
Randomization DEM (JSSC'76, JSSC'98)

- Converting static DAC noise due to element mismatch into time- varying signal, white noise distributed from 0 to fs
- Out-of-band noise can be removed by following filter
- Block diagram



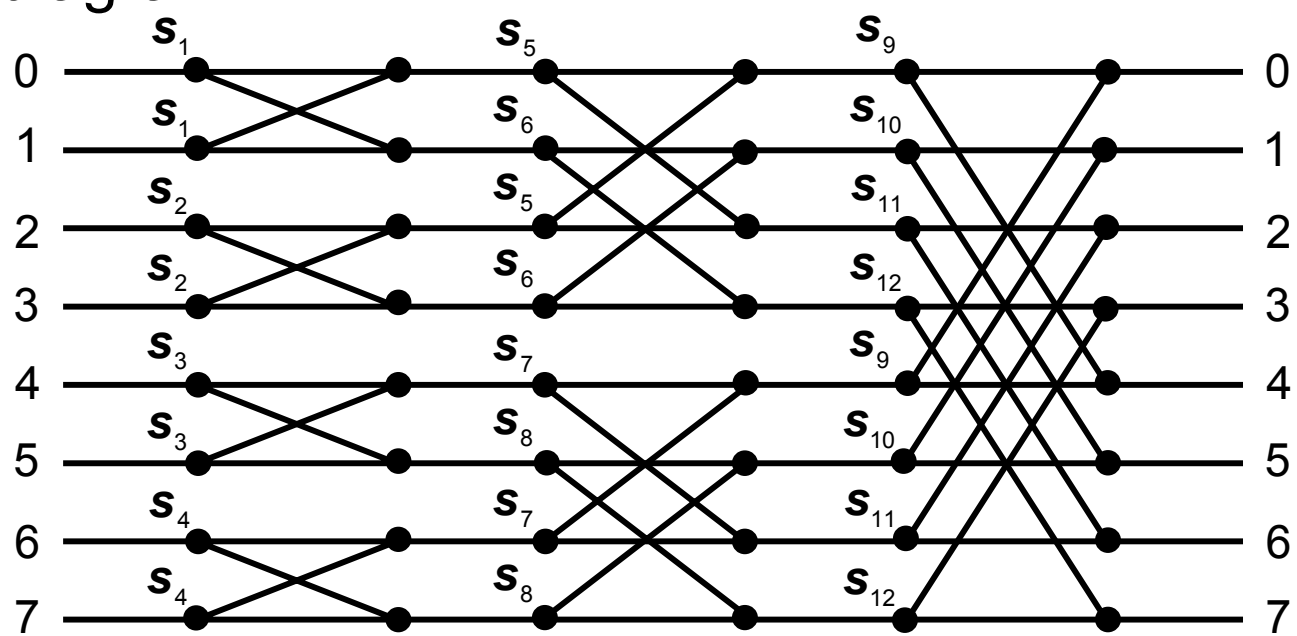
Randomization DEM (JSSC'76, JSSC'98)(cont.)

- simulation



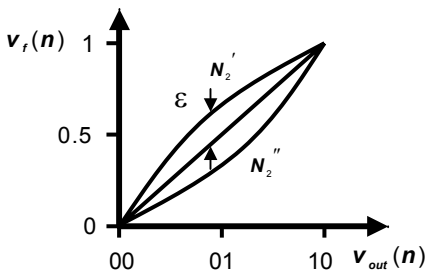
Randomization DEM (cont.)

- Can not completely convert DAC noise to white noise
  - Only pseudo random number generator is achieved
- Butterfly randomizer
  - Pseudo random generator generates control sequence for butterfly switches
  - Block diagram

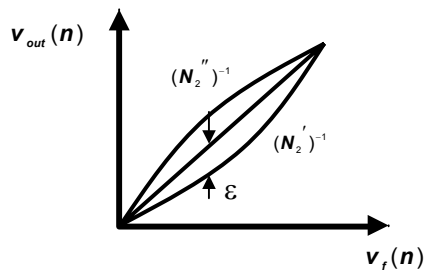


Clock Averaging - CLA (TCAS-II '92)

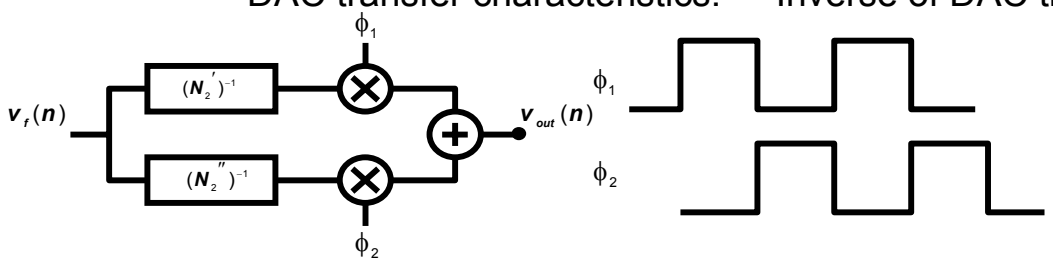
- Principle
  - Using various periodic clocks as switch control signal for selection of DAC elements
  - An element is used at minimum rate of fs/M where M is the number of total elements
  - Harmonic distortion of DAC noise is concentrated at k*fs/M
  - DAC noise is spread uniformly over 0-fs



DAC transfer characteristics.



Inverse of DAC transfer curve

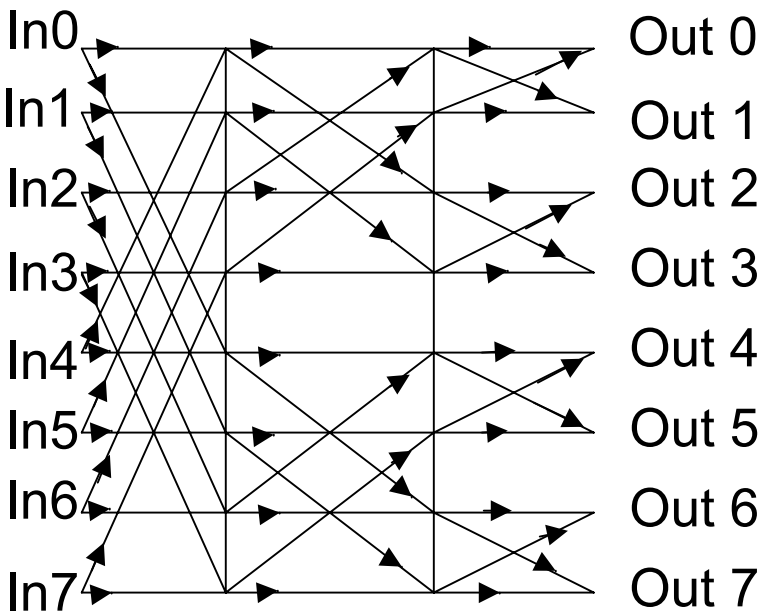


Equivalent representation of clock averaging.

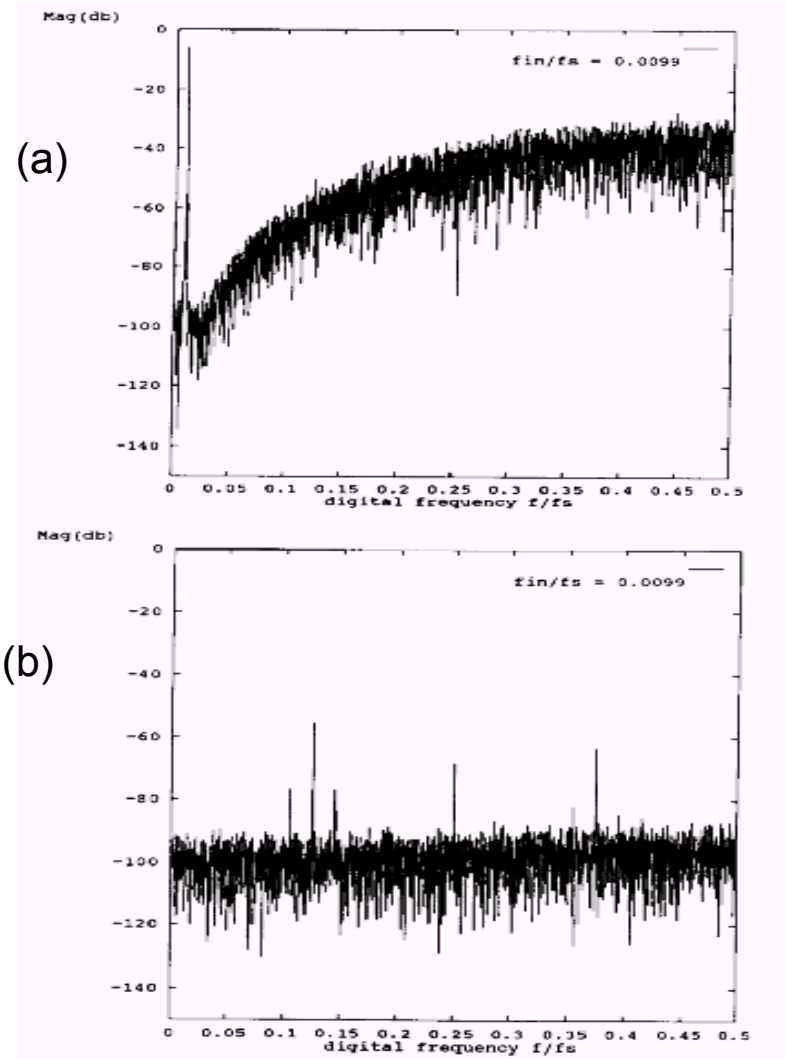
Clock Averaging (cont.)

- Example of 9-level 8 elements DAC

  - Clock flipped algorithm



  - Simulation



(a) Output spectrum of a second-order SDM using clock averaging
(b) DAC error frequency spectrum

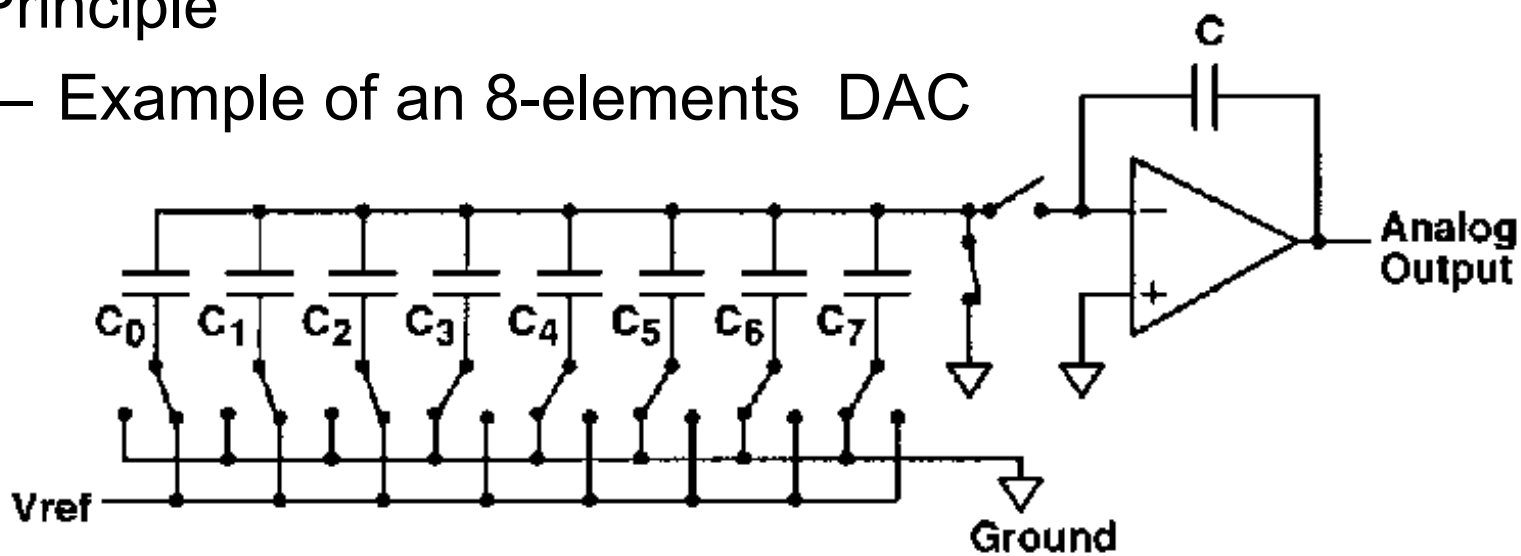
Individual Level Averaging, ILA (TCAS-II, '92)

- Principle
  - 8-elements DAC labeled as number of 1,2,3,4,5,6,7,8

time slot	n	n+1	n+2	n+3	n+4	n+5	n+6	n+7	n+8
Input code	2	3	4	2	4	5	3	5	2
selected elements	1 2	1 2 3	1 2 3 4	3 4	5 6 7 8	1 2 3 4 5	4 5 6	6 7 8 1 2	5 6

Data Weighted Averaging, DWA ('93 US Patent)

- Principle
  - Example of an 8-elements DAC



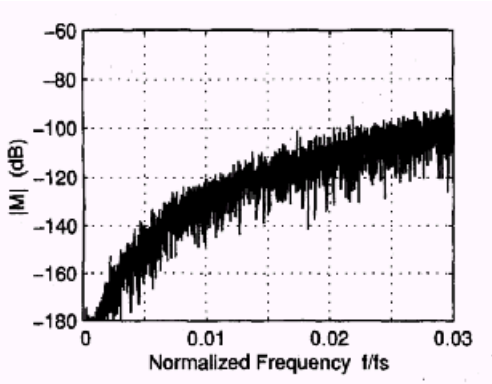
time slot	n	n+1	n+2	n+3	n+4	n+5
DAC input code, y(n)	3	4	0	2	5	3
pointer position, ptr(n)	3	7	7	1	6	1
selected elements	C_0 C_1 C_2	C_3 C_4 C_5 C_6		C_7 C_0	C_1 C_2 C_3 C_4 C_5	C_6 C_7 C_0

- DWA ideally performs first-order DAC-noise shaping

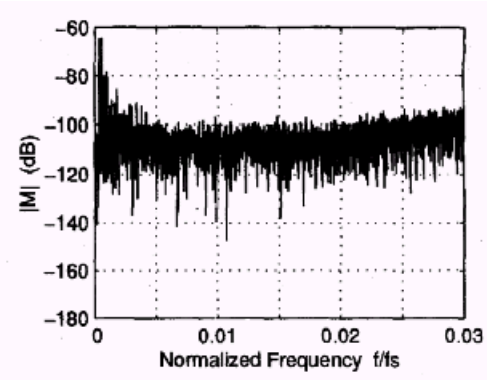
Performance Comparison

- Demonstrated by a 9-level 3rd-order SDM with 1% DAC component mismatch

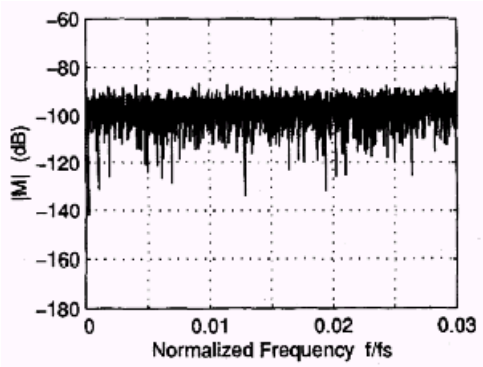
-Ideal DAC



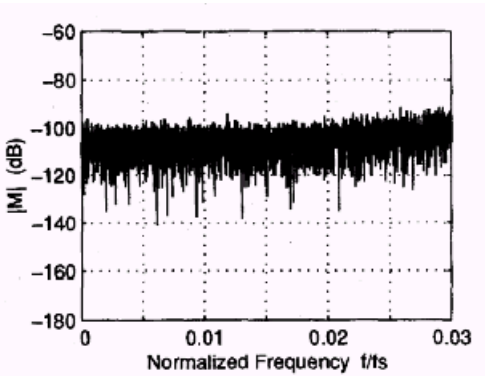
-DAC with 1% mismatch



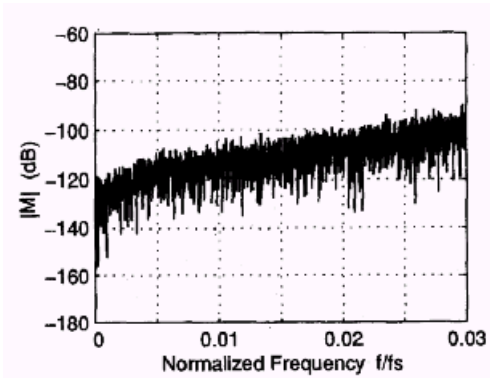
Randomization



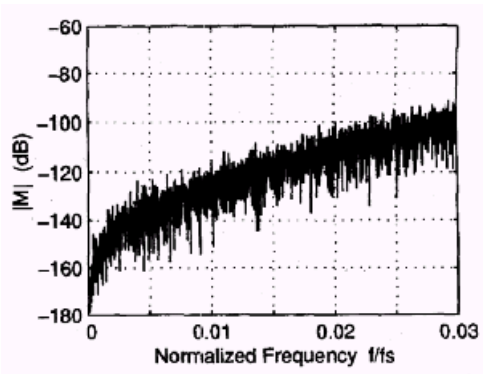
- CLA



-ILA



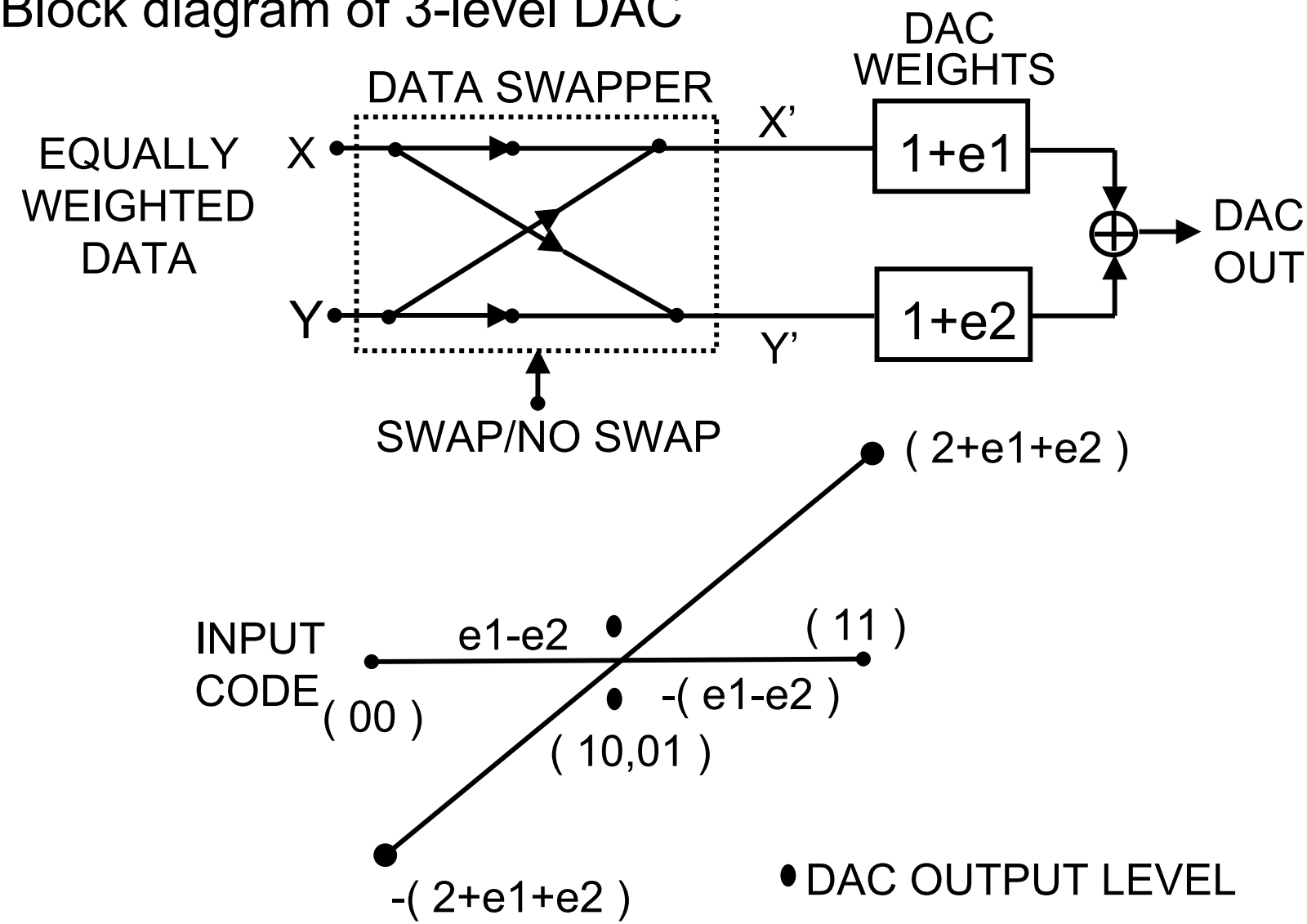
-DWA



- Data Weighted Averaging (DWA) has best performance

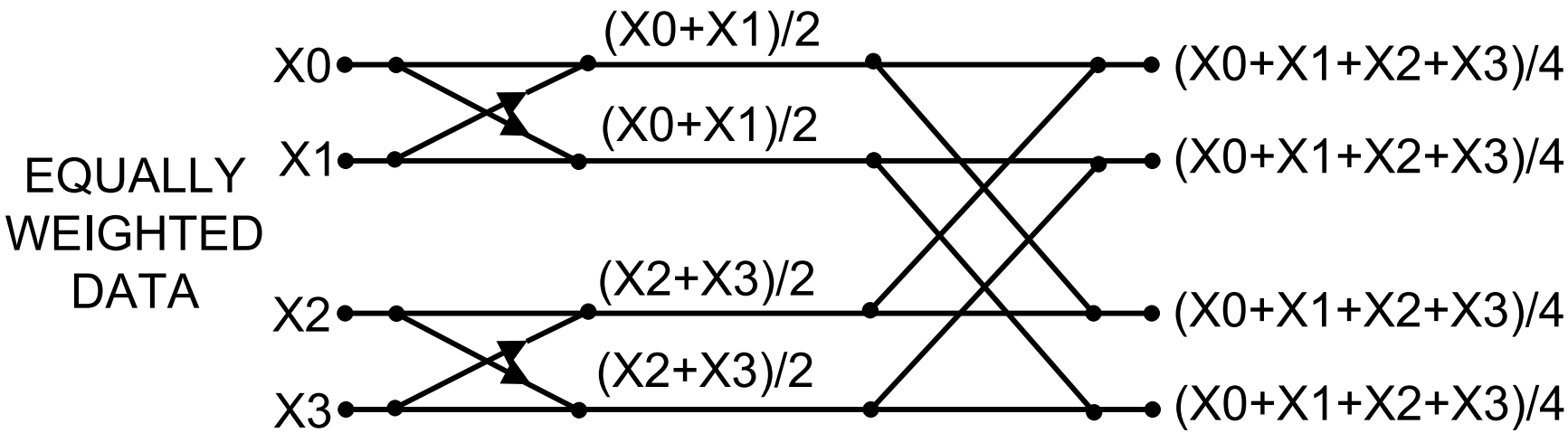
Data Directed Scrambling (‘95 US Patent)

- Block diagram of 3-level DAC



Data Directed Scrambling (‘95 US Patent)(cont.)

- A 4-element butterfly data-directed scrambler



Others DEM Techniques

- Second-order data weighted averaging (ISCAS'96)
  - DAC elements must be sampled two times
  - Doubling DAC sampling frequency or doubling OPAMP speed
- Grouped-level averaging (ISSCC'98)
  - Very similar to data-weighted averaging
- Tree structure noise shaping dynamic element matching (ISSCC'98)
  - Requirement of large extra digital circuits for implementation of this algorithm
  - higher cost

Summary

- Multibit sigma-delta converters become popular due to developments of novel dynamic element matching techniques

- Data weighted averaging algorithm
  - First-order DAC noise shaping ideally
  - Most efficient on attenuation of DAC noise
  - Lowest cost for implementation