Appendix 4B:Circuit Non-ideal Effect Analysis

Outlines

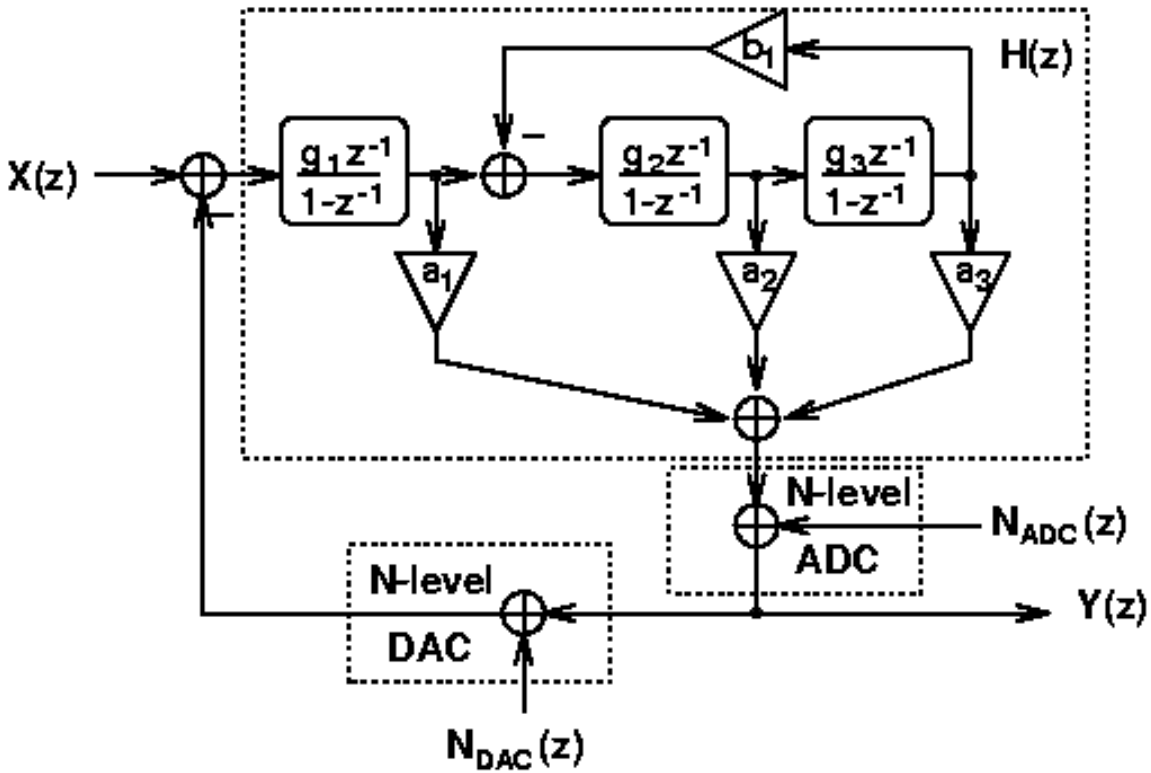
1. Design Example
2. Opamp DC gain and gain nonlinearity
3. Opamp bandwidth and slew rate
4. Capacitance nonlinearity
5. Coefficient mismatch
6. Noise Budget

Design Example

- A third-order 3-bit sigma-delta modulator
  - OSR=32
  - Bandwidth=20kHz
  - Fs=1.28MHz
  - PSNR=99dB (ideally)
  - DAC feedback reference(full scale)= ± 1
  - Maximum stable input (without clipping)=± 0.75
  - Maximum integrator output swing= ± 1
  - Integrator saturation level= ± 1.5

Third-Order 3-Bit Sigma-Delta Modulator

- Block diagram



- Coefficients

g1=2.9302

g2=1.1850

g3=0.2017

a1=0.6510

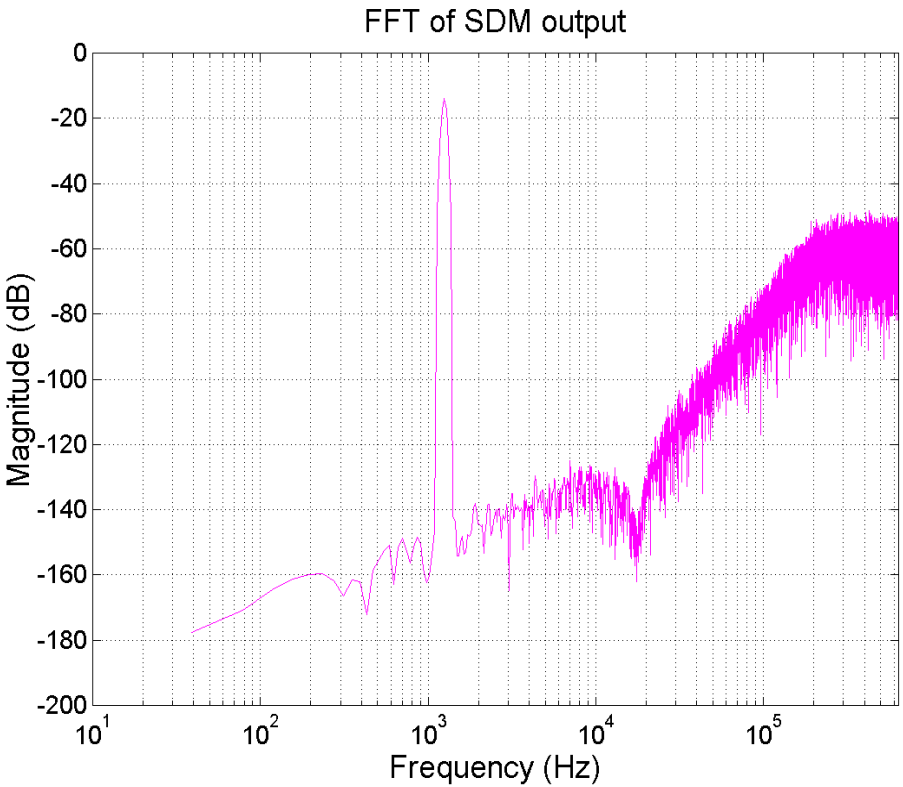
a2=0.4212

a3=0.6025

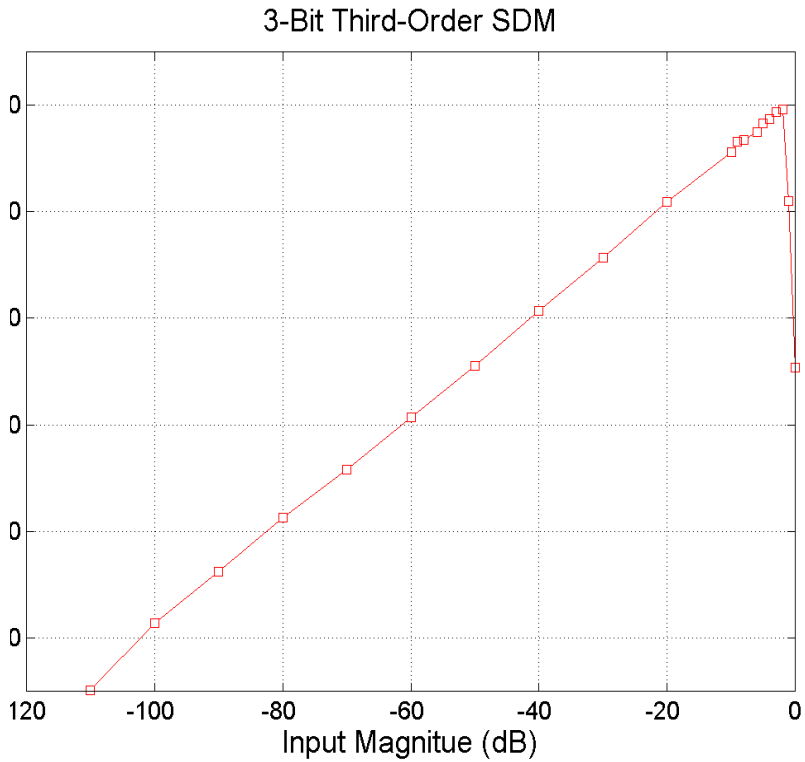
b1=0.0310

SNR Performance

- FFT plot

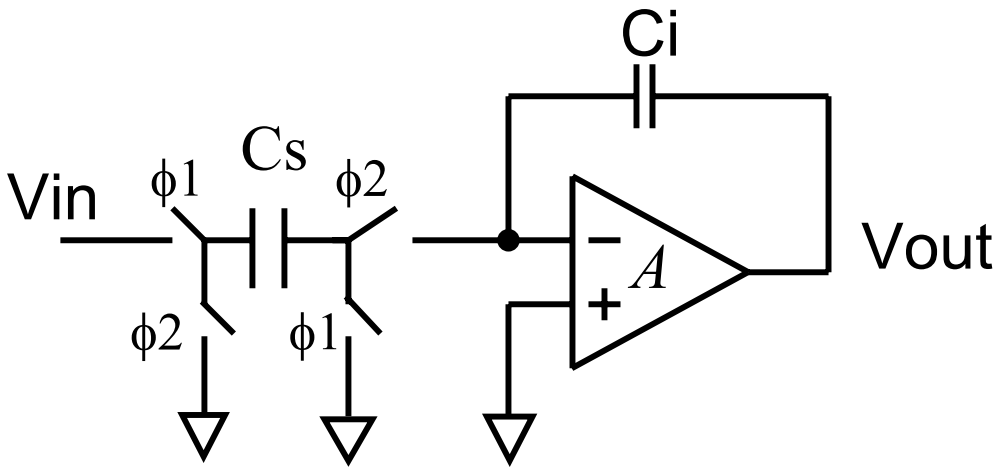


- SNR plot



Opamp DC gain

- SC integrator



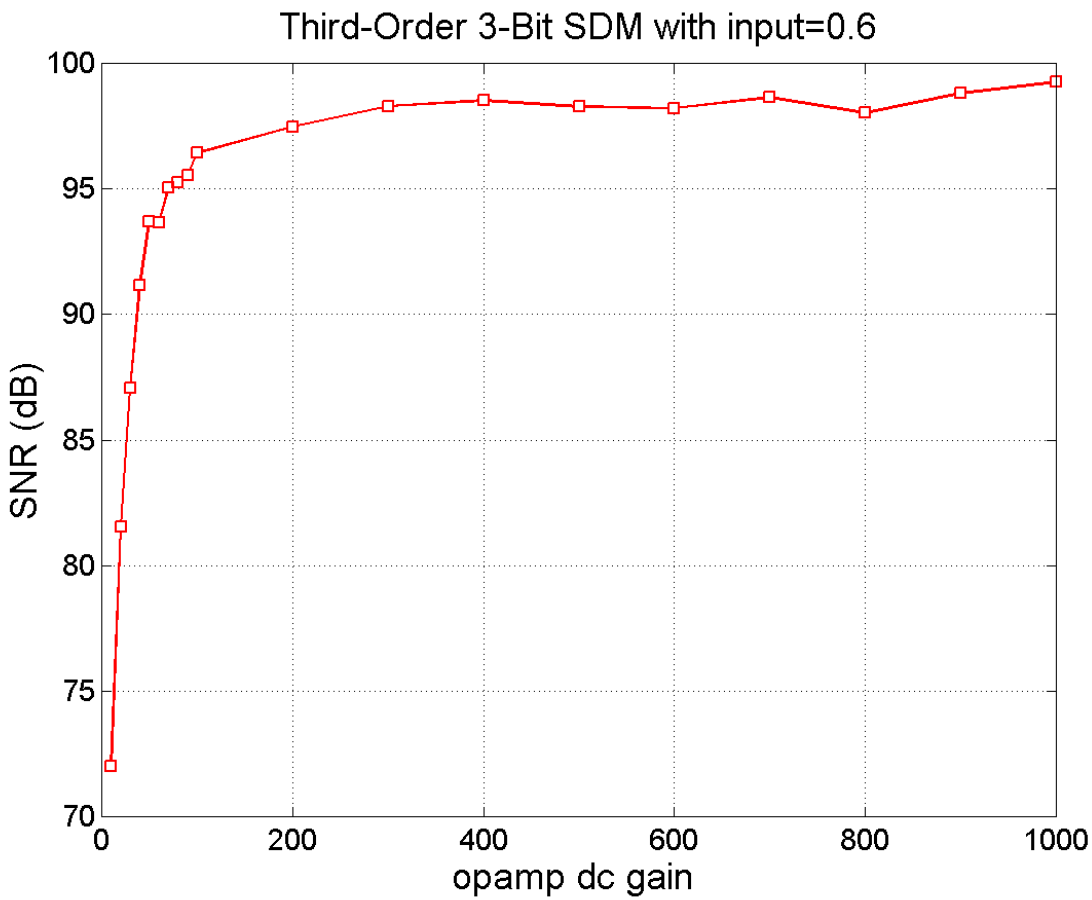
$$H(z) = \frac{Ci}{Cs}\frac{z^{-1}}{1-z^{-1}} = g\frac{z^{-1}}{1-z^{-1}} \qquad Ideal$$

$$H(z) = \frac{\alpha\ z^{-1}}{1-\beta\ z^{-1}} \qquad Nonideal$$

– where $\alpha = \dfrac{g}{1+\frac{1}{A}(1+g)}$ $\beta = \dfrac{1+\frac{1}{A}}{1+\frac{1}{A}(1+g)}$

Simulation

- Opamp gain > 400

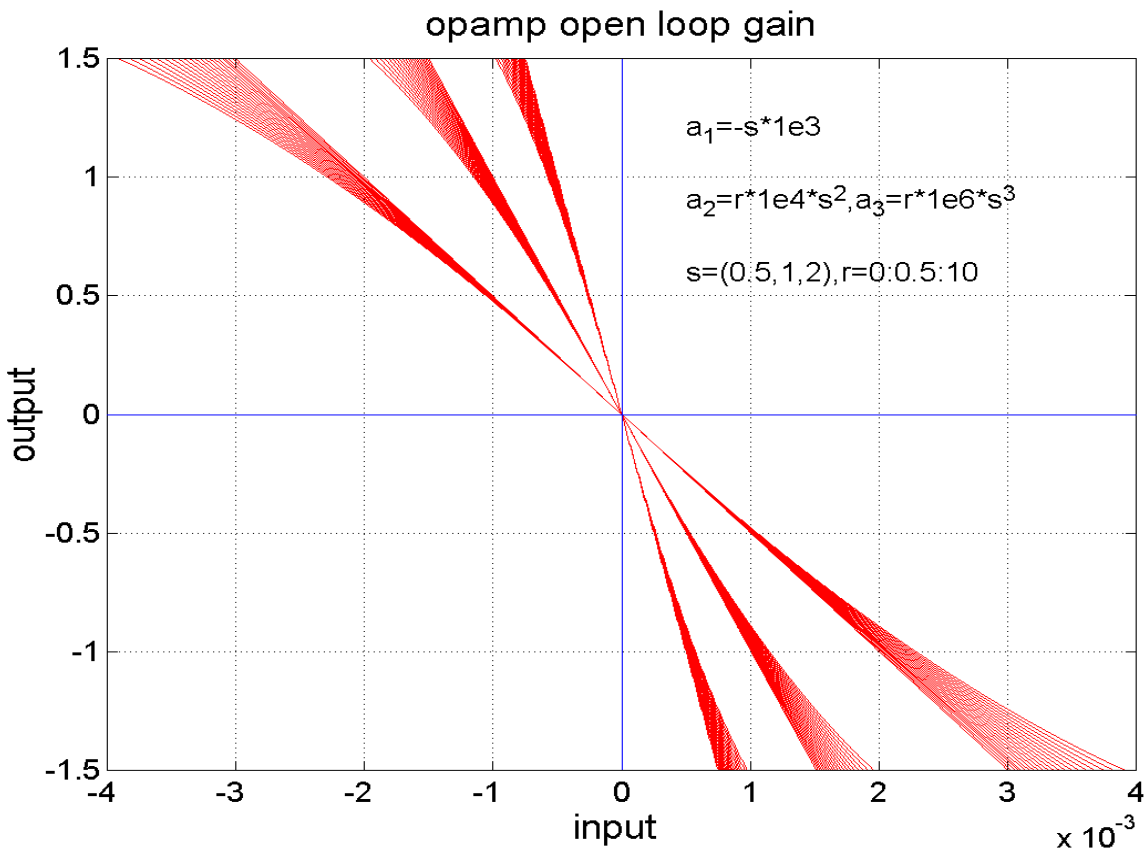


Opamp Gain Nonlinearity

- Assume opamp open loop output/input

$$v_o = a_1 v_i + a_2 v_i^2 + a_3 v_i^3$$

- Open loop gain simulation



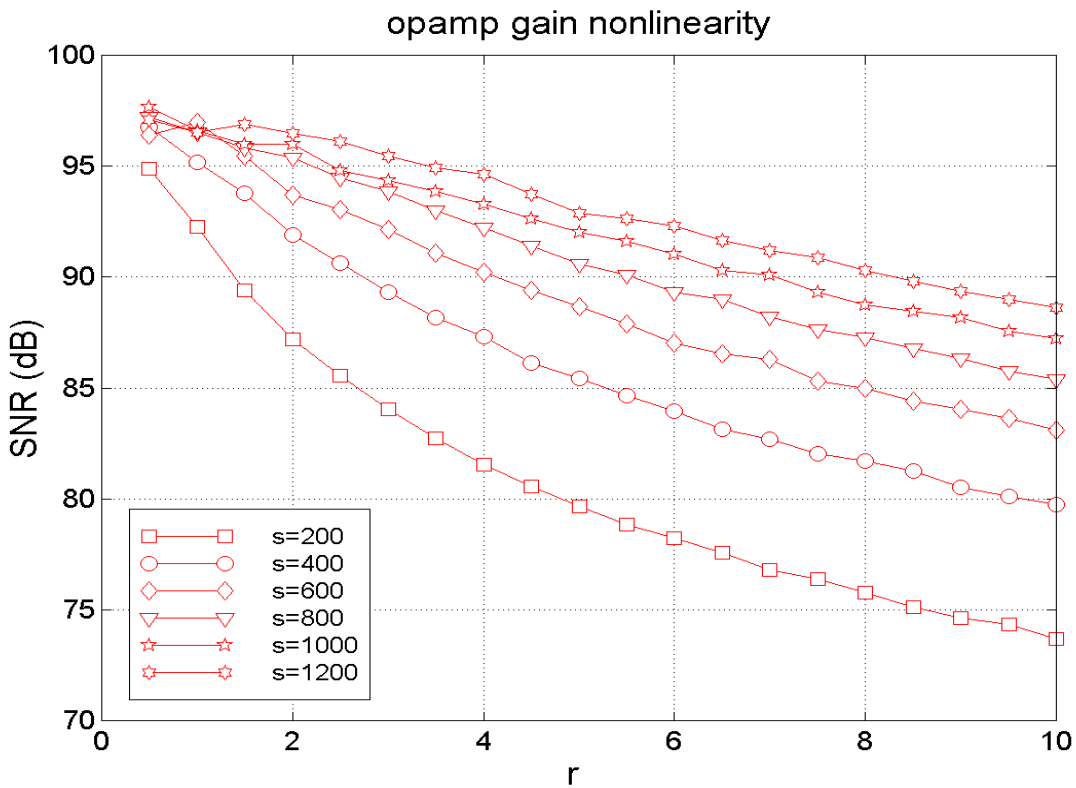
Opamp Gain Nonlinearity(cont.)

- Integrator output

$$v_o(n)-v_o(n-1)\cong g\{v_i(n-1)[1+\frac{1}{a_1}]-\frac{a_2}{a_1^3}[v_i(n-1)[v_o(n)+v_o(n-1)]-v_o^2(n)]$$

$$-\frac{a_3}{a_1^4}[v_i(n-1)[v_o^2(n)+v_o(n)v_o(n-1)+v_o^2(n-1)]-v_o^3(n)]$$

- Simulation



Opamp Gain Nonlinearity(cont.)

- Harmonic distortion

$$HD_2 = \frac{a_2}{a_1^3} v_o \sqrt{1 + (\frac{v_o}{2v_i})^2}$$

$$HD_3 = \frac{a_3}{a_1^4} v_o^2 \sqrt{9 + (\frac{v_o}{v_i})^2}$$

- Higher DC gain lowers the harmonic distortions due to opamp gain nonlinearity

Opamp Bandwidth and Slew Rate

- First-order model of the settling characteristics of a SC integrator

$$v_o(n) = v_o(n-1) + g(v_i(n-1))$$

$$g(x) = x(1-e^{-Ts/\tau}) \qquad |x| \le \tau\ S$$

$$= x - \mathrm{sgn}(x)\tau\ Se^{(\frac{|x|}{\tau\ S} - \frac{Ts}{\tau} - 1)} \qquad \tau\ S \le |x| \le (\tau\ + Ts)S$$

$$= \mathrm{sgn}(x)STs \qquad (\tau\ + Ts)S \le |x|$$

$$S = nS_n, \quad S_n = g1 \cdot \Delta / Ts = 2.134 * 10^6 \qquad \tau \cong \frac{Cc(1+g1)}{g_m} = \frac{1+g1}{\omega_t}$$

t : integrator time constant

Ts: sampling duration = 390.625nS

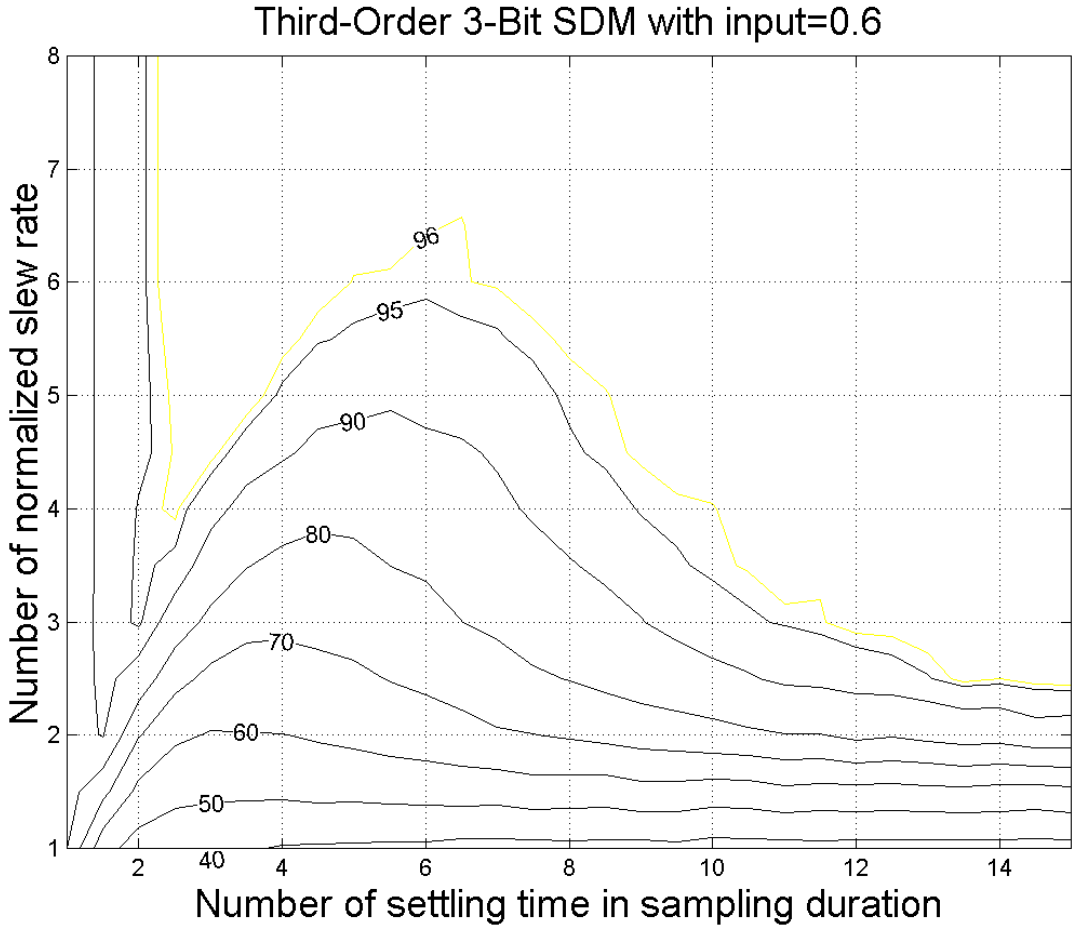
S : slew rate

wt : opamp unit gain frequency

Sn: normalized slew rate

Opamp Bandwidth and Slew Rate(cont.)

- Simulation



- Choose SR=6*SRn, Ts=7*t,SR=6*2.134*10^6=12.8V/u , t=Ts/7=55.8nS, ft= wt/(2p)=11.2MHz

Capacitance Nonlinearity

- Capacitance value is dependent on the voltage drop of the capacitor

$$C(v) = C_0(1 + k_1 v + k_2 v^2)$$

- Integrator output

$$v_o(n) - v_o(n-1) \cong g\{v_i(n-1) - \frac{k_1}{2} v_i(n-1)[-v_i(n-1) + v_o(n) + v_o(n-1)]$$

$$- \frac{k_2}{3} v_i(n-1)[-v_i^2(n-1) + v_o^2(n) + v_o(n)v_o(n-1) + v_o^2(n-1)]\}$$

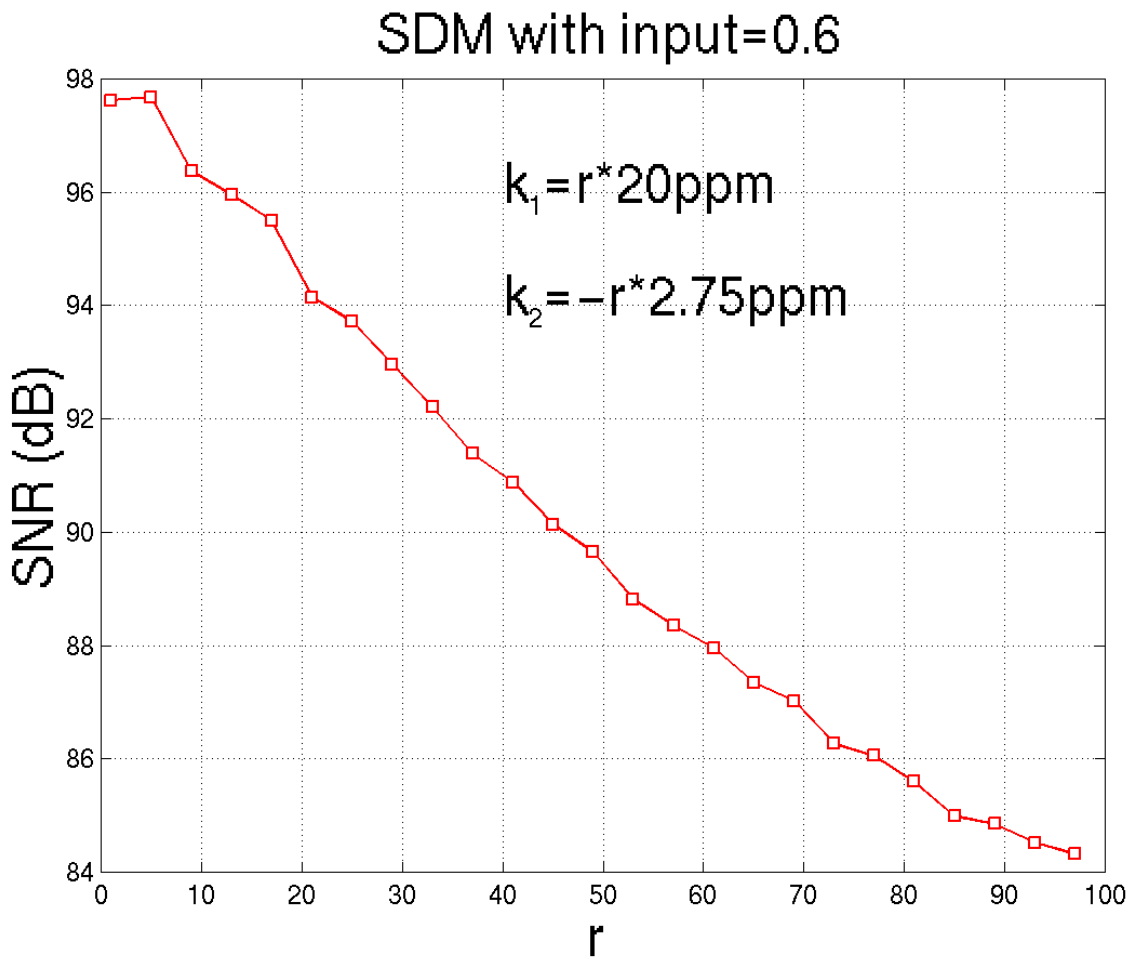
- Harmonic distortion

$$HD_2 = \frac{k_1}{2}\sqrt{v_o^2 + (\frac{v_i}{2})^2}$$

$$HD_3 = \frac{k_2}{2}\sqrt{3v_o^2 + (\frac{v_i}{2})^2}$$

Capacitance Nonlinearity(cont.)

- Simulation

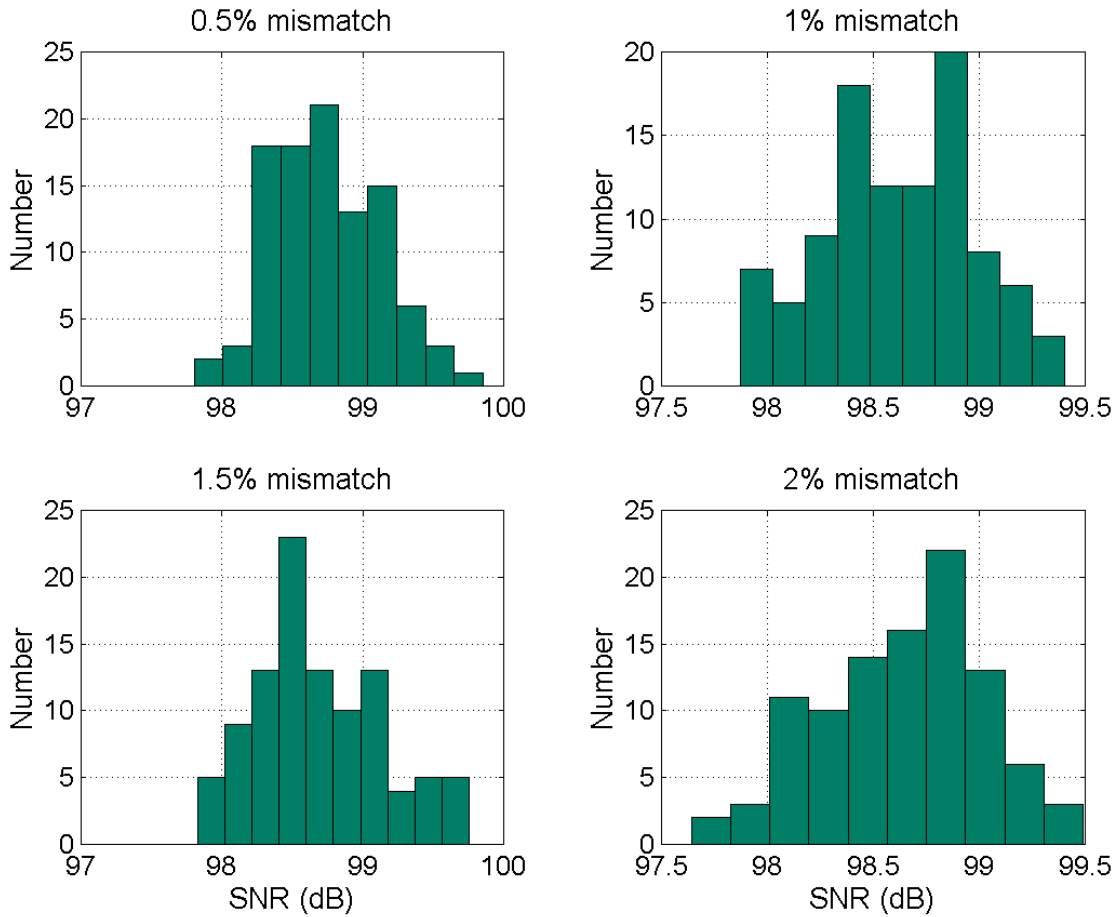


Coefficient Mismatch

- Coefficient mismatch with uniform random distribution (100 iterations)

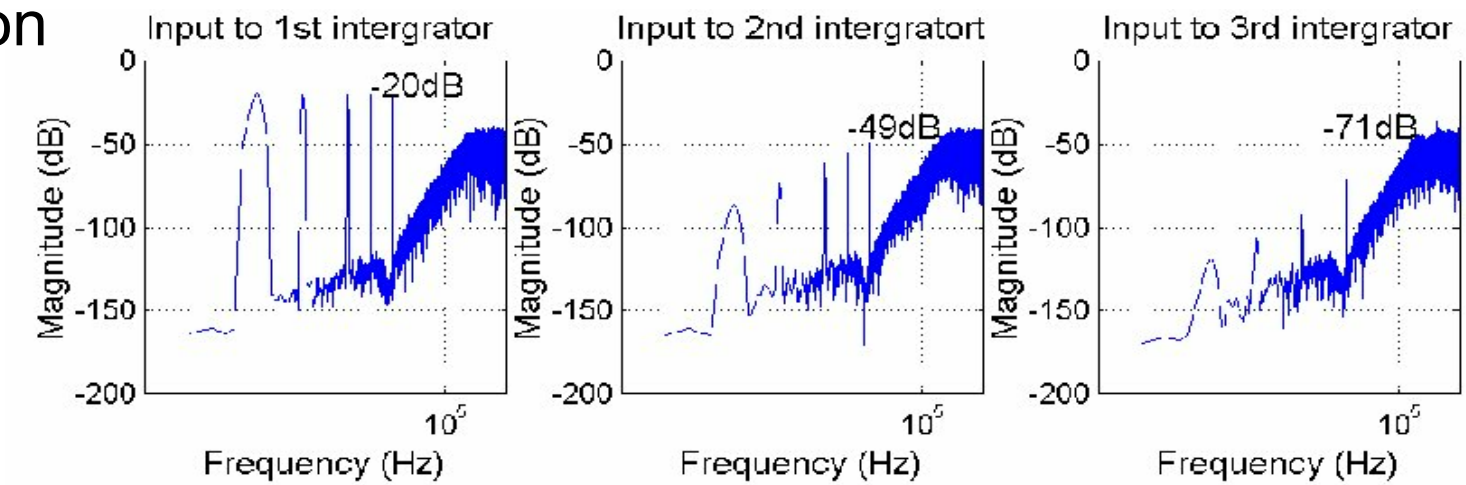
Coefficient Mismatch(conti.)

- SNR performance of the SDM with coefficient mismatch



Noise Budget

- Noise source in the baseband
  - Quantization noise (-101dB)
  - Switch noise=2kT/(OSR*Cs)
  - Amplifier noise(thermal noise+flicker noise)
  - DAC noise
- Noise budget of third integrators can be fast evaluated by SDM output spectrum while injecting the same signals to the input of each integrator
- Simulation



Noise Budget(conti.)

- Baseband quantization noise=-101dB
- For the 1st-stage integrator
  - Switch noise $\leq$ -104dB
  - Amplifier noise $\leq$ -104dB
  - $Cs_1 \geq 3.5pF$
- For the 2nd-stage integrator
  - Switch noise $\leq$ -85dB
  - Amplifier noise $\leq$ -85dB
  - $Cs_2 \geq 164fF$
- For the 3rd-stage integrator
  - Switch noise $\leq$ -63dB
  - Amplifier noise $\leq$ -63dB
  - $Cs_3 \geq 1.6fF$

DAC Noise

- Component mismatch with uniform distribution (50 iteration)