Laboratory #6
CMOS OPAMPs

I. Objectives

1. Learn the characteristic of an operational amplifier
2. Learn the fundamentals of transfer curve and frequency response

II. Components and Instruments

1. Components
   (1) MOSFET array IC : CD4007 ×1
   (2) OPAMP IC : LM324×1
   (3) Resistor : 1kΩ ×1, 10kΩ ×1, 100kΩ ×2, 1MΩ ×1
2. Instruments
   (1) DC power supply (Keysight E36311A)
   (2) Digital multimeter (Keysight 34450A)
   (3) Oscilloscope (Agilent MSOX 2014A)

III. Reading

1. Section 10-1 to 10-3 of “Microelectronics Circuits 6th edition, Sedra/Smith”.

IV. Preparation

In Lab. 6, the basic analysis of operational amplifiers (OPAMPs) is presented. OPAMPs are widely used in circuit design for various applications. Basic characteristics of OPAMPs can be simply be divided into gain, bandwidth, power consumption, and input/output range, etc. However, most of the performance indexes cannot be optimized simultaneously, and the circuit design will most probably be modified depending on the desired requirements. Hence, to have an IC outperformed in all aspects. OPAMPs characteristics analysis can be divided into DC and AC analysis. DC analysis is the transfer curve. And, AC analysis is the frequency response. The concept of transfer curve and frequency response will be explained as below.

1. Transfer curve
   (1) Introduction

   Transfer curve of an OPAMP is the most fundamental information; which not only helps users to know the input/output range directly and the corresponding

signal gain indirectly, but also helps designers to know whether the OPAMP is suitable for the adaptation in their IC/system. The Lab. starts from the introduction of the operation range of a simple OPAMP. The introduced OPAMP composes of one PMOS and one NMOS, and it performs an inverting behavior when it is operated as a dynamic CMOS circuit. And the basics of the transfer curve will be presented in (2). Finally, the characteristics of the transfer curve will be presented in (3).

(2) The transfer curve of the basic CMOS OPAMP

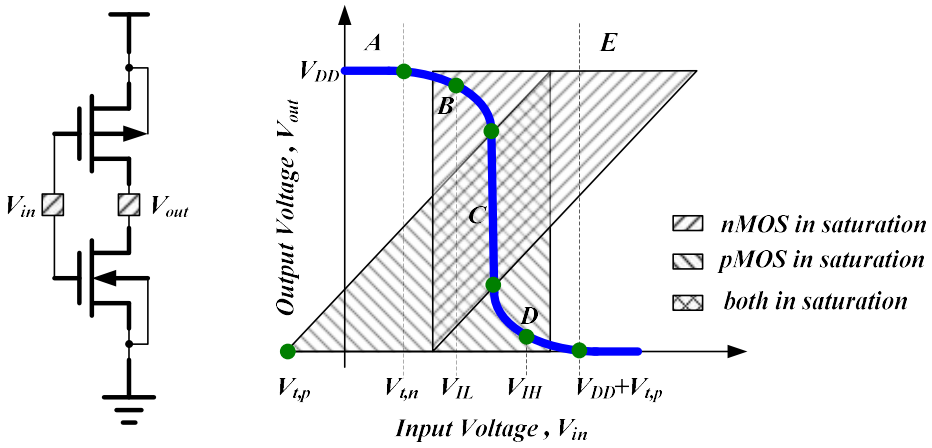

Fig. 6.1 The transfer curve of the basic CMOS OPAMP

In Fig. 6.1, the transfer curve simply describes the relationship between V_{in} and V_{out}. With the increasing of V_{in}, V_{out} will slightly decrease and suddenly down to zero once the transfer curve crosses the threshold of the inverter. Region A and E performs fully on/off state of basic CMOS OPAMP. Region B indicates the boundary between cut-off region and saturation region of the NMOS, while D represents the boundary of PMOS. In general, an analog CMOS OPAMP is biased at a predetermined DC input voltage, and operated with an AC signal loaded. Region C is the overlap area of saturation region of NMOS and PMOS, this region will be designed at the middle of range VDD-GND for extending the noise margin and operation region; this consideration will later be explored in this Lab.

Table. 6.1 The operation range of the CMOS OPAMP

Region	V_{in}	V_{out}	state of nMOS	state of pMOS
A	$<V_{t,n}$	V_{OH}	cut-off	linear
B	V_{IL}	$\sim V_{OH}$	saturation	linear
C	V_{th}	V_{th}	saturation	saturation

D	V_{IH}	~V_{OL}	linear	saturation
E	>V_{DD}+$V_{t,p}$	V_{OL}	linear	cut-off

Table 6.1 shows the detail relationship between input and output voltage, and the states of NMOS and PMOS are presented as well. Region C is determined by the occurrence when both PMOS and NMOS are in saturation, the threshold voltage can be calculated by shorting V_{in} to V_{out} (i.e. V_{in} =V_{out}). To maximize the noise margin, the region is designed to be near the middle point of range VDD-GND. Nevertheless, the desired transfer curve is not just determined by the noise margin. Other than that, rise and fall time, fan-in and fan-out, and circuit delay are all needed to be taken into considerations. Width and height of this region can be referred to the input and output voltage range, while the slope of the curve in this region indicates the maximal gain of the OPAMP. As it can be seen, there is a tradeoff between maximal gain and operation range.

(3) Characteristics of the transfer curve

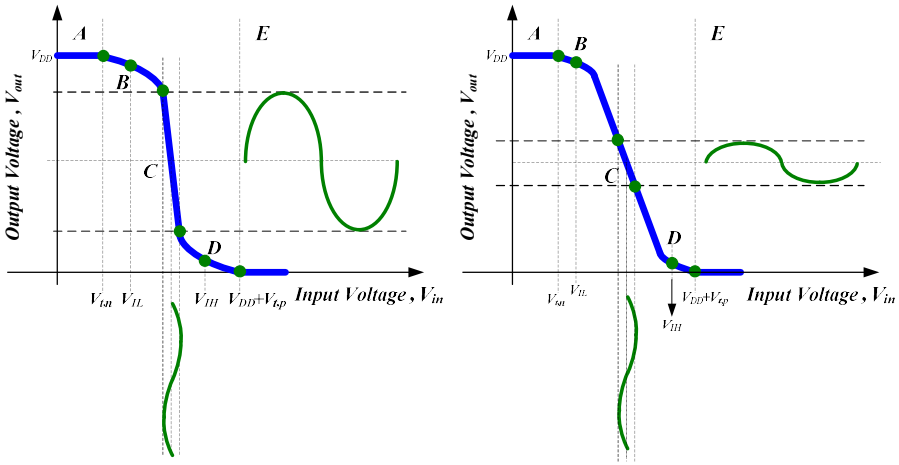

Fig. 6.2 The transfer curves with different input/output operation range

Fig. 6.2 shows the two transfer curves with different slopes at the transition region. As it can be seen, sharper slope makes larger gain, but it is noise-sensitive. Once the bias voltage of OPAMP is disturbed by either internal circuitry noise or external non-idealities, the output signal will most probably be distorted. Though, the input signal of the OPAMP can be designed smaller for preventing the distortion, still, the input signal will easily be coupled by noise.

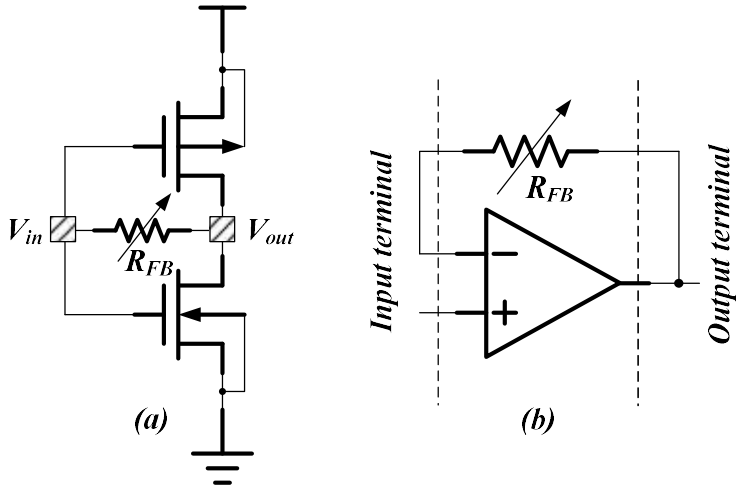

Fig. 6.3 (a) CMOS OPAMP with feedback (b) equivalent circuit

The transfer curve can be adjusted by simply changing the aspect ratio of MOSFETs in high-side or low-side network, but the driving capability and circuit delay will be changed correspondingly. The addition of the resistor on the feedback path in Fig. 6.3(a) can decrease the gain without changing the size of MOSFETs, and the behavior is similar to Fig. 6.3(b). Output signal will not be determined by the active device only, but also the input signal through the feedback resistor, and thus the threshold of the CMOS OPAMP will be moved, and so as the slope of the transfer curve.

DC analysis of the CMOS OPAMP helps the designers to know the operation range of the OPAMP, the distortion can be prevented, and so as the other non-idealities. The following labs will take a simple P-N CMOS OPAMP as an example, and the characteristics of the OPAMP will be explored. More detailed design considerations will be discussed in the explorations.

2. Frequency response

(1) Introduction

The AC analysis of CMOS OPAMP will be introduced. A CMOS OPAMP is biased at appropriate DC level as described in Lab.6, and the AC signal can be carried by the DC bias level, and then processed by the CMOS OPAMP. Method how to maintain the signal integrity by DC analysis is illustrated in Lab.6. As the input frequency changes, the corresponding output signal might not be maintained at the same amplitude due to the intrinsic frequency response of CMOS OPAMPs.

Frequency response is the profile of a system's output spectrum corresponding to its input signal. Transistors, such as BJT and CMOS, are all come with parasitic capacitances and resistances, leading delay to the integrated circuits. More importantly, impedance on the nodes between transistors is frequency-dependent. Every node in the circuit will bring various non-idealities, especially high impedance nodes. High impedance nodes such as the common-drain terminals of an OPAMP suffer greater possibilities of non-idealities than other nodes, which then lead performance degradations (e.g. gain, bandwidth, and power consumptions). The gain starts to decrease once the operating frequency crosses the dominant pole which basically results from the high impedance node and the corresponding parasitic capacitances. Therefore, the analysis of the parasitic capacitances and equivalent impedances in the OPAMP helps designers to master the frequency response of a system.

(2) Measurement of an open-loop frequency response

First of all, we start from the analysis of the small-signal model of a single-stage common-source (CS) CMOS amplifier;

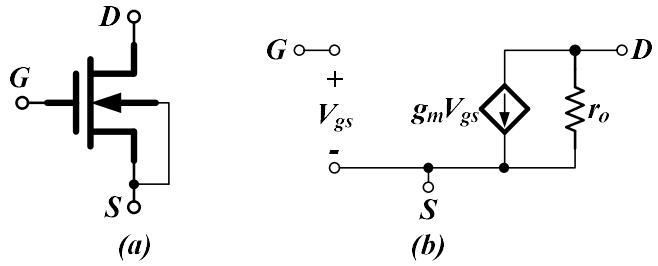

Fig 6.4 (a) Single-stage CMOS amplifier (b) Low-frequency hybrid-π model

Fig.6.4 shows the basic model for a MOSFET, which is simply a voltage-controlled current source modeling the electrical behavior of a MOSFET. The output voltage is generated from the input terminal through the transconductance, g_m, and the output impedance, r_o, of the MOSFET. However, the

open-loop gain will be changed with the input frequency as mentioned before. The model's gain shown in Fig. 6.4 is frequency-independent, which could be further modified into Fig. 6.5 (b).

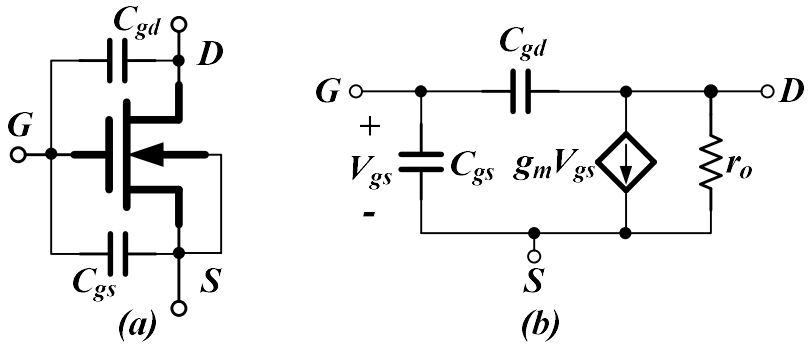

Fig. 6.5 (a) Single-stage CMOS amplifier (b) High-frequency hybrid-π model

Fig. 6.5 shows the modified model, hybrid-π with the parasitic capacitances added, which gradually dominates the magnitude gain as the frequency increases. In this Lab., the analysis to the small-signal model is based on the analysis of the parasitic capacitances, especially on the high impedance node. The common-drain terminal has the largest output impedance, thus we will analyze the circuit from this node. For the convenience of analysis, Fig. 6.5 (b) can be simplified by Miller theorem, as shown in Fig. 6.6.

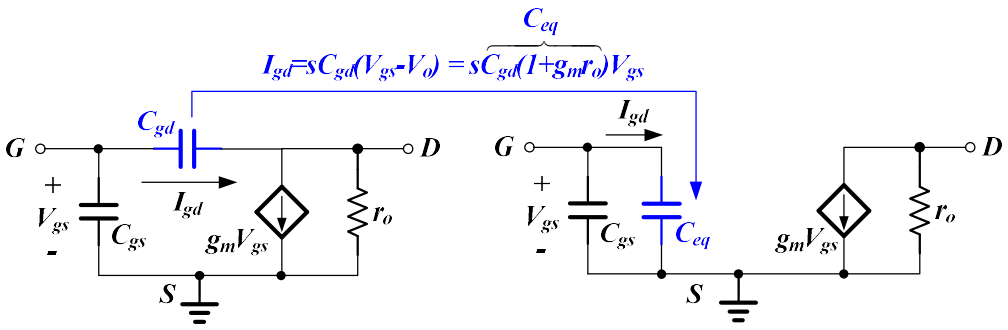

Fig. 6.6
Equivalent small-signal model of the common-source amplifier

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Fig. 6.6 shows the replacement of the gate-to-source parasitic capacitance of the MOSFET, and the open-loop transfer function can be further determined as follow.

$$\frac{V_{ds}}{V_{gs}} = k(g_m r_o)\frac{1}{1+\frac{s}{\omega_p}} \quad ,\textbf{where } \omega_p = \frac{1}{R_{in,eq}C_{eq}}$$

Criteria of an ideal CMOS OPAMP include infinite DC gain, bandwidth, input impedance, and zero output impedance. To have an insight into open-loop transfer function of the CMOS OPAMP, we are going to use closed-loop transfer function to

derive the open-loop transfer function indirectly; otherwise the high gain will simply lead output voltage to be saturated. In Lab.5, the usual feedback networks are introduced.

Fig. 6.7 (a) and (b) shows the basic inverting and non-inverting configuration, respectively.

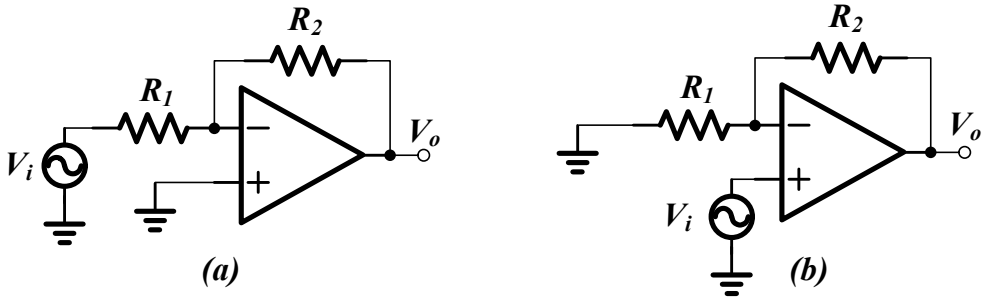


Fig. 6.7 (a) Inverting configuration (b) Non-inverting configuration

Ideally, the gain of the OPAMP will be infinite, thus the transfer function of the inverting configuration can be derived as follow.

$$\frac{V_o}{V_i} = \frac{-R_2}{R_1} \quad \text{.....(Eq. 6.1)}$$

If we model the finite gain (gain=A) effect to the feedback network and the transfer function becomes:

$$\frac{V_o}{V_i} = \frac{-R_2/R_1}{1+(1+R_2/R_1)/A} \approx \frac{A}{1+A\beta} \quad , where\ \beta = \frac{R_1}{R_2} \text{ .....(Eq. 6.2)}$$

And, we can further introduce the 3-dB pole in the equation, and the transfer function then becomes;

$$\frac{V_o}{V_i} = \frac{A(s)}{1+A(s)\beta} = \frac{A/(1+A\beta)}{1+s/\omega_{3dB}(1+A\beta)} \quad , where\ A(s) = \frac{A}{1+s/\omega_{3dB}} \text{ ....(Eq. 6.3)}$$

As shown in the equation above, the gain decreases due to the feedback network, this makes the measurement feasible. The open-loop transfer function can then be determined by the location of the 3-dB bandwidth, the feedback factor (β), and the unity-gain frequency.

However, an inherent problem existed in OPAMP design must be taken into considerations as experiment is conducted. The offset voltage will be amplified through the OPAMP and become part of the output signal, thus the accuracy of the estimation of the open-loop gain will be degraded. The simplest offset cancellation technique will be applied in this Lab. for better measurement result.

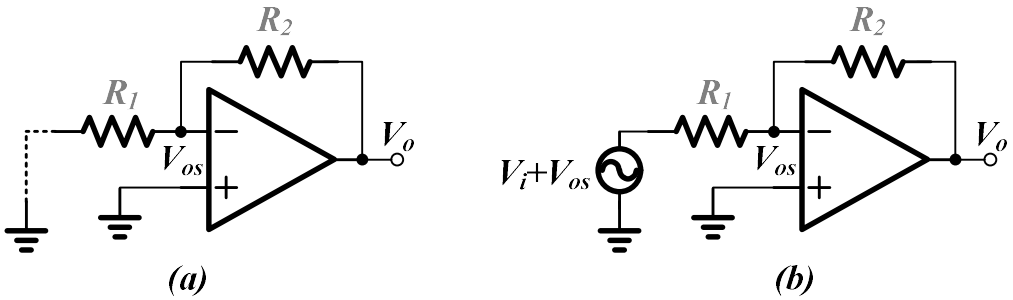


Fig. 6.8 (a) Measurement of the offset voltage (b) Cancelation of the offset voltage

The offset voltage can be measured by nulling the input voltage, and the output voltage signal will be about R_2/R_1 times of offset voltage as shown in Fig. 6.8 (a). Therefore, by simply adding the opposite offset voltage upon input signal, the offset voltage can be cancelled, and thus the output signal will be independent of the offset voltage and the accuracy of the measurement can be improved.

V. Exploration

1. Explore the transfer curve of CMOS OPAMP w/ and w/o feedback resistor

(1) Complete the wiring and setting as the figure below.

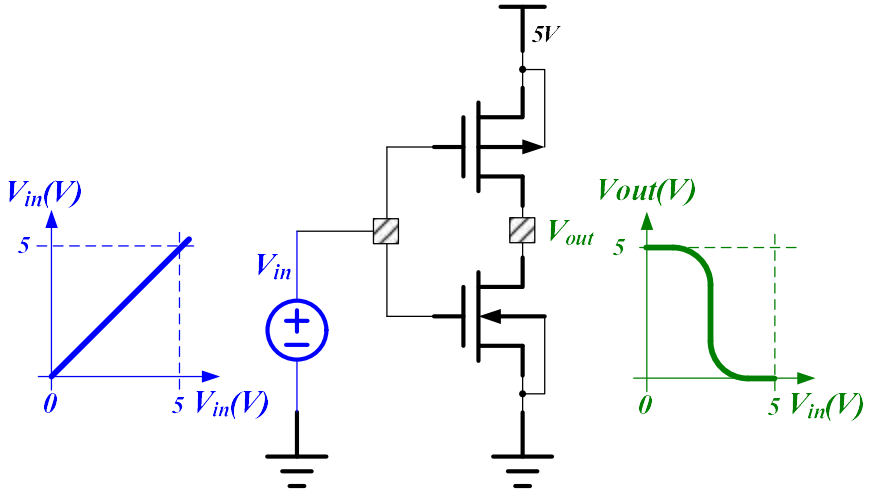


Fig. 6.9 (a) Schematic of the CMOS OPAMP without feedback resistor

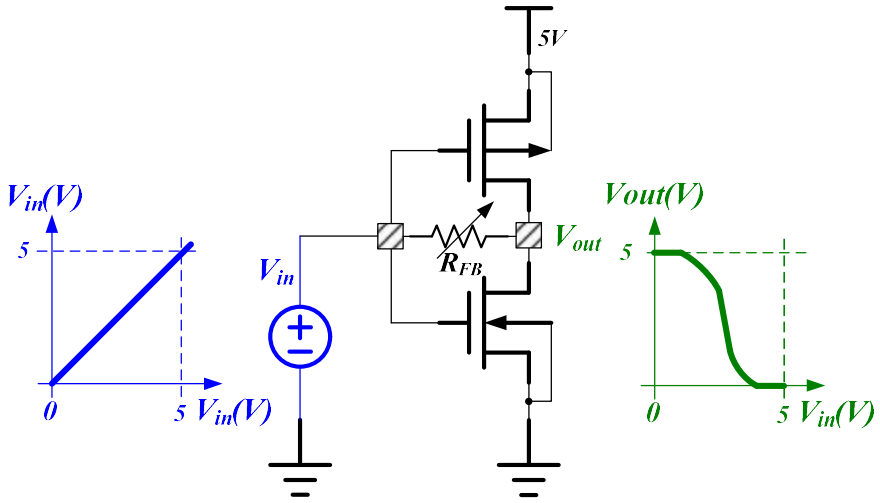


Fig. 6.9 (b) Schematic of the CMOS OPAMP with feedback resistor

(2) Set the source of the PMOS to DC 5V without R_{FB}, and make sure the drain terminal of the two MOSFETs are connected together. Vary input DC voltage from DC 0V to 5V, and record the output voltage value every 0.5V. Then change the resistor to
1kΩ, 100kΩ, and 1MΩ, respectively, and fill in the corresponding value in Table 6.2 as shown below in the report.

Table 6.2

V_{in}	V_{out} (Without R_{FB})	V_{out} (R_{FB}=1kΩ)	V_{out} (R_{FB}=100kΩ)	V_{out} (R_{FB}=1MΩ)
0.0				
0.5				
1.0				
1.5				
2.0				
2.5				
3.0				
3.5				
4.0				
4.5				
5.0				

(3) Plot the figure of input-output transfer curve and write down the approximate threshold voltage of the **4** transfer curve

2. Explore the circuit of CMOS OPAMP with input sine wave

Set the input voltage source as a sine wave with amplitude 0.1V and frequency 10Hz as Fig. 6.10. Show the figure of input voltage(V_{in}) and output voltage(V_{out}). What is the gain(amplitude of V_{out}/amplitude of V_{in}) of the OPAMP? Does the gain match to the transfer curve?

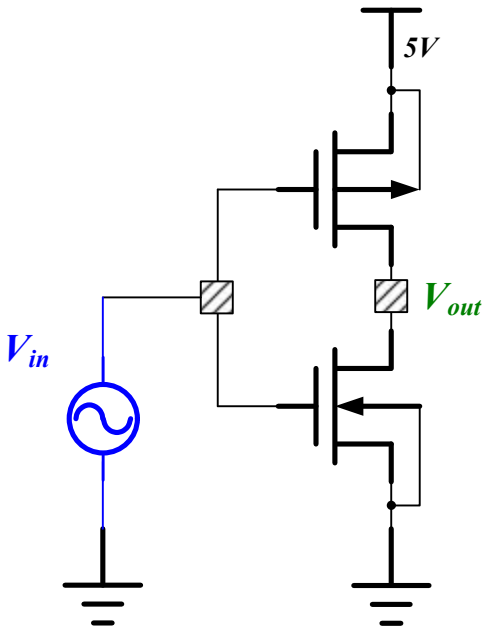


Fig. 6.10 Schematic of the CMOS OPAMP with input sine wave

3. Explore the offset voltage of an OPAMP
   (1) Complete the wiring and setting as Fig. 6.11, R_1=1kΩ, R_2=10kΩ, the output voltage is _____V.
   (2) Replace R_2 with 100kΩ, the output voltage is _____V.
   (3) The approximate offset voltage is_____V.

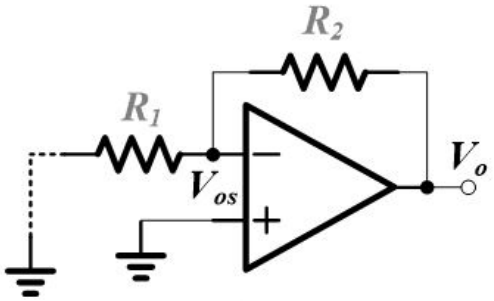


Fig. 6.11 Measurement of the offset voltage

4. Explore the frequency response of the inverting OPAMP with offset cancelation as shown in Fig 6.12, R_1=1kΩ, R_2=100kΩ, and fill in the corresponding value in Table 6.3 as shown below in the report.

Table 6.3

Freq. (Hz)	$V_{i,p\text{-}p}$ (mV)	$V_{o,p\text{-}p}$ (mV)	$V_{o,p\text{-}p}$ / $V_{i,p\text{-}p}$ (dB)
20	20		
100	20		
300	20		
500	20		
700	20		
900	20		
1k	20		
1.2k	20		
1.5k	20		
1.7k	20		
2k	20		
5k	20		
10k	20		
100k	20		
500k	20		
1Meg	20		

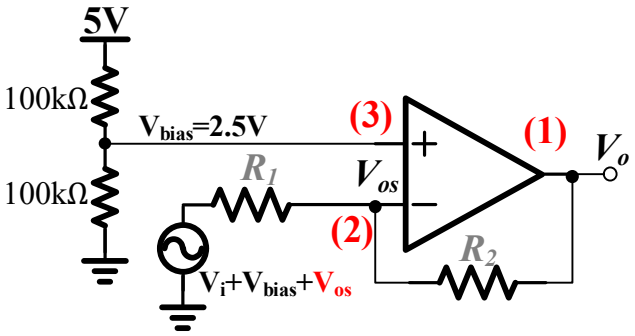


Fig. 6.12 Measurement of the offset voltage

5. Plot the closed-loop frequency response measured in 4. Estimate the open-loop transfer function of the OPAMP, and plot the open-loop frequency response of the OPAMP.

Laboratory #6 Pre-lab

Class:

Name: Student ID:

1. Explore the transfer curve of CMOS OPAMP

(1) Use PSpice to do the DC analysis on the circuit in Fig. 6.13, set the aspect ratio (W/L) of PMOS to 3/0.5 (μm) and 1/0.5 (μm) for NMOS. Both of the NMOS and PMOS can be found in SEDRA_LIB of Pspice (NMOSOP5_BODY and PMOSOP5_BODY). Plot the figure of the input-output transfer curve, and write down the threshold voltage by using the definition in page 3.

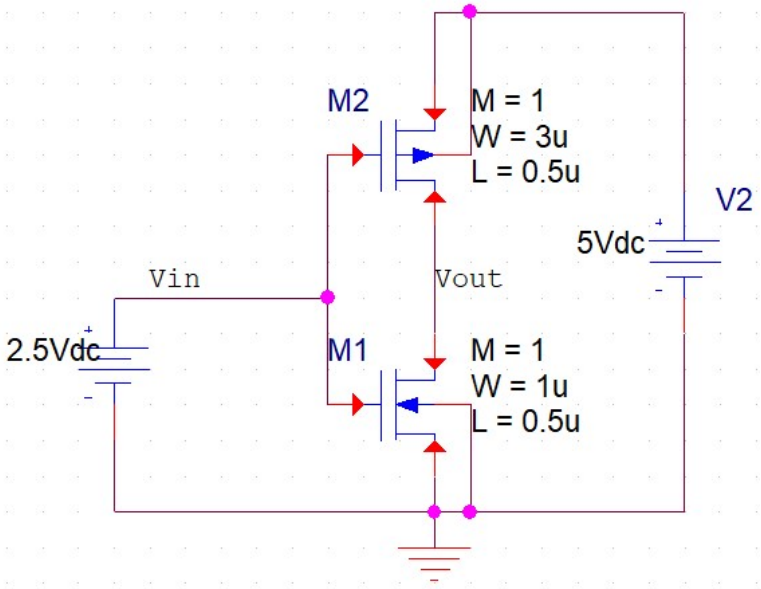


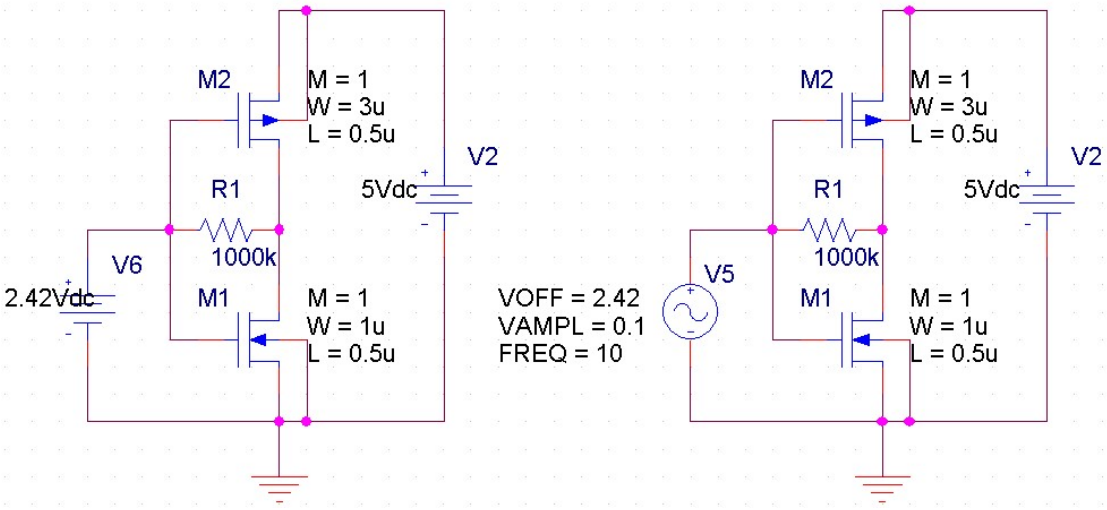
Fig. 6.13 Schematic of the CMOS OPAMP in PSpice

(2) Change W_{M2}/W_{M1} into 3/3(μm) and W_{M2}/W_{M1}=6/1(μm) with the same channel length (0.5 μm), and show the transfer curve respectively. Compare the transfer curves under two different conditions and explain the reasons for the movement of the threshold voltage.

2. Explore the transfer curve of CMOS OPAMP with feedback resistor

(1) Use PSpice to do the DC analysis on the circuits in Fig. 6.14 (a), set the aspect ratio (W/L) of PMOS to 3/0.5 (μm) and 1/0.5 (μm) for NMOS. Then connect a

resistor with 1MegΩ as shown in Fig. 6.14(a). Plot the input-output transfer curve of this circuit and write down the threshold voltage.



(a) (b)

Fig. 6.14 (a) DC analysis of the OPAMP with feedback resistor, (b) time domain analysis of the OPAMP

(2) Change the resistor to 1K in Fig. 6.14 (a) and compare the threshold voltage in (1). Please explain the simulation result

(3) Please use the circuit in Fig. 6.14 (a) and write down the threshold voltage. Change the input voltage source into VSIN and set the amplitude to 0.1V and frequency to 10Hz as Fig. 6.14 (b). Does the gain (amplitude of V_{out}/amplitude of V_{in}) match to the transfer curve? If the output signal amplitude does not match to the transfer curve, why? (Hint: please change the frequency of input signal, and briefly explain the reason for the differences of the output signal)

3. Explore the open-loop frequency response of Fig. 6.15

(1)

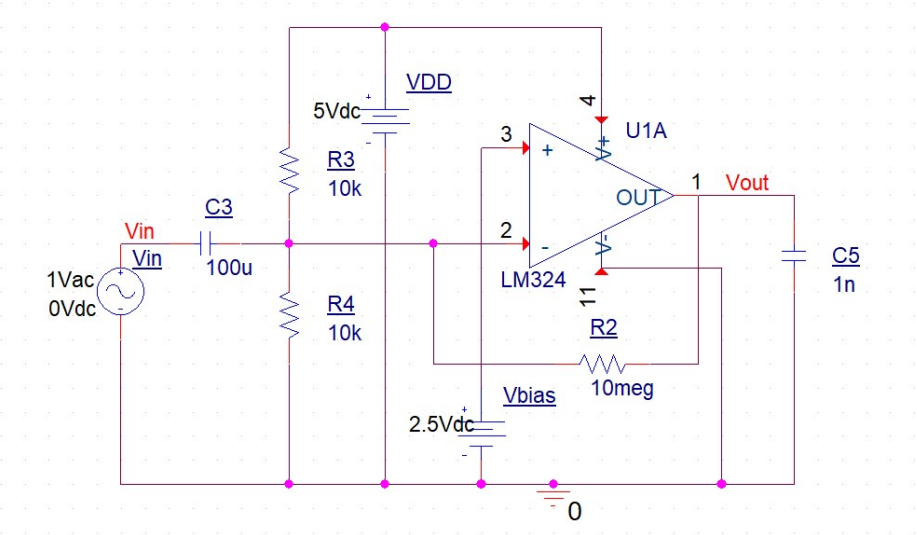


Fig. 6.15 Open-loop gain measurement of LM324

In exploration 3, please use LM324 (in Library "EVAL") as the OPAMP, R_2 = 10Meg, R_3 = R_4 = 10k and C_3 = 100 μF, C_5 = 1nF is equivalent to the load capacitance. Use the AC source (VAC=1V) for sweeping the input signal and plot the frequency response.

(2) Record down the open-loop gain and the 3dB pole frequency. The open-loop gain (A_{open}) =_____(dB), $\omega_{3dB,o}$=_____(Hz)

4. Explore the closed-loop frequency response of Fig. 6.16

(1)

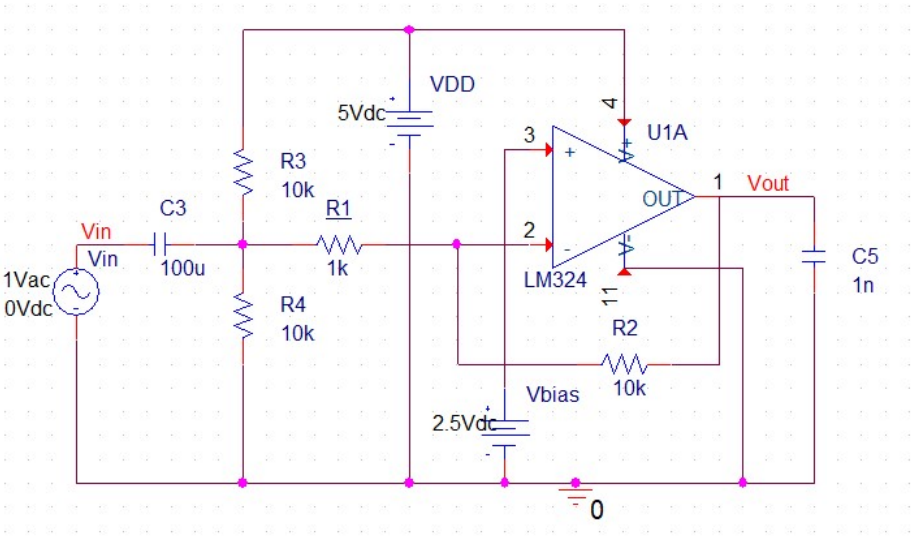


Fig. 6.16 Inverting configuration of LM324

In exploration 4, please use inverting configuration, set R_2 = 10k and R_1 = 1k. Use the AC source (VAC=1V) for sweeping the input signal and plot the frequency response.

(2) Record down the closed-loop gain and the 3dB pole frequency. The closed-loop gain (A_{close}) =_____(dB), $\omega_{3dB,c}$=_____(Hz)

5. Estimate the open-loop gain ($A_{open,est}$) with the result in exploration 4. The relationship between the closed-loop gain (A_{close}) and the open-loop gain ($A_{open,est}$) will be as follow.

$$20\log(A_{open,est}) = 20\log(A_{close}) + 20\log(\frac{\omega_{3dB,c}}{\omega_{3dB,o}})$$

Please calculate the open-loop gain, $A_{open,est}$ =_____(dB)

Is A_{open} in exploration 3 close to $A_{open,est}$ in exploration 5? Why?

Laboratory #6 Report

Class:

Name: Student ID:

1. Exploration 1

(1) Experimental result

Table 6.2

V_{in}	V_{out} (Without R_{FB})	V_{out} (R_{FB}=1K(Ω))	V_{out} (R_{FB}=100K(Ω))	V_{out} (R_{FB}=1Meg(Ω))
0.0				
0.5				
1.0				
1.5				
2.0				
2.5				
3.0				
3.5				
4.0				
4.5				
5.0				

(2) Plot the figure of input-output transfer curve

(3) The threshold voltage, V_{th} is about _____V with without R_{FB} ;
V_{th} is about _____V with R_{FB} = 1K(Ω); V_{th} is about _____V with R_{FB} = 100K(Ω);
and V_{th} is about _____V R_{FB} = 1Meg(Ω)

2. Exploration 2

(1) Show the figure of input voltage(V_{in}) and output voltage(V_{out}).

(2) The gain of the OPAMP is about ____V

3. Exploration 3

(1) The approximate offset voltage is _____V.

4. Exploration 4

(1) Frequency response of the inverting configuration

Table 6.3

Freq. (Hz)	$V_{i,p-p}$ (mV)	$V_{o,p-p}$ (mV)	$V_{o,p-p}$ / $V_{i,p-p}$ (dB)
20	200		
100	200		
300	200		
500	200		
700	200		
900	200		
1k	200		
1.2k	200		
1.5k	200		
1.7k	200		
2k	200		
5k	200		
10k	200		
100k	200		
500k	200		
1Meg	200		

5. Exploration 5

(1) Plot the close-loop frequency response.

(2) Plot the open-loop frequency response

6. Problem 1

Threshold voltage of the transfer curve will be increased or decreased with the increasing of W_p/W_n ratio? Why?

7. Problem 2

How does the current through NMOS change with the increasing of input voltage V_{in}? Try to explain the change of $i_{d,NMOS}$-to-V_{in} curve. Use PSpice simulation to verify your explanation.(hint: Table 6.1)

8. Problem 3

This Lab. derives the open-loop transfer function indirectly by decreasing the open-loop gain with the applying of feedback network. Please derive the relation between R_2/R_1 and the dc gain, and the location of 3-dB pole in inverting configuration, respectively.

9. Problem 4

Please briefly design a new measurement flow for deriving the open-loop transfer function with the non-inverting configuration.

10. Bonus 1

P-N type (similar to inverter) power stage is commonly used in the power stage, and the current through power PMOS/NMOS are usually very large. To prevent the current shooting through PMOS and NMOS, which causes large power loss, rise or fall time should be taken into considerations in the design of power stage. Try to analyze the relation between power loss at the transition region during either rise time or fall time.

11. Bonus 2

Comparison of the measurement result of open-loop transfer function by applying inverting and non-inverting configuration. Which of the configuration will be better for the measurement? (Hint: the offset cancelation method and its performance)

12. Conclusion