Laboratory #8
Basics of Analog-to-Digital Converters

I. Objectives

Acquaint you with some fundamentals of data converters, analog-to-digital converters (ADCs) will be introduced in this lab.

II. Components and Instruments

1. Components
   (1) ADC IC: ADC0804 ×1
   (2) Resistors: 10 kΩ ×1
   (3) Variable Resistor (R_V): 10 kΩ ×1, 20 kΩ ×1, 100 kΩ ×1
   (4) Capacitors: 150 pF ×1, 0.1μF ×2, 10μF ×1
   (5) Switch: DIP switch ×1
2. Instruments
   (1) DC power supply (Keysight E36311A)
   (2) Digital multimeter (Keysight 34450A)
   (3) Oscilloscope (Agilent MSOX 2014A)

III. Reading

Section 1.3 of the Textbook “Microelectronic circuits, 6^h edition, Sedra/Smith.”

IV. Preparation

1. Digital Processing of Signals

Digital signal processing (DSP) is concerned with the representation of signals by a sequence of numbers or symbols and the processing of these signals. Digital and analog signal processing are subfields of signal processing. DSP includes subfields like: audio and speech signal processing, digital image processing, signal processing for communications, control of systems, biomedical signal processing, etc.

The goal of DSP is usually to measure, filter and/or compress continuous real-world analog signals. The first step is usually to convert the signal from an analog form to a digital form, by sampling it using an analog-to-digital converter (ADC), which turns the analog signal into a stream of numbers. However, the required output signal is another analog output signal, which requires a digital-to-analog converter (DAC). Even though this process is more complex than analog processing and has a discrete value range, the powerful computation of

digital signal processing allows many advantages over analog signal processing in many applications, such as error detection and correction in data transmission as well as data compression.

2. Analog-to-Digital Converter

(1) Ideal Analog-to-Digital Converter

The block diagram of an N-bit ADC is shown in Fig. 8.1. , D is defined to be an N-bit digital output word where v_A and V_{REF} are the analog input and the reference signals, respectively. The relationship between these signals is given by

$$v_A + v_Q = V_{REF} \cdot \left(\frac{b_1}{2^1} + \frac{b_2}{2^2} + ... + \frac{b_N}{2^N} \right) \text{.....(Eq. 8.1)}$$

where $-0.5 \cdot V_{LSB} \le v_Q \le 0.5 \cdot V_{LSB}$

We define b_1 as the most significant bit (MSB) and b_N as the least significant bit (LSB) . V_{LSB} is defined as the voltage change when one LSB change, or, mathematically,

$$V_{LSB} = \frac{V_{REF}}{2^N} \text{……(Eq. 8.2)}$$

Transfer curve of an A/D converter (2-bit ADC as an example) can be plotted as shown in Fig. 8.2. Concept of V_{LSB} can be observed in this figure. Note that the transitions along the V_A axis are offset by 1/2 V_{LSB}.

In equation (1), the range of v_A should remain less than V_{REF} - 0.5xV_{LSB} and greater than -0.5xV_{LSB}. Otherwise, the quantizer will be overloaded.

Note that there is a range of valid input values that maps to the same digital output word. This process is called quantization and the error induced in this process which is called the quantization error.

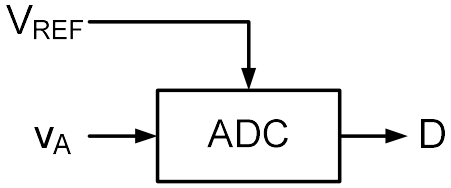

Fig. 8.1 The block diagram of an N-bit ADC

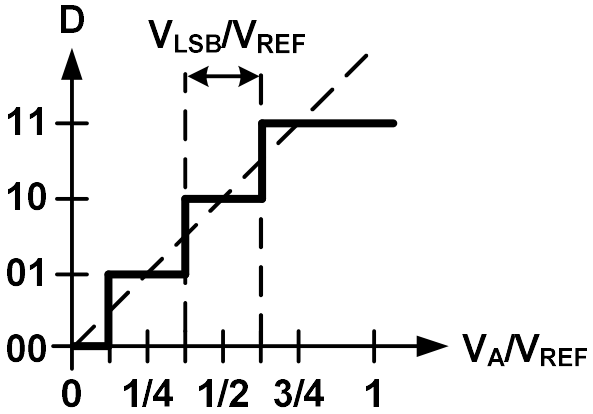

Fig. 8.2 Transfer curve of a 2-bit A/D converter

(2) An N-bit Charge-Redistribution ADC

Successive-approximation (SAR) ADC is one of the most popular approaches for realizing ADC. The basic operation of SAR ADC is based on the binary search algorithm. A flow chart for a signed conversion using successive-approximation approach is shown in Fig. 8.3.

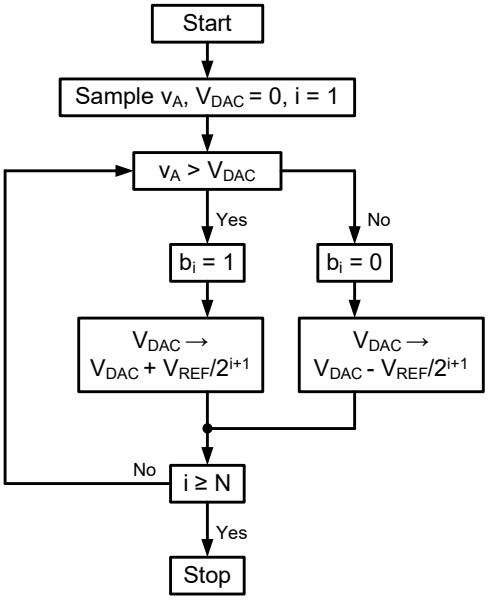

Fig. 8.3 The flow chart of successive-approximation approach

The modified flow chart is shown in Fig. 8.4. An N-bit charge-redistribution ADC is one type of SAR ADCs. A 5-bit ADC utilized the concept of charge redistribution is taken as an example, and its modes' transitions are shown Fig. 8.5.

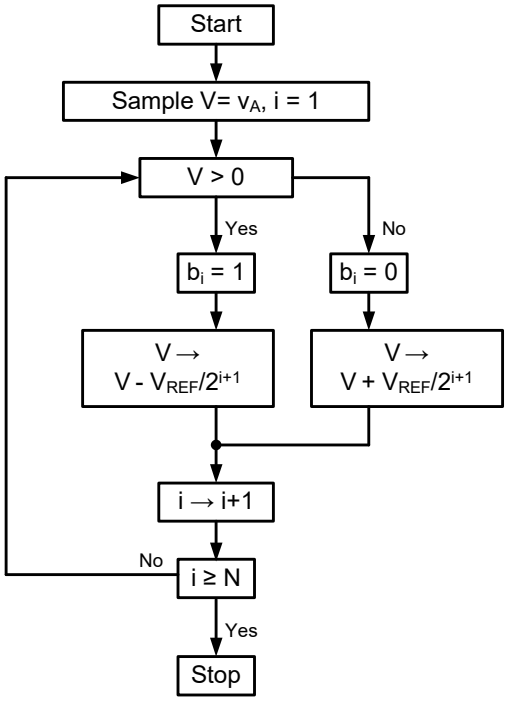

Fig. 8.4 The modified flow chart of SAR approach

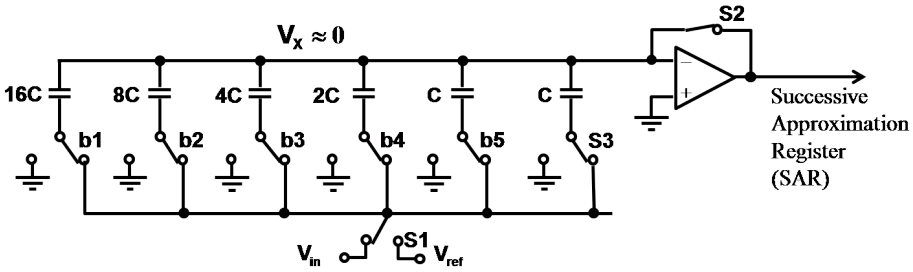

Fig. 8.5(a) Sample mode

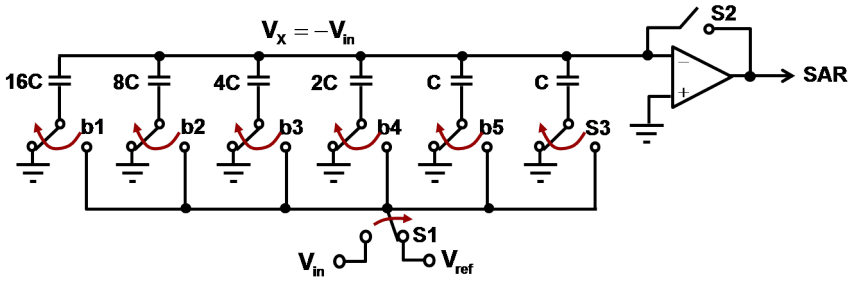

Fig. 8.5(b) Hold mode

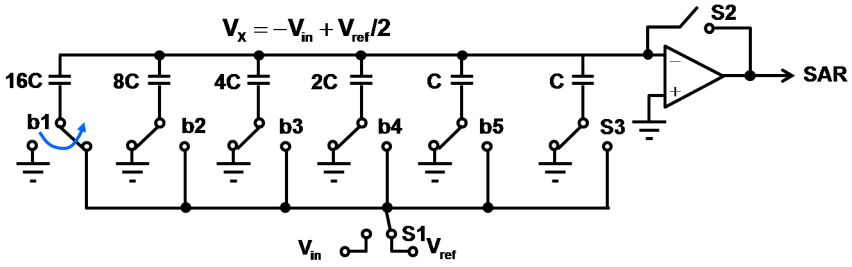

Fig. 8.5(c) Bit cycling

3. ADC Dynamic Testing Setup

The performance index of signal-to-noise ratio (SNR), Signal-to-noise-and-distortion ratio (SNDR), worst spur can be obtained using hardware setup shown in Fig. 8.6. The basic setup for dynamic testing includes a signal generator, low-pass or band-pass filter, test fixture, low noise power supply, data acquisition module, and data analysis software.

To avoid aliasing, the input to an ADC must be low-pass filtered to remove frequencies above half of the sampling rate. This filter is called the anti-aliasing filter, and it is essential for a practical ADC system to filter the out-of-Nyquist-band high frequency content of the applied analog signals. Another purpose of low-pass filter or band-pass filter is to reduce the signal distortion from signal generator. In this lab, a low resolution(4-bit) ADC is tested, quantization error is more dominant than signal distortion, so we exclude low-pass filter or band-pass filter from this lab for simple implementation.

In post-processing, coherent Fast Fourier Transform (FFT) testing is usually used. FFT is a common tool to investigate the performance of the data converters and other sampled systems. Coherent sampling refers to a certain relationship between input frequency, f_{in}, sampling frequency, f_s, number of cycles, N_{cycles}, in the sampled set and number of samples, $M_{samples}$. With coherent sampling one is assured that the signal power in an FFT is contained within one FFT bin, as single input frequency is being assumed. The relationship is given by $\frac{f_{in}}{f_s} = \frac{N_{cycles}}{M_{samples}}$.(Eq. 8.3)

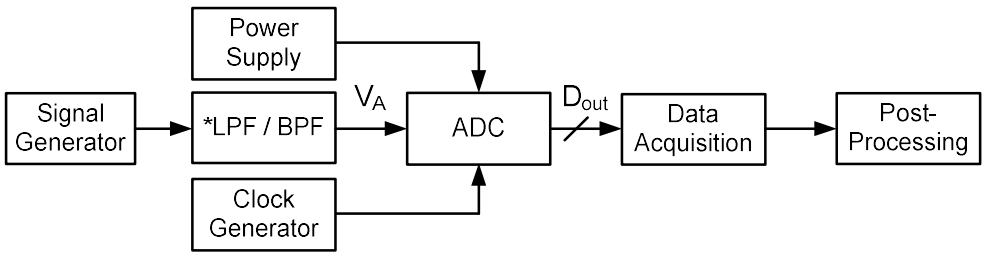

Fig. 8.6 ADC Test Setup

Note : we exclude LPF/BPF from this lab for simple implementation.

4. Reference

(1) Adel S. Sedra and Kenneth C. Smith, “Microelectronic circuits, 5th edition, “Oxford University Press, Inc., 2007.

(2) Adel S. Sedra and Kenneth C. Smith, “Microelectronic circuits, 6th edition, “Oxford University Press, Inc., 2011.

(3) David A. Johns and Ken Martin. “Analog integrated circuit design,” John Wiley

& Sons, Inc., 1997.
(4) National Semiconductor, Datasheet of ADC0804, “ADC0801/ ADC0802/ADC0803/ADC0804/ADC0805 8-Bit μP Compatible A/D Converters,” November, 1999.

5. Pin Information

ADC0804:

(https://pdf1.alldatasheet.com/datasheet-pdf/view/83230/PHILIPS/ADC0804.html)

ADC080X
Dual-In-Line and Small Outline (SO) Packages

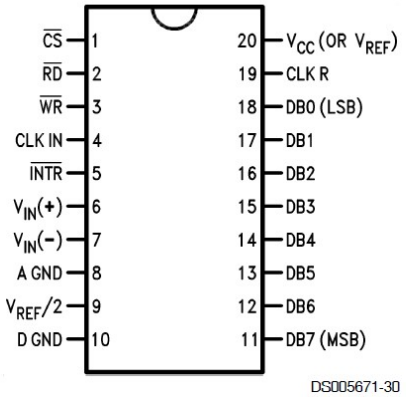

Fig. 8.7 Pin diagram of ADC0804

V. Explorations

1. ADC 0804 Basic Testing Circuit for 4-bit Operation

(1) Circuit setup

Connect the circuit as shown in Fig. 8.8.

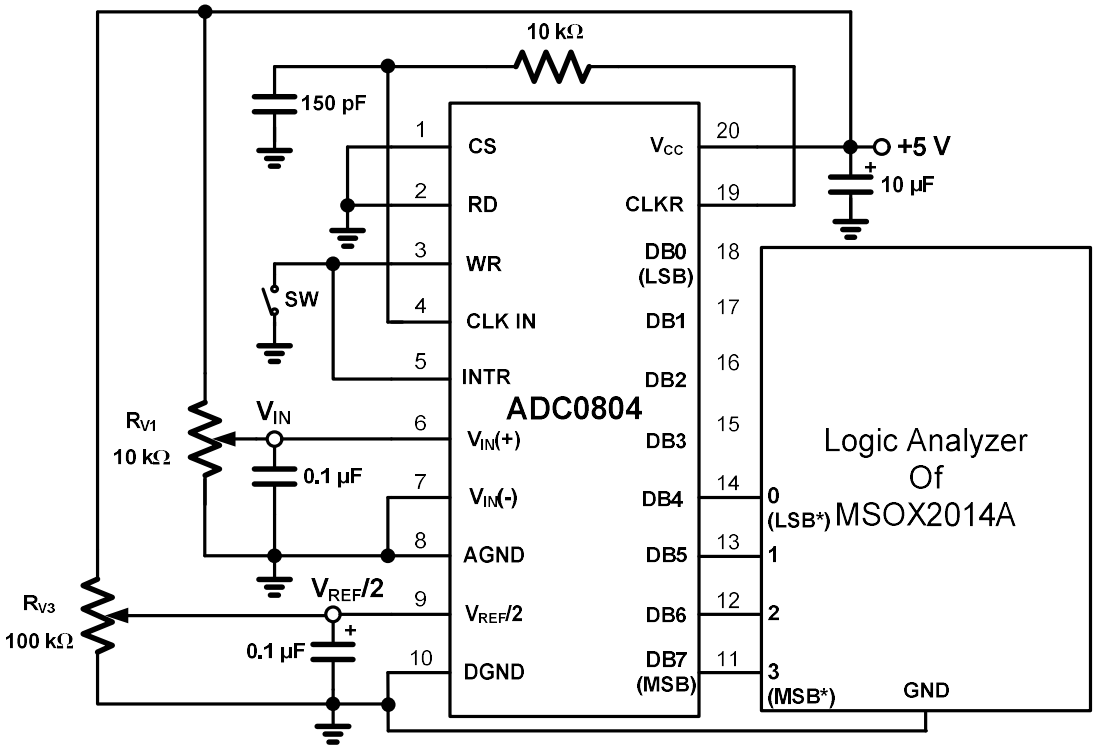

Fig. 8.8 Basic ADC tester for 4-bit operation

Note: LSB* (or MSB*) represents the least (or most) significant bit of 4-bit operation in this lab

(2) Reset the internal SAR latches and the shift register stage

A. Switch on the SW, so that the **CS** and **WR** are set in logic low value.

B. Switch off the SW, so that disconnect the **WR** and **INTR** are disconnected from **GND**.

(3) Full-scale adjustment

A. Apply DC input voltage with $\mathbf{V_{IN} = 4.531\ V}$ (5 V - 1.5 V_{LSB*}).

B. The value of the $\mathbf{V_{REF}/2}$ input voltage is adjusted until the digital output code is just changing from 1110 to 1111. ($0 \leqq \mathbf{V_{REF}/2} \leqq 2.6$ V)

C. Record the value of $\mathbf{V_{REF}/2}$, which is then be used for exploration 2 in this lab.

(4) Finish Table 8.1

Table 8.1

Analog input V_{IN} (V)	*Digital output (Binary)(0~3)*
	0000 → 0001
	0001 → 0010
	0010 → 0011
	0011 → 0100
	0100 → 0101
	1010 → 1011
	1011 → 1100
	1100 → 1101
	1101 → 1110
	1110 → 1111

2. ADC Dynamic Performance Testing for 4-bit Operation

(1) Circuit setup

Connect the circuit shown in Fig. 8.9. But only turn on the power supply. Maintain the voltage of $V_{REF}/2$ from exploration 1.

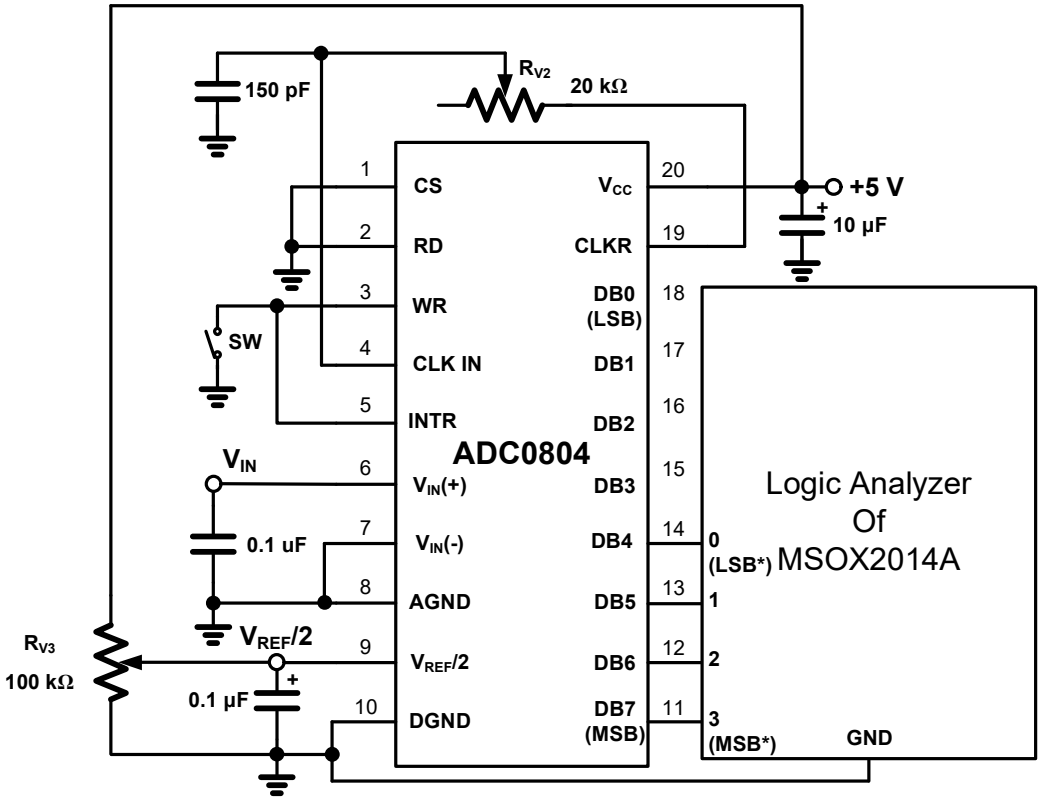

Fig. 8.9 Dynamic Performance Testing Circuit

Note: LSB* (or MSB*) represents the least (or most) significant bit of 4-bit operation in this lab

(2) Reset the ADC0804

A. Switch on the SW, so that the **CS** and **WR** are set in logic low value.
B. Switch off the SW, so that disconnect the **WR** and **INTR** are disconnected from **GND**.

(3) Adjust the conversion rate

A. Connect channel 7 of the logic analyzer with the **INTR** pin.
B. Use cursors to measure the period between **INTR** pulses.
C. Adjust the value of R_{V2} to make the frequency of **INTR** pulses equal to 5 kHz
D. Download the screens of the scope for your report.
E. Observe the voltage of ADC Pin 19 on the scope and record its internal clock frequency. How many internal clock cycles does this period represent?

(4) Set the input signal with a ramp signal

A. Set the output impedance of **function generator** to **high Z**, and check the output signal before connecting to the device under test.
B. Observe ADC output bus (0000, initial value) on analyzer channels 0 to 3 for a ramp input with the range of 0 to 5 V ramp and the frequency of 1 Hz. Observe the binary count from 0000 to 1111.
C. Download the screen of the scope for your report, and the information must include any three successive data.

(5) Replace the input signal with a sine wave signal

A. By **function generator**, apply a sine wave with peak-peak of 5 V, DC offset of 2.5 V and frequency of 100 Hz. Check the waveform with oscilloscope before connecting the **function generator**'s output to $\mathbf{V_{IN}}$.
B. Use the FFT function of the oscilloscope to observe the spectrum of $\mathbf{V_{IN}}$.
    i. The sampling rate of the scope: 50 kS/s
    ii. Span: 2 kHz
    iii. Center: 1 kHz
    iv. Window: Blackman-Harris
C. Download the screen of the scope for your report, and record the measurement condition, i.e. the span frequency and adopted window function.

(6) Acquisition of the digital output data from (5)

A. Set the sampling rate of scope to 50 kS/s.

B. Save the digital output data

i. File format: *.csv

ii. Press the Settings softkey ➔ Length: 20000

3. ADC 0804 Basic Testing Circuit for 8-bit Operation **(Optional)**

(1) Circuit setup

For 8-bit ADC application, you can reconfigure the circuit as shown in Fig. 8.10.

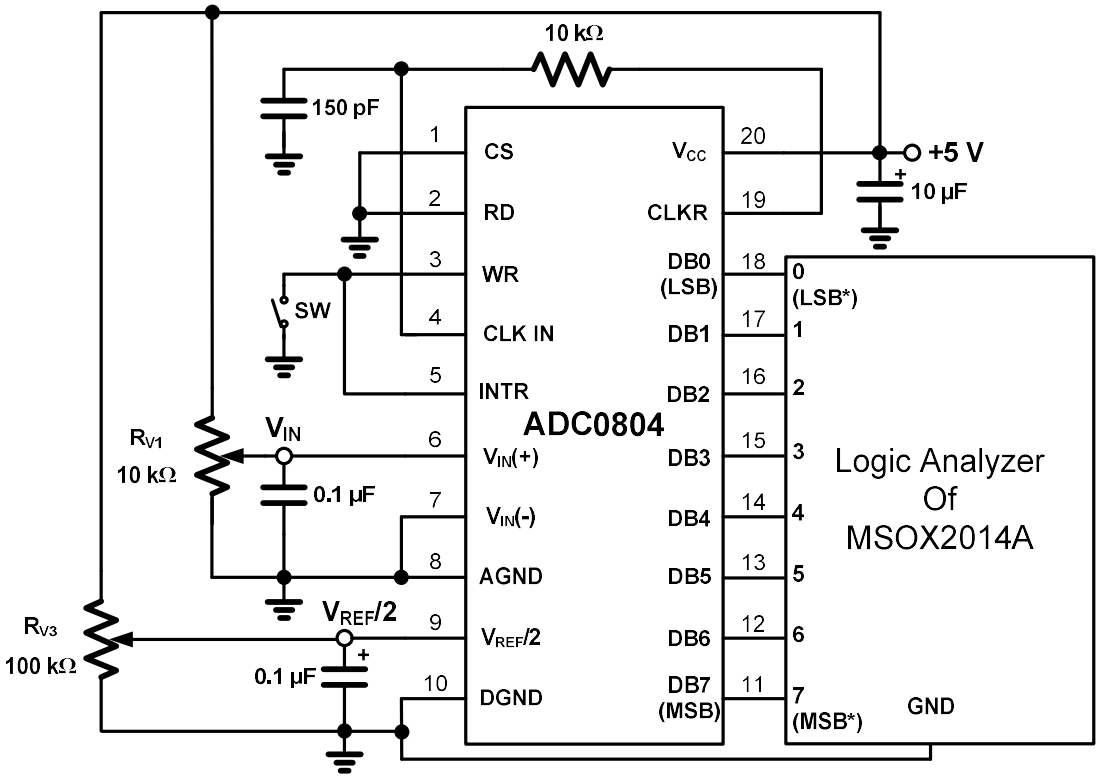

Fig. 8.10 Basic ADC tester for 8-bit operation

Note: LSB* (or MSB*) represents the least (or most) significant bit of 8-bit operation in this lab

(2) Reset the internal SAR latches and the shift register stage

A. Switch on the SW, so that the **CS** and **WR** are set in logic low value.

B. Switch off the SW, so that disconnect the **WR** and **INTR** are disconnected from **GND**.

(3) Full-scale adjustment

A. Apply DC input voltage with $\mathbf{V_{IN}}$ = 4.971 V (5 V - 1.5 V_{LSB}).

B. The value of the **$V_{REF}/2$** input voltage is adjusted until the digital output code is just changing from 1111 1110 to 1111 1111. (0 ≦ **$V_{REF}/2$** ≦ 2.6 V)

C. Record the value of **$V_{REF}/2$**, which is then be used for exploration 4 in this lab.

(4) Finish Table 8.2

Table 8.2

Analog input V_{IN} (V)	*Digital output (Binary)*
	0000 0000 → 0000 0001
	0000 0001 → 0000 0010
	0000 0010 → 0000 0011
	0000 0011 → 0000 0100
	0000 0100 → 0000 0101
	1111 1010 → 1111 1011
	1111 1011 → 1111 1100
	1111 1100 → 1111 1101
	1111 1101 → 1111 1110
	1111 1110 → 1111 1111

4. ADC Dynamic Performance Testing for 8-bit Operation**(Optional)**

(1) Circuit setup

Connect the circuit as shown in Fig. 8.11. But only turn on the power supply. Maintain the voltage of $V_{REF}/2$ from exploration 3.

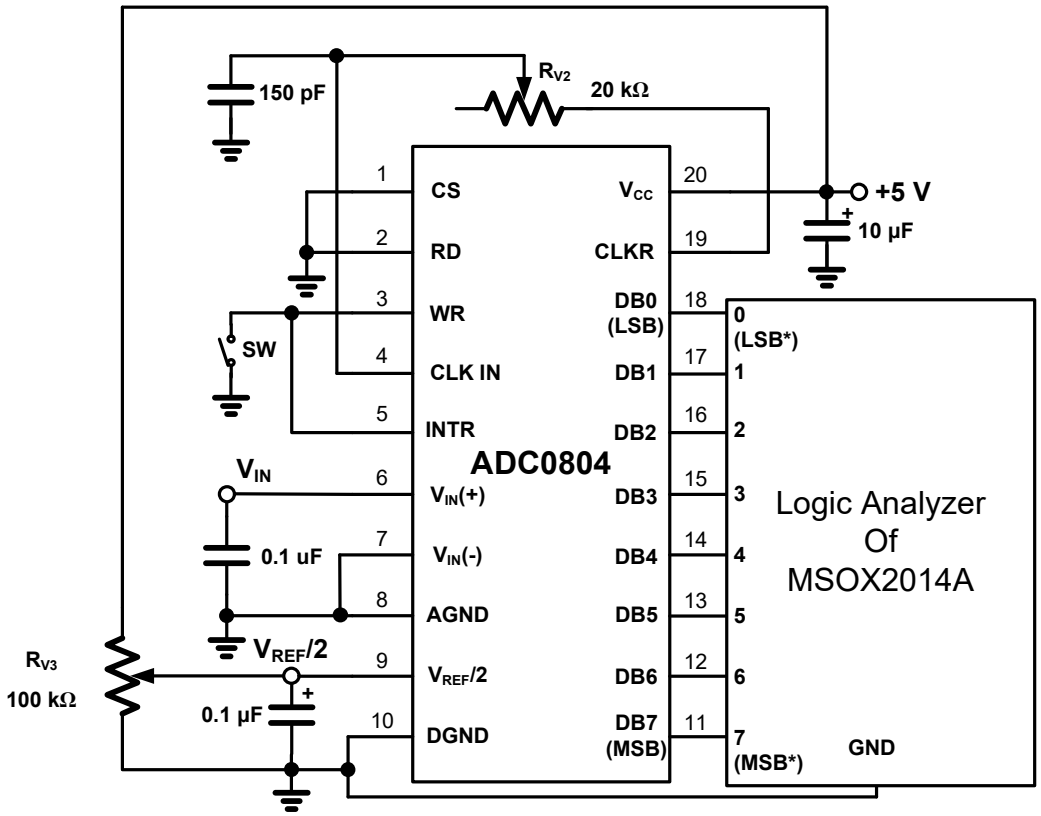

Fig. 8.11. Dynamic Performance Testing Circuit for 8-bit Operation

Note: LSB* (or MSB*) represents the least (or most) significant bit of 8-bit operation in this lab

(2) Reset the ADC0804

A. Switch on the SW, so that the **CS** and **WR** are set in logic low value.

B. Switch off the SW, so that disconnect the **WR** and **INTR** are disconnected from **GND**.

(3) Adjust the conversion rate

A. Connect channel 7 of the logic analyzer with the **INTR** pin.

B. Use cursors to measure the period between **INTR** pulses.

C. Adjust the value of R_{V2} to make the frequency of **INTR** pulses equal to 5 kHz

(4) Set the input signal with a ramp signal

A. Set the output impedance of **function generator** to **high Z**, and check the output signal before connecting to the device under test.

B. Observe ADC output bus (00000000, initial value) on analyzer channels 0 to 7 for a ramp input with the range of 0 to 5 V ramp and the frequency of 1

Hz. Observe the binary count from 00000000 to 11111111.

C. Download the screen of the scope for your report, and the information must include any three successive data.

(5) Replace the input signal with a sine wave signal

A. By **function generator**, apply a sine wave with peak-peak of 5 V, DC offset of 2.5 V and frequency of 100 Hz. Check the waveform with oscilloscope before connecting the **function generator**'s output to $\mathbf{V_{IN}}$.

B. Use the FFT function of the oscilloscope to observe the spectrum of $\mathbf{V_{IN}}$.

i. The sampling rate of the scope: 50 kS/s

ii. Span: 2 kHz

iii. Center: 1 kHz

iv. Window: Blackman-Harris

C. Download the screen of the scope for your report, and record the measurement condition, i.e. the span frequency and adopted window function.

(6) Acquisition of the digital output data from (5)

A. Set the sampling rate of scope to 50 kS/s.

B. Save the digital output data

i. File format: *.csv

ii. Press the Settings softkey ➔ Length: 20000

Laboratory #8 Pre-lab

Class:

Name: Student ID:

1. In lab 8, we will test a 4-bit ADC with V_{REF}=5V using IC ADC0804. What is the V_{LSB} in this work ? Please plot the input-output transfer curve (You can refer to Fig. 8.2). Use binary code to represent the output signal. Normalize the input voltage to reference voltage (V_{REF}).

2. Please briefly describe the pins function of ADC0804. You can find the information from datasheets and the related links could be found in page 6.

Laboratory #8 Report

Class:

Name: Student ID:

1. Exploration 1

(1) **$V_{REF}/2$** = _____ V.

Table 8.1

Analog input V_{IN} (V)	*Digital output (Binary)(4~7)*
	0000 → 0001
	0001 → 0010
	0010 → 0011
	0011 → 0100
	0100 → 0101
	1010 → 1011
	1011 → 1100
	1100 → 1101
	1101 → 1110
	1110 → 1111

2. Exploration 2

(1) The figure that includes the information of **INTR.**

(2) The internal clock frequency = _____ Hz.

(3) How many internal clock cycles does this period represent? _____

(4) The figure that includes any three successive data when V_{in} is ramp signal.

(5) The FFT plot of the sine wave signal.

3. Problem 1

Please plot the input-output transfer curve according to the Table 8.1 by MATLAB or EXCEL. Use decimal code to represent output digital code of ADC. Normalize the input voltage to reference voltage.

4. Problem 2 **(Optional)**

Please do the FFT analysis to the saved digital code of the ADC, where the Matlab code can be found from the course website. You can change the value of parameter **(shift) from 0 to 9** to get the correct data.

5. Exploration 3**(Optional)**

(1) **$V_{REF}/2$** = _____ V.

Table 8.2

Analog input V_{IN} (V)	*Digital output (Binary)*
	0000 0000 → 0000 0001
	0000 0001 → 0000 0010
	0000 0010 → 0000 0011
	0000 0011 → 0000 0100
	0000 0100 → 0000 0101
	1111 1010 → 1111 1011
	1111 1011 → 1111 1100
	1111 1100 → 1111 1101
	1111 1101 → 1111 1110
	1111 1110 → 1111 1111

6. Exploration 4**(Optional)**

(1) The figure that includes any three successive data when V_{in} is ramp signal.

7. Problem 3**(Optional)**

Repeat the problem 1 and problem 2 for 8-bit ADC operation.

8. Conclusion