Laboratory #6 Report

Class:

Name: Student ID:

1. Exploration 1
   1. Experimental result

Table 6.2

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Vin | Vout  (Without RFB) | Vout  (RFB=1K(Ω)) | Vout  (RFB=100K(Ω)) | Vout  (RFB=1Meg(Ω)) |
| 0.0 |  |  |  |  |
| 0.5 |  |  |  |  |
| 1.0 |  |  |  |  |
| 1.5 |  |  |  |  |
| 2.0 |  |  |  |  |
| 2.5 |  |  |  |  |
| 3.0 |  |  |  |  |
| 3.5 |  |  |  |  |
| 4.0 |  |  |  |  |
| 4.5 |  |  |  |  |
| 5.0 |  |  |  |  |

* 1. Plot the figure of input-output transfer curve
  2. The threshold voltage, Vth is about \_\_\_\_\_V with without RFB ;

Vth is about \_\_\_\_\_V with RFB = 1K(Ω); Vth is about \_\_\_\_\_V with RFB = 100K(Ω); and Vth is about \_\_\_\_\_V RFB = 1Meg(Ω)

1. Exploration 2
2. Show the figure of input voltage(Vin) and output voltage(Vout).
3. The gain of the OPAMP is about \_\_\_\_V/V
4. Exploration 3
   1. The approximate offset voltage is V.
5. Exploration 4
   1. Frequency response of the inverting configuration

Table 6.3

|  |  |  |  |
| --- | --- | --- | --- |
| Freq. (Hz) | Vi,p-p (mV) | Vo,p-p (mV) | Vo,p-p / Vi,p-p (dB) |
| 20 | 20 |  |  |
| 100 | 20 |  |  |
| 300 | 20 |  |  |
| 500 | 20 |  |  |
| 700 | 20 |  |  |
| 900 | 20 |  |  |
| 1k | 20 |  |  |
| 1.2k | 20 |  |  |
| 1.5k | 20 |  |  |
| 1.7k | 20 |  |  |
| 2k | 20 |  |  |
| 5k | 20 |  |  |
| 10k | 20 |  |  |
| 100k | 20 |  |  |
| 500k | 20 |  |  |
| 1Meg | 20 |  |  |

1. Exploration 5
2. Plot the close-loop frequency response.
3. Plot the open-loop frequency response
4. Problem 1

Threshold voltage of the transfer curve will be increased or decreased with the increasing of Wp/Wn ratio? Why?

1. Problem 2

How does the current through NMOS change with the increasing of input voltage Vin? Try to explain the change of id,NMOS-to-Vin curve. Use PSpice simulation to verify your explanation.(hint: Table 6.1)

1. Problem 3

This Lab. derives the open-loop transfer function indirectly by decreasing the open-loop gain with the applying of feedback network. Please derive the relation between R2/R1 and the dc gain, and the location of 3-dB pole in inverting configuration, respectively.

1. Problem 4

Please briefly design a new measurement flow for deriving the open-loop transfer function with the non-inverting configuration.

1. Bonus 1

P-N type (similar to inverter) power stage is commonly used in the power stage, and the current through power PMOS/NMOS are usually very large. To prevent the current shooting through PMOS and NMOS, which causes large power loss, rise or fall time should be taken into considerations in the design of power stage. Try to analyze the relation between power loss at the transition region during either rise time or fall time.

1. Bonus 2

Comparison of the measurement result of open-loop transfer function by applying inverting and non-inverting configuration. Which of the configuration will be better for the measurement? (Hint: the offset cancelation method and its performance)

1. Conclusion