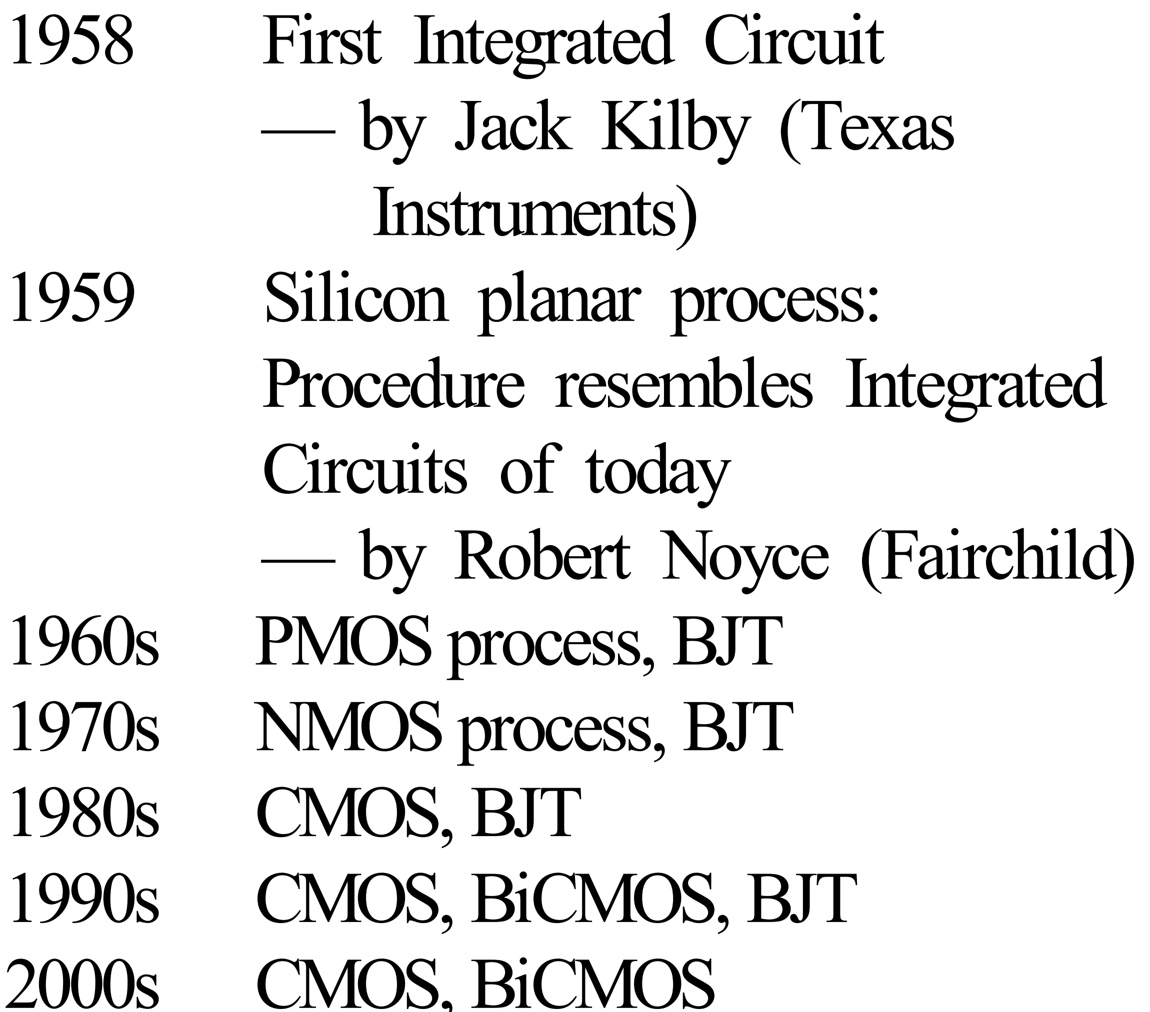
Brief Historical Overview of Technology Development

1925 FET theoretical development
— by Lilienfeld

1935 Modern FET structure
— by Heil

1947 Bipolar Junction Transistor (BJT)
— by Brattin, Bardin, and Schockley (Bell Lab.)



1958 First Integrated Circuit
— by Jack Kilby (Texas Instruments)

1959 Silicon planar process:
Procedure resembles Integrated Circuits of today
— by Robert Noyce (Fairchild)

1960s PMOS process, BJT

1970s NMOS process, BJT

1980s CMOS, BJT

1990s CMOS, BiCMOS, BJT

2000s CMOS, BiCMOS

Semiconductor Material

- Germanium
  — was widely used in the early discrete device.

- Silicon.
  — dominant in IC for the past two decades and will remain dominant for the next decade 25% of the earth's crust
  --- very rich.

- Gallium Arsenide
  — niche market
  — maybe quite profitable.

Big Chance for Talented Engineers

In spite of the sophistication and cost of both the hardware and software necessary to remain competitive in the field of **VLSI** design, most major contributions to this field are based upon relatively simple and basic innovations by the
engineer. These innovations occur in circuit design, processing, and modeling as well as in the evolution of the **CAD** tools themselves. They are often made by young engineers. Because of the economic impact of innovations in the **VLSI** design field, advancement potential and rewards for talented and ambitious engineers are essentially unlimited. This potential exists for both young and old in institutions ranging from small start-up companies to the giants of the industry

●Terminology

An *integrated circuit(IC)* is a combination of interconnected circuit elements inseparably associated on or within a continuous substrate.

The *substrate* is the supporting material upon or within which an IC is fabricated or to which an IC is attached.

A *monolithic IC* is an IC whose elements are formed in place upon or within a semiconductor substrate with at least one of the elements formed within the substrate.

A *hybrid IC* consists of a combination of two or more IC types or an IC with some discrete elements.

A *wafer* (or *slice*) is the basic physical unit used in processing. It generally contains a large number of identical ICs. Typically, the wafer is circular; production wafers have a diameter of 4, 5, or 6 in.

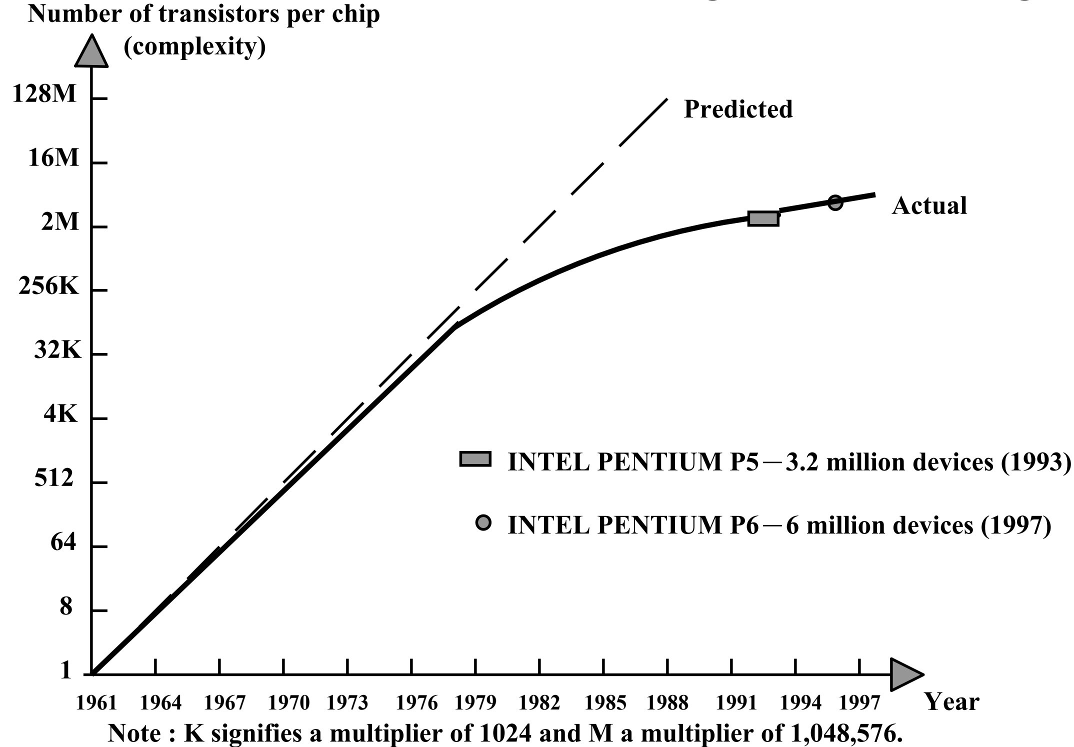
The *chip* is one of the repeated ICs on a wafer. A typical production wafer may contains as few as 20 or 30 ICs as many as several hundred or even several thousand, depending upon the complexity and size of the circuit being fabricated. The terms die and bar are used interchangeably for chip in some companies.

A *test plug*, or process control bar (PCB), or process control monitor(PCM), is a special chip that is repeated only a few times on each wafer. It is used to monitor the process parameters of the technology. After processing, the validity of the process is verified by measuring , at the wafer probe level, the characteristics of devices and/or circuits on the test plug. If the measurements of key parameters at the test plug level are not acceptable, the wafer is discarded.

A *test cell*, or *test lead*, is a special chip repeated only a few times on each wafer. It differs from the test plug in that the circuit designer includes this cell specifically to monitor the performance of elementary subcircuits or subcomponents.

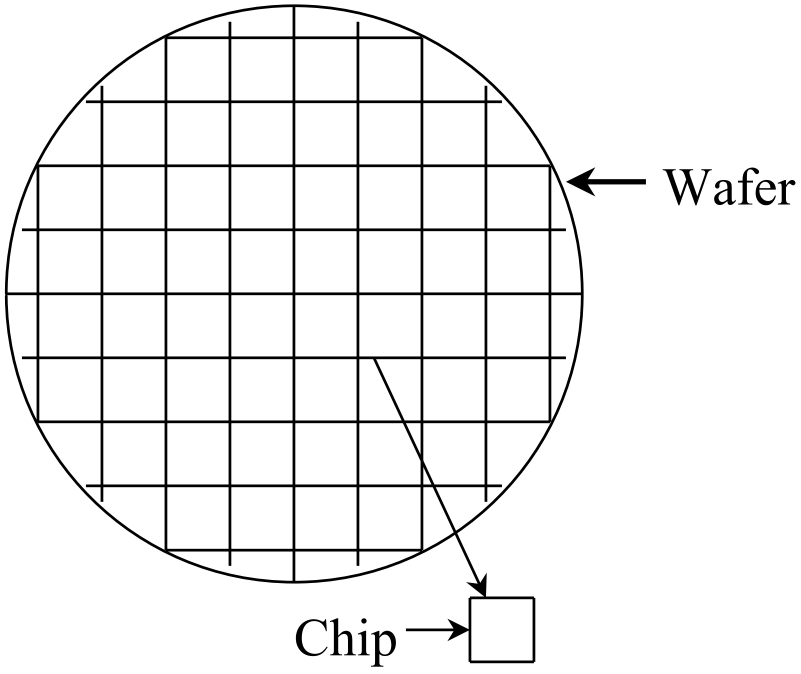
Size and Complexity of Integraled Circuits

- Moore's first law : Transistors integrated on a single chip

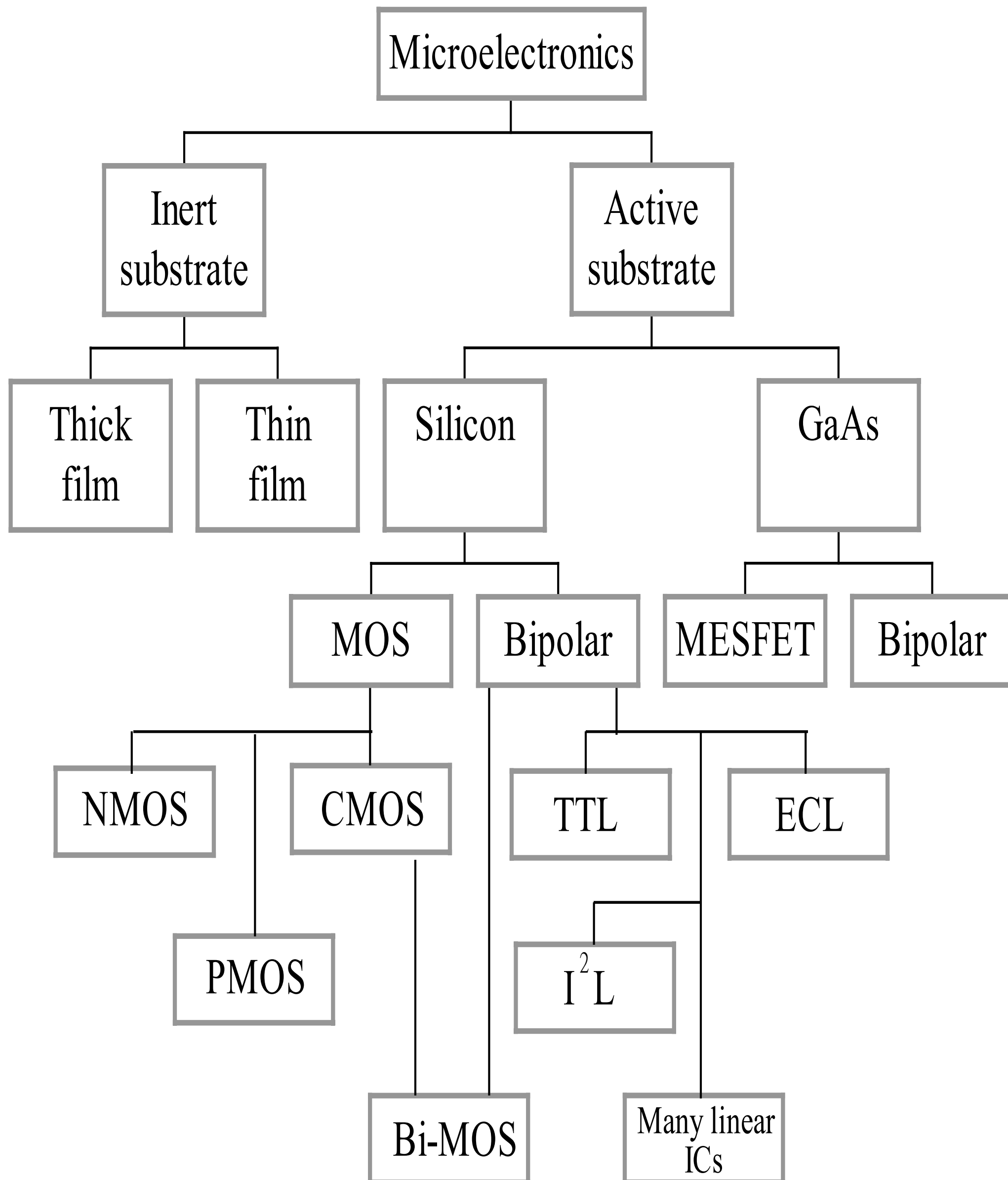


Note : K signifies a multiplier of 1024 and M a multiplier of 1,048,576.

- Sketch of a wafer showing repeated chips



Major Processes Used in IC Fabrication

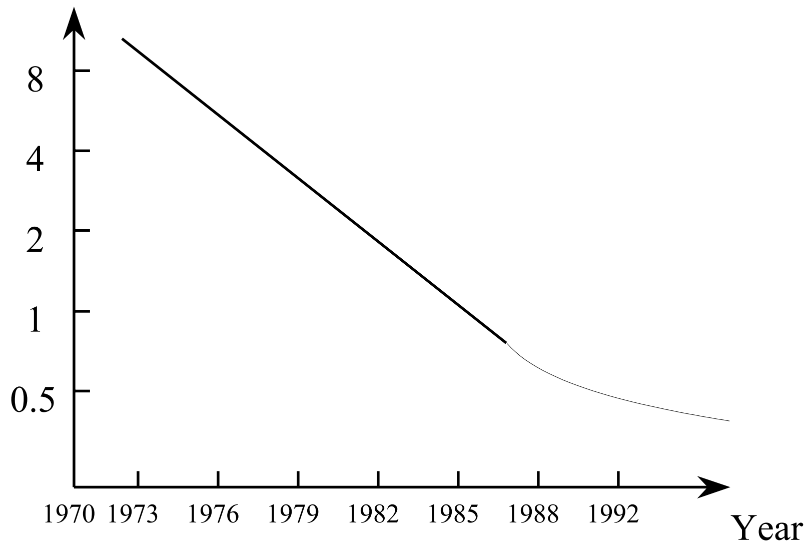


Microelectronics Evolution

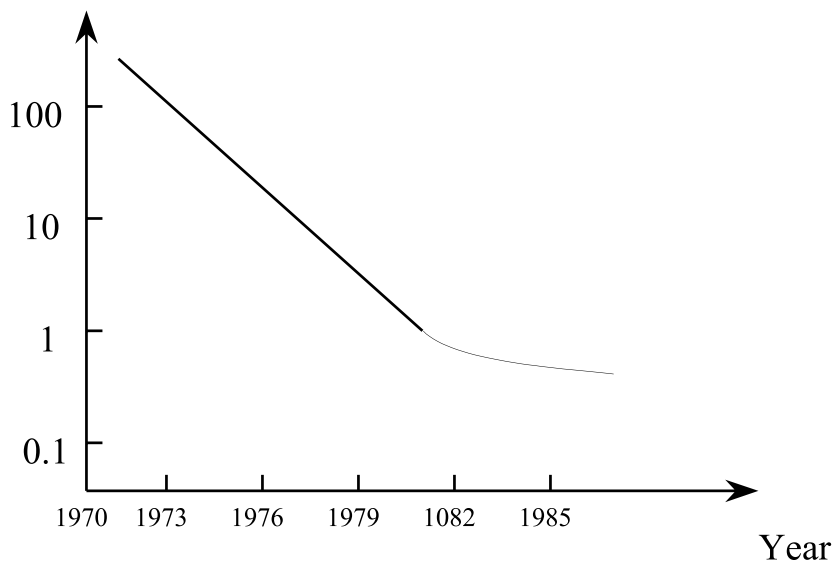
Year	1947	1950	1961	1966	1971	1980	1990	2000
Technology	*Invention of transistor*	*Discrete components*	*SSI*	*MSI*	*LSI*	*VLSI*	*ULSI**	*GSI⌖*
Approximate number of transistors per chip in commercial products	1	1	10	100-1000	1000-20,000	20,000-1,000,000	1,000,000-10,000,000	>10,000,000
Typical products	-	Junction transistor and diode	Planar devices Logic gates Flip-flops	Counters Multiplexers Adders	8-bit micro-processors ROM RAM	16 and 32 bit micro-processors Sophisticated peripherals	Special processors, Virtual reality machines, Smart sensors	

*Ultra large-scale integration
⌖Giant-scale integration

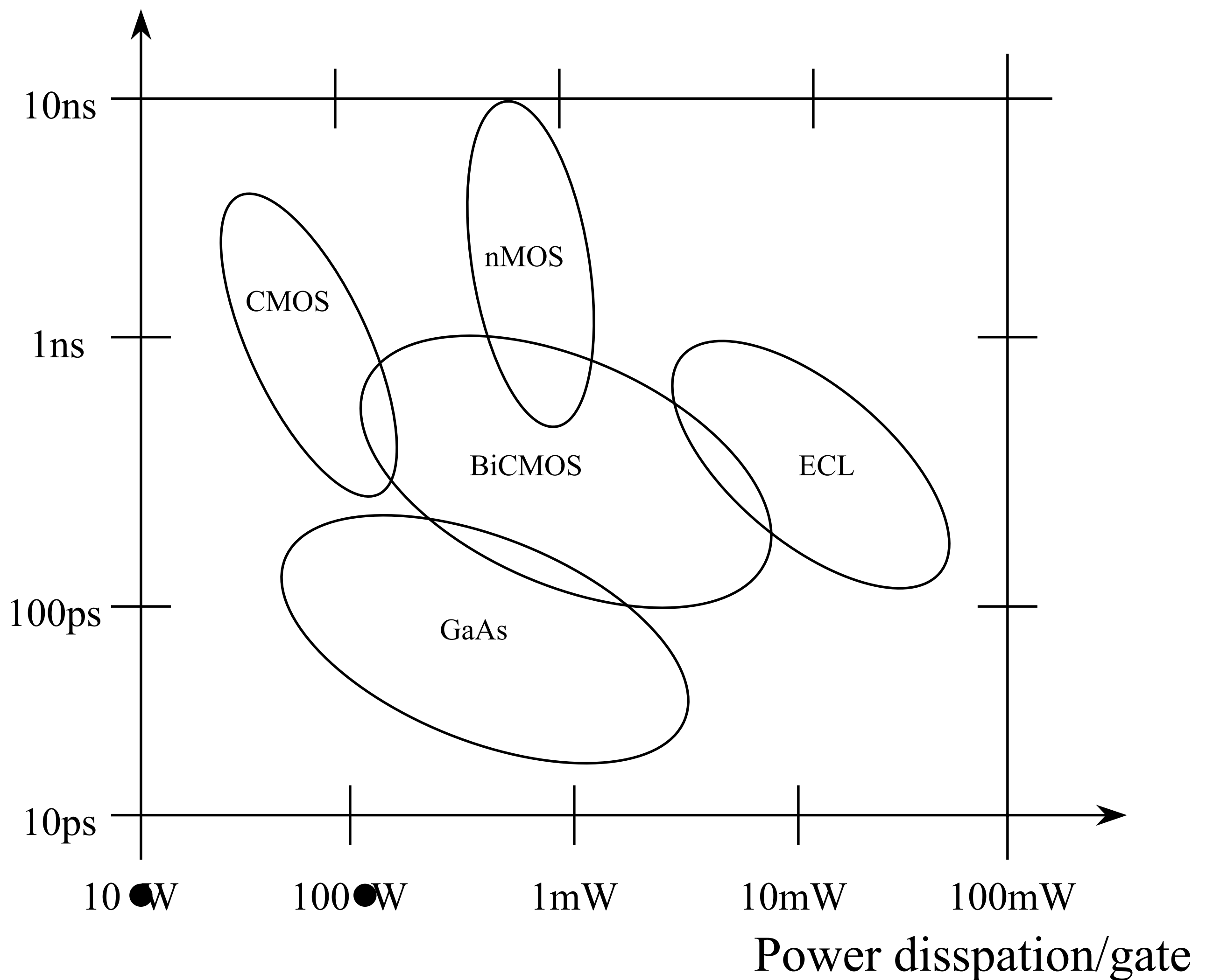
Approximate Minimum Line Width of Commercial Products versus Year



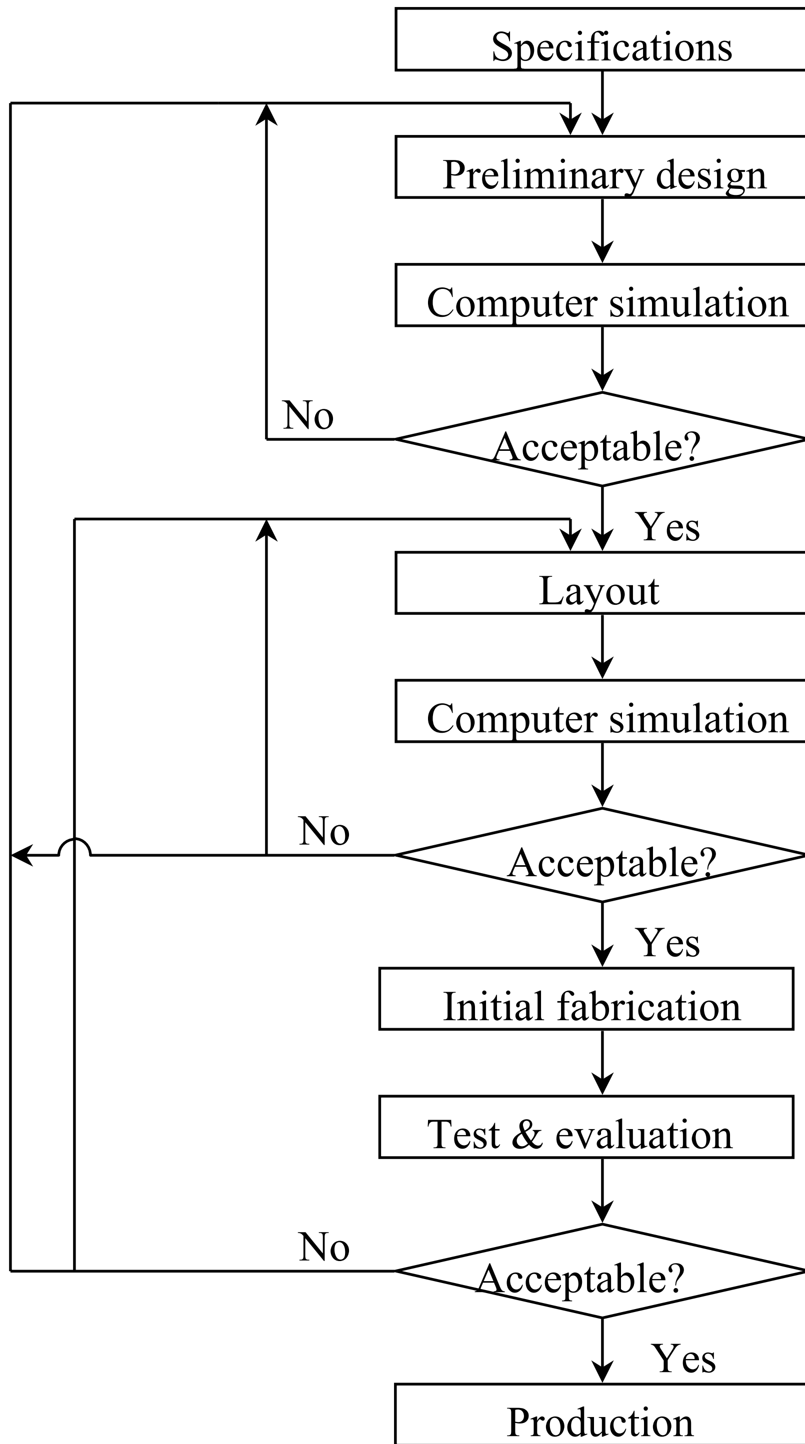
Delay-Power Product per Gate vs. Year



Speed/Power Performance of Available Technologies

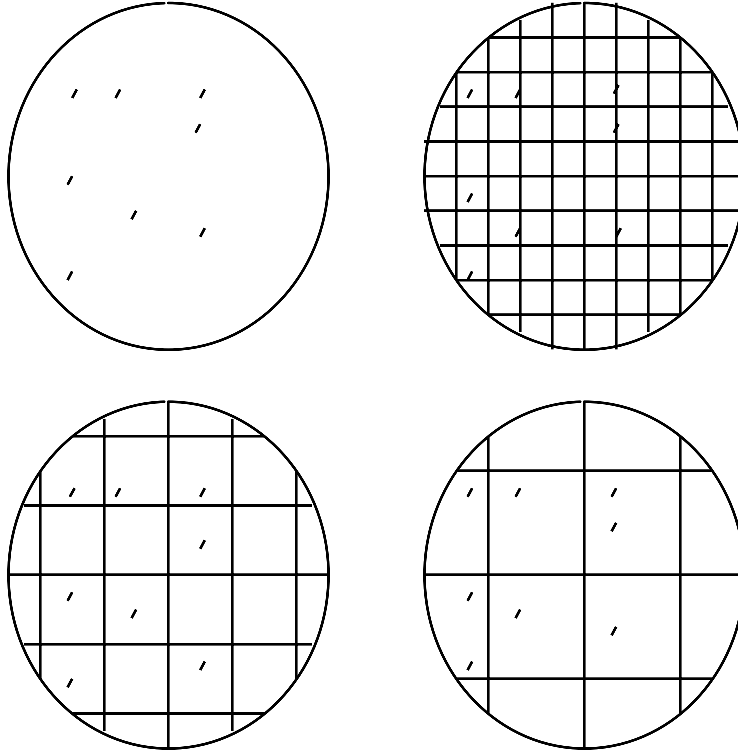


IC Design Process



Yield

- Defect effects



- Probability that a die is good : P

  P is a function of A&D

  A:die area

  D:defect density

  e.g. $P=e^{-AD}$

  $P=e^{-\sqrt{AD}}$

  $P=\left(\frac{1 \quad e^{-AD}}{AD}\right)^{2}$

Economics

- Major costs associated with wafer processingand and fabrication

		Cost	
		per wafer	per die
Wafer fabrication			
Blank wafer	x_1	√	
Wafer processing	x_2	√	
Wafer probe	x_3	√	
Wafer sawing	x_4	√	
Die attach, bonding and packaging	x_5	√	
Packaging	x_6		√
Final test	x_7		√

- Typical processing and packaging costs for 12-mask,_ 3u CMOS process(1988) based upon volume production

processing costs		
	4" process	5"process
Wafer fabrication		
Blank wafer	x_1=\$10	x_1=\$15
Wafer processing	x_2=\$140	x_2=\$150
Wafer probe (per wafer)	x_3=\$25	x_3=\$40
Wafer sawing (per wafer)	x_4=\$3	x_4=\$3
Die attach and bonding (per wafer)	x_5=\$3	x_5=\$5
Packaging	x_6 (see below)	x_6(see below)
Final test (per package)	x_7=30 /cm^2	x_7=30 /cm^2

Package costs		
Plastic DIP	8pin	\$0.032
Plastic DIP	16pin	0.048
0.048Plastic DIP	24pin	0.091
Plastic DIP	64pin	0.70
Ceramic side brazed	16pin	1.05
Ceramic side brazed	24pin	1.50
Ceramic side brazed	64pin	4.95
Ceramic CERDIP	16pin	0.096
Ceramic CERDIP	24pin	0.26
Ceramic CERDIP	40pin	0.64
Ceramic pin grid array	68pin	6.40
Ceramic pin grid array	84pin	7.50
Ceramic pin grid array	132pin	10.15
Ceramic pin grid array	224pin	18.00

Trends in VLSI Design

- Continual Shrinking of minimum geometrical feature size
- Increasing speed in digital circuits
  --- may use GaAs for high speed
- Increasing circuit complexity on a die
- Increasing designer productivity and growing dependence on CAD
- Shift to Far Eastern
  design => more developed countries
  production => less developed countries
- Performance of process depends on equipment
- Increasing complexity of process
  e.g BiCOMS=MOS+Bipolar