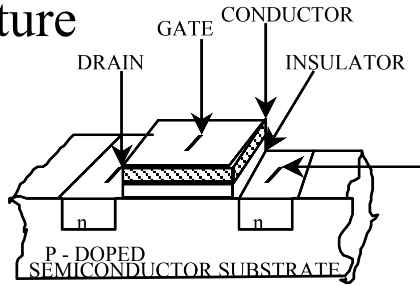
MOS Technology and Design Rule / Layout Rule

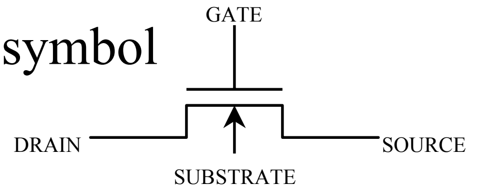
- Silicon semiconductor Technology
- CMOS process
- Layout Rules
- Latchup
- CAD issue
- Technology-related

MOS Transistors

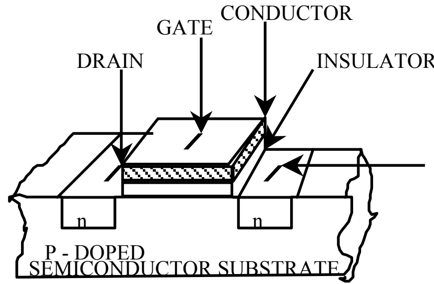
- MOS structure
  - NMOS



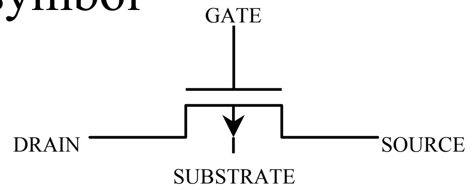
  - symbol



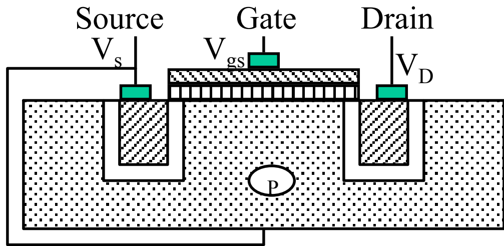
  - PMOS



  - symbol



- MOS cross section view
  - Enhancement NMOS



Metal

Polysilicon

Oxide

n-diffusion

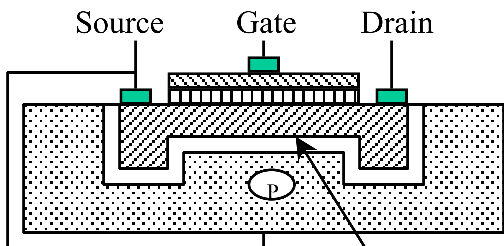
p-diffusion

p-substrate

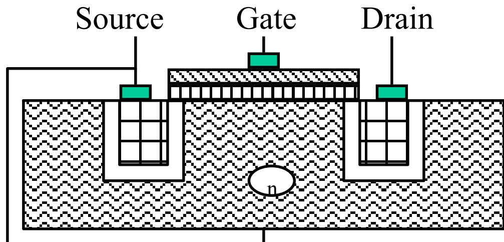
n-substrate

Depletion

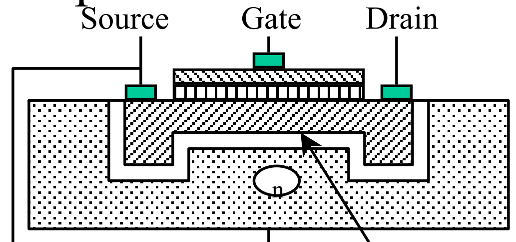
  - Depletion NMOS



  - Enhancement PMOS

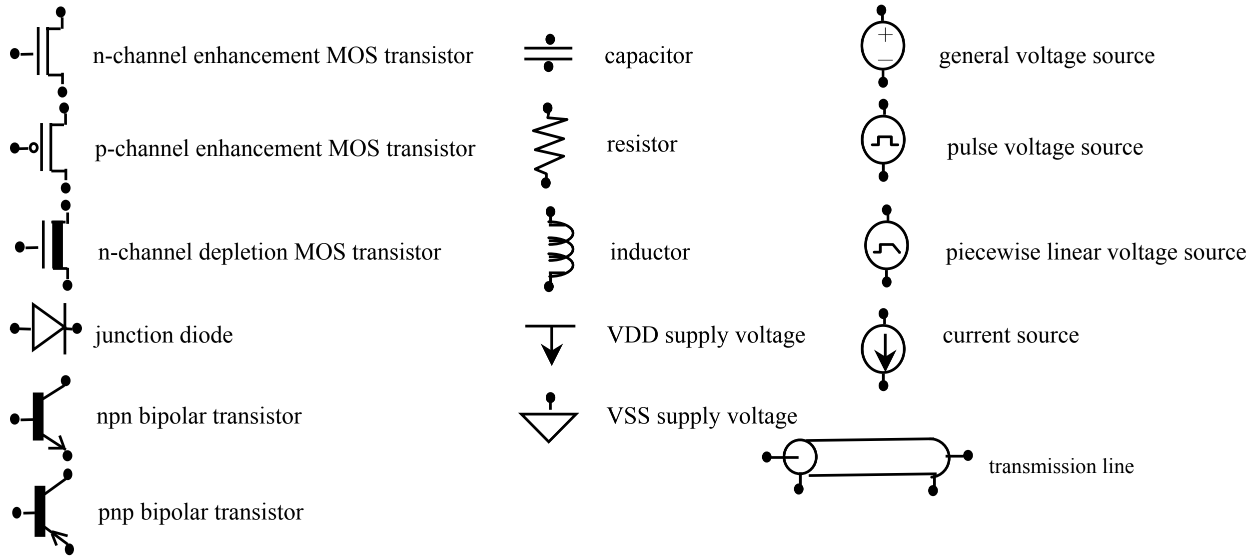


  - Depletion PMOS

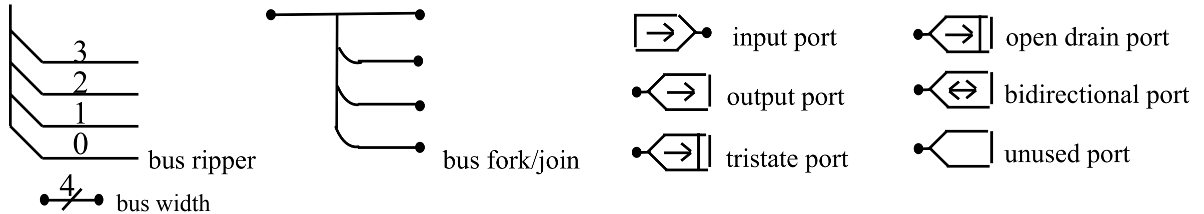


Key to Schematics Used in The Book

PRIMITIVES



BUSSES

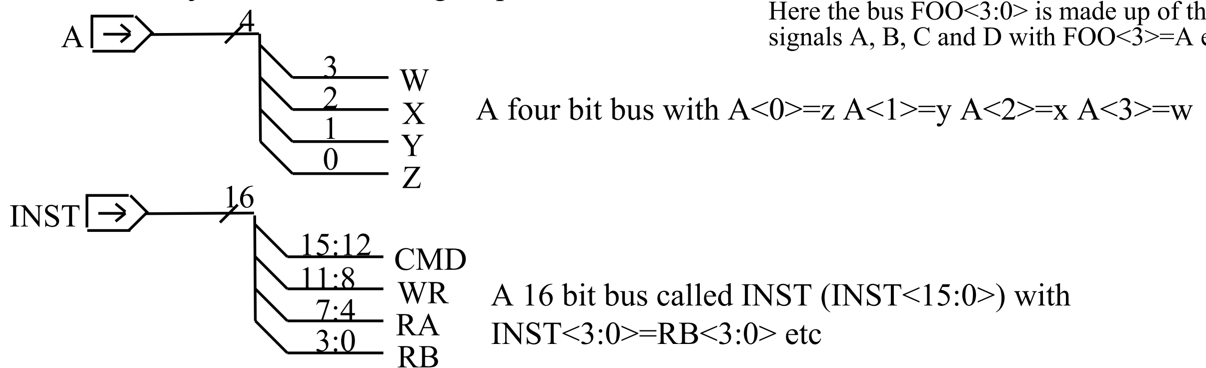


a bus width specifies the width of the bus and the bus ripper or bus fork/join specify which subfields of the bus are extracted from the bus

a bus ripper can extract arbitrary fields per connection, while a bus fork/join extracts one signal per connection

FOO —/4— A, B, C, D

a bus can be named by concatenating names or fields
Here the bus FOO<3:0> is made up of the signals A, B, C and D with FOO<3>=A etc.

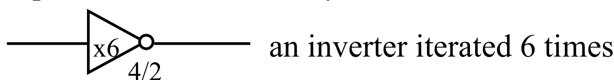


A four bit bus with A<0>=z A<1>=y A<2>=x A<3>=w

A 16 bit bus called INST (INST<15:0>) with INST<3:0>=RB<3:0> etc

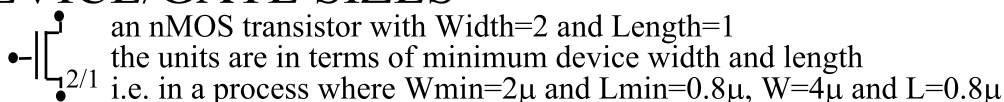
REPLICATION

replication is indicated by a small x and a number on a schematic icon

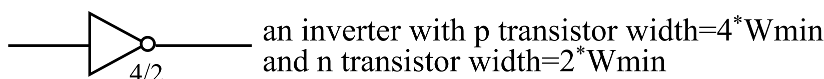


an inverter iterated 6 times

DEVICE/GATE SIZES



an nMOS transistor with Width=2 and Length=1
the units are in terms of minimum device width and length
i.e. in a process where Wmin=2μ and Lmin=0.8μ, W=4μ and L=0.8μ



an inverter with p transistor width=4*Wmin
and n transistor width=2*Wmin

Silicon Semiconductor Technology

- Wafer processing
  - Wafer are cut from ingots of single-crystal silicon that have been pulled from a crucible melt of pure molten polycrystalline silicon.
  - Controlled amounts of impurities are added to the melt to provide the crystal with the required electrical properties.
  - The crystal orientation is determined by a seed crystal that is dipped into the melt to initiate single-crystal growth.
- Oxidation
  - SiO_2 is extremely important for making silicon ICs
  - Two common approaches to achieve silicon oxidation on silicon wafers.
    1. Wet oxidation: when the oxidizing atmosphere contains water vapor.
    2. Dry oxidation: when the oxidizing atmosphere is pure oxygen
  - The oxidation process consumes silicon. Since SiO_2 has approximately twice the volume of silicon, the SiO_2 layer grows almost equally in both vertical directions.

SiO_2 | unoxidized silicon surface | SiO_2 ← field oxide (Thick oxide)

- SiO_2 by deposition

SiO_2 | silicon surface | SiO_2

Silicon Semiconductor Technology (Cont.)

- Epitaxy

  Its aim is to grow high-purity single-crystal layers of controlled thickness with accurately determined dopant concentrations distributed homogenerously throughout the layer

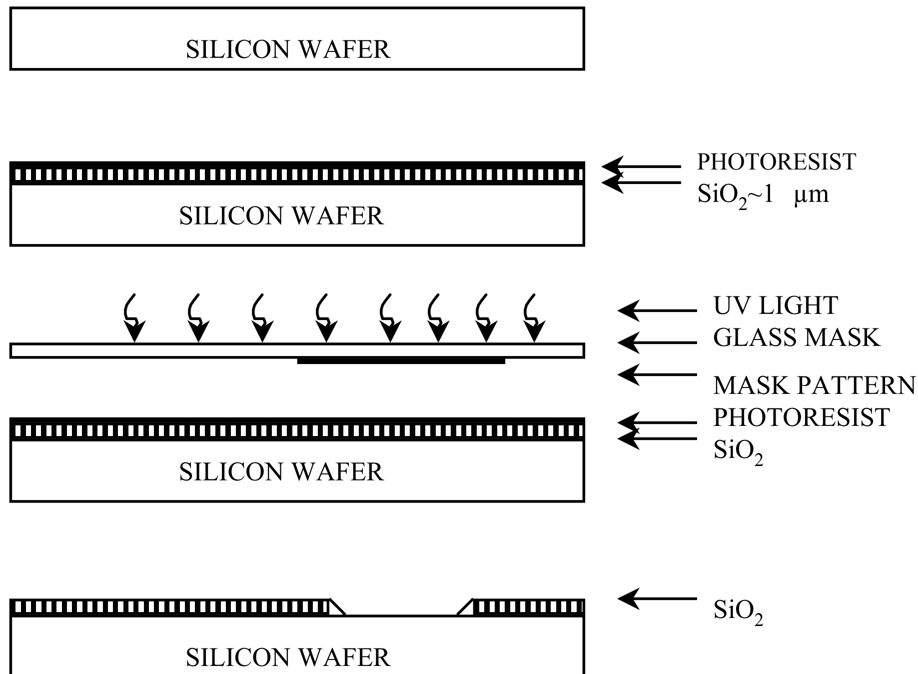
  The electrical properties of epi-layers are determined by the dopant and its concentration

- Deposition
- Ion implantation
- Diffusion
- Donors and acceptors
  - Boron is frequently used for creating acceptor silicon
  - Arsenic and Phosphorous are commonly used to create donor silicon
- The common materials used as masks

  1. photoresist
  2. polysilicon
  3. SiO_2 (silicon dioxide)
  4. SiN (silicon nitride)

Etched SiO_2 Pattern

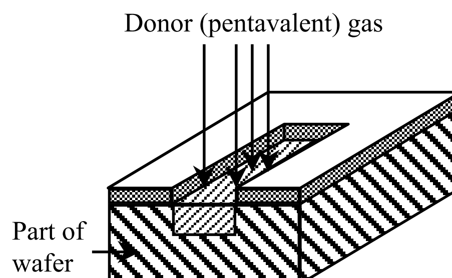
- Simplified steps



- Photoresists:

NEG — first historically
POS — better for dimensions<2.5 µm
NEG — insoluble where exposed
POS — soluble where exposed

- Diffusion process

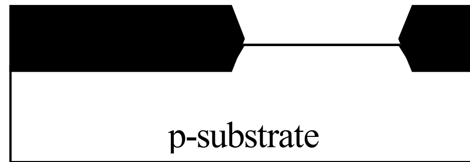


Fabrication of NMOS Transistors

— Self-aligned process (poly gate)

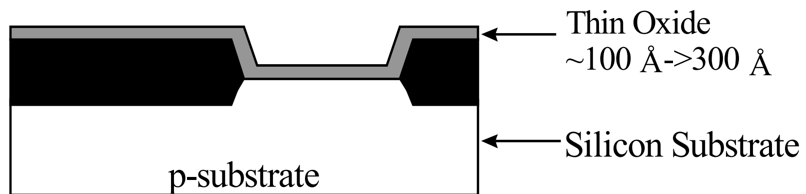
Patterning SiO_2 Layer

(a)



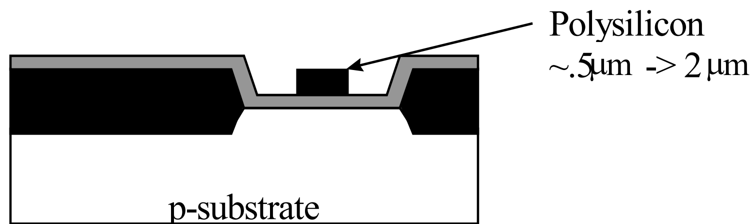
Gate Oxidation

(b)



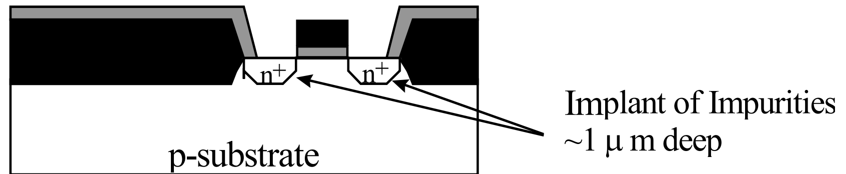
Patterning Polysilicon

(c)



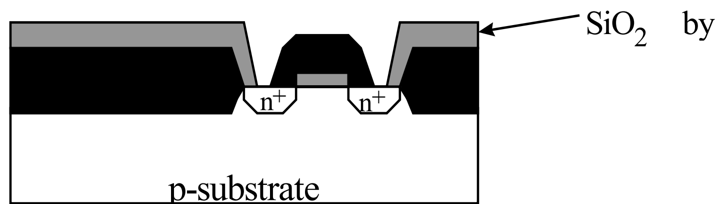
Implant or Diffusion

(b)



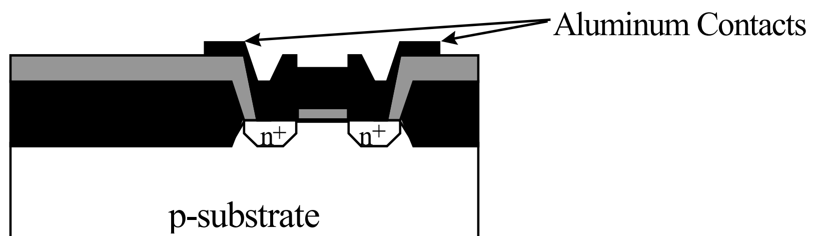
Contact Cuts

(e)



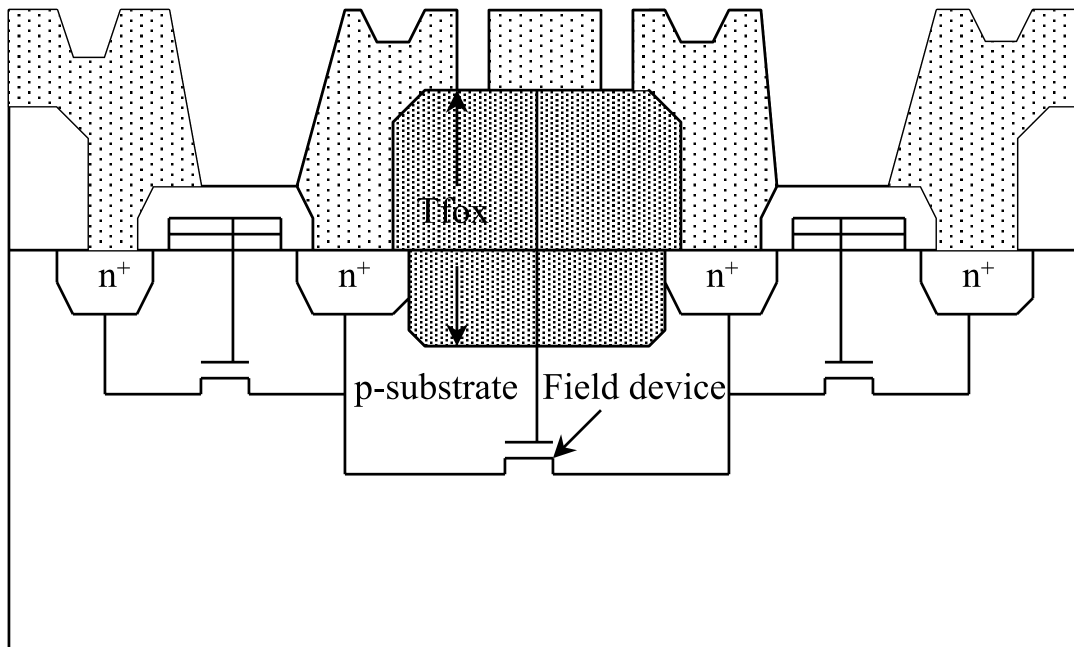
Patterning of Aluminum Layer

(f)



Field Transistors

- parasitic transistor

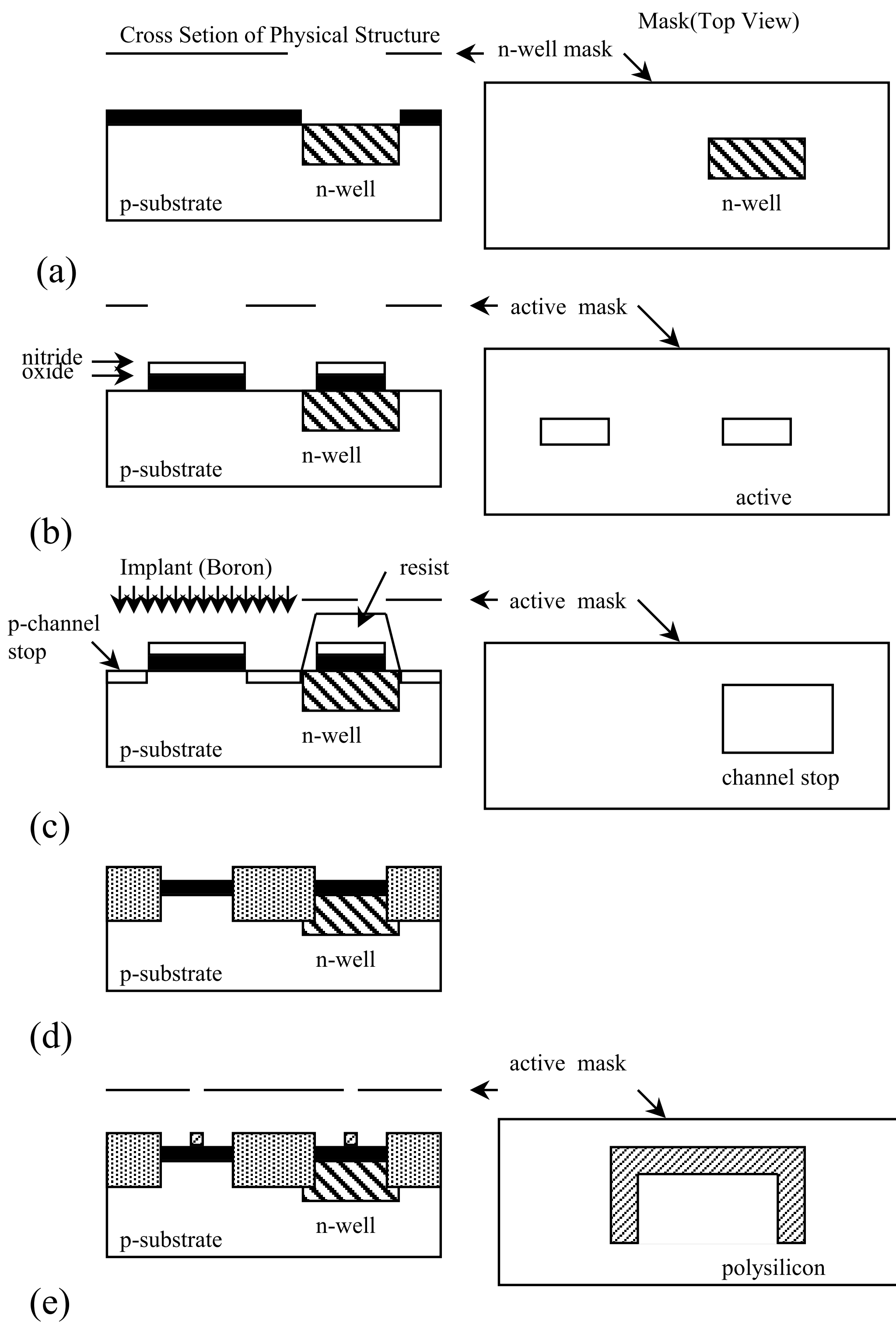


- It's threshold voltage is much higher than that of a regular transistor.

- High threshold is usually ensured by
  1. making the field oxide thick enough.
  2. introducing a " channel-stop " diffusion.

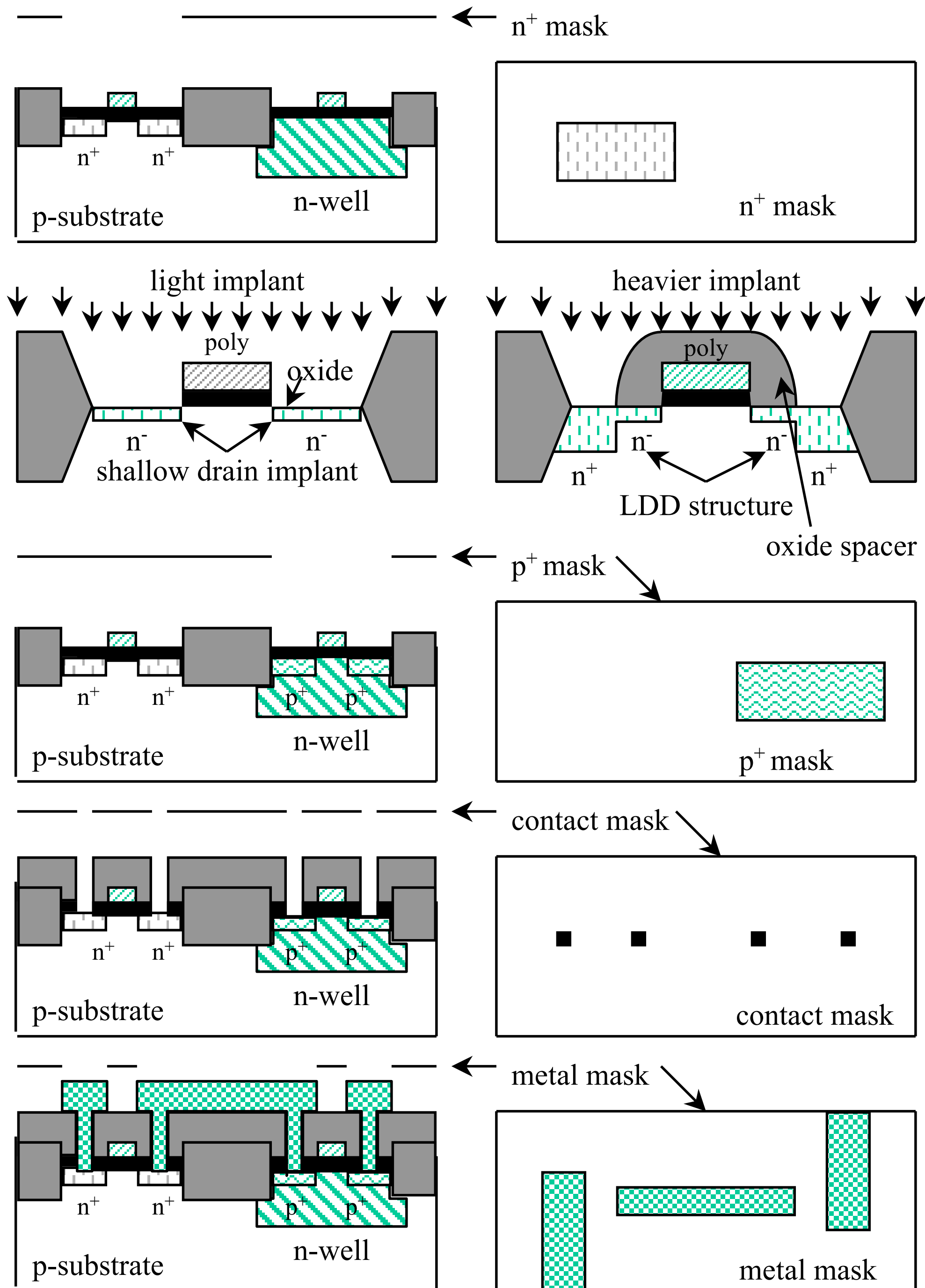
$$\Delta V_{th} \sim \frac{\sqrt{N}}{C} \sim t_{fox}\sqrt{N}$$

N-well CMOS Process



✧lateral movement of field oxide results in "bird's beak" (Fig.(d))

N-well CMOS Process(Cont.)



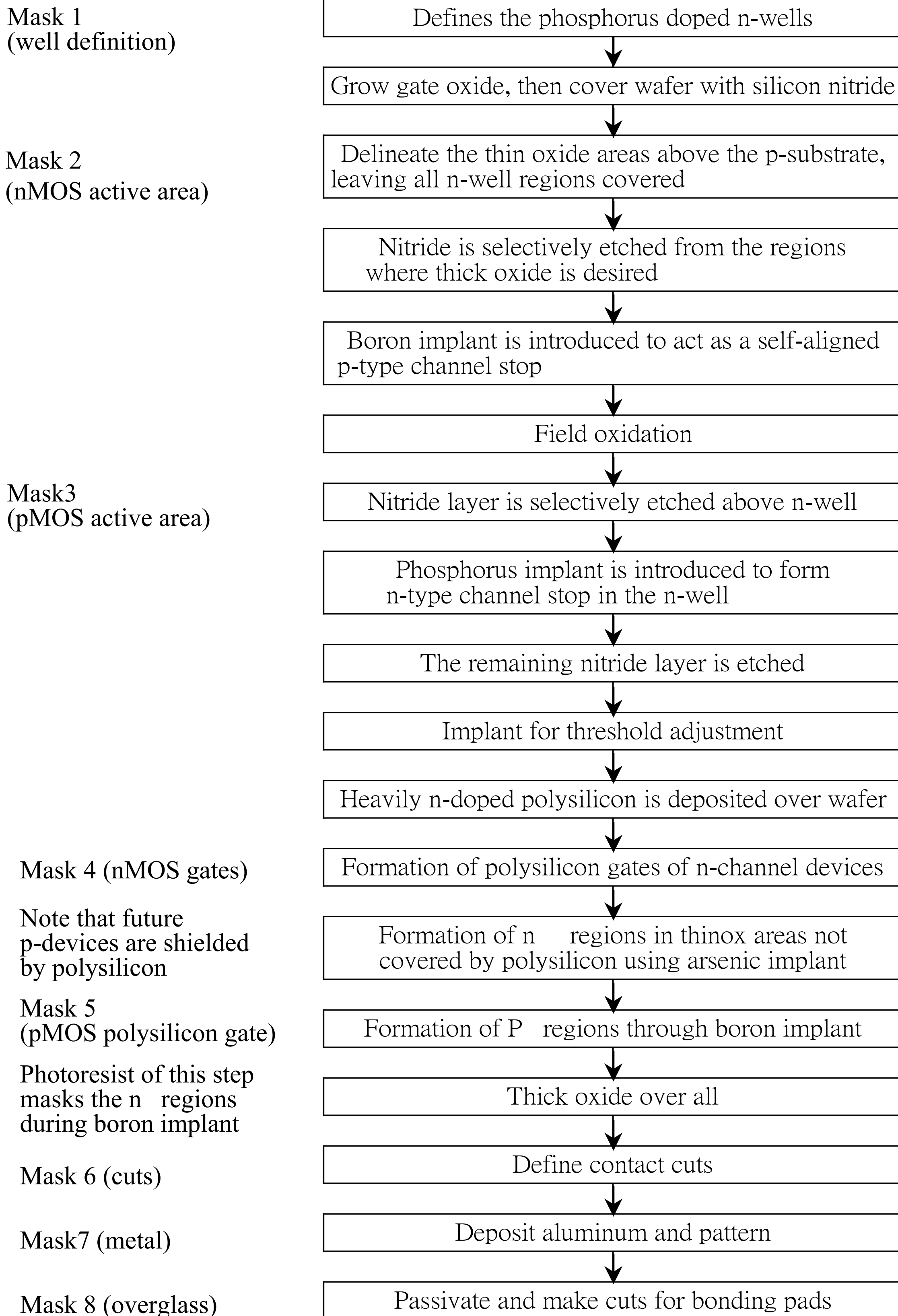
- final step (not shown):

  1. passivation
     — protect silicon surface from contaminants

  2. openings to bond pads

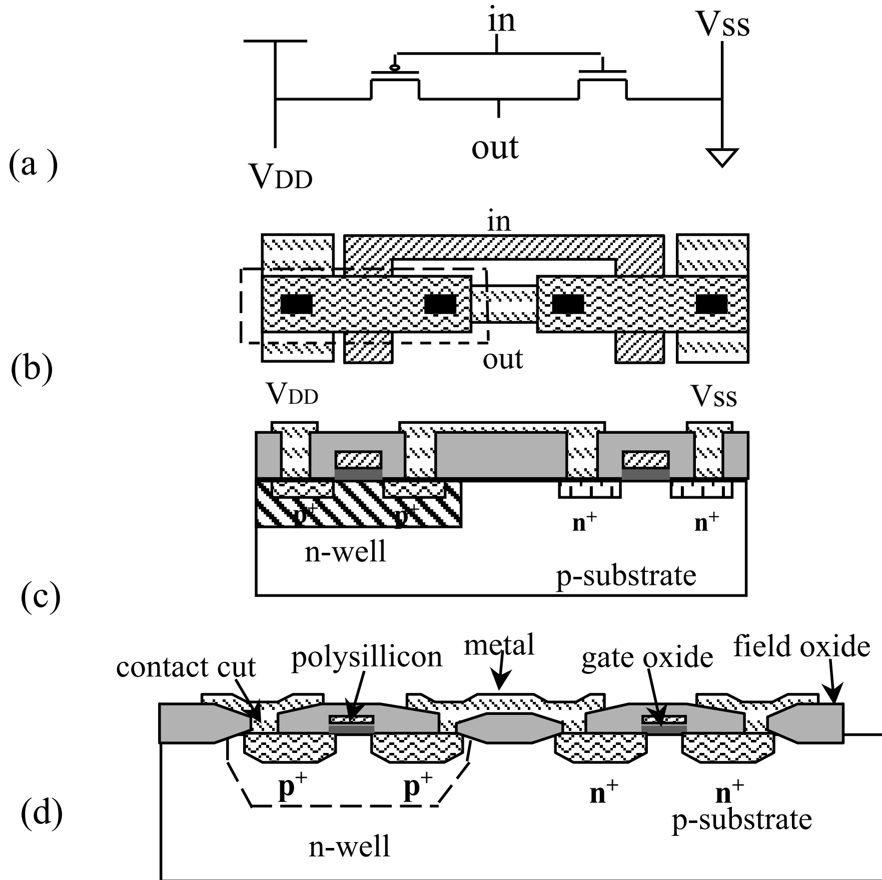
N-well CMOS Process (Cont.)

- Flow diagram of Berkeley n-well fabrication

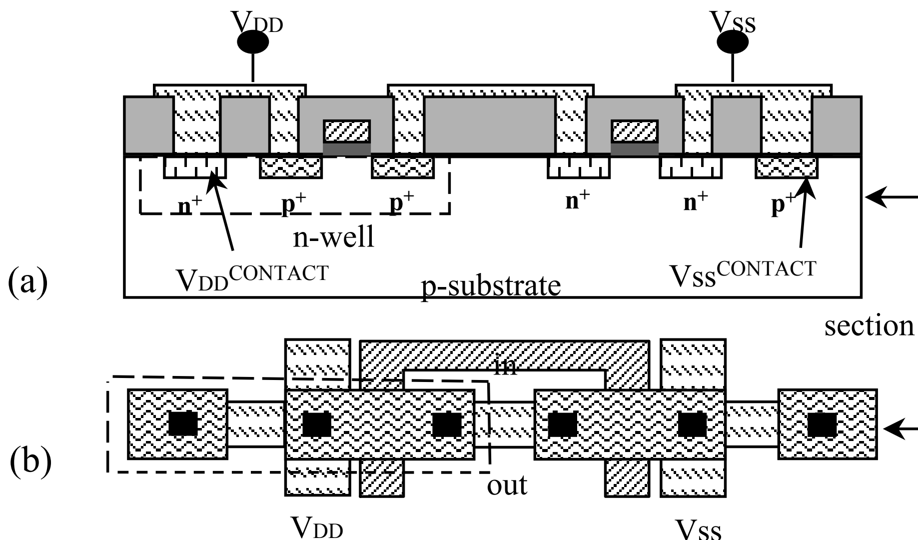


Cross Section of a CMOS Inverter

- N-well process



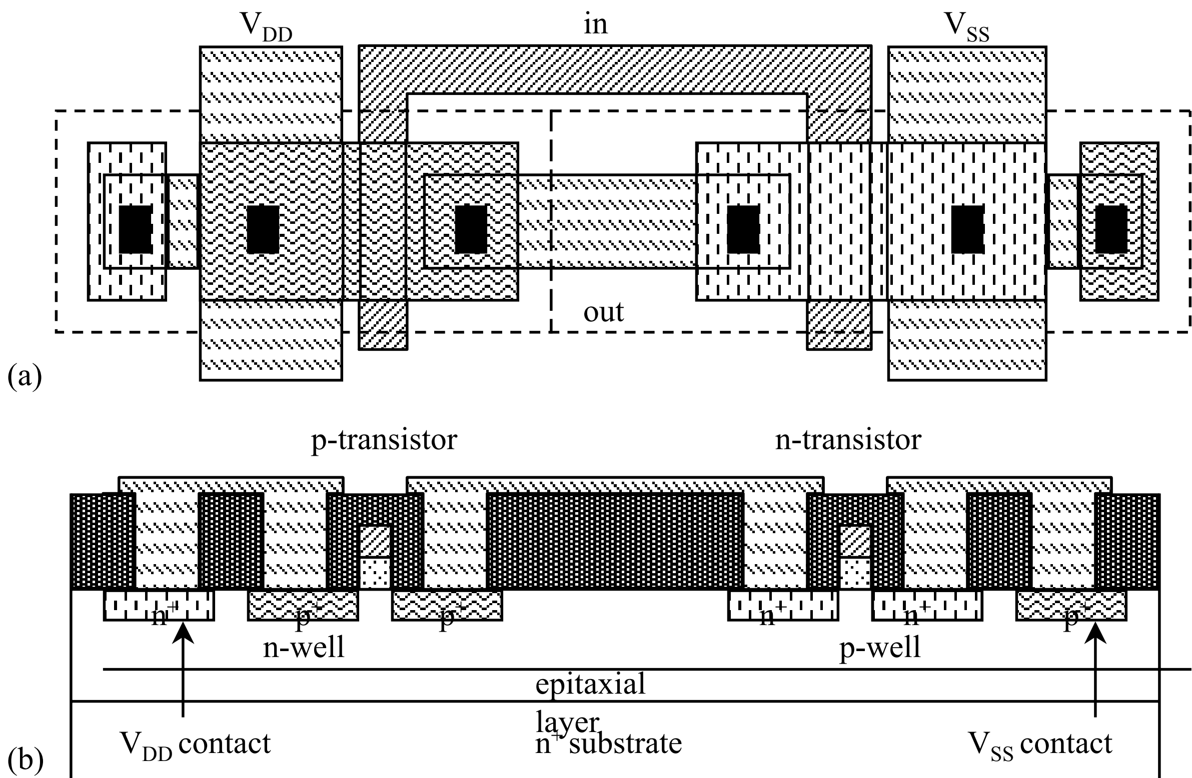
— with substrate contact



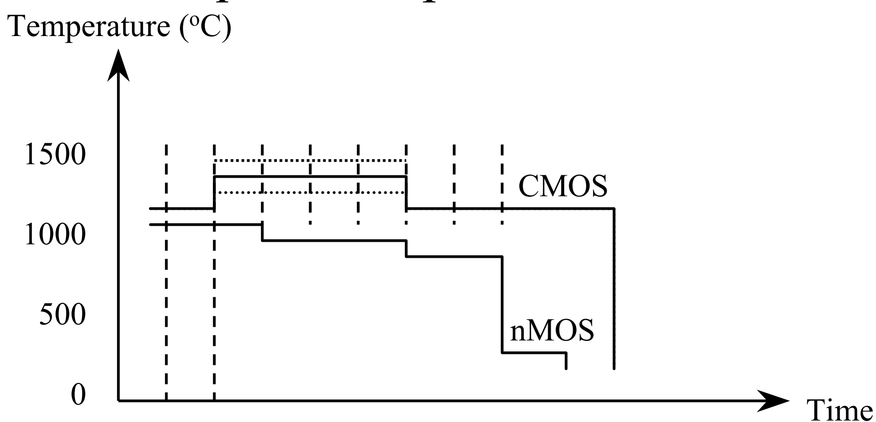
- P-well process can be similarly obtained

Cross Section of a CMOS Inverter (Cont.)

- Twin - well process
  --- provides the basis for separate optimization of the p-type and n-type transistors.
  --- starting material is either an n^+ or p^+ substrate with a lightly doped epilayer, which is used for protection against latchup.



- Thermal sequence of processes



Process Enhancements

- high-quality capacitors for
  1. analog circuits : e.g. double-poly capacitor
  2. memories : e.g. a. trench

     b. stack

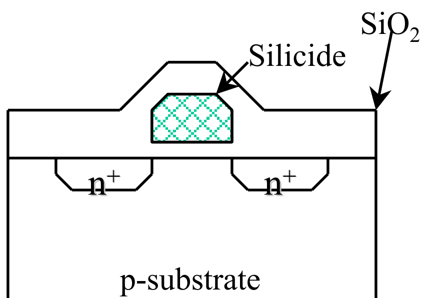
- resistors of variable characteristics

- double-metal, triple-metal(or more)

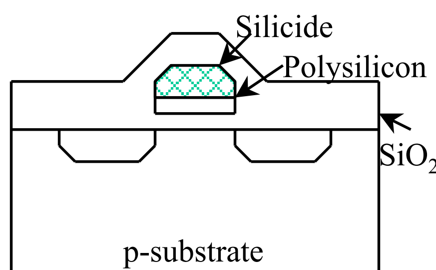
  double-poly, triple-poly(or more)

  (Via is required)

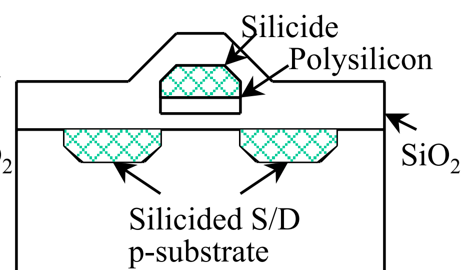
- Polysilicon/Refractory metal
  - silicide: silicon and metal are mixed
  - polycide = poly + silicide
  - salicide: self-aligned polycide



(a) Silicide Gate



(b) Polysilicon Silicide (Polycide)



(c) Salf-Aligned Polysilicon/Silicide (Salicide)

Layout Design Rules

- Layout rules, i.e. design rules => mask-making rules

  — a communication link between circuit designer and process engineer
  — represent the best possible compromise between performance and yield
  — define feature sizes, separations, and overlaps

- Two popular approaches

  1. micron rules:
     — most popular approach
     — given as a list of minimum feature sizes and spacings for all masks reguired in a given process
     — e.g. minimum gate length = 0.25μm
  2. lambda(λ)- based rules:
     — base on a single parameter, λ , which characterizes the linear feature and permits first-order scaling
     — popularized by Mead and Conway
     — have been successfully used for 4 ~ 1.2 μm processes
     (probably not suitable for submicron processes)

Layout Design Rules (Cont.)

- minimum grid dimension
  - — design rules are expressed in terms of minimum grid dimension
  - — At the 1.25 ~ 2 μm level, a minimum grid unit of 0.2 ~0.25μ m was adequate.
  - — In submicron processes, a value of 0.05 ~ 0.1 μ m is more common.
- layer representations
  - — At the mask level, some layers may be omitted for clarity
  - — At the symbolic level only n- and p-transistors will be shown
    (refer to page 378 of textbook)

Layer Representations for the n-well CMOS process

LAYER	COLOR	SYMBOLIC	COMMENTS
N-well	Brown		Inside brown is n-well, outside is p-type substrate.
Thin-oxide	Green	n-transistor	Thinox may not cross a well boundary.
Poly	Red	Polysilicon	Generally n^+.
P^+	Yellow	p-transistor	Inside is p^+.
Metal1	Light blue	Metal1	
Metal2	Tan	Metal2	
Contact-cut, via	Black	Contact	
Metal3	Gray	Metal3	
Overglass			

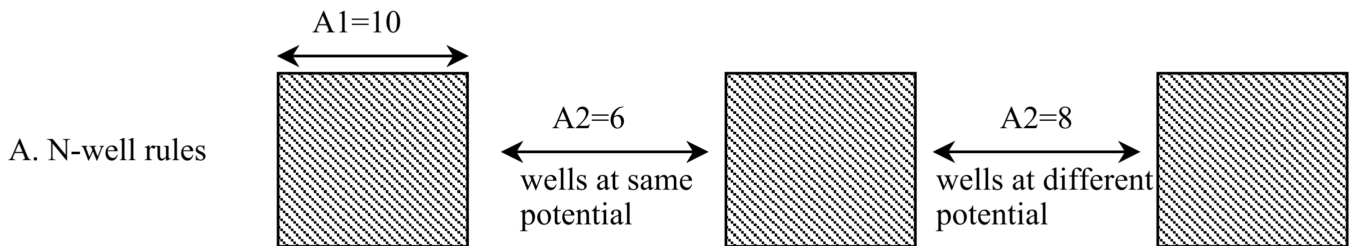
Layout Rules of a 1μm CMOS N-well Process

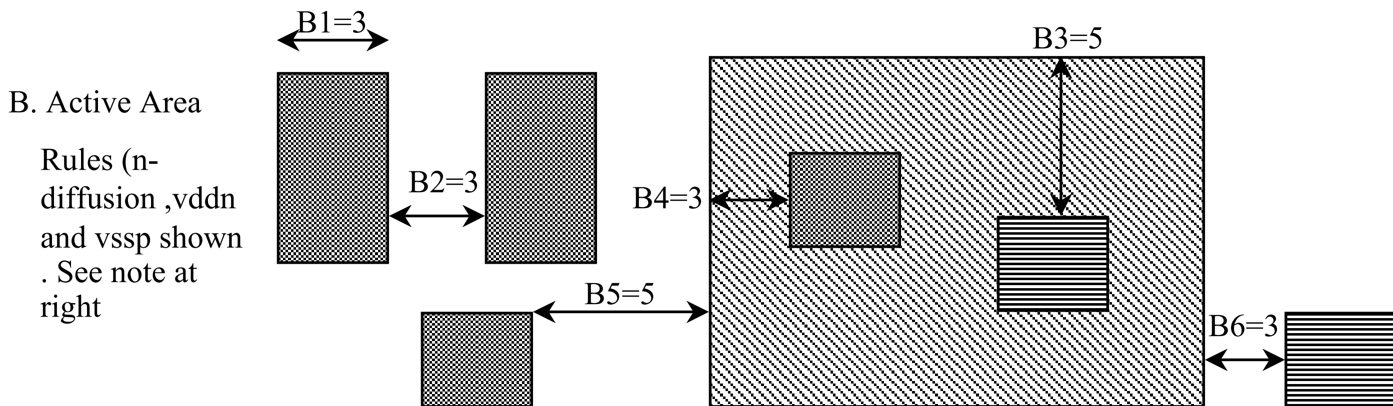
- Example

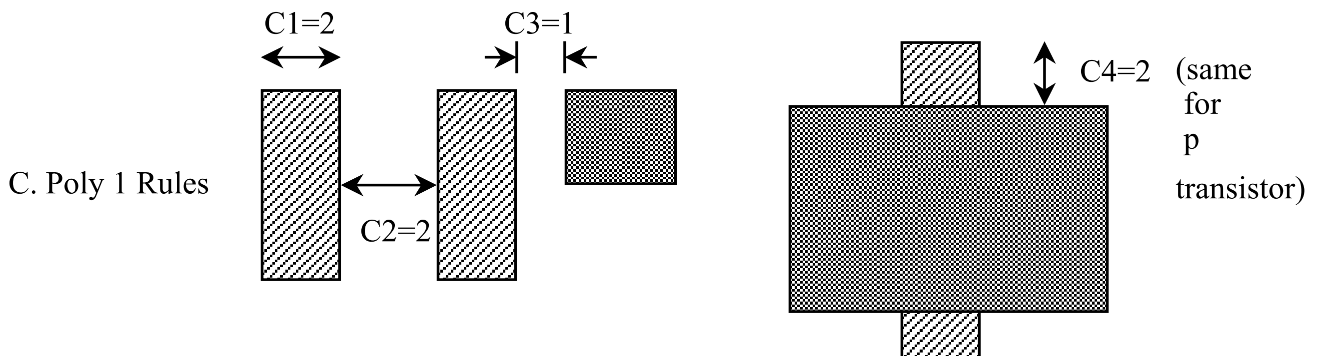
	λRULE	λ/μRULE (0.5μ)	μRULE
A.N-well layer			
A.1 Minimum size	10 λ	5 μ	2 μ
A.2 Minimum spacing (wells at same potential)	6 λ	3 μ	2 μ
A.3 Minimum spacing (wells at different potentials)	8 λ	4 μ	2 μ
B.Active Area			
B.1 Minimum size	3 λ	1.5 μ	1 μ
B.2 Minimum spacing	3 λ	1.5 μ	1 μ
B.3 N-well overlap of *p+*	5 λ	2.5 μ	1 μ
B.4 N-well overlap of *n+*	3 λ	1.5 μ	1 μ
B.5 N-well space to *n+*	5 λ	2.5 μ	5 μ
B.6 N-well space to *p+*	3 λ	1.5 μ	3 μ
C.Poly 1			
C.1 Minimum size	2 λ	1 μ	1 μ
C.2 Minimum spacing	2 λ	1 μ	1 μ
C.3 Spacing to Active	1 λ	0.5 μ	0.5 μ
C.4 Gate Extension	2 λ	1 μ	1 μ
D.p-plus/n-plus(*p+*,*n+*for short)			
D.1 Minimum overlap of Active	2 λ	1 μ	1 μ
D.2 Minimum size	7 λ	3.5 μ	3 μ
D.3 Minimum overlap of Active in abutting contact(see Fig. 3.2.7)	1 λ	0.5 μ	2 μ
D.4 Spacing of *p+/n+* to *n+/p+* gate	3 λ	1.5 μ	1.5 μ
E.Contact			
E.1 Minimum size	2 λ	1 μ	0.75 μ
E.2 Minimum spacing(Poly)	2 λ	1 μ	1 μ
E.3 Minimum spacing(Active)	2 λ	1 μ	0.75 μ
E.4 Minimum overlap of Active	2 λ	1 μ	0.5 μ
E.5 Minimum overlap of Poly	2 λ	1 μ	0.5 μ
E.6 Minimum overlap of Metal1	1 λ	0.5 μ	0.5 μ
E.7 Minimum spacing to Gate	2 λ	1 μ	1 μ
F.Metal1			
F.1 Minimum size	3 λ	1.5 μ	1 μ
F.2 Minimum spacing	3 λ	1.5 μ	1 μ
G.Via			
G.1 Minimum size	2 λ	1 μ	0.75 μ
G.2 Minimum spacing	3 λ	1.5 μ	1.5 μ
G.3 Minimum Metal1 overlap	1 λ	0.5 μ	0.5 μ
G.4 Minimum Metal2 overlap	1 λ	0.5 μ	0.5 μ
H.Metal2			
H.1 Minimum size	3 λ	1.5 μ	1 μ
H.2 Minimum spacing	4 λ	2 μ	1 μ
I.Via2			
I.1 Minimum size	2 λ	1 μ	1 μ
I.2 Minimum spacing	3 λ	1.5 μ	1.5 μ
J.Metal3			
J.1 Minimum size	8 λ	4 μ	4 μ
J.2 Minimum spacing	5 λ	2.5 μ	2.5 μ
J.3 Minimum Metal2 overlap	2 λ	1 μ	1 μ
J.4 Minimum Metal3 overlap	2 λ	1 μ	1 μ
K.Passivation			
K.1 Minimum opening		100μ	100μ
K.2 Minimum spacind		150μ	150μ

Layout Rules of a 1μm CMOS N-well Process

(Cont.)

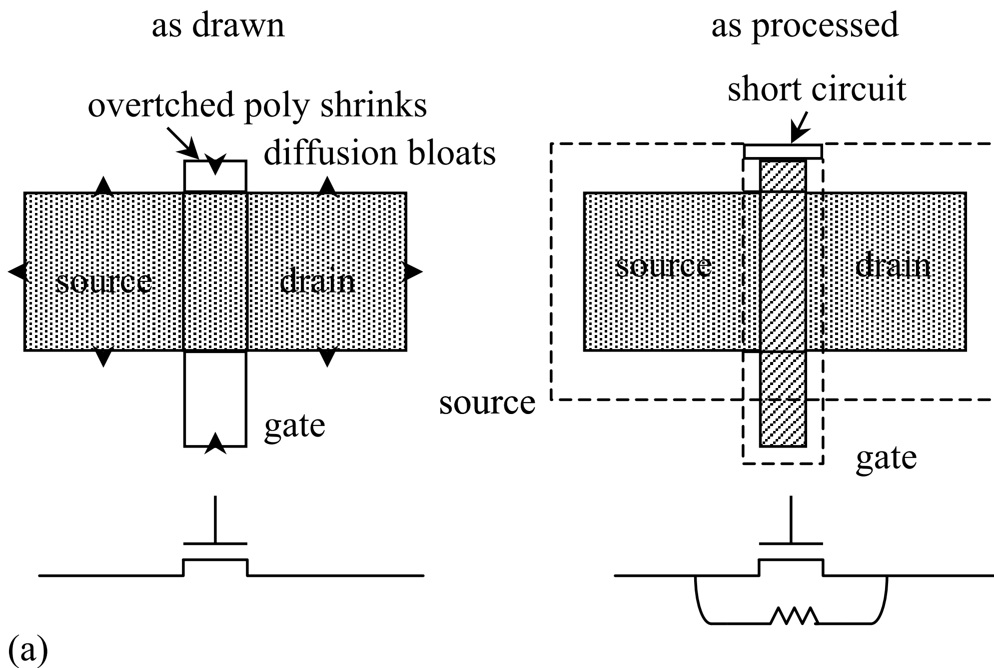


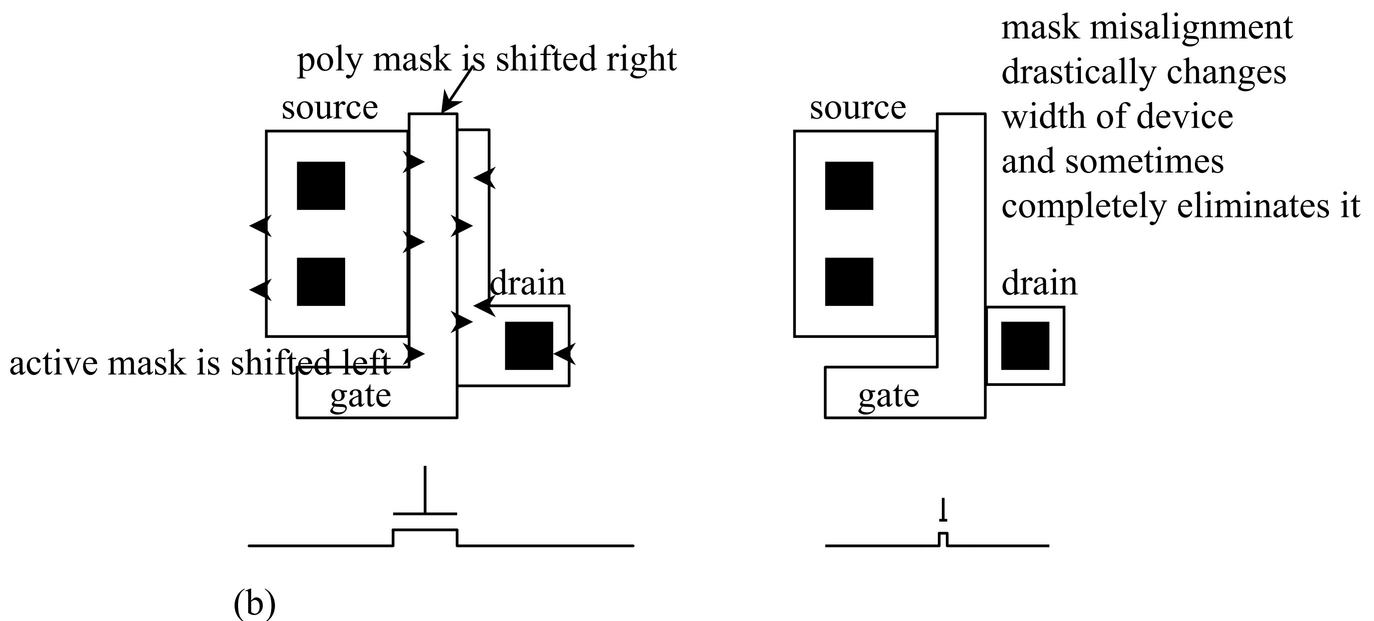




Design Rule Background

- Example: effects of insufficient gate extension and source-drain extension





Scribe Line

- Surrounds the completed chip and is the point at which the chip is cut with a diamond saw
- Where test circuits can be placed for wafer probe

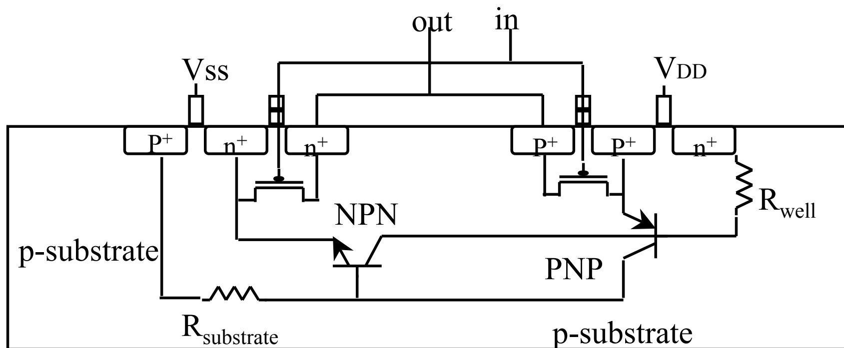
Layer Assignments

LAYER	CIFLAYER NAME	CALMANUMBER
Well	CWG	14
N-well	CWN	1
P -well	CWP	2
Active	CAA	3
Select	CSG	15
P-select	CSP	8
N-select	CSN	7
Poly	CPG	4
Poly Contact	CCP	45
Poly 2 (Electrode)	CEL	5
Electrode Contact	CCE	55
Active Contact	CCA	35
Metal1	CMF	10
Via	CVA	11
Metal2	CMS	12
Via2	CVB	65
Metal3	CMT	14
Overglass	COG	13

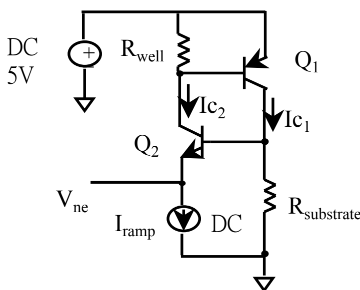
Latchup

- May occur in both p-well and n-well CMOS processes
- CMOS N-well example

— Cross section of an inverter

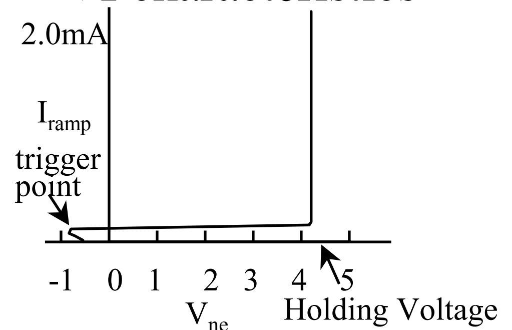


— Circuit model



latchup
=> loop gain > 1
=> $g_{m1}R_{sub}g_{m2}R_{well} > 1$
=> $(1/V_T)2(Ic_1R_{sub}Ic_2R_{well}) > 1$

— VI characteristics



(Once latched-up, this condition will be maintained until the latch-up voltage/current drops below the holding voltage/current)

- Causes
  — internal transient currents or voltages during power-up
  — external glitches on I/O pad
  — external radiation
- Triggering methods
  1. current injected into the NPN emitter
  2. current injected into the PNP emitter
  3. drastic current/voltage changes on any mode

Latchup Prevention

- Two basic concepts (for reducing loop gain)
  1. reduce R*well* and R*substrate*
  2. reduce βnpn and βpnp (i.e. reduce Ic1 and Ic2)

- Two basic ways
  1. latchup resistant CMOS process
  2. layout techniques

- Internal latchup prevention techniques
  — Every well must have a substrate contact of the appropriate type.
  — Every substrate contact should be connected to metal directly to a supply pad (i.e., no diffusion or polysilicon underpasses in the supply rails).
  — Place substrate contacts as close as possible to the source connection of transistors connected to the supply rails (i.e., Vss n-devices, VDD p-devices). This reduces the value of R*substrate* and R*well*. A very conservative rule world place one substrate contact for every supply(Vss or VDD) connection.
  — otherwise a less conservative rule is to place a substrate contact for every 5-10 transistors or every 25-100μm.
  — Lay out n- and p-transistors with packing of n-devices toward Vss and packing of p-devices toward VDD (see layout styles in Chapter5). Avoid "convoluted" structures that interwire n- and p-devices in checkerboard styles (unless you are designing in SOI which is latchup free).

Latchup Prevention (Cont.)

- I/O latchup prevention
  - —Physically separate the n- and p-driver transistors (i.e., with the bonding pad).
  - —Include P^+ guard rings connected to Vss around n-transistors.
  - —Include n^+ guard rings connected to VDD around p-transistors.
  - —Source diffusion regions of the n-transistors should be placed so that they lie along equipotential lines when current flows between Vss and the p-wells: that is, source fingers should be perpendicular to the dominant direction of current flow rather than parallel to it. This reduces the possibility of latchup through the n-transistor source, due to an effect called "field aiding."
  - —Shorting n-transistor source regions to the substrate and the p-transistor source regions to the n-well with metallization along their entire lengths will aid in preventing either or these diodes from becoming forward-biased, and hence reduces the contribution to latchup from these components.
  - —The n-well should be hard-wired (via n^+) to power so that any injected charge is diverted to VDD via a low-resistance path. The n-well has relatively high sheet-resistance and is susceptible to charge injection.
  - —The spacing between the n-well n+ and the p-transistor source contact should be kept to a minimum. This allows minority carriers near the parasitic pnp-transistor emitter-base junction to be collected, and reduces R_{well}. The rules for the 1μ process suggest one contact for every 10μ -50μ.
  - —The separation between the substrate P+ and the n-transistor source contact should be minimized. This results in reduced minority carrier concentration near the npn-emitter-base junction. Similar spacings to those suggested above apply for processes in the 1μ range.

Technology-Related CAD Issues

- Design rule check(DRC)

  --- check if layout rules are obeyed

  --- e.g. CADENCE DRACULA DRC
- Circuit extraction

  --- generate netlist from layout
  (SPICE format)

  --- can be used for post-layout simulation
  e.g. SPICE simulation

  --- can be used for layout-vs-schematic
  (LVS) check