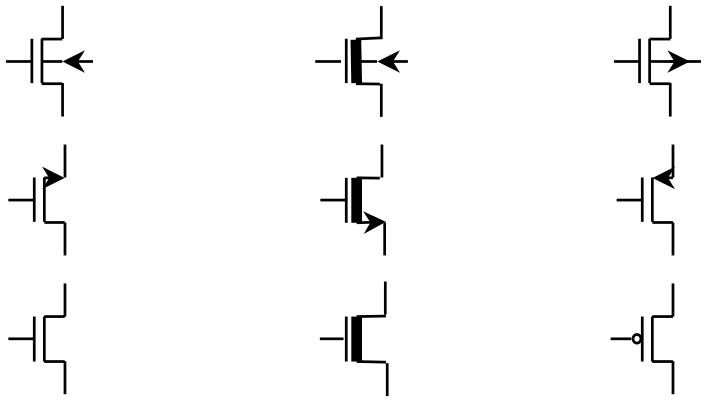
Basic Electrical Properties of MOS Circuits

- Basic MOS operation and equations
- Small-signal characteristics
- Complentary CMOS inverter (DC characteristics)
- Noise Margin
- Static load invrters and transmission gate

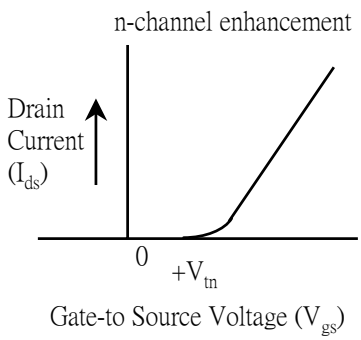
MOS Transistor Types

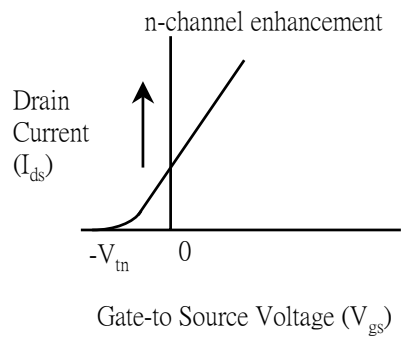
- MOS Transistor Symbol

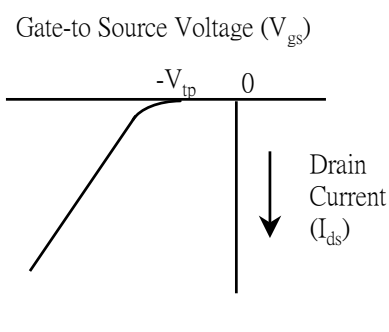


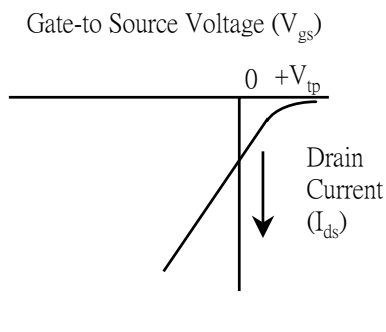
nMOS enhancement | nMOS depletion | pMOS enhancement

- Conduction characteristics for enhancement and depletion mode MOS transistors
  - Assuming fixed V_{DS}



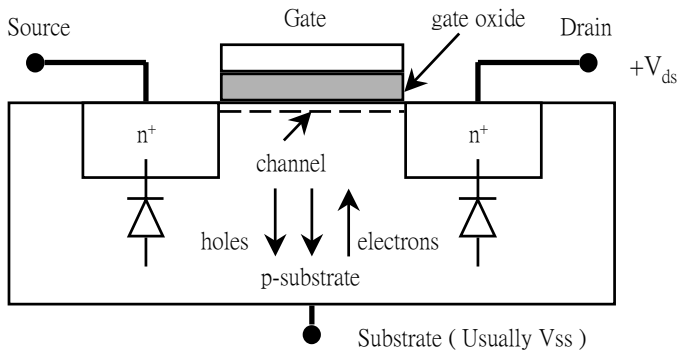




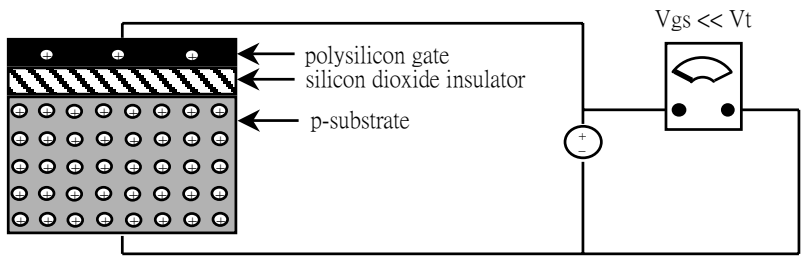


MOS Enhancement Transistor

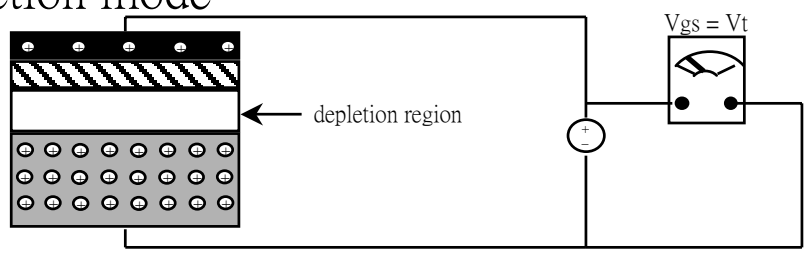
- Physical structure of a nMOS transistor



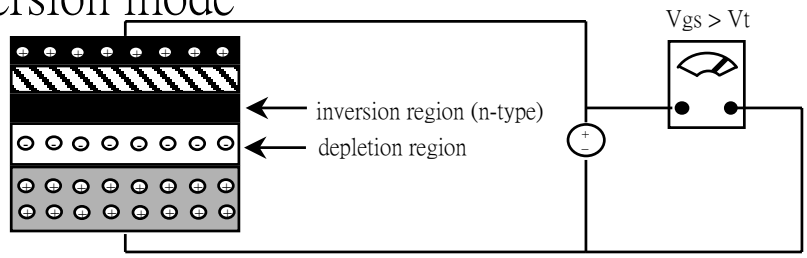
- 3 modes of transistor channel (nMOS)
  - — Accumulation mode



  - — Depletion mode



  - — Inversion mode

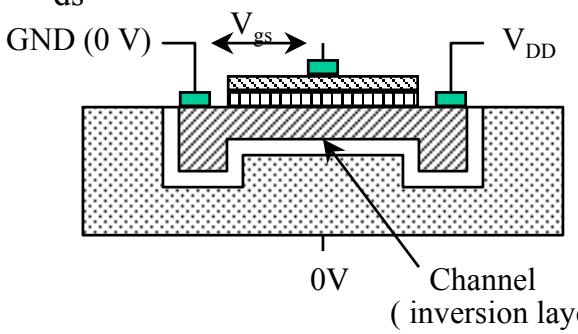


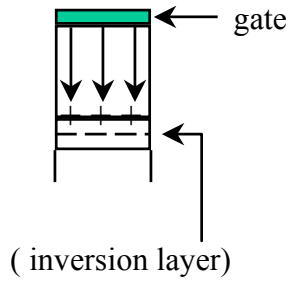
- pMOS (refer to textbook)

MOS Transistor Operation

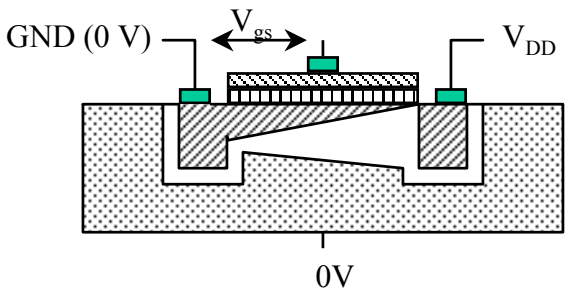
- Example : n MOS

1. $V_{gs} > V_t$, $V_{ds} = 0$

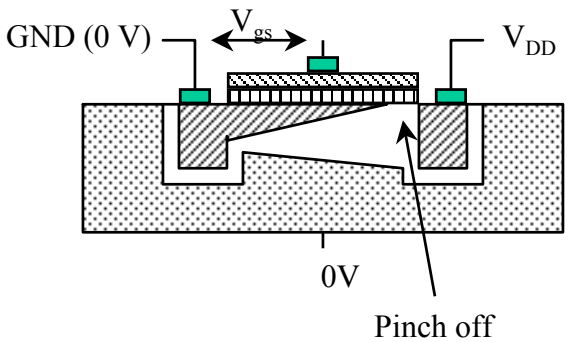




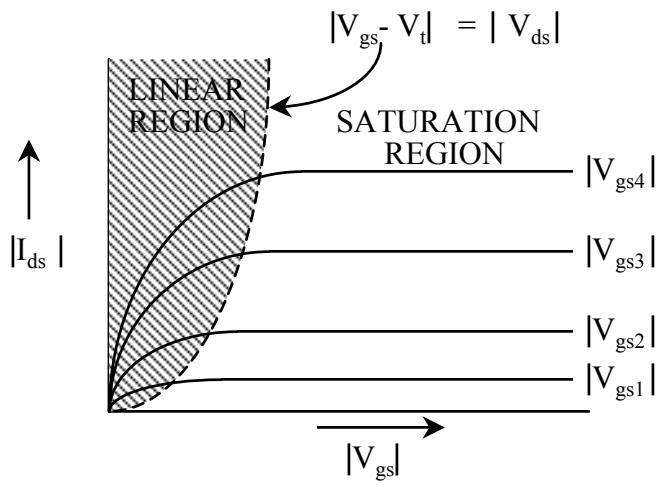
2. $V_{gs} > V_t$, $V_{gs} - V_{ds} = V_{gd} > V_t$



3. $V_{gs} > V_t$, $V_{gs} - V_{ds} = V_{gd} < V_t$



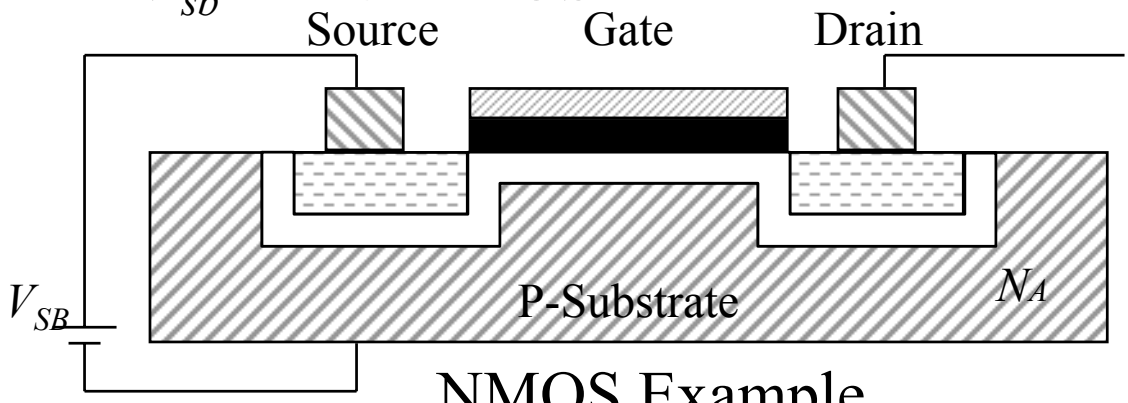
- I-V characteristic of nMOS



Body Effect

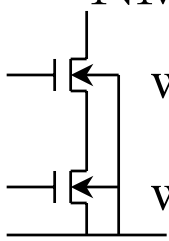
- Threshold voltage is increased when back bias voltage is increased
- Junction between channel (or drain&source) and substrate must be reverse-biased to reduce current leakage

  $V_{sb} > 0$ for NMOS
  $V_{sb} < 0$ for PMOS



NMOS Example

- Example



- $V_t = V_{fb} + 2\phi_b + \dfrac{\sqrt{2\varepsilon_{si} q N_A (2\phi_b + |V_{sb}|)}}{C_{ox}}$

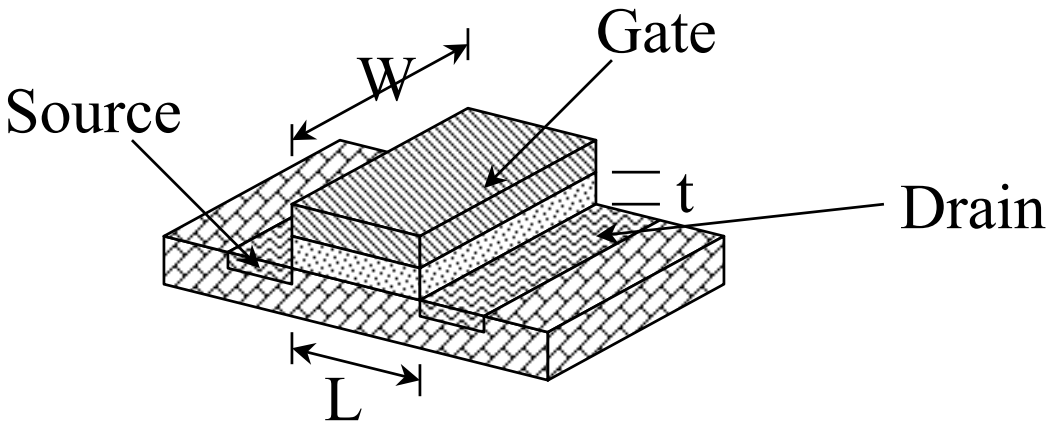
$$V_t = V_{t0} + \gamma\left[\sqrt{(2\phi_b + |V_{sb}|)} - \sqrt{2\phi_b}\right]$$

$$\gamma = \frac{t_{ox}}{\varepsilon_{ox}}\sqrt{2\varepsilon_{si} q N_A} = \frac{1}{C_{ox}}\sqrt{2\varepsilon_{si} q N_A}$$

V_{fb} : flat-band voltage ε_{ox} : permitivity of gate oxide
ϕ_b : Fermi potential
V_{sb} : substrate bias
V_{t0} : V_t for V_{SB}=0
N_A : substrate doping concentration

MOS Device Equation

- NMOS Transistor Structure



- I_{DS} VS. V_{DS} Relationship

$$I_{DS} = \frac{\text{charge induced in channel}(Q_c)}{\text{electron transit time}(\tau)}$$

$$\text{Transit time } \tau_{DS} = \frac{\text{length of channel}(L)}{\text{velocity}(\upsilon)}$$

$$\text{Velocity } \upsilon = \mu E_{DS}$$

where μ is electron or hole mobility

E_{DS} is electric field

$$E_{DS} = \frac{V_{DS}}{L}$$

$$\tau_{DS} = \frac{L^2}{\mu V_{DS}}$$

MOS DEVICE Equation(Cont.)

- Nonsaturation Region

Eg: Average electric field
(gate to channel)

ε: permittivity of insulator between gate and channel

$$Eg = \frac{(Vg-Vt)-V_{DS}/2}{t}$$; Assume average channel voltage $V_{DS}/2$

t: oxide thickness

$$Qc = \frac{\varepsilon WL}{t}\left[(Vgs-Vt)-\frac{V_{DS}}{2}\right]$$

$$I_{DS} = \frac{\mu\varepsilon}{t}\frac{W}{L}\left[(Vgs-Vt)-\frac{V_{DS}}{2}\right]V_{DS}$$

$$= \mu Cox\frac{W}{L}\left[(Vgs-Vt)-\frac{V_{DS}}{2}\right]V_{DS}$$

Cox: gate capacitance/unit area

Total gate capacitance $C_g = CoxWL$

Let $K = \mu Cox$ or $\beta = K\frac{W}{L} = \frac{\mu CoxW}{L}$

$$\Rightarrow I_{DS} = K\frac{W}{L}\left[(Vgs-Vt)V_{DS}-\frac{V_{DS}^2}{2}\right]$$

$$= \beta\left[(Vgs-Vt)V_{DS}-\frac{V_{DS}^2}{2}\right]$$

MOS Device Equation(Cont.)

- Saturation Region

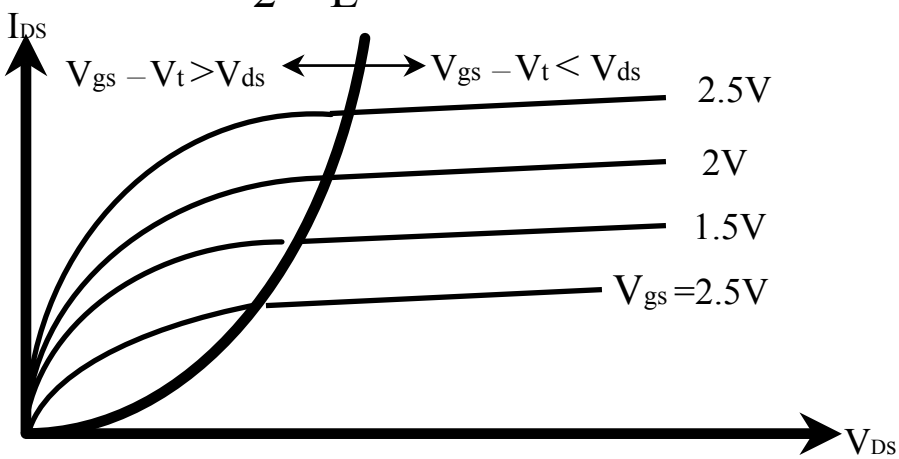
$$V_{DS}=V_{gs}-V_t$$

$$I_{DS}=\frac{k}{2}\frac{W}{L}(V_{gs}-V_t)^2=\frac{\beta}{2}(V_{gs}-V_t)^2$$

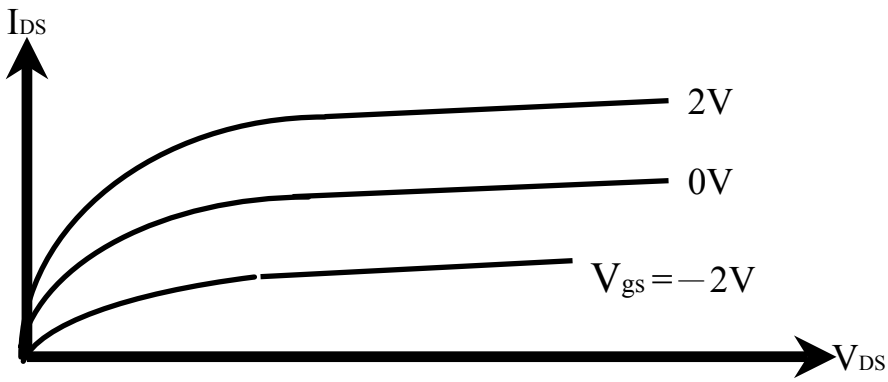
λ : channel length modulation factor

If we include λ, then

$$I_{DS}=\frac{k}{2}\frac{W}{L}(V_{gs}-V_t)^2(1+\lambda V_{DS})$$



Enhancement NMOS ($V_t > 0$)



Depletion NMOS ($V_t < 0$)

- Cutoff Region

$$V_{gs} < V_t \Rightarrow I_{DS}=0$$

MOS Device Equation(Continued)

1. Cutoff Region $V_{gs} - V_t < 0$

2. Nonsaturation $0 < V_{ds} < V_{gs} - V_t$

3. Saturation $0 < V_{gs} - V_t < V_{ds}$

$$I_{DS} = \begin{cases} 1.\ 0 \\ 2.\ \beta[(V_{gs} - V_t)V_{DS} - \dfrac{V_{DS}^2}{2}] \\ 3.\ \dfrac{\beta}{2}(V_{gs} - V_t)^2 \end{cases}$$

- Channel-length modulation

  —— Device in saturation

$$I_{DS} = \frac{\beta}{2}(V_{gs} - V_t)^2(1 + \lambda V_{DS})$$

Subthreshold Region

- i.e. weak inversion region
  $0 < V_{gs} < V_t$

Drain Puchthrough

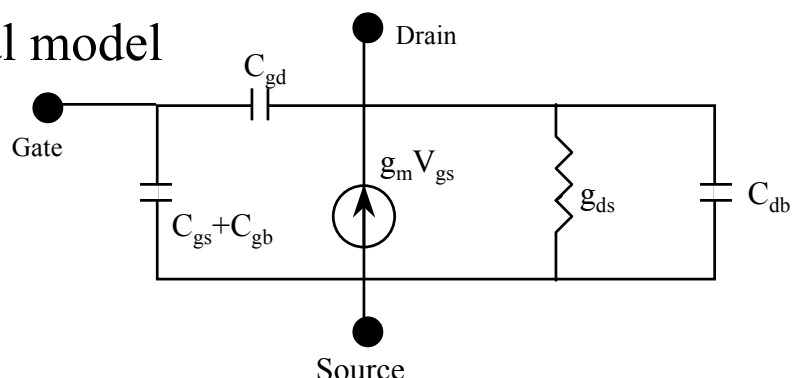
When the drain is at a high enough voltage with respect to the souce, the depletion region around the drain may extend to the source, thus causing current to flow irrespective of the gate voltage(i.e., even if it is zero). This is known as a punchthrough condition. Currently, this effect is used in I/O protection circuits to limit the voltages across internal circuit nodes, although it will impact design as devices are scaled down by requiring that internal circuit voltages be reduced to a point where the effect does not occur.

MOS Models

refer to textbook

Small Signal AC Characteristics

- small signal model



Transcondutorance g_m

- $g_m = \left. \frac{d\ I_{DS}}{d\ V_{GS}} \right|_{V_{DS} = \text{constant}}$

- For devices in saturation region

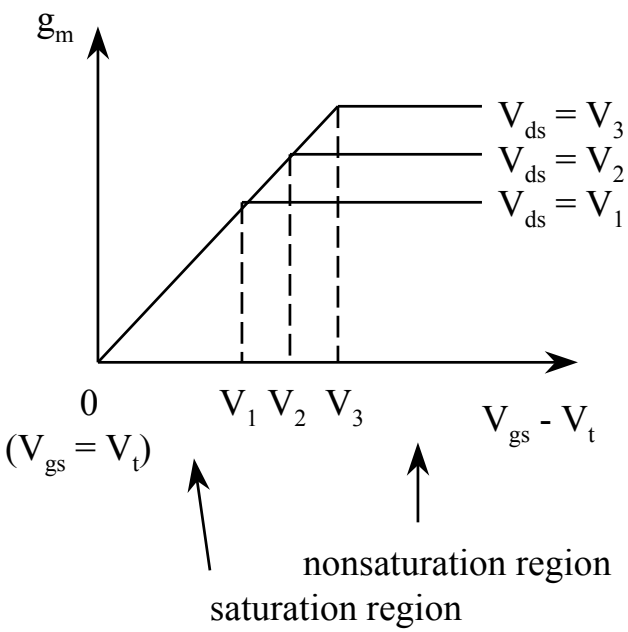
$$g_m = \frac{d\ I_{DS}}{d\ V_{GS}} = \frac{C_g\ \mu}{L^2} (V_{gs} - V_t) \ ; \ C_g = CoxWL$$

$$= \beta (V_{gs} - V_t)$$

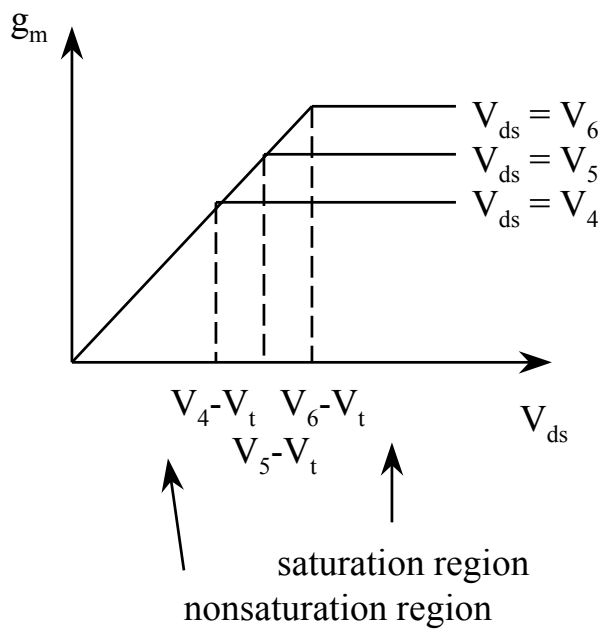
- For devices in nonsaturation region

$g_m = \beta\ V_{DS}$

- With fixed V_{ds}

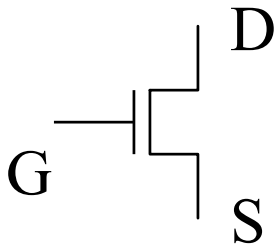


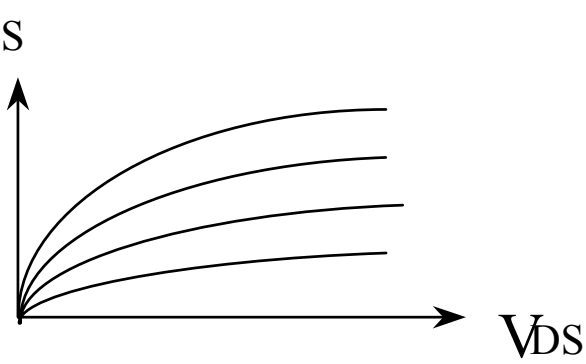
- With fixed $V_{gs} > V_t$



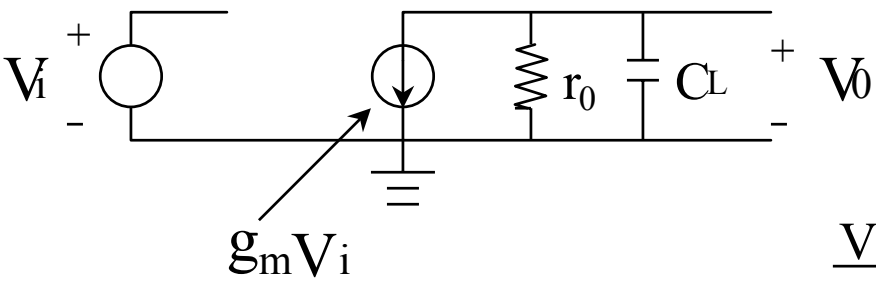
Indication of Frequency Response

- Large signal



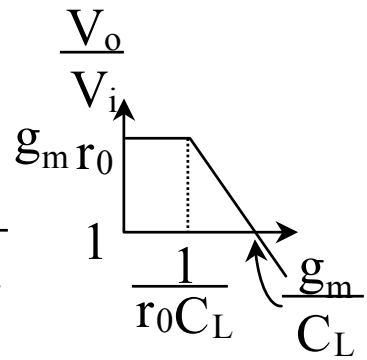


- Small signal model



$$V_0 = -g_m V_i \left(r_0 /\!/ \frac{1}{sC_L} \right)$$

$$\frac{V_0}{V_i} = \frac{-g_m r_0}{1+sr_0 C_L} = \frac{-g_m r_0}{1+j\omega r_0 C_L}$$



$$\left| \frac{V_0}{V_i} \right| = 1 \Longrightarrow \omega_u = \frac{g_m}{C_L}$$

Assume $g_m r_0 >> 1$

- $\omega_u = \dfrac{g_m}{C_g} = \dfrac{\mu}{L^2}(V_{gs} - V_t)$

Assume $C_L = C_g$ i.e. ability to drive itself

Output Resistance

- Nonsaturation
  - Small signal

$$g_0 = \left.\frac{dI_{DS}}{dV_{DS}}\right|_{V_{DS}\ \text{small}} \approx \beta(V_{gs}-V_t)$$

  - Large signal $G_0 = \frac{I_{DS}}{V_{DS}} \approx \beta(V_{gs}-V_t)$

$$\Rightarrow R_0 = r_0 = \frac{1}{\beta(V_{gs}-V_t)}$$

$$\frac{1}{G_0} \quad \frac{1}{g_0}$$

- Saturation Region

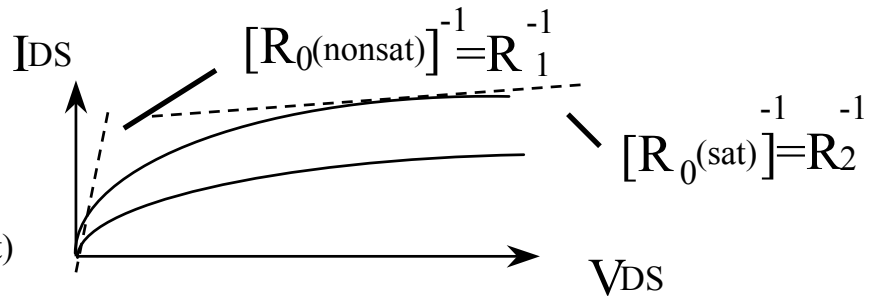
  *Only small signal

$$g_0 = \frac{dI_{DS}}{dV_{DS}} = \lambda I$$

$$r_0 = \frac{1}{\lambda I}$$

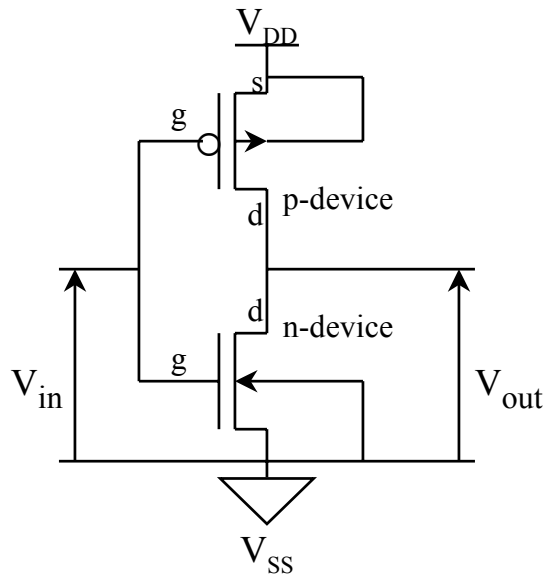
- $R_2 > R_1$

$r_{0(sat)}$ $R_{0(nonsat)}$



Complementary CMOS Inverter

- A MOS inverter with substrate connections

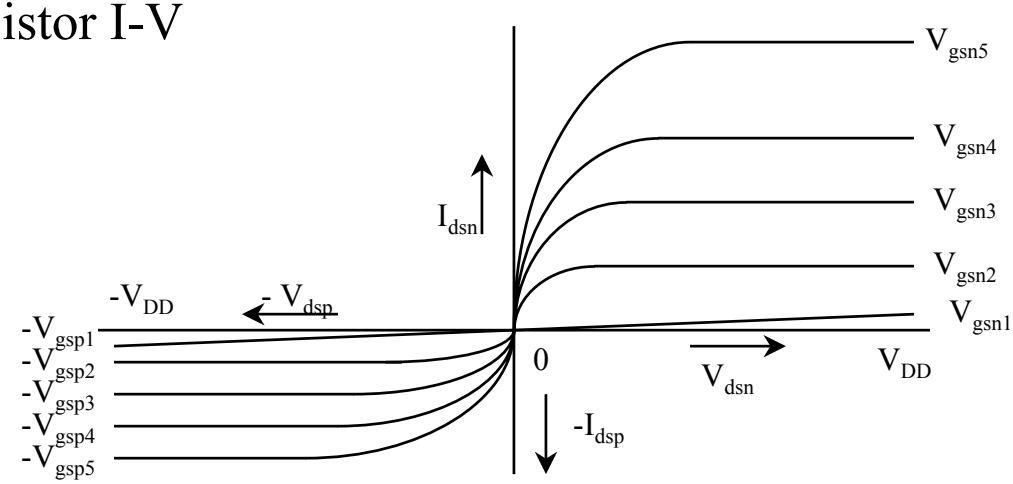


- Relations between voltages for the three regions of operation of a CMOS inverter

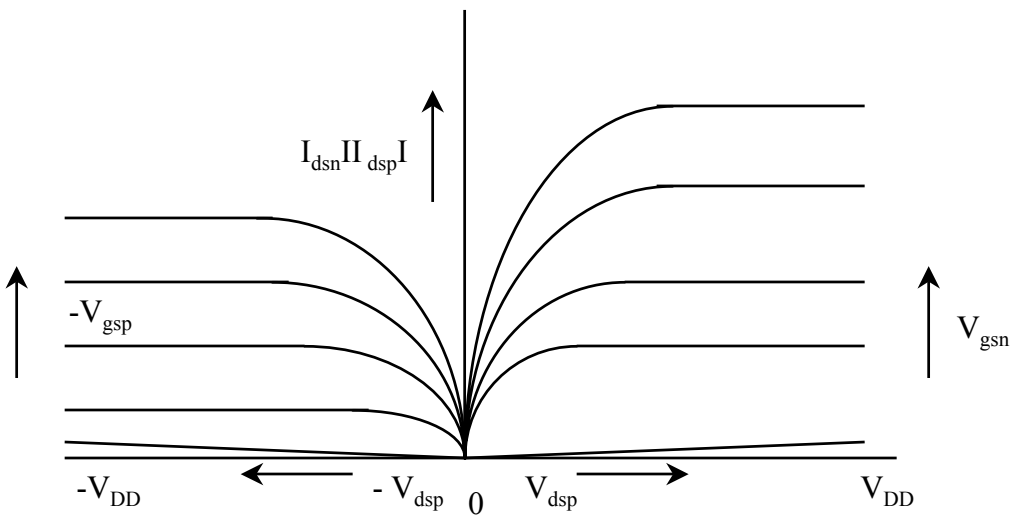
	CUTOFF	NONSATURATED	SATURATED
p-device	$V_{gsp} > V_{tp}$ $V_{in} > V_{tp} + V_{DD}$	$V_{gsp} < V_{tp}$ $V_{in} < V_{tp} + V_{DD}$ $V_{dsp} > V_{gsp} - V_{tp}$ $V_{out} > V_{in} - V_{tp}$	$V_{gsp} < V_{tp}$ $V_{in} < V_{tp} + V_{DD}$ $V_{dsp} < V_{gsp} - V_{tp}$ $V_{out} < V_{in} - V_{tp}$
n-device	$V_{gsn} < V_{tn}$ $V_{in} < V_{tn}$	$V_{gsn} > V_{tn}$ $V_{in} > V_{tn}$ $V_{dsn} < V_{gs} - V_{tn}$ $V_{out} < V_{in} - V_{tn}$	$V_{gsn} > V_{tn}$ $V_{in} > V_{tn}$ $V_{dsn} > V_{gs} - V_{tn}$ $V_{out} > V_{in} - V_{tn}$

Graphical Derivation of CMOS Inverter Characteristics

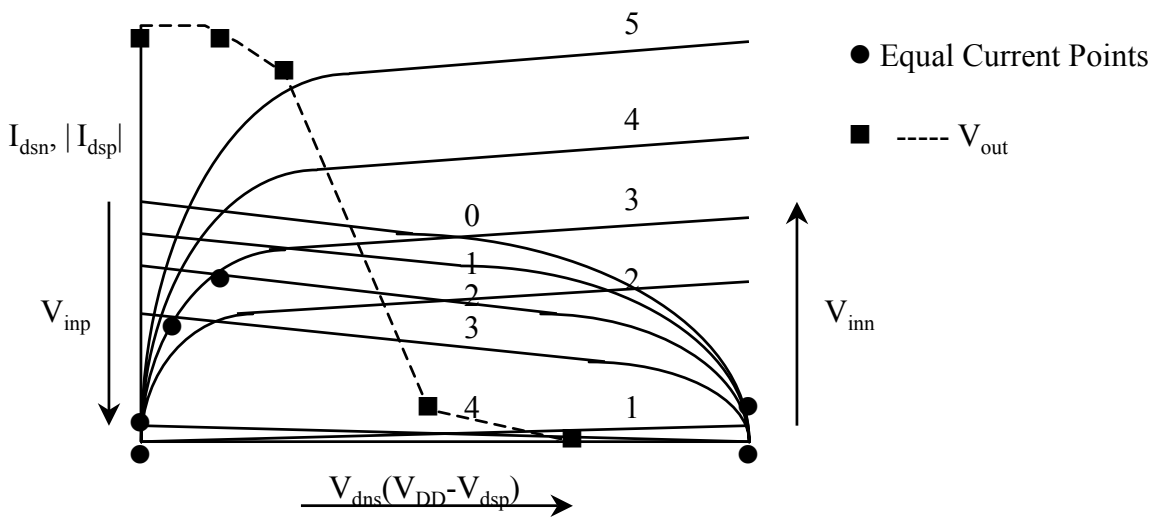
- transistor I-V



- Taking absolute value of I_{dsp}

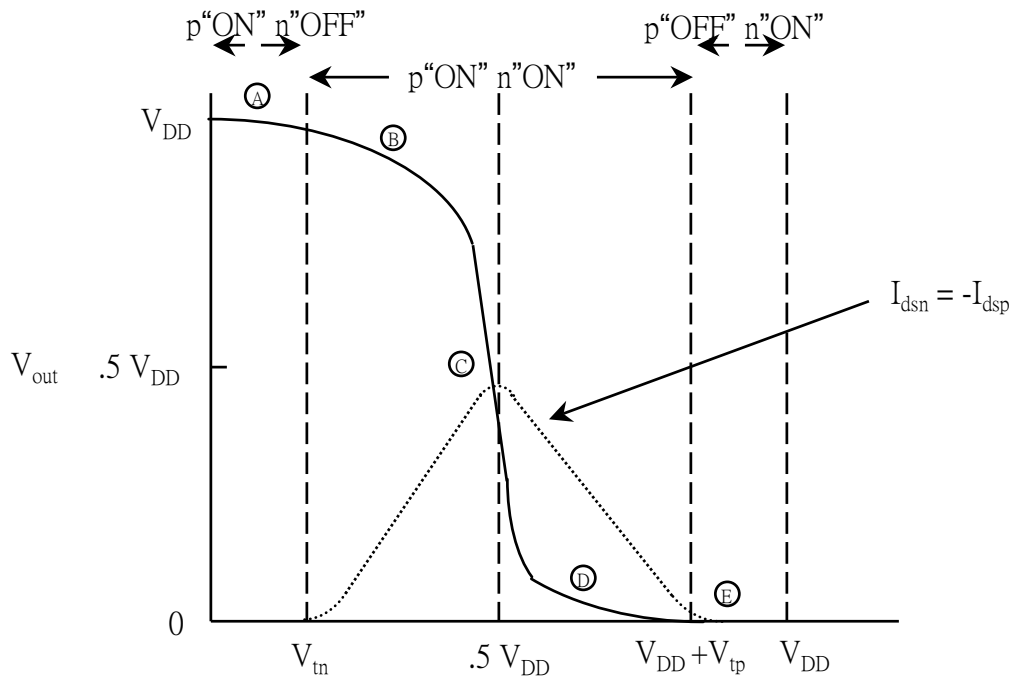


- Load line



CMOS Inverter DC Transfer Characteristic and Operating Regions

- Transfer curve



- 5 regions (A, B, C, D, and E)
  - In all of five regions, $I_{dsn} = -I_{dsp}$
  - Region A

    $V_{out} = V_{DD}$
    nMOS: off
    pMOS: nonsaturation (triode) region

— Region B: n: saturation p: nonsaturation

$$I_{dsp} = \frac{\beta_n}{2}(V_{in} - V_{tn})^2$$

$$I_{dsp} = -\beta_p[(\underbrace{V_{in} - V_{DD}}_{V_{gsp}} - V_{tp})(\underbrace{V_O - V_{DD}}_{V_{dsp}}) - \frac{1}{2}(V_O - V_{DD})^2]$$

$$I_{dsn} = -I_{dsp}$$

$$\Rightarrow V_O = [(V_{in} - V_{tp}) + [(V_{in} - V_{tp})^2 - 2(V_{in} - \frac{V_{bb}}{2} - V_{tp})V_{DD} - \frac{\beta_n}{\beta_p}(V_{in} - V_{tn})^2]^{1/2}$$

— Region C: Both the n and p-device are in saturation

$$I_{dsp} = \frac{\beta_p}{2}(V_{in} - V_{DD} - V_{tp})^2$$

$$I_{dsp} = \frac{\beta_n}{2}(V_{in} - V_{tp})^2$$

$$I_{dsp} = -I_{dsn}$$

$$\Rightarrow V_{in} = \frac{V_{DD} + V_{tp} + V_{tn}\sqrt{\frac{\beta_n}{\beta_p}}}{1 + \sqrt{\frac{\beta_n}{\beta_p}}}$$

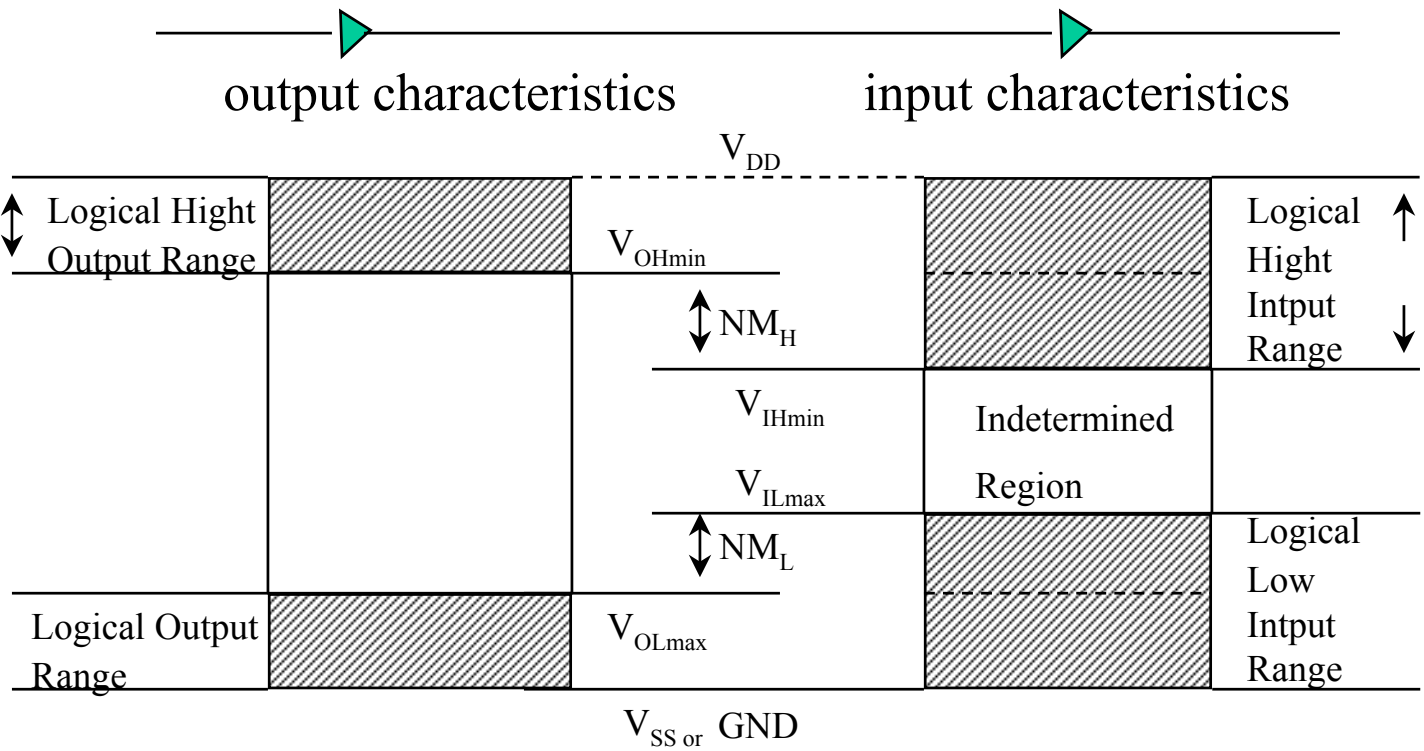
By setting $\beta_n = \beta_p$ and $V_{tn} = -V_{tp}$

$\Rightarrow V_{in} = \frac{V_{DD}}{2} = V_O = V_{inv}$ where V_{inv} is gate threshold voltage

— Region D & E can be similarly derived

Noise Margin

- Definitions



$$NM_L = | V_{ILmax} - V_{OLmax} |$$

$$NM_H = | V_{OHmin} - V_{IHmin} |$$

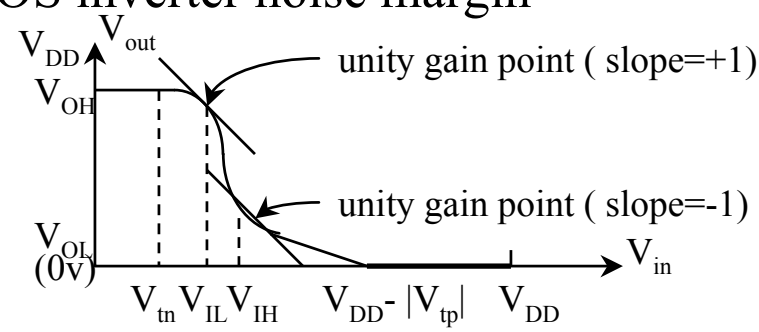
V_{IHmin} = Minimum HIGH input voltage

V_{ILmax} = Maximum LOW input voltage

V_{OHmin} = Minimum HIGH output voltage

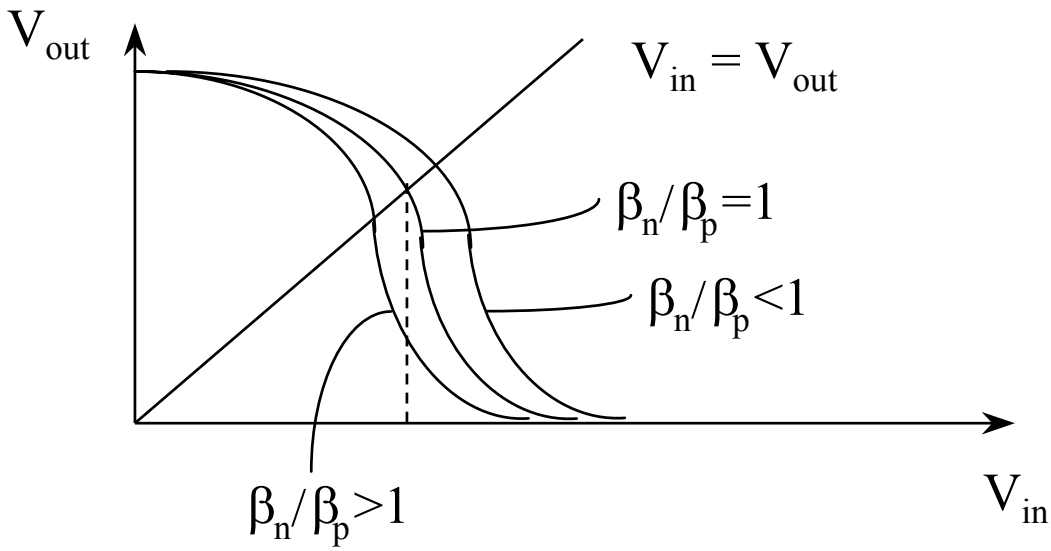
V_{OLmax} = Maximum LOW output voltage

- CMOS inverter noise margin



Influence of β_n/β_p Ratio on Transfer Curve

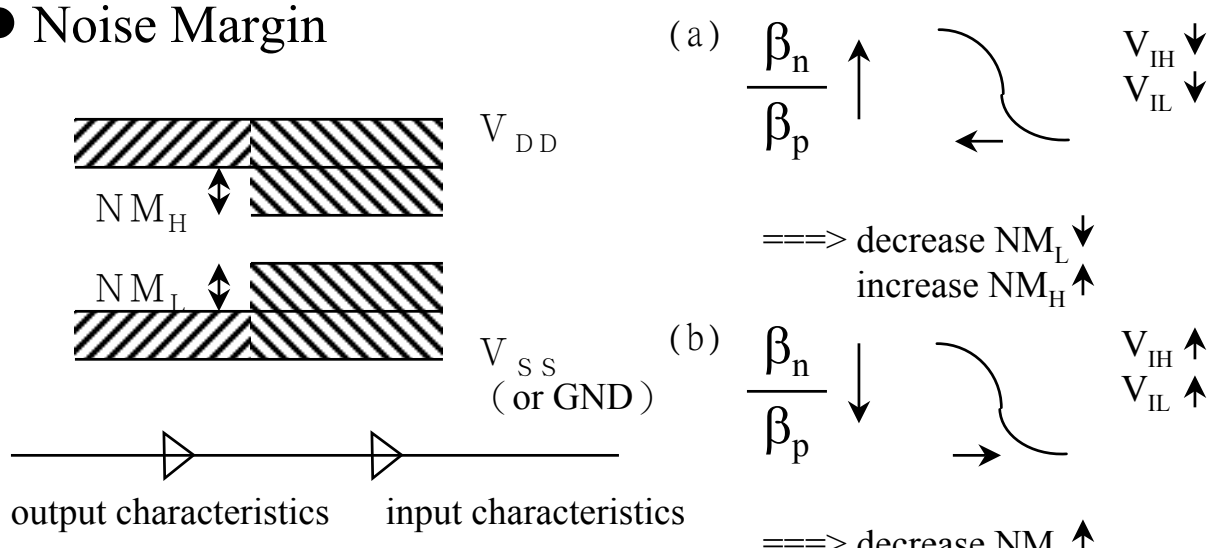
- Transfer curves for defferent β_n/β_p ratio



- For $\dfrac{\beta n}{\beta p} = 1 \Longrightarrow \dfrac{\mu pWp}{Lp} = \dfrac{\mu nWn}{Ln}$

$$\Longrightarrow \frac{(Wp/Lp)}{(Wn/Ln)} = \frac{\mu n}{\mu p} \approx 2\sim 3$$

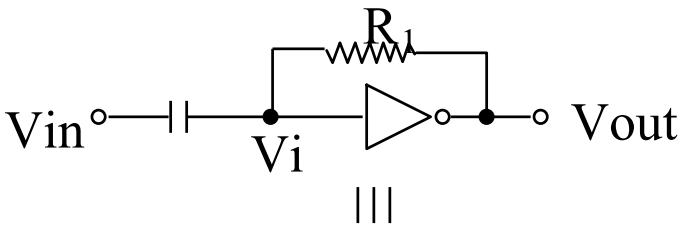
- Noise Margin

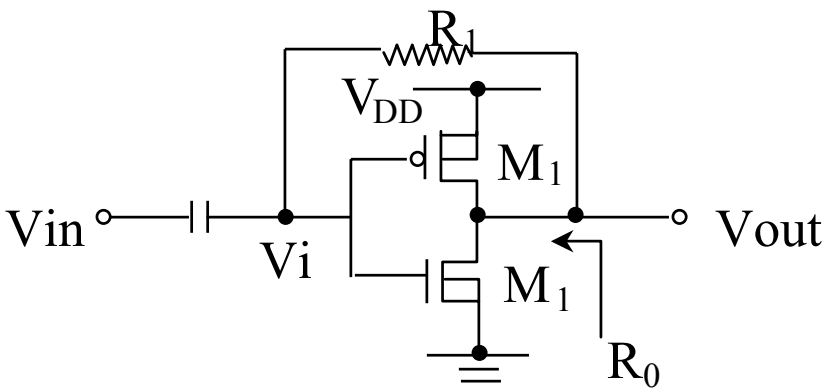


- For equal noise margins, $NM_H = NM_L$
  $V_{inv} = 0.5V_{DD}$

CMOS Inverter As An Amplifier

- Schematic





— DC bias: Vi=Vout=Vinv.

— both M_1 and M_2 are biased in saturation region

— Assuming $R_1 >> R_0$, C is large enough

$$A = \frac{Vout}{Vin} \approx \frac{Vout}{Vi} \approx GmR_0$$

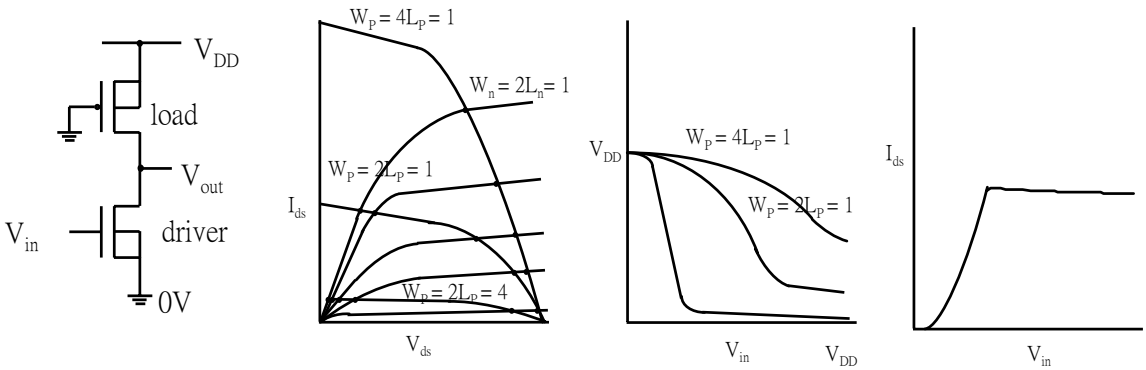
$$= (g_{mn} + g_{mp})(r_{dsn} /\!/ r_{dsp})$$

— Increase channel length => $\begin{cases} R_0 \nearrow \Rightarrow A \nearrow \\ W_u \swarrow \Rightarrow \text{speed} \swarrow \end{cases}$

$$\left(\begin{array}{l} \lambda \sim 1/L \text{ , } R_0 \sim 1/\lambda \Rightarrow R_0 \sim L \\ W_u \sim 1/L^2 \Rightarrow \text{ speed} \sim 1/L^2 \end{array} \right)$$

Pseudo - nMOS Inverter

- Roughly eqivalent to nMOS depletion load inverter
  — consumes more power than CMOS



- V_{in} = logic 0 $\Rightarrow V_{out} \approx V_{DD}$

- V_{in} = logic 1

$$\frac{\beta_n}{2}\left(V_{in}-V_{tn}\right)^2=\beta_p\left[\left(-V_{DD}-V_{tp}\right)\left(V_{out}-V_{DD}\right)-\frac{\left(V_{out}-V_{DD}\right)^2}{2}\right]$$

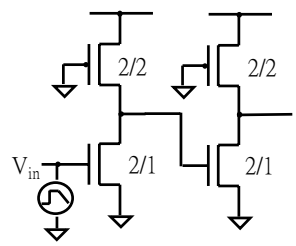
$$\Rightarrow \frac{\beta_n}{\beta_p}=\frac{\left(V_{DD}+V_{tp}\right)^2-\left(V_{out}+V_{tp}\right)^2}{\left(V_{in}-V_{tn}\right)^2}$$

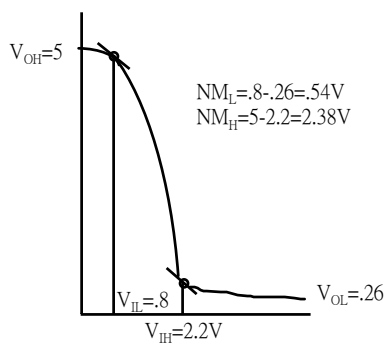
— with $V_{inv.}=0.5V_{DD}, V_{tn}=\left|V_{tp}\right|=0.2V_{DD}, V_{DD}=5V$

$$\Rightarrow \frac{\beta_n}{\beta_p} = 6$$

$$(1)\ \text{for}\ \frac{\mu_n}{\mu_p} = 2 \Rightarrow \frac{\left(\frac{W}{L}\right)_n}{\left(\frac{W}{L}\right)_p} = 3$$

$$(2)\ \text{for}\ \frac{\mu_n}{\mu_p} = 3 \Rightarrow \frac{\left(\frac{W}{L}\right)_n}{\left(\frac{W}{L}\right)_p} = 2$$

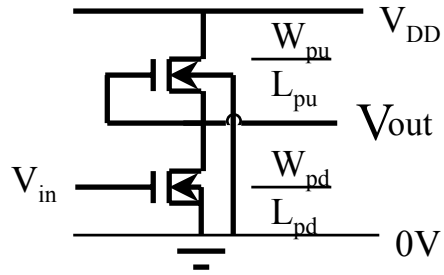




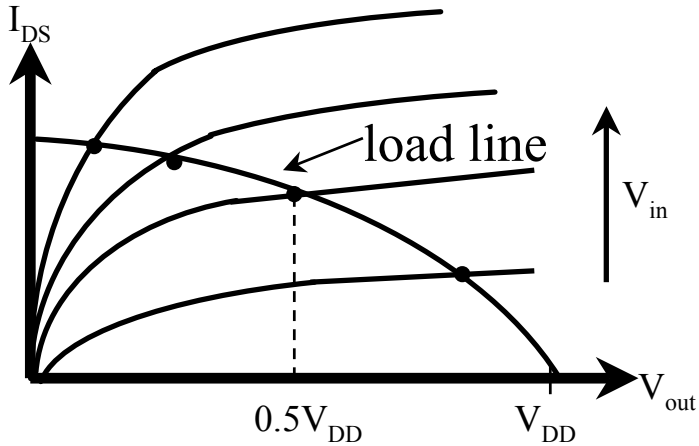
- In general, $NM_H > NM_L$

nMOS Depletion Load Inverter

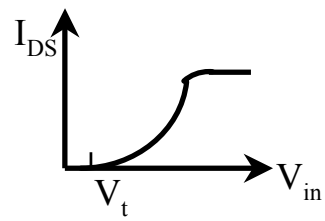
- Schematic



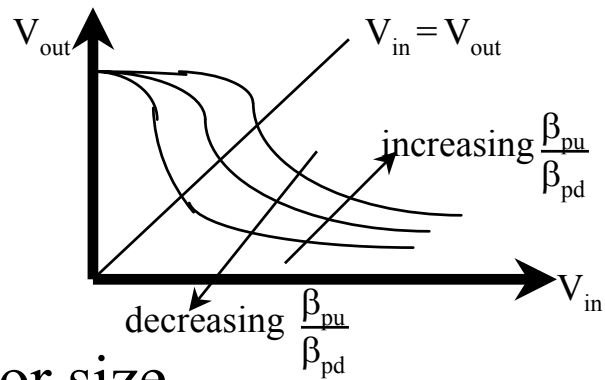
- Load line



- Consumes more power than CMOS



- Transfer cruve



- Transistor size
  - Assuming $V_t \cong 0.2V_{DD}$, $V_{td} \cong -0.6V_{DD}$

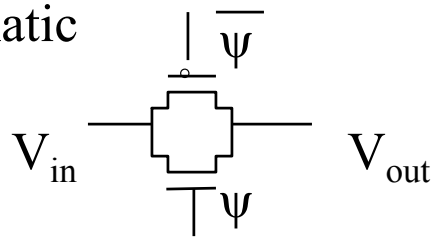
$$I_{ds(pu)} = \frac{k}{2}\frac{W_{pu}}{L_{pu}}(-V_{td})^2 = \beta_{pu}(-V_{td})^2$$

$$I_{ds(pd)} = \frac{k}{2}\frac{W_{pd}}{L_{pd}}(V_{inv.} - V_{td})^2 = \beta_{pd}(V_{inv.} - V_{td})^2$$

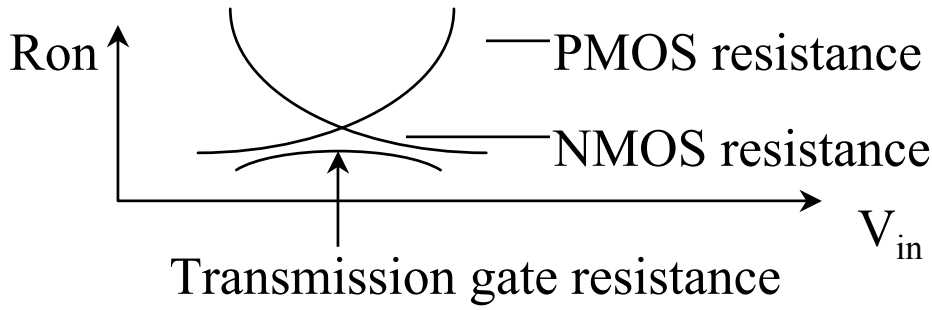
  - For $V_{inv} \simeq 1/2\ V_{DD}$, $\frac{W_{pu}/L_{pu}}{W_{pd}/L_{pd}} = \frac{1}{4}$ or $\frac{1/4}{1/1}$

Transmission Gate

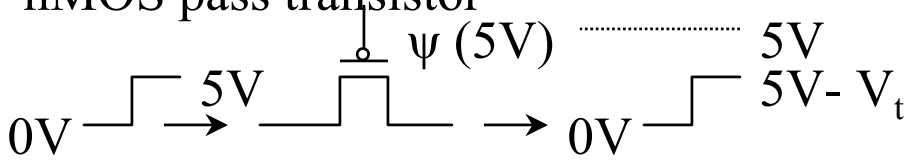
- Schematic



- Resistance (ϕ=High)

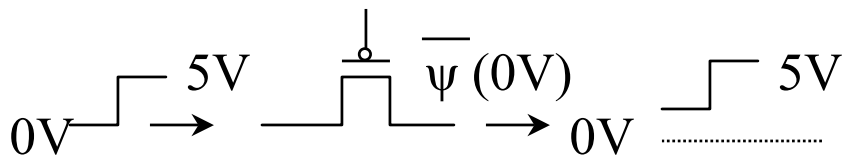


- Signal transmission
  - nMOS pass transistor



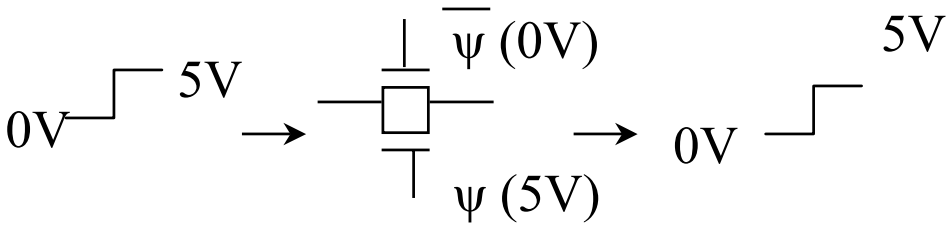
(degraded logic 1)

  - pMOS pass transistor



(degraded logic 0)

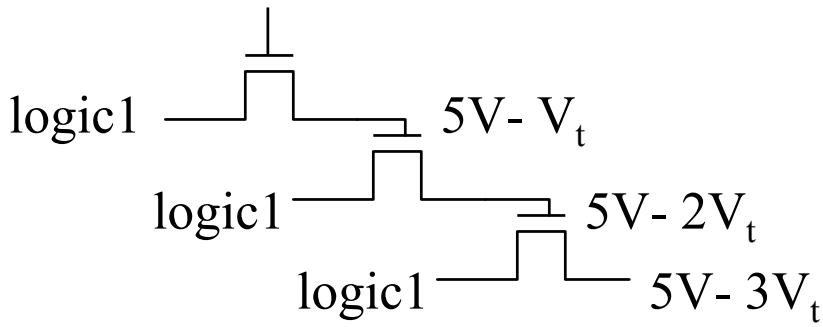
  - Transmission gate



(good logic levels)

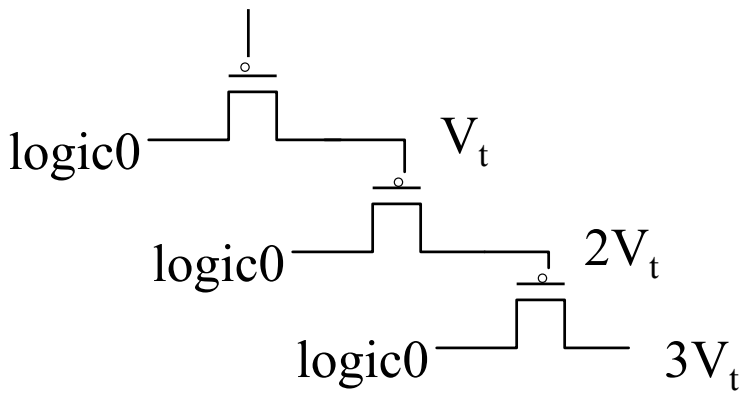
Transmission Gate (cont.)

- Cascaded stage
  - nMOS



(loss of logic level 1)

  - pMOS



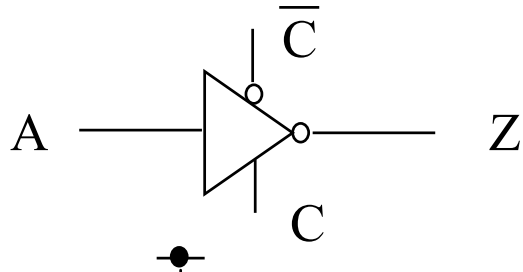
(loss of logic level 0)

  - Transmission gate

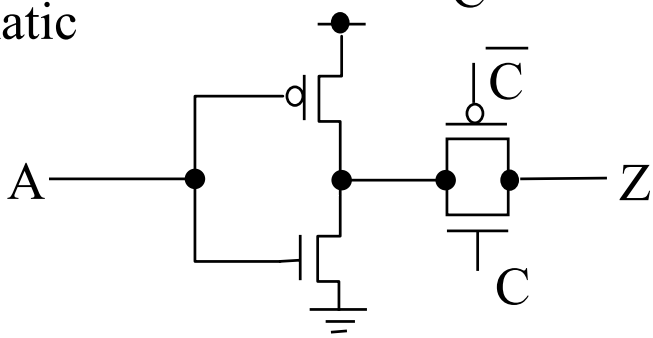
    good logic levels

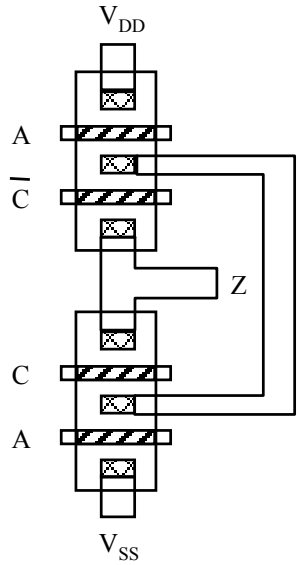
Tristate Inverter

- Symbol



- Schematic

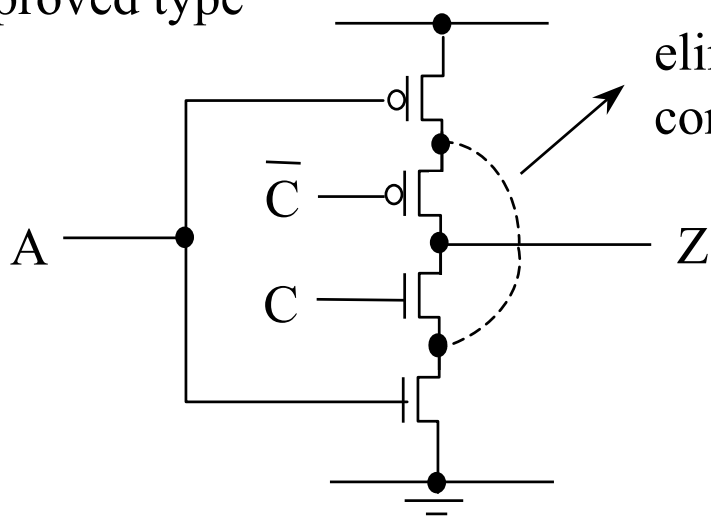


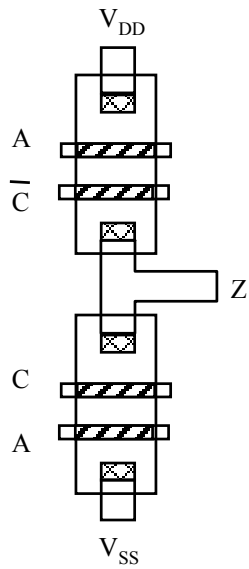


--- C=1, $\overline{C}$=0 ===> inverter function Z=$\overline{A}$

--- C=0, $\overline{C}$=1 ===> high impedance output Z

- Improved type





— eliminate a metal connection

===> smaller size & higher speed

Other Inverter Types

Reading Assignment