BiCMOS Circuit Design

1. Introduction to BiCMOS
2. Process, Device, and Modeling
3. BiCMOS Digital Circuit Design
4. BiCMOS Analog Circuit Design
5. BiCMOS Subsystems and Practical Considerations

Introduction to BiCMOS

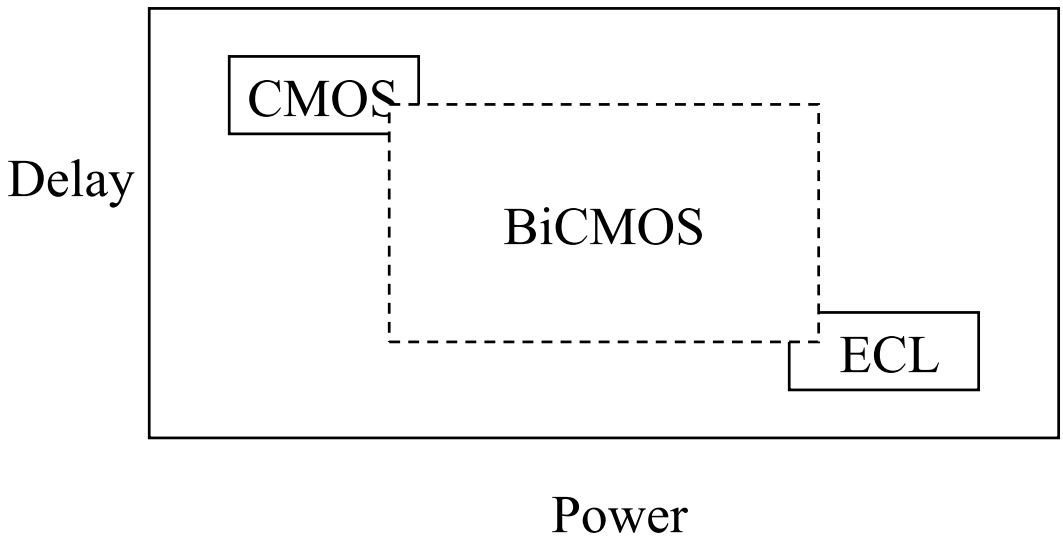
- BiCMOS Characteristics
- Advantages of BiCMOS
- Drawbacks of BiCMOS
- BiCMOS Evolution
- BiCMOS Technology
- BiCMOS Applications
- Summary

BiCMOS Characteristics

- Bipolar and MOS transistors are fabricated in a chip
- Advantages of bipolar and CMOS circuits can be retained in BiCMOS chips
- BiCMOS technology enables high performance integrated circuits ICs but increases process complexity

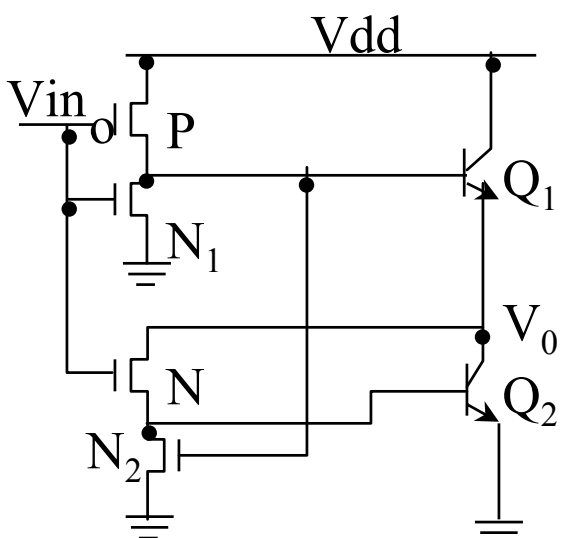
BiCMOS Characteristics (cont)

- Delay and power



- First BiCMOS circuit (An inverter)

  －proposed by Hung-Chung Lin in 1969



BJT & CMOS Advantages

- CMOS over BJT
  - Power dissipation
  - Noisee margin
  - Packing density
  - Ability to integrate large and complex circuits and functions with high yield
  - Good switch

- BJT over CMOS
  - Switching speed
  - Current drive per unit area
  - Noise performance no 1/f noise
  - Analog capability
  - I/O speed
  - High transconductance

BiCMOS Circuit Advantages

- Improved speed over CMOS
- Lower power dissipation over BJT (Simplifies packing and board requirements)
- Flexible I/O (ECL, CMOS, or TTL)
- High performance analog
- Latchup immunity
- High impedance input (FET)
- High gain (BJT)
- Low 1/f noise
- >1 GHz toggle frequency

BiCMOS Circuit Advantages (Cont.)

- Low input offset voltage for differential pair
- Zero offset analog switches
- Gain-bandwidth product extended
- Good voltage reference

Drawbacks of BiCMOS

- Add process complexity
  - — higher cost
  - — longer fabrication cycle time

BiCMOS process	BiCMOS process
‖	‖
CMOS process	Bipolar process
+	+
Buried layer & Epi	Well
+	+
?	Gate Oxide & Poly
	+
	LDD

- Technology choice: BiCMOS
  Market choice: not necessarily

BiCMOS Evolution

> 1st generation (1969 - mid 1970s)

- 1st publication in 1969 (by H.C. Lin)
- BiCMOS OPAMPs by RCA in the mid 1970s

> 2nd generation (1970s - mid 1980s)

- Smart power (major product):

  high current (>20A)

  high voltage (>500V)
- high voltage BiCMOS at Standford
- BiDEFT (combined CMOS, bipolar, and high voltage lateral DMOS transistor)

  Applications: display drivers, voltage regulators

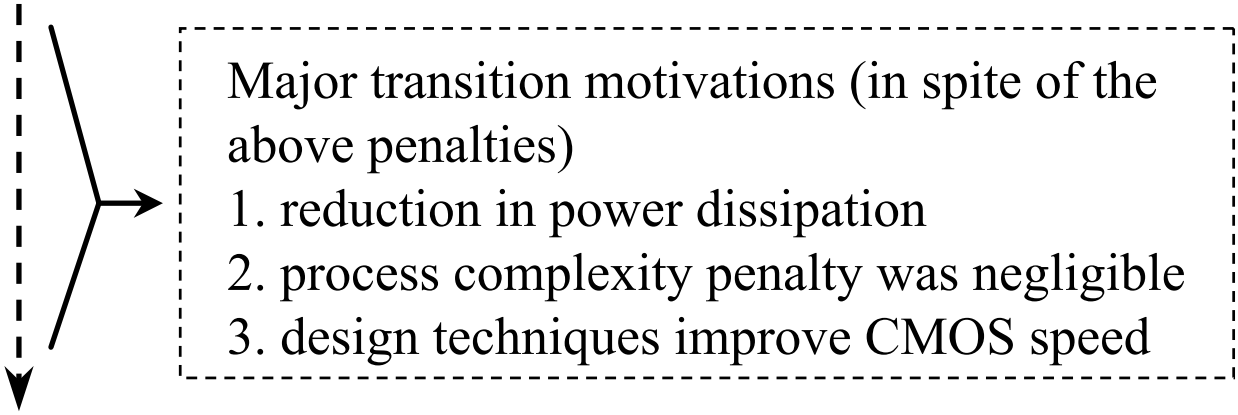
> 3rd generation (mid 1980s - present)

- 5V digital BiCMOS (major)
- Motivated by:

  1. power dissipation constraints of BJT
  2. speed limitations of MOSFET
  3. repuirements for higher I/O throughput
- Major players: Hitachi, Motorola, GE, NEC, SGS, National, TI
- Major products: memory, smart power, μPs

Evolution of High Performance Digital MOSFET Related Technology

- 1970s NMOS dominates
  - claimed that CMOS was too slow, too complex & too area intensive to be competitive



- 1980s CMOS dominates
  - claimed that BiCMOS required added process complexity
- 1990s CMOS & BiCMOS will share domination
  - BiCMOS could be the right choice
    1. if greater performance was required
    2. as CMOS process complexity increased, the percentage difference between CMOS and BiCMOS mask steps decreased

BiCMOS Device Technology

- Optimal device parameters are driven by circuit performance

- Three key circuit performance parameters
  a. speed
  b. power dissipation
  c. noise margin

- Circuit parameters depend on device parameters while device parameters depend on process parameters
  — device parameters:
    e.g. saturation current, capacitance
  — process parameters:
    e.g. oxide thickness, channel length, bulk doing, basewidth, epitaxial layer profile,emitter width.

- Technology challenges
  —optimization of impurity profiles between bipolar and CMOS transistors

BiCMOS Process Technology

- Three groups
  1. High performance(high speed)
     —receiving the most attention
     (e.g. short channel)
  2. Low cost (only NPN)
  3. Analog compatible
     —e.g. high voltage
     precision resistors and capacitors
     high performance PNPs

- Comparison of process characteristics

Step	CMOS	H.Perf.	BiCMOS low Cost	Analog	Bipolar
Masks	12	15	13	16	13
Etches	11	12	11	12	11
Epi	Optional	Required	Optional	Required	Required
Furnace	16	19	16	19	16
Implant	8	12	9	13	7
Metal	2	2	2	2	2
Total	49	61	51	63	50

* Epitaxy is an expensive and defect added step.

BiCMOS Applications

- Mixed analog/digital systems
  - use bipolar analog for high performance
  - use CMOS digital for high-density and low-power

- High density , high speed RAMs
  - use MOS cells
  - use BiCMOS sense amps. and peripheral circuits

- High performance microprocessor

- Gate array

- Flash A/D converters
  - use bipolar comparators
    1. high speed
    2. low offset
    3. low power
  - use CMOS encoding logic
    1. hgh density
    2. low power

SUMMARY

- Advantages:
  - BiCMOS technology significantly enhances speed performance while incuring negligible power and area penalty
  - BiCMOS can provide applications with CMOS power and densities at speeds which were previously the exclusive domain of bipolar
  - The concept of a “system on a chip” becomes a reality with BiCMOS
- Disadvantages:
  - Greater process complexity
  - Higher cost
  - 1.25-1.4 times increase in die cost over conventional CMOS
  - Takin into account packaging and testing costs, the total manufacturing costs of supplying a BiCMOS chip ranges from 1.1-1.3 times that of CMOS

SUMMARY (Cont.)

- Facts:

  — The extra cost incurred in developing a BiCMOS technology is more than offset by the fact that the enhanced chip performance obtained extends the usefulness of manufacturing equipment and clean rooms by at least one technology generation

  — For current BiCMOS technology(e.g. > 0.5 μm), it will extend the conventional |5V|TTL and ECL interfaces, thereby maintain the investment in 5V system

- From the above descriptions, one can see that BiCMOS will have a significant impact on the IC industry