Process, Device, and Modeling

- Process
  - CMOS
  - BiCMOS
- Device Models
  - Large signal model
  - Small signal model
- Comparison of BJT & MOSFET
  - Transconductance
  - Intrinsic gain
  - Frequency response
  - Matching
  - Other parameters

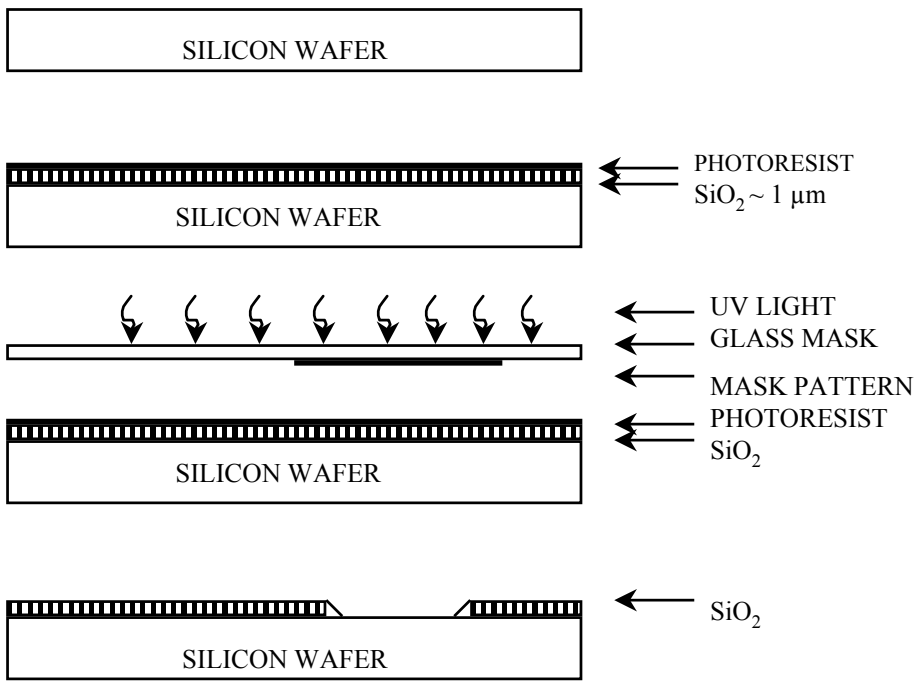
BiCMOS Process

- CMOS based BiCMOS
  (driven from a CMOS processing base)

  — Digital BiCMOS circuits tend to be CMOS-intensive because of power dissipation limitations(e.g. RAMs, uPs, gate arrays,..., etc.)
  => hightest possible CMOS performance
  — Analog BiCMOS circuits are most often combined with large digital circuit
  => results in CMOS-oriented
  — Extra steps required for BJT fabrication (e.g. isolation structure) have been introduced with only minimal changes to the actual CMOS transistor fabrication sequence

- Process commonality between the bipolar and CMOS flows has been adopted whenever possible

Device Patterning



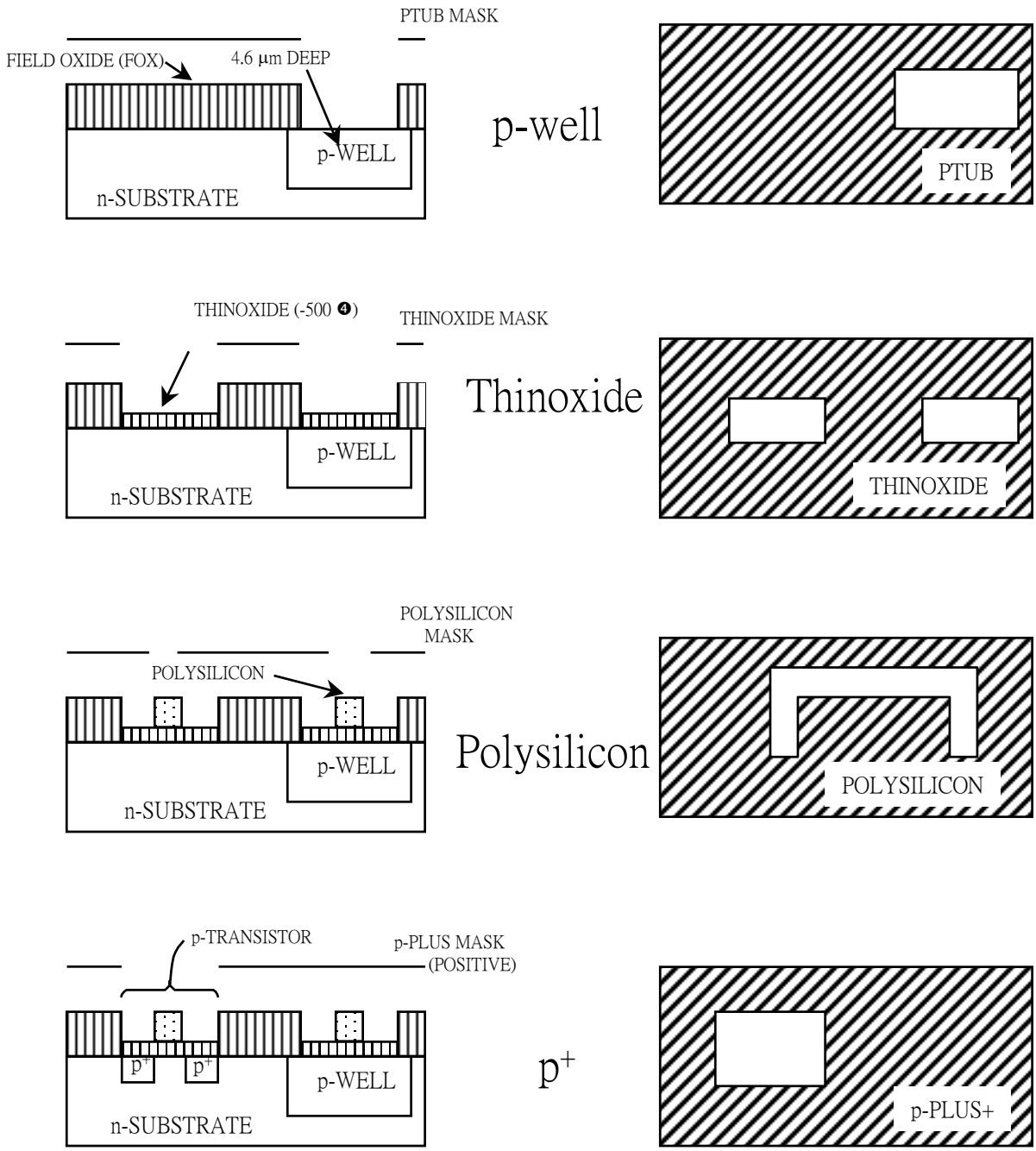
Photoresists

- NEG - first historically
- POS - better for dimensions < 2.5um
- NEG - insoluble where exposed
- POS - soluble where exposed

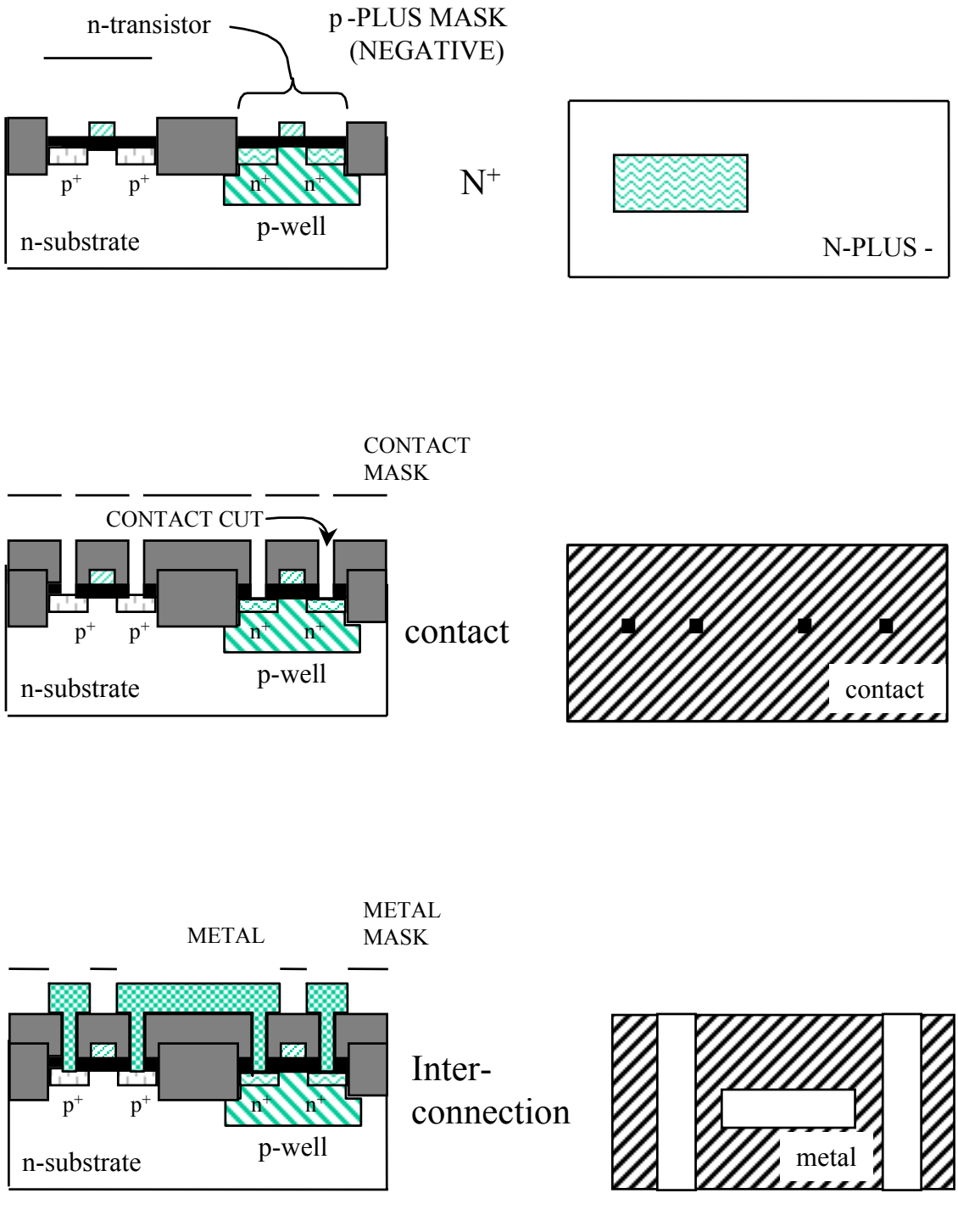
CMOS P-well Process Flow

Cross section of physical structure (side View)

Mask (Top View)

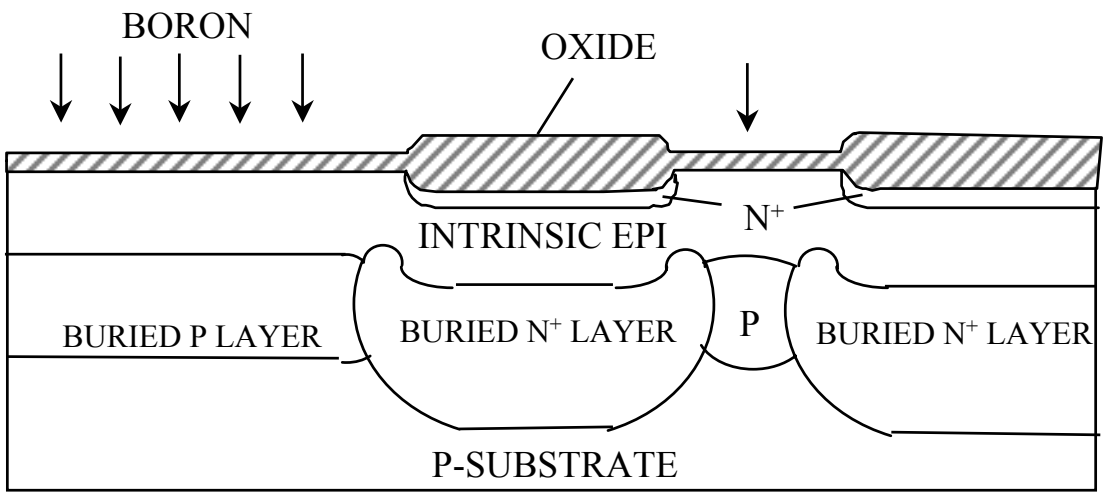


CMOS P-well Process Flow (Continued)

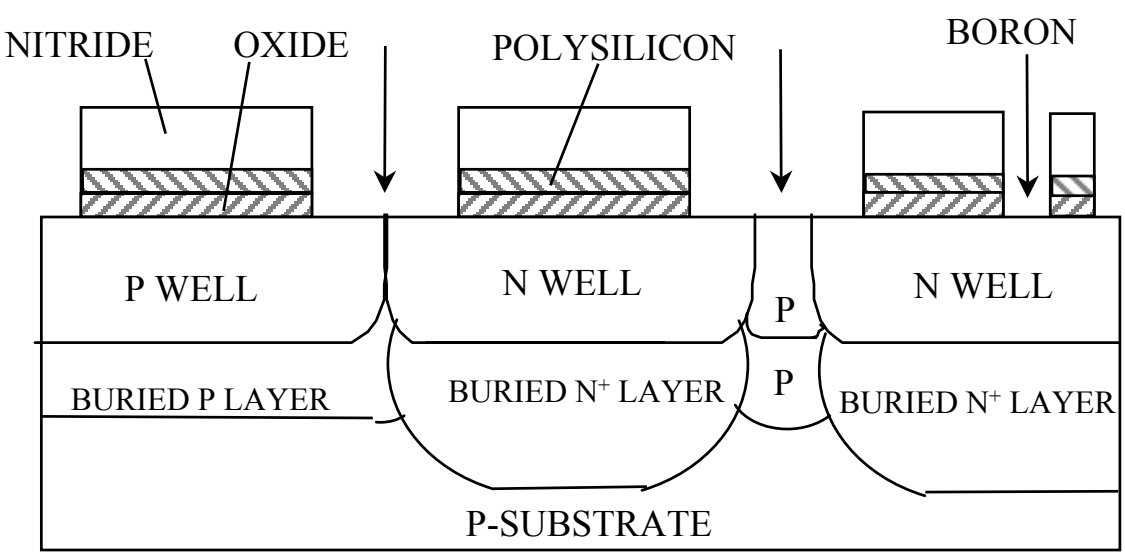


Digital BiCMOS Process Flow

1. P-substrate
2. N^+ buried & oxide over N^+ buried
3. Self-aligned buried P^+
4. Epitaxial layer with intrinsic doping

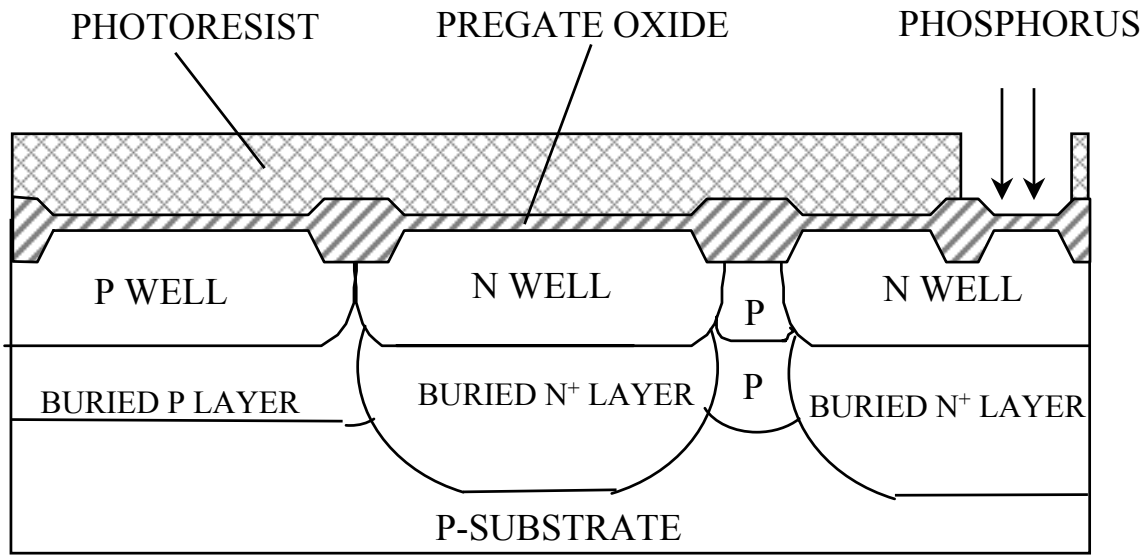


5. N-well formation & oxide over N-well
6. Self-aligned P-well
7. Active region and channel stop formation

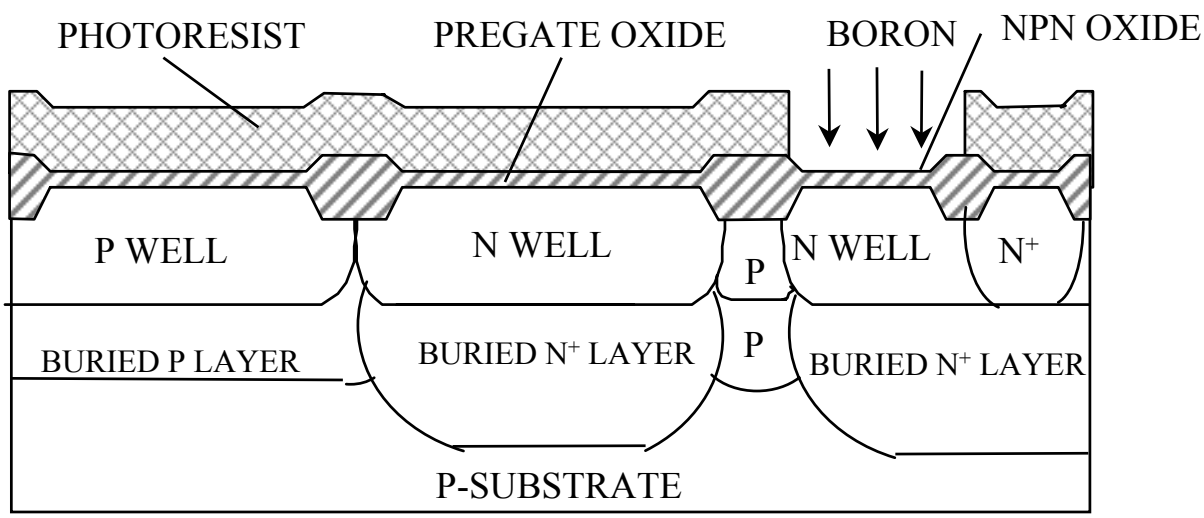


Digital BiCMOS Process Flow(Cont.)

8. N^+ collector to deep buried N^+ layer

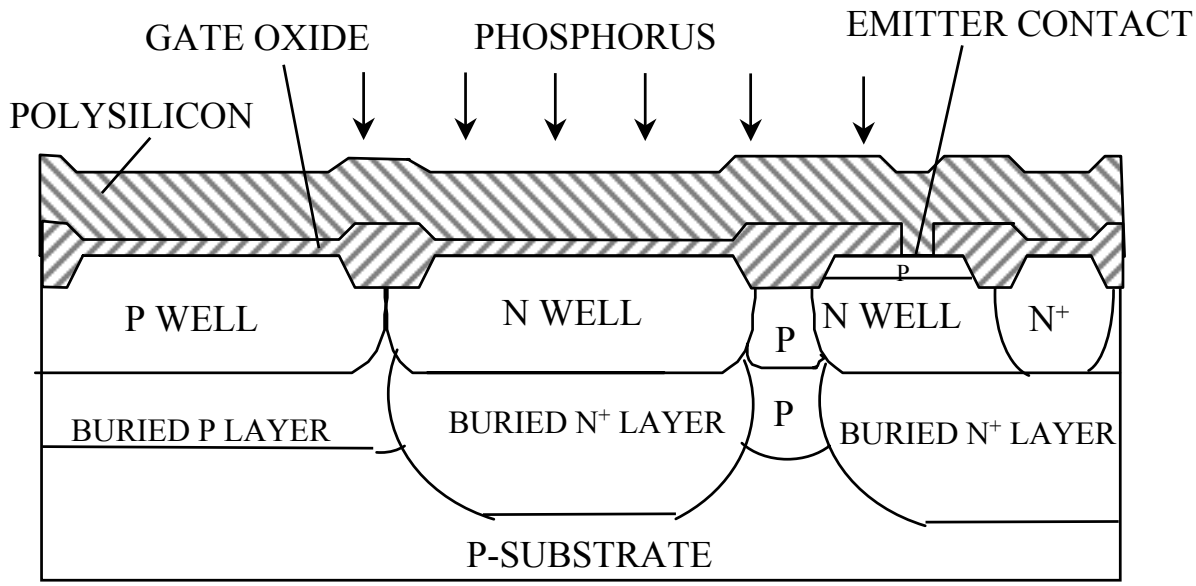


9. P-base and P-type resistor

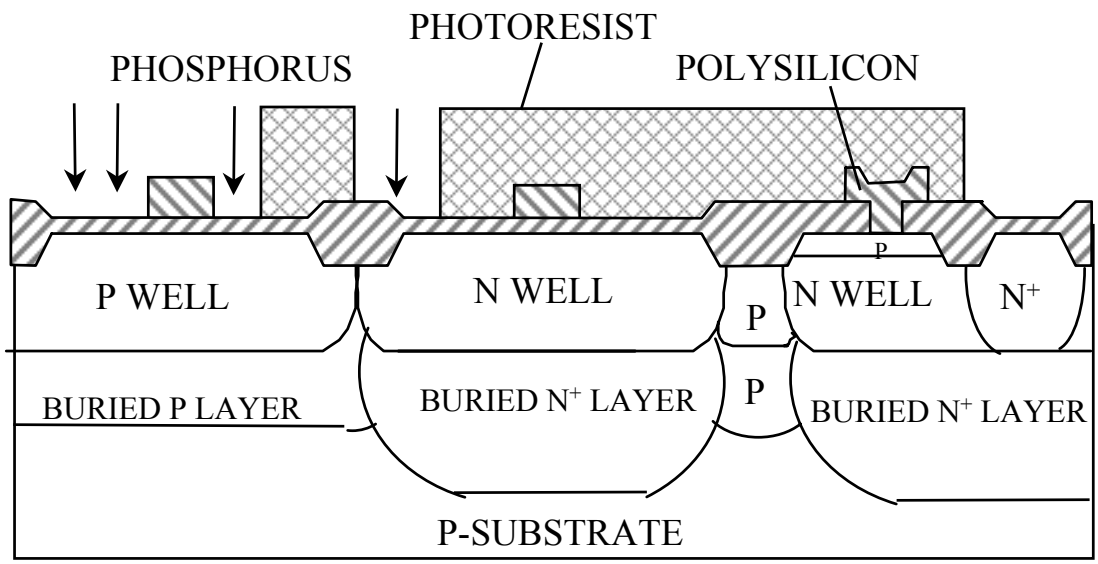


Digital BiCMOS Process Flow(Cont.)

10. Poly emitter & N^+ implant into poly emitter to form diffused emitter junction

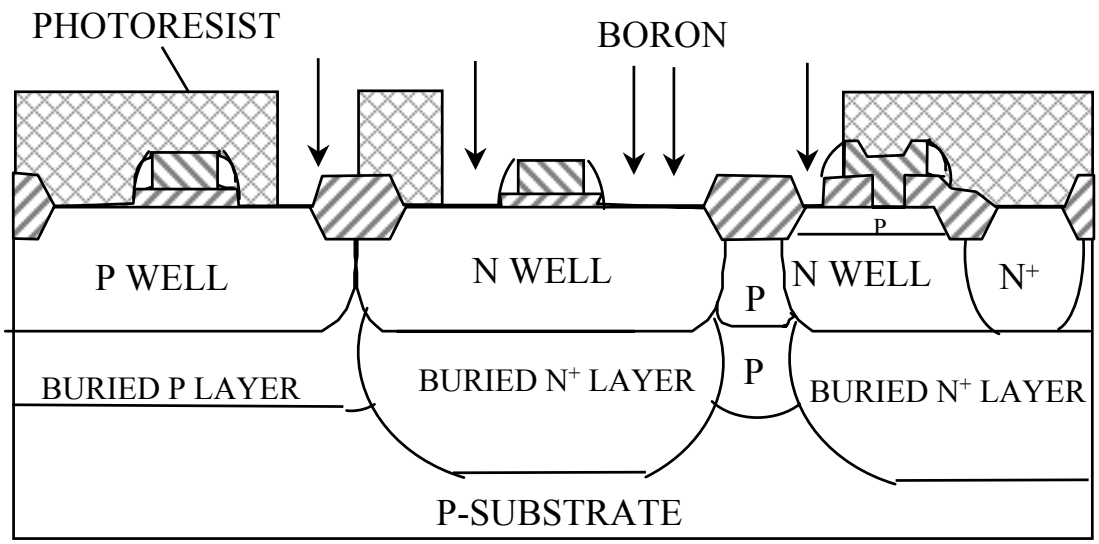


11. Gate & LDD formation

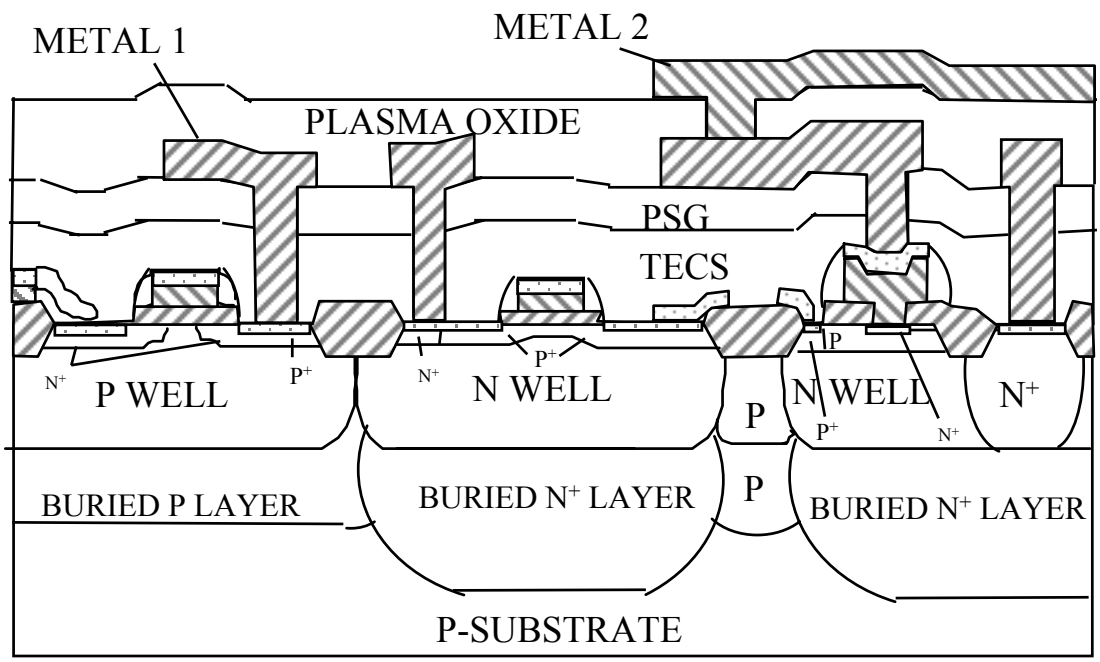


Digital BiCMOS Process Flow(Cont.)

12. N^+ & P^+ S/D implant



13. Interconnection: silicide, contact, metal
14. Passivation



Analog BiCMOS Process Components

- BJT components
  - isolated structure with
    a. low collector resistance
      - required for high current operation
    b. high Early voltage
      - high output resistance
  - adding PNP will result in high cost and increase process complexity

- CMOS components
  - minimum channel length of 2-3 μm is preferred for required high output resistance

- Passive components
  - capacitors
    poly-poly capacitors show low TC & VC, and is used to reduce parasitic effects
  - resistors
    poly resistor & thin film resistor are used to reduce TC & VC

- Component matching BJT > CMOS

- Component noise BJT < PMOS < NMOS

CMOS I-V Characteristics

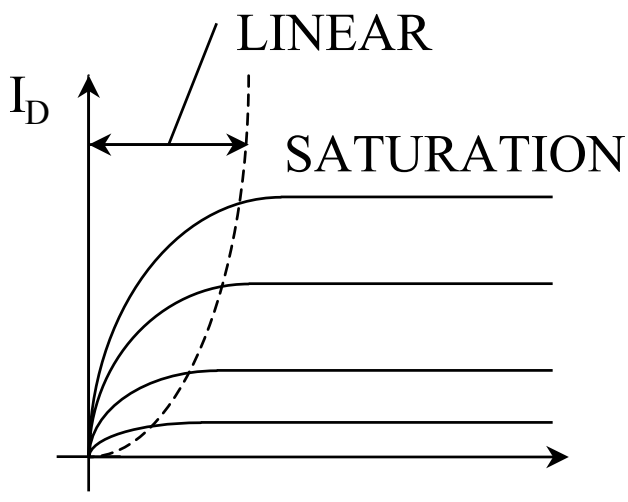
(Example: NMOS)

- Three regions
  1. Cutoff region (digital circuit)
     Subthreshold region (analog circuit) } $V_{GS} < V_{TH}$
  2. Nonsaturation region: $V_{GS} > V_{TH}$, $V_{GD} > V_{TH}$
     (also called linear or triode region)
  3. Saturation region: $V_{GS} > V_{TH}$, $V_{GD} < V_{TH}$

- Current equations for the above three regions
  1. $\cong 0$ (very small)
  2. $\mu_n Cox \frac{W}{L}(V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2}$
  3. $\frac{\mu_n Cox}{2}\frac{W}{L}(V_{GS} - V_{TH})^2 (1+\lambda V_{DS})$

  where $V_{TH} = V_{TO} + \gamma(\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F})$

$$\gamma = \sqrt{\frac{2q\varepsilon N_A}{Cox}} \quad , \quad \lambda = \frac{dX_d / dV_{DS}}{L_{eff}}$$



BJT I-V Characteristics

(Example: NPN)

- Regions:
  1. Cutoff region: $V_{BE} < 0$, $V_{BC} < 0$
  2. Saturation region: $V_{BE} > 0$, $V_{BC} < 0$
  3. Forward active region: $V_{BE} > 0$, $V_{BC} < 0$
  4. Reverse active region: $V_{BE} < 0$, $V_{BC} > 0$

- Current equation of the forward active region

$$I_C = I_S\left[\exp\left(\frac{V_{BE}}{V_t}\right)\right]\left(1+\frac{V_{CE}}{V_A}\right)$$

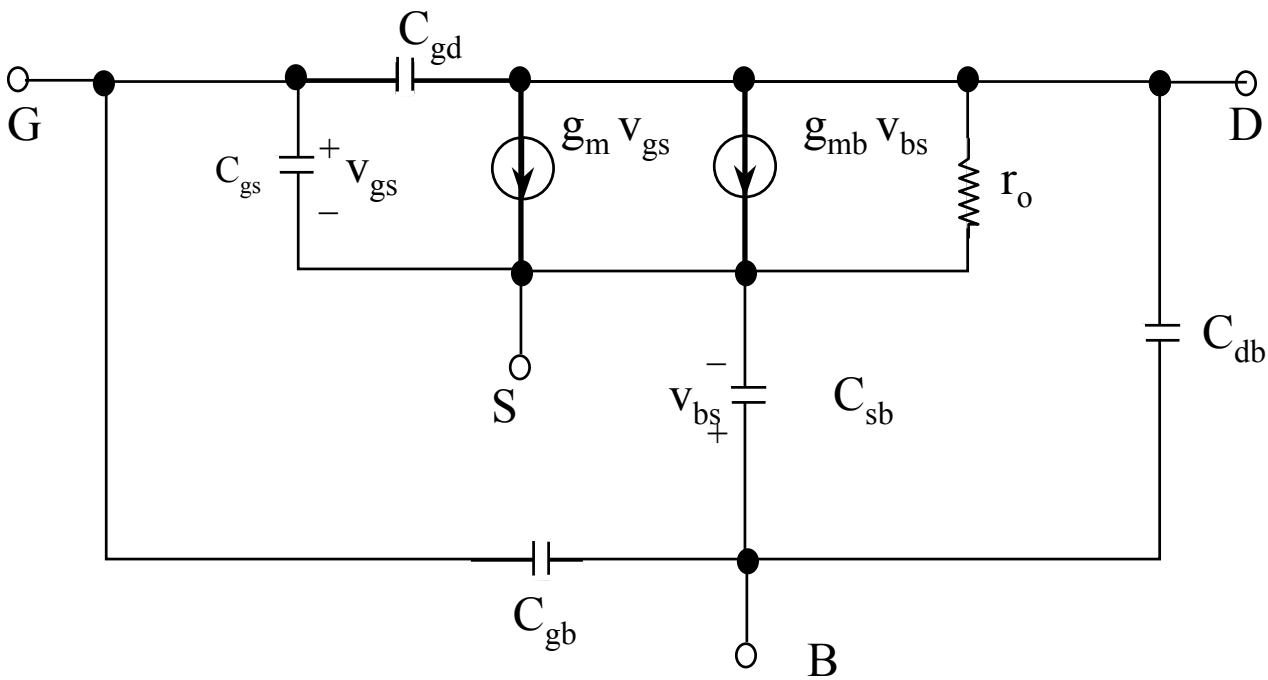
where $I_B = \frac{I_C}{\beta_F}$, $I_S = \frac{qAD_n n_i^2}{Q_B}$

$$V_t = \frac{KT}{q}, \quad V_A = -W_B\left(\frac{dW_B}{dV_{CE}}\right)^{-1}$$

CMOS Small Signal Models

(NMOS-saturation region)

- $g_m = \dfrac{d\ I_D}{d\ V_{GS}} \cong \sqrt{2\ \mu_n Cox(W/L)\ I_D}$
- $r_o = \left(\dfrac{d\ I_D}{d\ V_{DS}} \right)^{-1} = \dfrac{1}{\lambda\ I_D}$
- $g_{mb} = \dfrac{d\ I_D}{d\ V_{BS}} = \dfrac{\gamma}{2\sqrt{2\ \Phi_F + V_{SB}}}\ g_m$
- $C_{gs} \cong \dfrac{2}{3}$ WLCox +Cgso; Cgso is gate-soure overlap capacitance
- $C_{gd} \cong C_{gdo}$ (gate-drain overlap capacitance)
- C_{sb} , C_{db} : junction capacitances



BJT Small Signal Model

(NPN-forward active region)

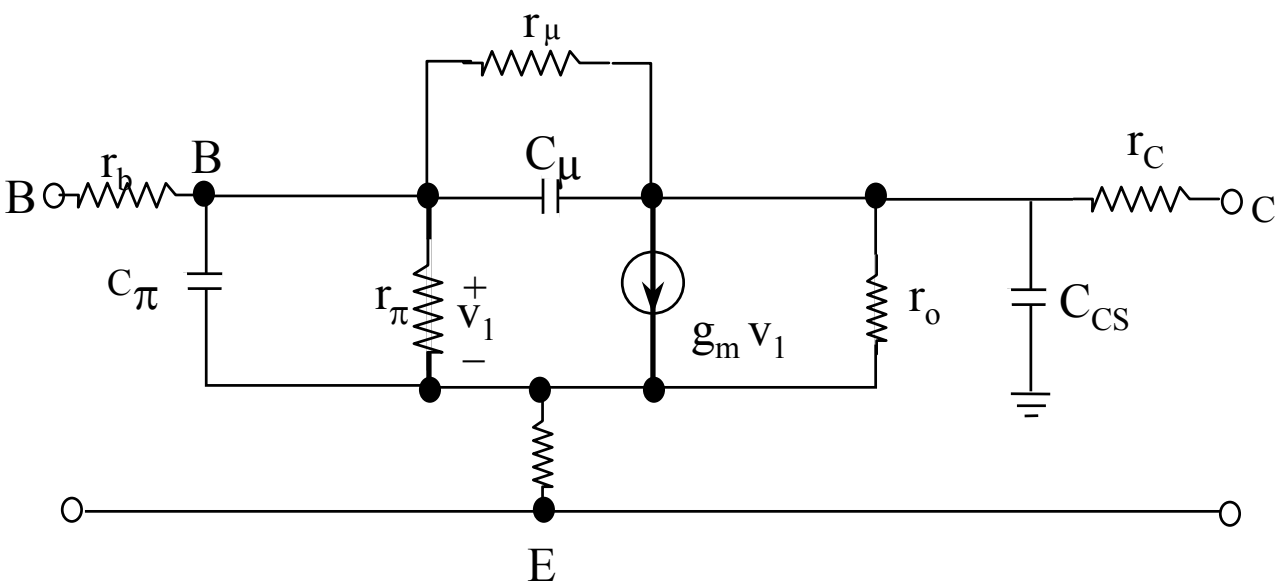
$$g_m = \frac{I_C}{V_t}$$

$$r_o = \frac{I_C}{V_A}$$

$$r_\mu = \left(\frac{d\,I_B}{d\,V_{CB}}\right)^{-1} = K\beta_o\, r_o \quad (\text{typically, } 1<K<10)$$

$$C_b = \frac{d\,Q_B}{d\,V_{BE}} = \blacklozenge_F g_m; \text{ where } \blacklozenge_F = \frac{W_B^2}{D_n}$$

C_{je}: base-emitter junction capacitance
C_μ : collector-base junction capacitance
C_{cs}: collector-substrate junction capacitance
r_b: ohmic resistance from base terminal to internal base
r_c , r_{ex}: collector and emitter ohmic resistances



Comparison of BJT & MOSFET Devices

(General case)

- Transconductance
  BJT > MOSFET
- Intrinsic gain
  BJT > MOSFET
- Frequency response
  BJT > MOSFET
- Input offset voltage for differential amplifier
  MOSFET > BJT
- Noise
  MMOS > PMOS >BJT
- Input impedence
  MOSFET > BJT
- Back-bias effect (i.e. body effect)
  only MOSFET
- Switch
  MOSFET is a voltage switch.
  BJT is a current switch.

Transconductance

- MOSFET

$$I_{DS}=\frac{\mu C_{OX}}{2}\frac{W}{L}\left(V_{GS}-V_{TH}\right)^2$$

$$g_m=\frac{dI_{DS}}{dV_{GS}}=\sqrt{2\mu C_{ox}\frac{W}{L}I_{DS}}$$

1. Process dependent
2. Size dependent
3. Varies as $\sqrt{I_{DS}}$

- BJT

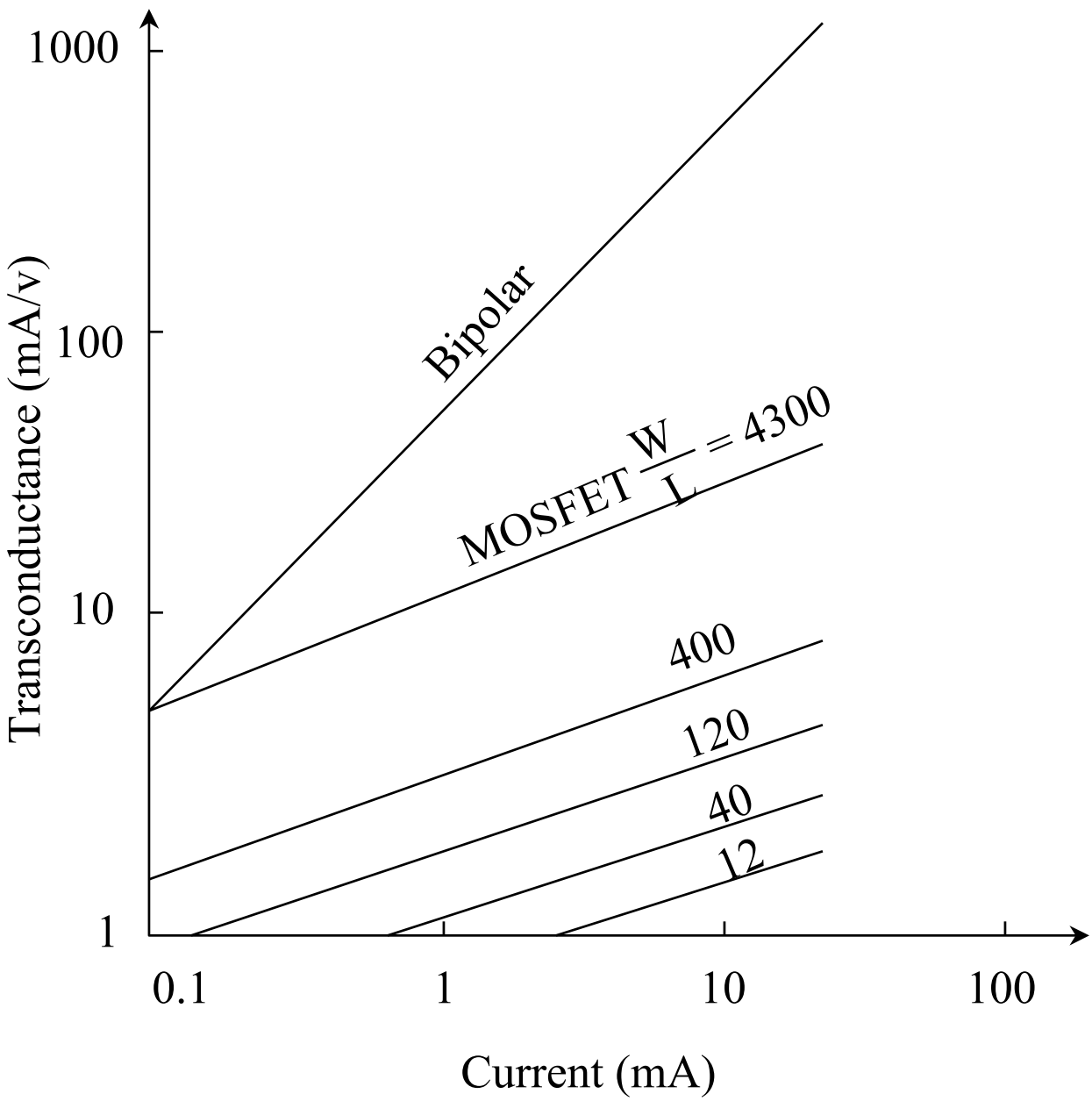
$$I_C=I_S\exp\left(\frac{V_{BE}}{V_t}\right);\quad V_t=\frac{kT}{q}$$

$$g_m=\frac{dI_C}{dV_{BE}}=\frac{I_C}{V_t}$$

1. Process independent
2. Size independent
3. Varies as I_C

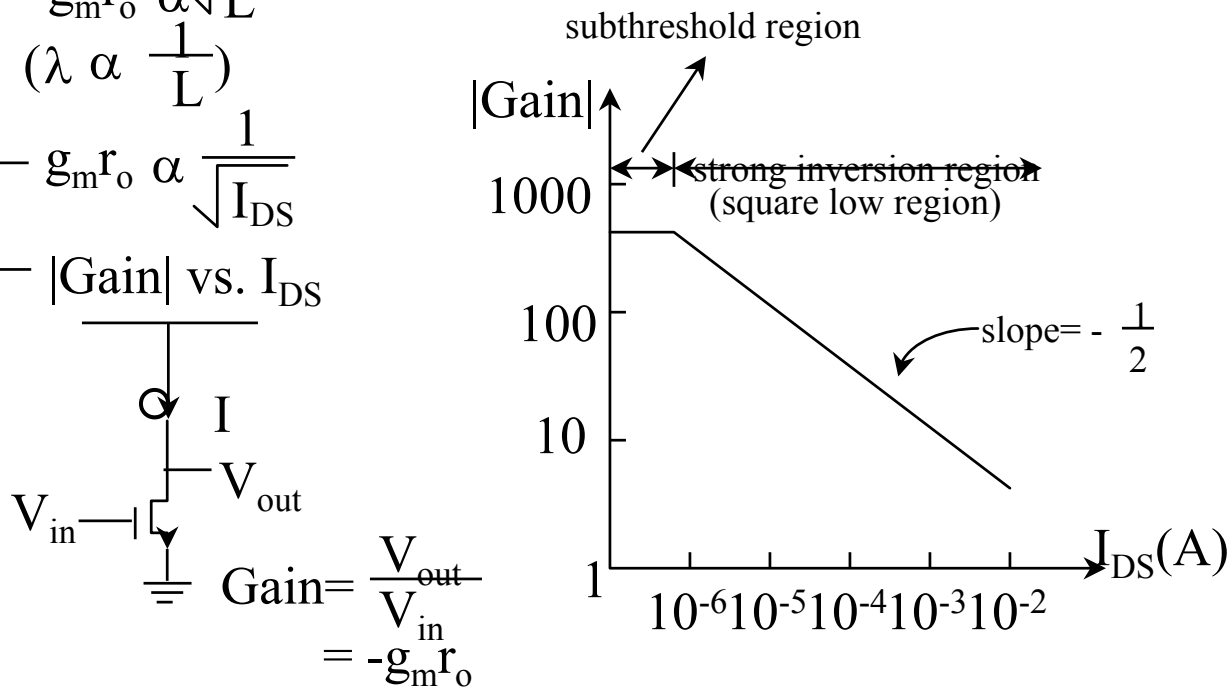
Comparision of Transconductance vs. Current between MOSFEETs and BJTs

- $V_t = \frac{KT}{q} = 25.9$ mv
- $\frac{\mu C_{ox}}{2} = 10\ \mu A / V^2$



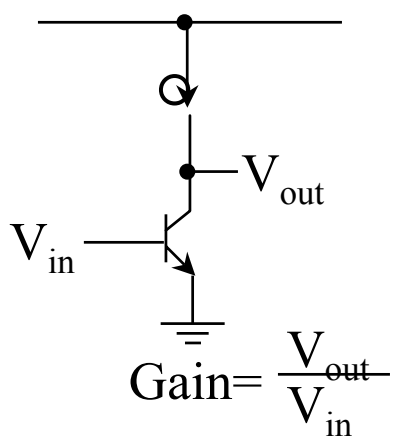
Intrinsic Gain

- MOS
  - $g_m r_o = \sqrt{2\mu C_{OX} \frac{W}{L} I_{DS}} \; \frac{1}{\lambda I_{DS}}$
  - $g_m r_o \; \alpha \sqrt{L}$ $(\lambda \; \alpha \; \frac{1}{L})$
  - $g_m r_o \; \alpha \; \frac{1}{\sqrt{I_{DS}}}$
  - |Gain| vs. I_{DS}



  - high input impedance
  - I ↑ ==> gain ↓ and bandwidth ↑

- Bipolar
  - $g_m r_o = \frac{V_A}{V_T}$ = const. (= $\frac{1}{\eta}$)
  - Typical case
    $V_A \approx 50V$
    $g_m r_o \approx 2 \times 10^3$
  - low input impedance ≈ r_π



Frequency Response

- MOS

$$\omega_T = \frac{g_m}{C_{gs}} \approx \frac{\sqrt{2\mu C_{ox}\frac{W}{L} I_{DS}}}{WLC_{ox}} = \frac{\mu}{L^2}(V_{gs} - V_{th})$$

$$\omega_T \propto L^{-2}, \omega_T \propto \sqrt{I_{DS}} \propto (V_{gs} - V_{th})$$

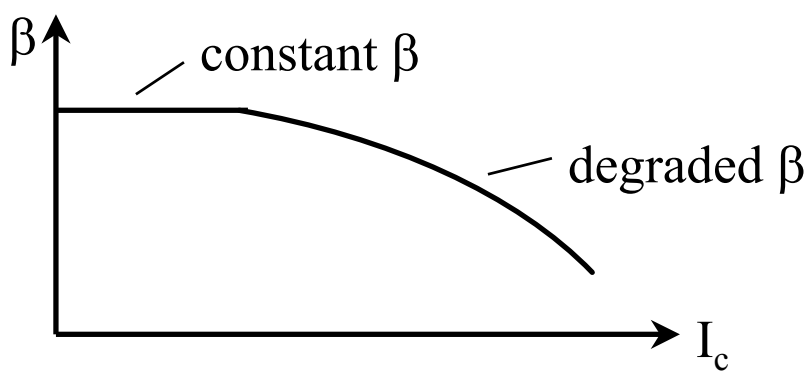
- In terms of I_{DS}, high ω_T is incompatible with high gain

$$(g_m r_0 \propto \sqrt{L} \quad but \quad g_m r_0 \propto \frac{1}{\sqrt{I_{DS}}})$$

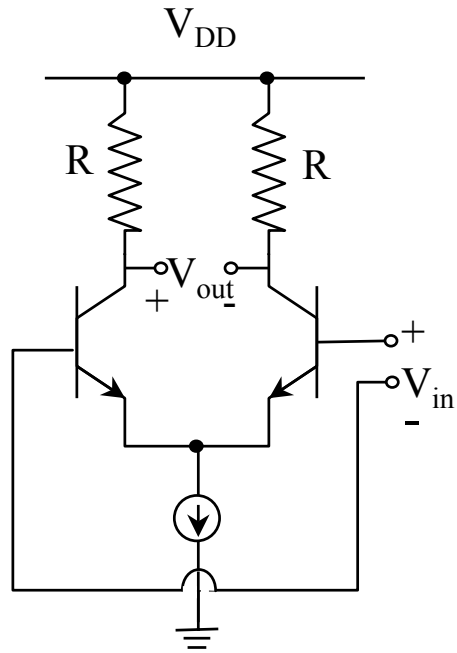
- Bipolar

$$\omega_T = \frac{g_m}{c_\pi + c_\mu} \propto I_c \qquad where \qquad g_m = \frac{I_c}{V_T}$$

- For BJT, β is decreased at high current



Input Offset Voltage of Differential Amp.



- Amp. with resistor load
  - BJT

$$V_{OS} = \frac{KT}{q}\left[-\frac{\delta R}{R} - \frac{\delta A_E}{A_E} - \frac{\delta Q_B}{Q_B}\right]$$

where

$\frac{KT}{q}$ is thermal voltage

R is load resistor

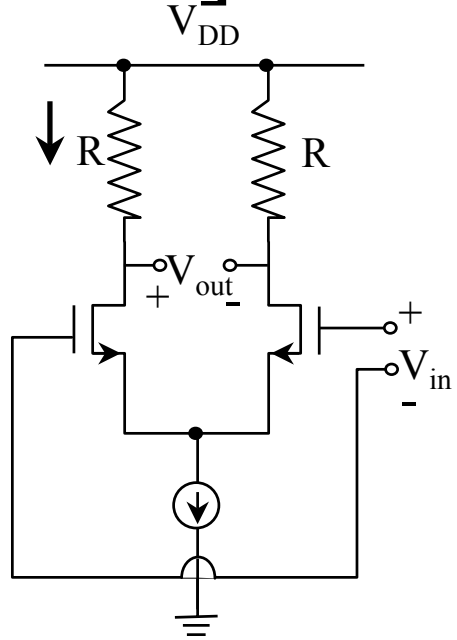
A_E is emitter area

Q_B is base Gummel number

δ represents the mismatch between the parameters

  - MOSFET

$$V_{OS} = \delta V_{TH} + \frac{V_{GS}-V_{TH}}{2}\left[-\frac{\delta R}{R} - \frac{\delta (W/L)}{W/L}\right]$$



$\frac{V_{GS}-V_{TH}}{2}$ ↓ => V_{OS} ↓ and speed ↓

- $V_{OS(MOSFET)} >> V_{OS(BJT)}$

  δV_{TH} only in MOSFET

  $\frac{V_{GS}-V_{TH}}{2}$ is about the order of 1V

  $\frac{KT}{q}$ is about 25.9mV

$$\Rightarrow \begin{cases} V_{OS(BJT)} \sim 1mV \\ V_{OS(MOSFET)} \sim 5\text{-}10mV \end{cases}$$