Process, Device, and Modeling

- Process
  - CMOS
  - BiCMOS

- Device Models
  - Large signal model
  - Small signal model

- Comparison of BJT & MOSFET
  - Transconductance
  - Intrinsic gain
  - Frequency response
  - Matching
  - Other parameters
BiCMOS Process

- **CMOS based BiCMOS**
  (driven from a CMOS processing base)

  - Digital BiCMOS circuits tend to be CMOS-intensive because of power dissipation limitations (e.g. RAMs, uPs, gate arrays, ..., etc.)
  => highest possible CMOS performance

  - Analog BiCMOS circuits are most often combined with large digital circuit
  => results in CMOS-oriented

  - Extra steps required for BJT fabrication (e.g. isolation structure) have been introduced with only minimal changes to the actual CMOS transistor fabrication sequence

- Process commonality between the bipolar and CMOS flows has been adopted whenever possible
Device Patterning

Photoresists

NEG - first historically
POS - better for dimensions < 2.5µm
NEG - insoluble where exposed
POS - soluble where exposed
CMOS P-well Process Flow

Cross section of physical structure (side View)

Mask (Top View)

PTUB MASK

FIELD OXIDE (FOX) 4.6 µm DEEP

n-SUBSTRATE p-WELL

THINOXIDE (-500 Å)

n-SUBSTRATE p-WELL

THINOXIDE MASK

THINOXIDE

POLYSILICON

POLYSILICON MASK

n-SUBSTRATE p-WELL

POLYSILICON

p-TRANSISTOR p-PLUS MASK (POSITIVE)

p+ p+

p-WELL

p-PLUS+

Tai-Haur Kuo, EE, NCKU, 1997

BiCMOS Circuit Design 2-4
CMOS P-well Process Flow (Continued)

1. n-transistor
2. p-PLUS MASK (NEGATIVE)
3. N+
4. N-PLUS -
5. CONTACT CUT
6. CONTACT MASK
7. contact
8. METAL MASK
9. METAL
10. Inter-connection

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Digital BiCMOS Process Flow

1. P-substrate
2. N⁺ buried & oxide over N⁺ buried
3. Self-aligned buried P⁺
4. Epitaxial layer with intrinsic doping

5. N-well formation & oxide over N-well
6. Self-aligned P-well
7. Active region and channel stop formation
8. N\(^+\) collector to deep buried N\(^+\) layer

9. P-base and P-type resistor
10. Poly emitter & $N^+$ implant into poly emitter to form diffused emitter junction

11. Gate & LDD formation
Digital BiCMOS Process Flow (Cont.)

12. N⁺ & P⁺ S/D implant

13. Interconnection: silicide, contact, metal

14. Passivation
Analog BiCMOS Process Components

- **BJT components**
  - isolated structure with
    - a. low collector resistance
    - required for high current operation
    - b. high Early voltage
    - high output resistance
    - adding PNP will result in high cost and increase process complexity

- **CMOS components**
  - minimum channel length of 2-3 \( \mu \)m is preferred for required high output resistance

- **Passive components**
  - capacitors
    - poly-poly capacitors show low TC & VC, and is used to reduce parasitic effects
  - resistors
    - poly resistor & thin film resistor are used to reduce TC & VC

- **Component matching**  
  - BJT > CMOS

- **Component noise**  
  - BJT < PMOS < NMOS

Tai-Haur Kuo, EE, NCKU, 1997

BiCMOS Circuit Design 2-10
CMOS I-V Characteristics

(Example: NMOS)

- Three regions
  1. Cutoff region (digital circuit)
  2. Nonsaturation region: \( V_{GS} > V_{TH}, V_{GD} > V_{TH} \)
    (also called linear or triode region)
  3. Saturation region: \( V_{GS} > V_{TH}, V_{GD} < V_{TH} \)

- Current equations for the above three regions
  1. \( \mu_nCox \frac{W}{L} (V_{GS} - V_{TH}) V_{DS} - \frac{V_{DS}^{2}}{2} \approx 0 \) (very small)
  2. \( \mu_nCox \frac{W}{L} (V_{GS} - V_{TH}) V_{DS} - \frac{V_{DS}^{2}}{2} \)
  3. \( \frac{\mu_nCox}{2} \frac{W}{L} (V_{GS} - V_{TH})^{2} (1 + \lambda V_{DS}) \)

where \( V_{TH} = V_{TO} + \gamma (\sqrt{2 \phi_{F}} + V_{SB} - \sqrt{2 \phi_{F}}) \)

\( \gamma = \sqrt{\frac{2q \varepsilon N_{A}}{Cox}}, \quad \lambda = \frac{dX_{d}/dV_{DS}}{L_{eff}} \)
BJT I-V Characteristics

(Example: NPN)

- Regions:
  1. Cutoff region: $V_{BE} < 0$, $V_{BC} < 0$
  2. Saturation region: $V_{BE} > 0$, $V_{BC} < 0$
  3. Forward active region: $V_{BE} > 0$, $V_{BC} < 0$
  4. Reverse active region: $V_{BE} < 0$, $V_{BC} > 0$

- Current equation of the forward active region

$$I_C = I_S \left[ \exp \left( \frac{V_{BE}}{V_t} \right) \right] \left[ 1 + \frac{V_{CE}}{V_A} \right]$$

where

$$I_B = \frac{I_C}{\beta_F}, \quad I_S = \frac{qAD_n n_i^2}{Q_B}$$

$$V_t = \frac{KT}{q}, \quad V_A = -W_B \left( \frac{dW_B}{dV_{CE}} \right)^{-1}$$
CMOS Small Signal Models

(NMOS-saturation region)

- $g_m = \frac{d I_D}{d V_{GS}} \approx \sqrt{2 \mu_n C_{ox} (W/L)} I_D$

- $r_o = \left( \frac{d I_D}{d V_{DS}} \right)^{-1} = \frac{1}{\lambda I_D}$

- $g_{mb} = \frac{d I_D}{d V_{BS}} = \frac{\gamma}{2 \sqrt{2 \Phi_F + V_{SB}}} g_m$

- $C_{gs} \approx \frac{2}{3} W L C_{ox} + C_{gso}; C_{gso}$ is gate-source overlap capacitance

- $C_{gd} \approx C_{gdo}$ (gate-drain overlap capacitance)

- $C_{sb} , C_{db}$: junction capacitances
BJT Small Signal Model

(NPN-forward active region)

g_m = \frac{I_C}{V_t}

r_o = \frac{I_C}{V_A}

r_\mu = \left(\frac{d I_B}{d V_{CB}}\right)^{-1} = K\beta_o r_o \text{ (typically, } 1 < K < 10)\]

C_b = \frac{d Q_B}{d V_{BE}} = \Phi g_m; \text{ where } \Phi = \frac{W_B^2}{D_n}

C_{je}: \text{ base-emitter junction capacitance}
C_\mu: \text{ collector-base junction capacitance}
C_{cs}: \text{ collector-substrate junction capacitance}
r_b: \text{ ohmic resistance from base terminal to internal base}
r_c, r_ex: \text{ collector and emitter ohmic resistances}
Comparison of BJT & MOSFET Devices

(General case)

- Transconductance
  BJT > MOSFET
- Intrinsic gain
  BJT > MOSFET
- Frequency response
  BJT > MOSFET
- Input offset voltage for differential amplifier
  MOSFET > BJT
- Noise
  MMOS > PMOS > BJT
- Input impedance
  MOSFET > BJT
- Back-bias effect (i.e. body effect)
  only MOSFET
- Switch
  MOSFET is a voltage switch.
  BJT is a current switch.
Transconductance

- **MOSFET**
  \[ I_{DS} = \frac{\mu C_{OX}}{2} \frac{W}{L} (V_{GS} - V_{TH})^2 \]
  \[ g_m = \frac{dI_{DS}}{dV_{GS}} = \sqrt{2\mu C_{ox} \frac{W}{L}} I_{DS} \]
  1. Process dependent
  2. Size dependent
  3. Varies as \( \sqrt{I_{DS}} \)

- **BJT**
  \[ I_C = I_s \exp \left( \frac{V_{BE}}{V_T} \right) ; \quad V_T = \frac{kT}{q} \]
  \[ g_m = \frac{dI_C}{dV_{BE}} = \frac{I_C}{V_T} \]
  1. Process independent
  2. Size independent
  3. Varies as \( I_C \)
**Comparision of Transconductance vs. Current between MOSFETs and BJTs**

- $V_t = \frac{KT}{q} = 25.9 \text{ mV}$
- $\frac{\mu C_{ox}}{2} = 10 \mu \text{A} / V^2$

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![Graph showing comparison of transconductance vs. current between MOSFETs and BJTs.](image)

- **Bipolar**
- **MOSFET $\frac{W}{L} = 4300$**
- **MOSFET $\frac{W}{L} = 400$**
- **MOSFET $\frac{W}{L} = 120$**
- **MOSFET $\frac{W}{L} = 40$**
- **MOSFET $\frac{W}{L} = 12$**
Intrinsic Gain

- **MOS**
  \[ g_{m}\alpha = \sqrt{\frac{2\mu}{L}} \cdot \frac{W}{L} \cdot I_{DS} \cdot \frac{1}{\lambda I_{DS}} \quad \text{gain} = \frac{V_{out}}{V_{in}} \]

- **Bipolar**
  \[ g_{m}\alpha = \frac{V_{A}}{V_{T}} = \text{const.} \left( = \frac{1}{\eta} \right) \]

**Typical case**
- \( V_{A} \approx 50V \)
- \( g_{m}\alpha \approx 2 \times 10^{3} \)
- low input impedance \( \approx r_{i} \)

Tai-Haur Kuo, EE, NCKU, 1997

BiCMOS Circuit Design 2-18
Frequency Response

- MOS

\[ \omega_T = \frac{g_m}{C_{gs}} \approx \frac{\sqrt{2\mu C_{ox} W}}{L} \frac{I_{DS}}{WLC_{ox}} = \frac{\mu}{L^2} (V_{gs} - V_{th}) \]

\[ \omega_T \propto L^{-2}, \quad \omega_T \propto \sqrt{I_{DS}} \propto (V_{gs} - V_{th}) \]

\( \Rightarrow \) In terms of \( I_{DS} \), high \( \omega_T \) is incompatible with high gain

( \( g_{m0} \propto \sqrt{L} \quad \text{but} \quad g_{m0} \propto \frac{1}{\sqrt{I_{DS}}} \))

- Bipolar

\[ \omega_T = \frac{g_m}{c_\pi + c_\mu} \propto I_c \quad \text{where} \quad g_m = \frac{I_c}{V_T} \]

\( \Rightarrow \) For BJT, \( \beta \) is decreased at high current

\[ \beta \]

constant \( \beta \)

degraded \( \beta \)
Input Offset Voltage of Differential Amp.

- Amp. with resistor load
  - BJT
  \[ V_{OS} = \frac{KT}{q} \left[ - \frac{R}{R} - \frac{A_E}{A_E} - \frac{Q_B}{Q_B} \right] \]
  where
  \( \frac{KT}{q} \) is thermal voltage
  \( R \) is load resistor
  \( A_E \) is emitter area
  \( Q_B \) is base Gummel number
  \( \nabla \) represents the mismatch between the parameters

- MOSFET
  \[ V_{OS} = \nabla V_{TH} + \frac{V_{GS}-V_{TH}}{2} \left[ - \frac{R}{R} - \frac{(W/L)}{W/L} \right] \]
  \[ \frac{V_{GS}-V_{TH}}{2} \downarrow \Rightarrow V_{OS} \downarrow \text{ and speed} \]

  \( V_{OS(MOSFET)} \gg V_{OS(BJT)} \)
  \( \nabla V_{TH} \) only in MOSFET
  \( \frac{V_{GS}-V_{TH}}{2} \) is about the order of 1V
  \( \frac{KT}{q} \) is about 25.9mV

  \[ \Rightarrow \begin{cases} 
  V_{OS(BJT)} \sim 1mV \\
  V_{OS(MOSFET)} \sim 5-10mV 
  \end{cases} \]