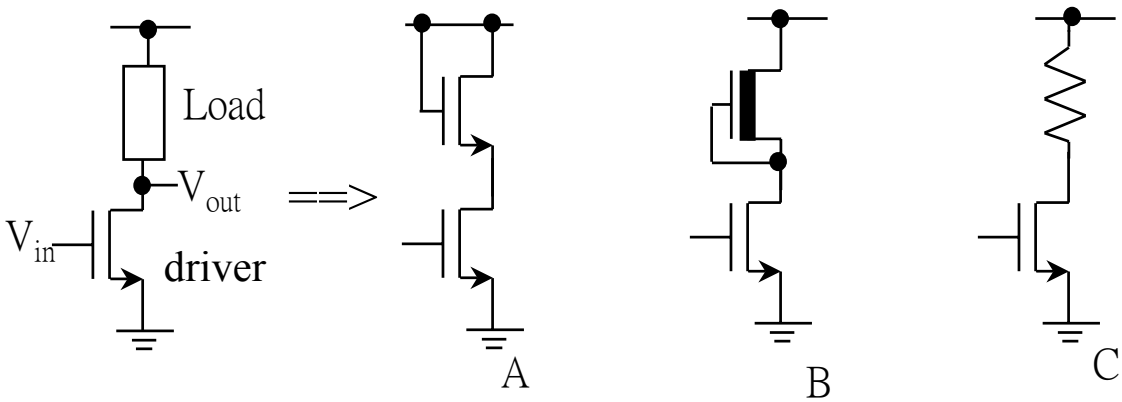
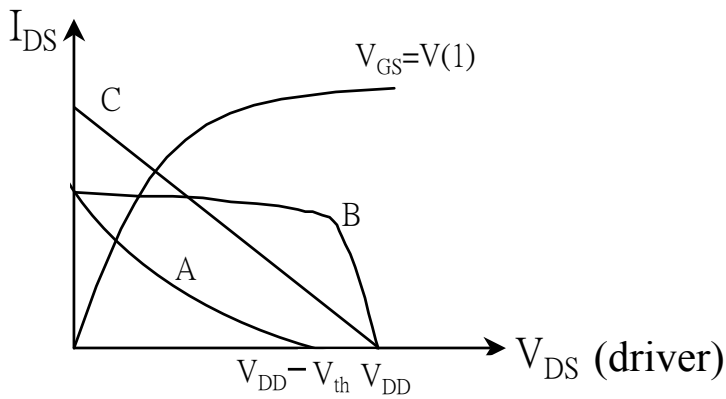
BiCMOS Digital Circuit Design

- Review of CMOS & NMOS Inverter Design
  - delay time
  - pair delay
  - driving large capacitive loads
- Features of BiCMOS Digital Circuit
- BiCMOS Inverters
  - basic type
  - delay time
  - improved type
  - full swing
  - design example
    a. size optimization
    b. driving large capacitive loads
- BiCMOS Gate
- Power-Supply Sensitivity
  - voltage scaling
  - low voltage gate
- I/O Interface
  - input
  - output
  - logic conversion

NMOS DIGITAL CIRCUITS

- Static inverters





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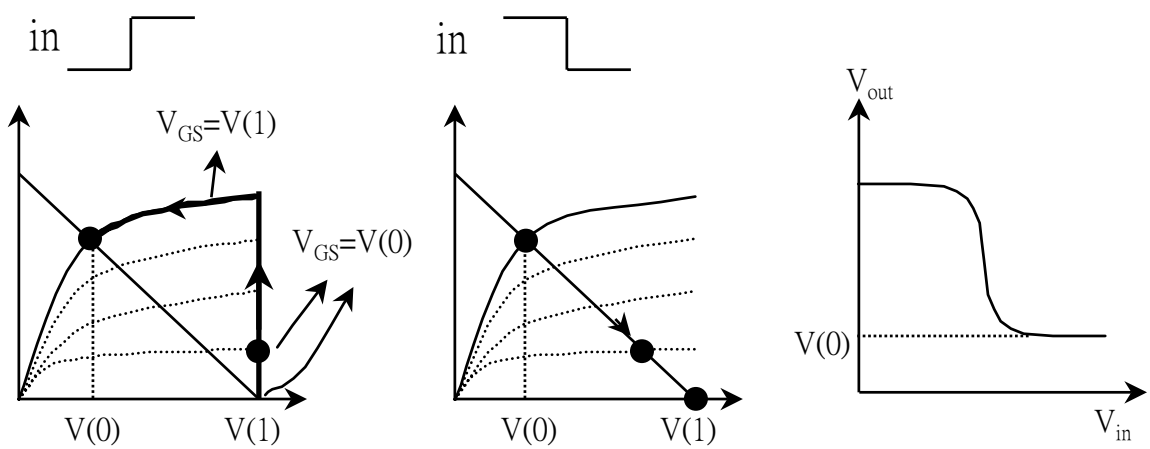
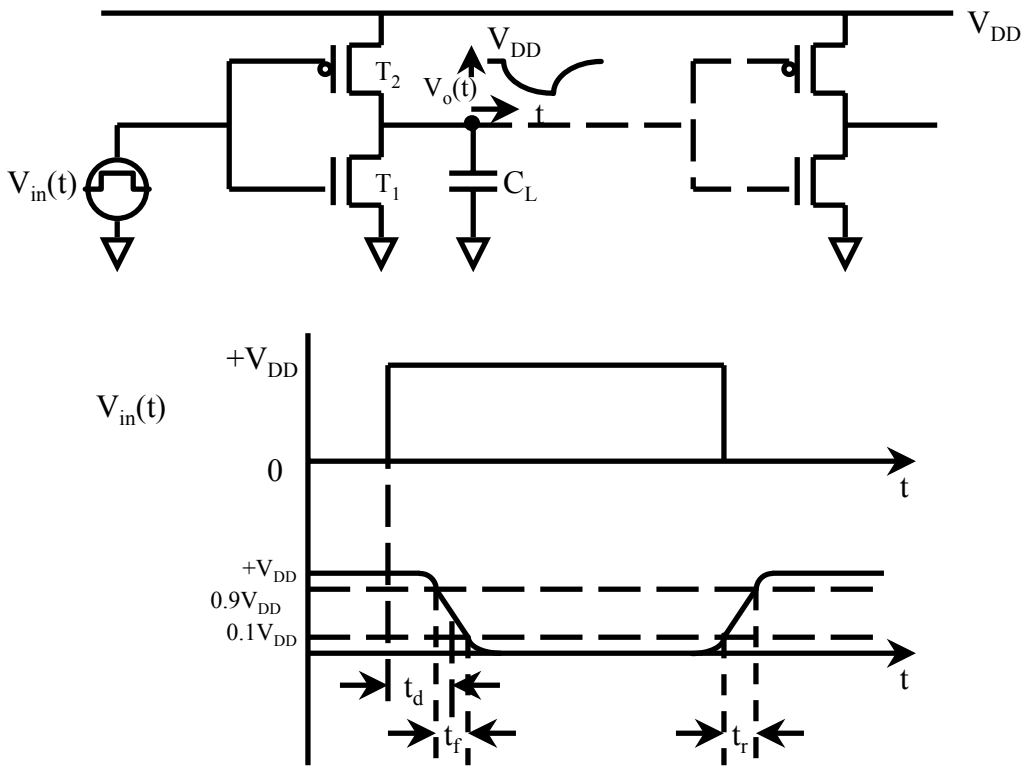


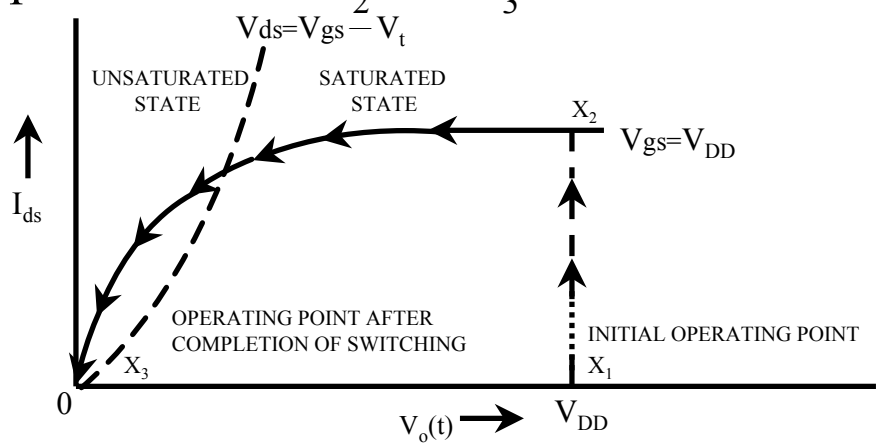
— Static power dissipation during V_{out}=V(0)

Switching Characteristics of CMOS Inverter

- CMOS inverter



- Trajectory of n-transistor operating point during switching in CMOS inverter
  — Input transition : $X_1 \rightarrow X_2$
  Output transition: $X_2 \rightarrow X_3$

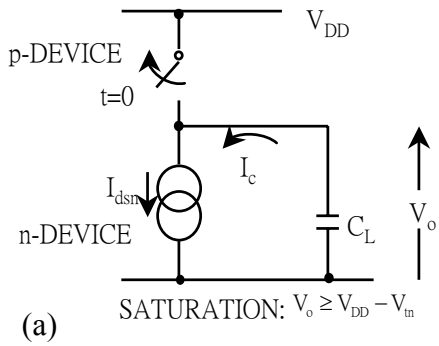


Rise Time and Fall Time of CMOS Inverter

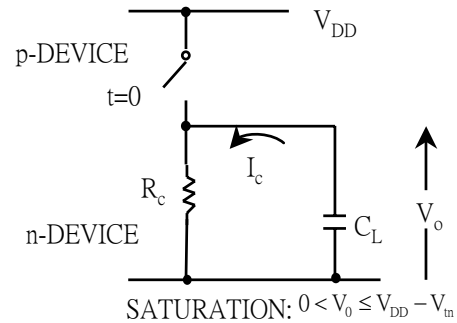
> Equivalent Circuit

> Fall

$\begin{pmatrix} V_{in} \uparrow \\ V_o \downarrow \end{pmatrix}$

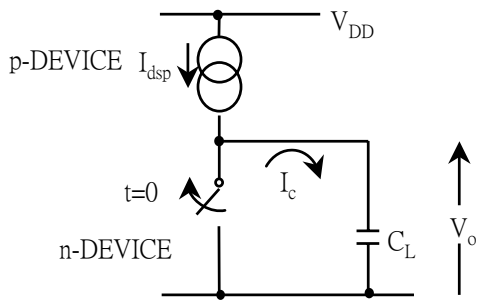


(a)

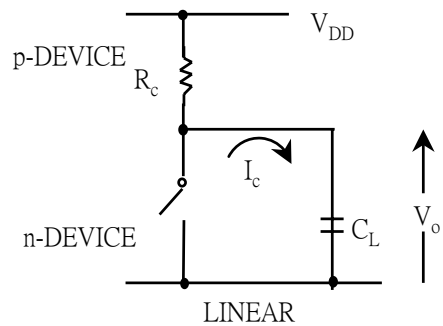


> Rise

$\begin{pmatrix} V_{in} \downarrow \\ V_o \uparrow \end{pmatrix}$



(b)



> $t_f = t_{f1} + t_{f2}$; fall time

$| t_{f1} |$ t_{f2} |

$V_o = 0.9V_{DD}$ $V_o = 0.1V_{DD}$

$V_o = V_{DD} - V_{tn}$

$| t_{f1} |$ t_{f2} |

$\begin{cases} I_{DS(PMOS)} = 0 \\ I_{DS(NMOS)} \text{ in saturation} \end{cases}$ $\begin{cases} I_{DS(PMOS)} = 0 \\ I_{DS(NMOS)} \text{ in triode} \end{cases}$

Fall Time (Cont.)

- t_f
  - $V_o : 0.9\,V_{DD} \longrightarrow V_{DD} - V_{tn}$
  - NMOS in saturation region

$$C_L \frac{dV_o}{dt} - \frac{\beta_n}{2}(V_{DD} - V_{tn})^2 = 0$$

$$t_{f1} = \frac{2C_L}{\beta_n (V_{DD} - V_{tn})^2} \int_{V_{DD}-V_{tn}}^{0.9V_{DD}} dV_o$$

$$= \frac{2C_L (V_{tn} - 0.1\,V_{DD})}{\beta_n (V_{DD} - V_{tn})^2}$$

- t_{f2}
  - $V_o : V_{DD} - V_{tn} \rightarrow 0.1\,V_{DD}$
  - NMOS in triode region

$$C_L \frac{dV_o}{dt} = \frac{\beta_n}{2}[\,2(V_{gs} - V_{tn})V_{ds} - V_{ds}^2\,]$$

$$\uparrow$$

$$V_{DD}$$

$$t_{f2} = \frac{C_L}{\beta_n (V_{DD} - V_{tn})} \int_{0.1V_{DD}}^{V_{DD}-V_{tn}} \frac{dV_o}{\frac{V_o^2}{2(V_{DD} - V_{tn})} - V_o}$$

Fall Time (Cont.)

- $t_{f2} = \frac{C_L}{\beta_n (V_{DD} - V_{tn})} \ln\left(\frac{19V_{DD} - 20V_{tn}}{V_{DD}}\right)$

$$t_f = t_{f1} + t_{f2}$$

$$= \frac{2C_L}{\beta_n (V_{DD} - V_{tn})} \times \left[\frac{V_{tn} - 0.1V_{DD}}{V_{DD} - V_{tn}} + \frac{1}{2} \ln\left(\frac{19V_{DD} - 20V_{tn}}{V_{DD}}\right)\right]$$

- e.g. $V_{DD} = 5V$, $V_{tp} = -1V$, $V_{tn} = 1V$

$$t_f \approx \frac{4C_L}{\beta_n V_{DD}}$$

- Rise time

Similarly, $t_r \approx \frac{4C_L}{\beta_p V_{DD}}$

Fall Time and Rise Time (Cont.)

- $$t_f \approx \frac{4C_L}{\beta_n V_{DD}}$$
$$t_r \approx \frac{4C_L}{\beta_{p[} V_{DD}}$$

- For equally sized n and p devices

$$\beta_n = 2\beta_p$$

$$t_f = \frac{t_r}{2}$$

- For $t_r = t_f$

$$\Rightarrow \beta_p = \beta_n \qquad \Rightarrow W_p = 2.5W_n$$

For simplicity, 2 is used sometimes.

$$t_{df} = \frac{t_f}{2}$$

$$t_{dr} = \frac{t_r}{2}$$

Equivalent Circuit

- Equivalent Resistance
  - $t_f = \frac{4C_L}{\beta_n V_{DD}} = R_{eq} C_L$
  - $R_{eq} = \frac{4}{\beta_n V_{DD}}$ for minimum sized NMOS
  - $R_{eq}(\text{PMOS}) = \frac{4}{\beta_n V_{DD}} \approx 2.5 R_{eq}$ for minimum sized PMOS

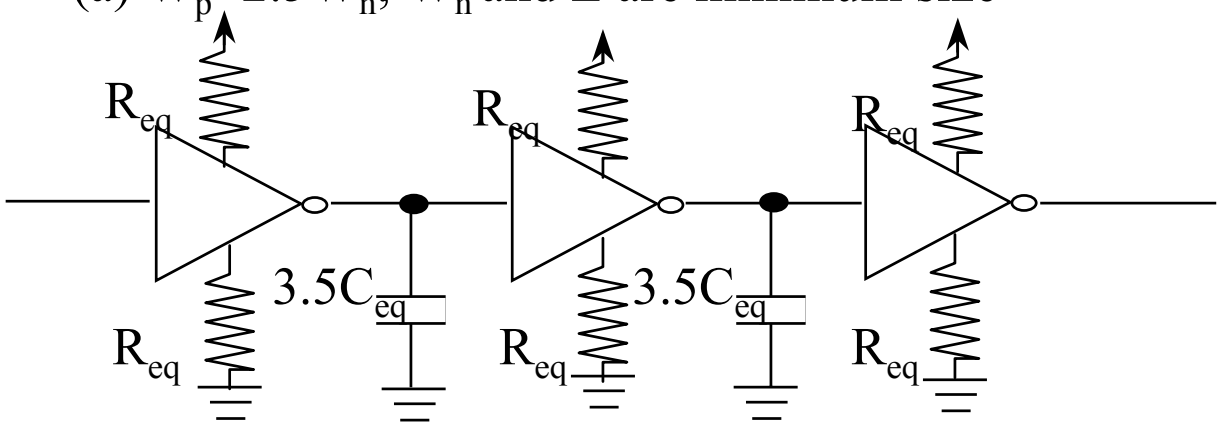
- Equivalent capacitance

  $C_{eq} = C_{gs}$ of minimum sized transistors

Inverter-pair Delay

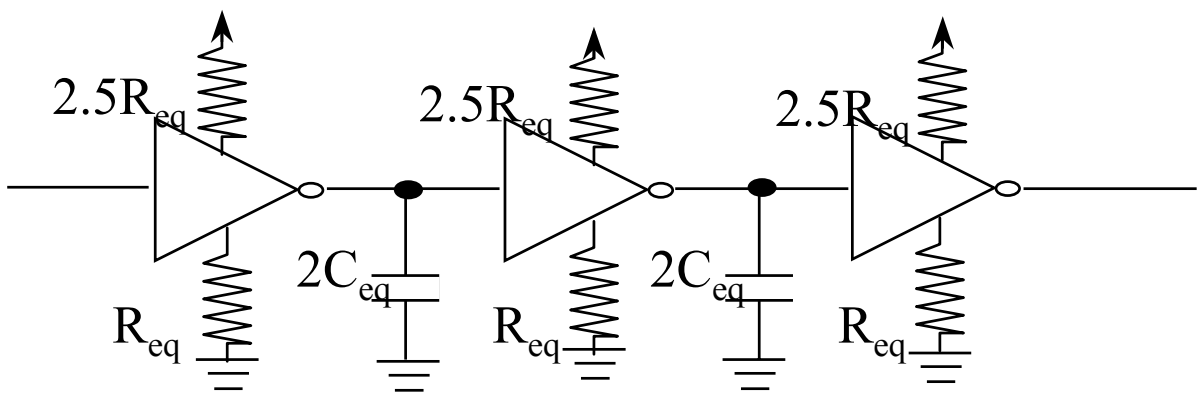
> CMOS

(a) W_p=2.5W_n; W_n and L are minimum size



$$t_{inv\text{-}pair} = t_f + t_r = 3.5R_{eq}C_{eq} + 3.5R_{eq}C_{eq} = 7R_{eq}C_{eq}$$

(b) W_p=W_n; All minimum sized devices

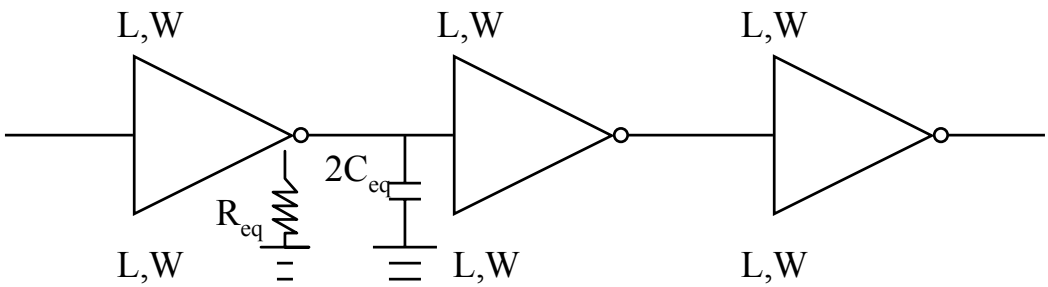


$$t_{inv\text{-}pair} = 5R_{eq}C_{eq} + 2R_{eq}C_{eq} = 7R_{eq}C_{eq}$$

— $W_p = 2.5W_n$ ==> V_{inv}=2.5V
$W_p = W_n$ ==> V_{inv} =2.2V
} same delay time
V_{inv} ~10% variation

Inverter-pair Delay (Cont.)

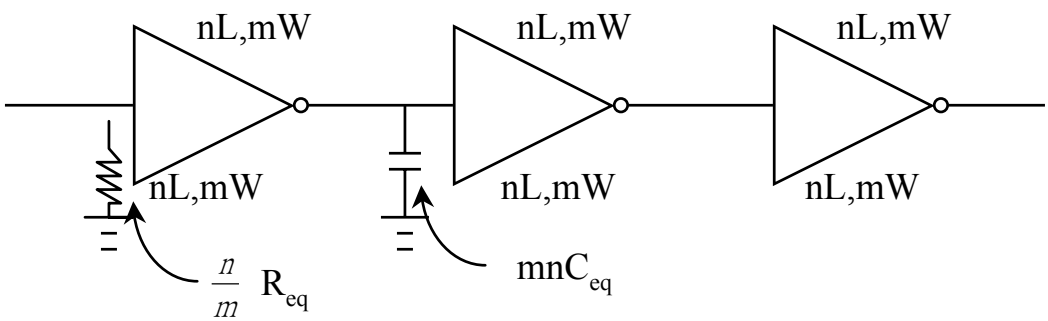
- Driving same size inverter



L&W are minimum size

Inverter-pair Delay $= 7R_{eq}C_{eq} = 7\tau$

where $\tau = R_{eq}C_{eq}$



Inverter-pair Delay $= 7n^2 R_{eq}C_{eq} = 7n^2\tau$

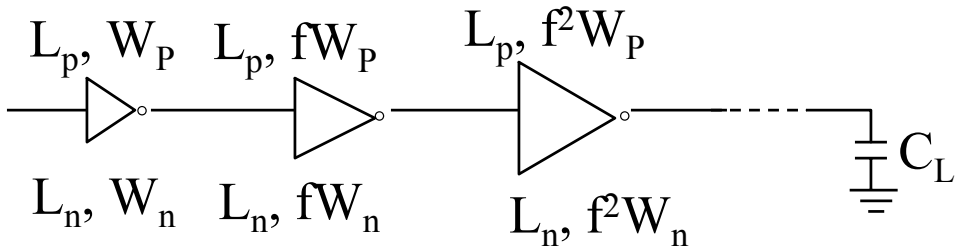
where $\tau = R_{eq}C_{eq}$

(Depends on channel length independent of channel width)

❄Recall that $W_u = \frac{g_m}{C_g} = \frac{\mu}{L^2}(V_{gs} - V_t)$

Driving Large Capacitive Loads

> CMOS



(i) If L_p & L_n are minimum channel length ,

$t_{inv\text{-}pair} = 7f\,\tau$

(ii) If L_p & L_n are not minimum channel length, additional calculation is required to obtain $t_{inv\text{-}pair}$

- Delay per stage (minimum L)

(i) For $\triangle V_{in}$: (a) 3.5τ ($W_p = 2.5W_n$), (b) 2τ ($W_p = W_n$)

(i) For $\triangledown V_{in}$: (a) 3.5τ ($W_p = 2.5W_n$), (b) 5τ ($W_p = W_n$)

> NMOS

$t_{inv\text{-}pair} = 5f\tau$

Delay per stage = $f\tau$ for $\triangle V_{in}$

Delay per stage = $4f\tau$ for $\triangledown V_{in}$

Driving Large Capacitive Loads (Cont.)

Let $y = \frac{C_L}{\square C_g} = f^N$

($\square C_g$: gate capacitance of the first stage inverter)

$\ln y = N \ln a$

$N = \frac{\ln y}{\ln a}$

For N even , total delay

$t_d = \frac{N}{2}\ 7a \leftarrow = 3.5Na \leftarrow$ (CMOS)

(or) $= \frac{N}{2}\ 5a \leftarrow = 2.5Na \leftarrow$ (NMOS)

Delay α Nf $\leftarrow = \frac{\ln y}{\ln a} f \leftarrow$

(for both CMOS and NMOS)

==> For minimum t_d

$\frac{d}{df}\left(\frac{\ln y}{\ln f} f \leftarrow\right) = 0$ => obtain f = e to have the minimum value of Nf $\leftarrow$

Driving Large capacitive Loads (Cont.)

Assuming f = e, then

N = ln(y)

Overall delay t_d

(i) N even: $t_d = 2.5Ne\tau$ (NMOS)

or $t_d = 3.5Ne\tau$ (CMOS)

(ii) N is odd

$$\left.\begin{aligned} t_d &= [2.5(N-1)+1]e\tau \text{ (NMOS)} \\ t_d &= [3.5(N-1)+2]e\tau \text{ (CMOS)} \end{aligned}\right\} \text{ for } \Delta Vin$$

$$\left.\begin{aligned} t_d &= [2.5(N-1)+4]e\tau \text{ (NMOS)} \\ t_d &= [3.5(N-1)+5]e\tau \text{ (CMOS)} \end{aligned}\right\} \text{ for } \nabla Vin$$

** For optimum speed f=e=2.71828
But values from 2 to 10 may be used to obtain more flexibility and reduce cost(# of stages)

Features of BiCMOS Digital Circuit

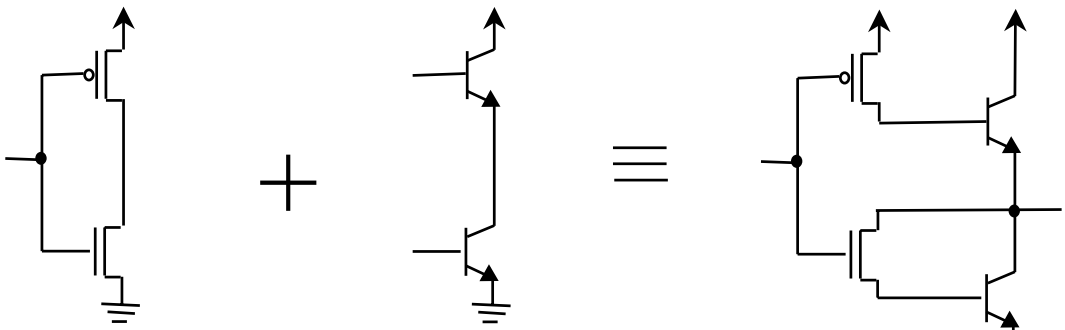
- Combines CMOS and bipolar
  - CMOS
    Low power dissipation
    High density

  - Bipolar
    High drive capability
    Small swing logic

- "System on a chip" is possible
  - Mixed analog/digital
    Analog circuit can be incorporated
  - High voltage, high power interface
    (e.g. sensor, drive, ...) can be
    incorporated if special process is developed

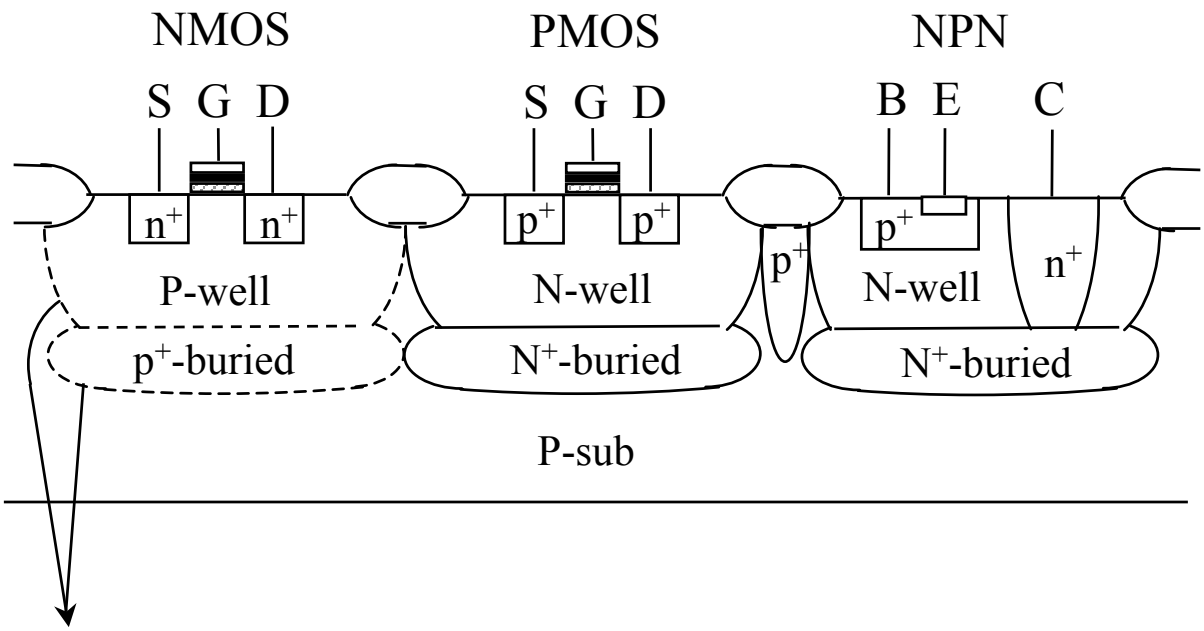
BiCMOS Inverter

- Basic type



CMOS Bipolar(buffer)

- Physical structure

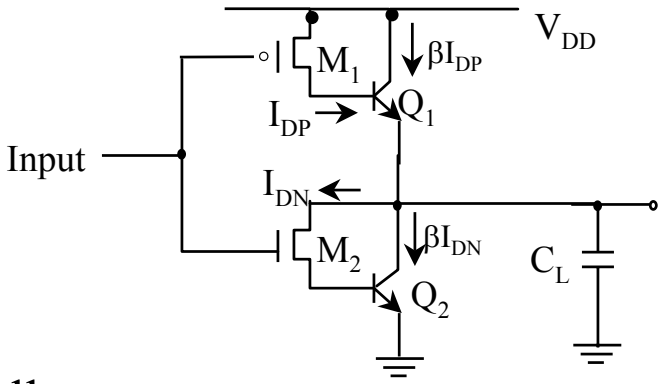


can be added to increase latchup immunity

PMOS drain and NPN base may be merged to reduce
(a) area
(b) capacitance
(c) # of contact

Pull-up of BiCMOS Inverter

- Basic type BiCMOS inverter

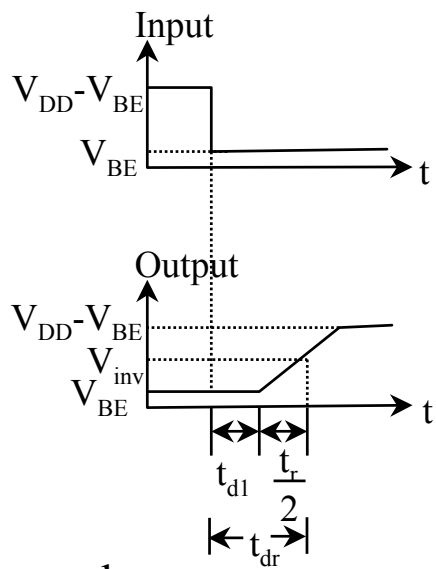


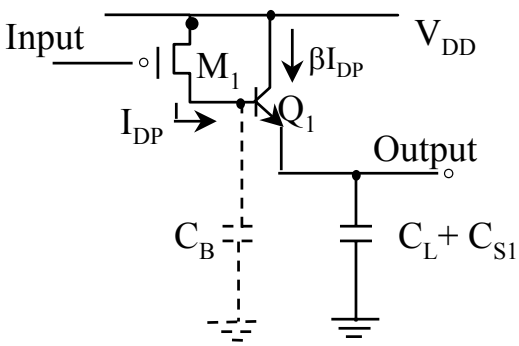
- Pull-up

— assume (initial condition) M_1 & Q_2 are off

1

$V_{BE1} = 0$





C_B is the capacitance at the Q_1 base node

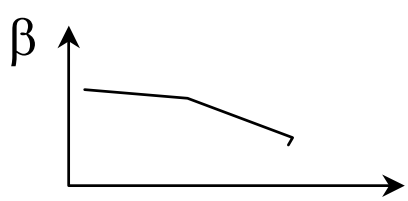
C_{S1} is the capoacitance at the output node when $C_L = 0$

— $t_{d1} = \frac{V_{BE}C_B}{I_{DN}}$ ...time required to turn on Q_1

— $\frac{t_r}{2} = \frac{V_{inv}(C_L+C_{S1})}{\beta I_{DP}}$ ...time required to change C_L TO V_{inv}

where $I_{DP} \approx \frac{\mu_p C_{OX}}{2}(\frac{W}{L})_{M1}(V_{dd}-V_{BE}-V_{tp})^2$

— β vs. Ic



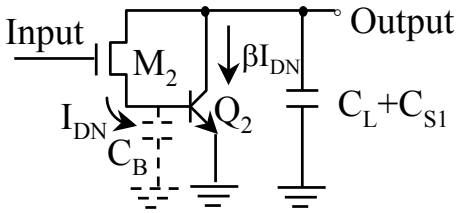
— delay time $t_{dr} = t_{d1} + \frac{t_r}{2}$

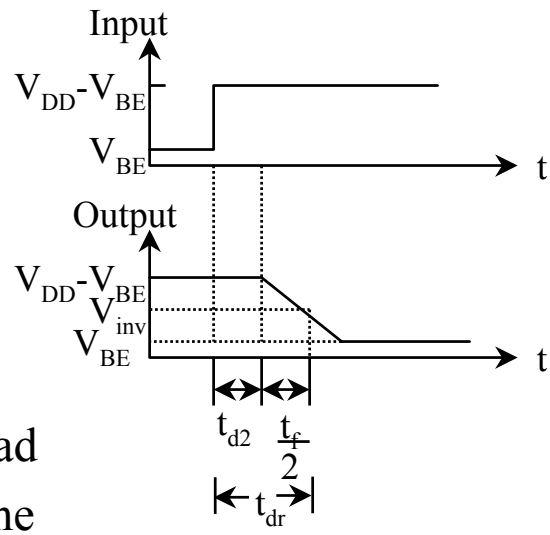
Pull-down of BiCMOS Inverter

- Pull-down

  — assume ❶ M_1 & Q_1 are off ❷ initial condition

  $V_{BE2} = 0$





where C_L is added capacitive load

C_S is the capacitance at the output node when $C_L = 0$

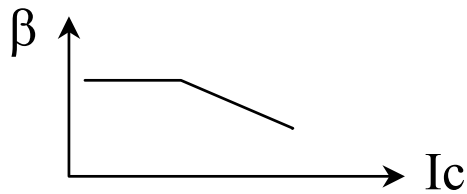
— $t_{df} \simeq \frac{V_{BE} C_B}{I_{DN}} + \frac{V_{inv}\,(C_L + C_{S1})}{\beta I_{DN}} = t_{d2} + \frac{t_f}{2}$

where $I_{DN} \approx \frac{\mu_n C_{OX}}{2} \left(\frac{W}{L}\right)_{M2} (V_{DD} - 2V_{BE} - V_{tn})^2$

$V_{SB} \simeq V_{BE}$

(body effect)

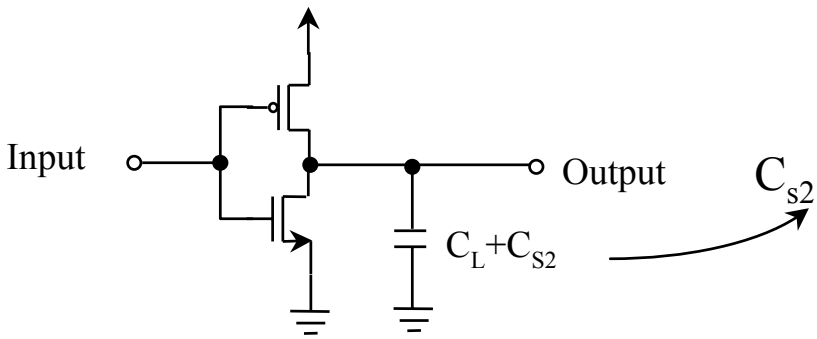
— β vs. Ic

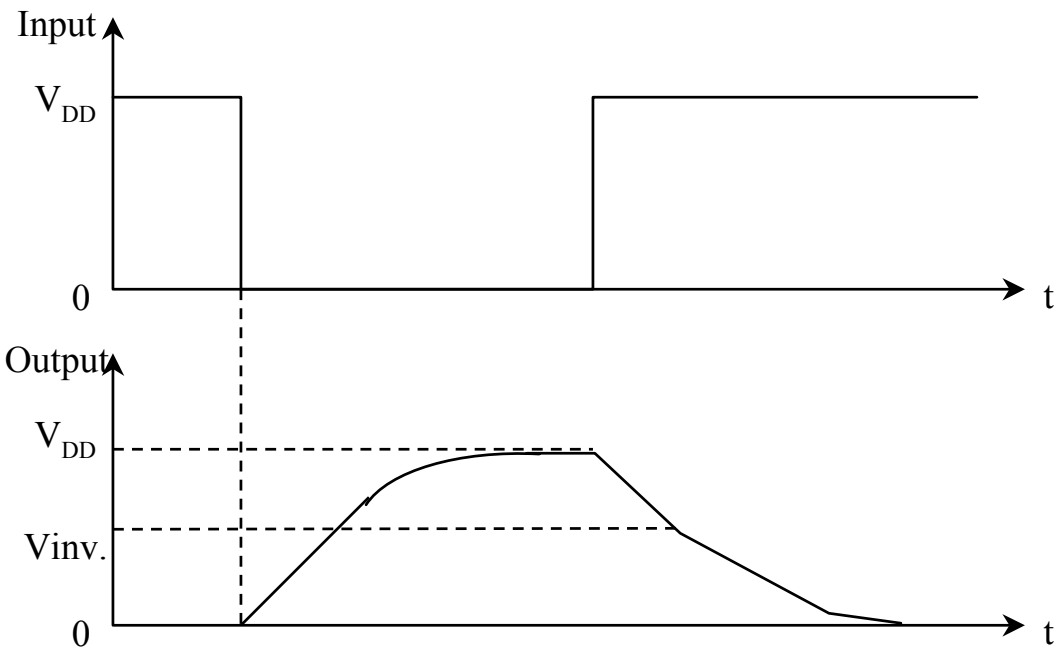


- Adjusting the size of M_1 and M_2, one can obtain $t_{dr} = t_{df}$

Delay Time of CMOS Inverter

- CMOS inverter

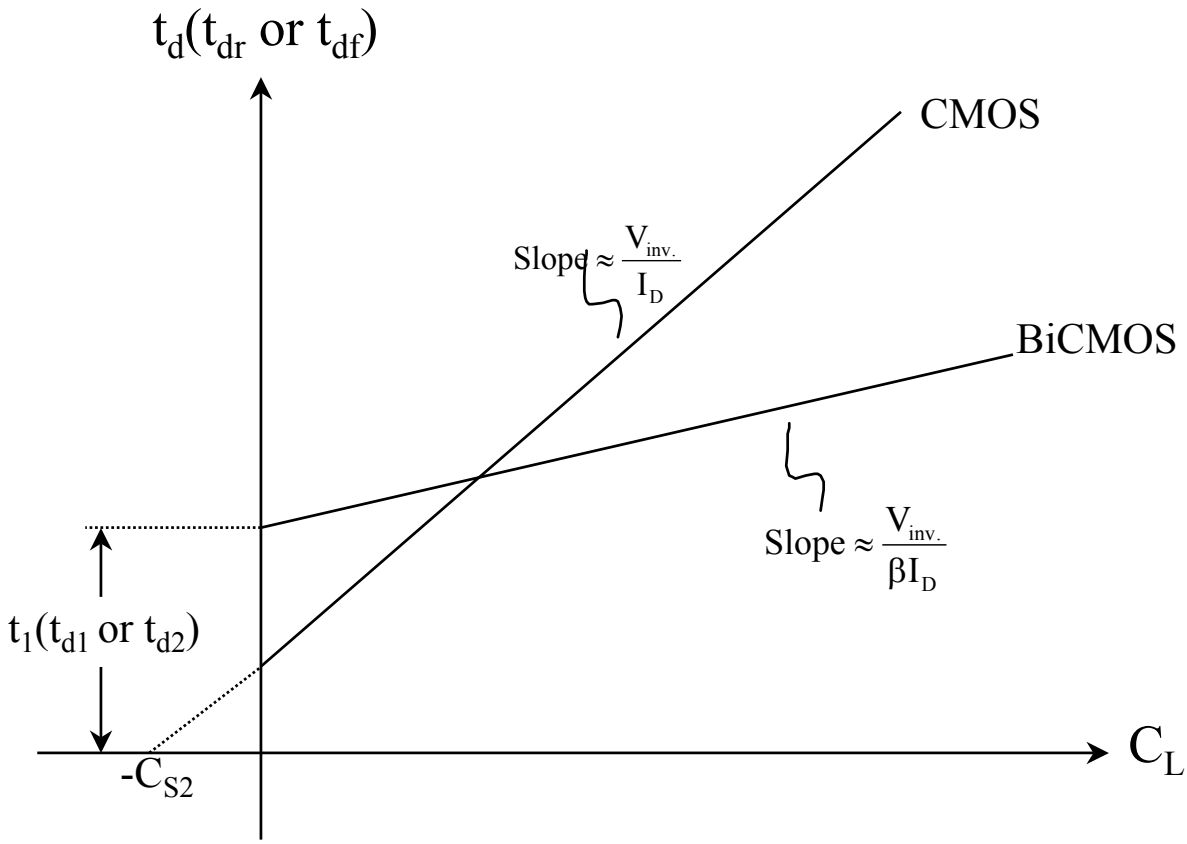




- $t_d \cong \dfrac{V_{inv.}\,(C_L+C_{S2})}{I_D}$ (rough estimation)

where $I_D \cong \dfrac{\mu Cox}{2}\left(\dfrac{W}{L}\right)(V_{DD}-V_t)^2$

Delay Time Comparison between BiCMOS and CMOS

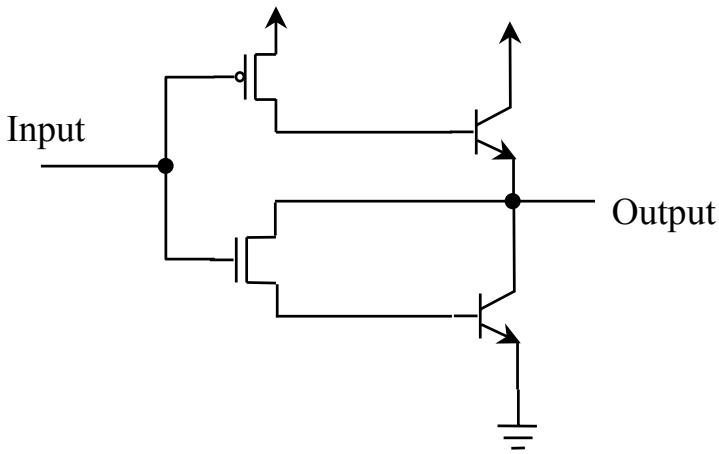


- Rough estimation

$$t_d = \begin{cases} t_1 + \dfrac{V_{inv}(C_L + C_{s1})}{\beta I_D}; BICMOS \\ \dfrac{V_{inv}(C_L + C_{s2})}{I_D}; CMOS \end{cases}$$

Drawbacks of Basic-Type Inverter

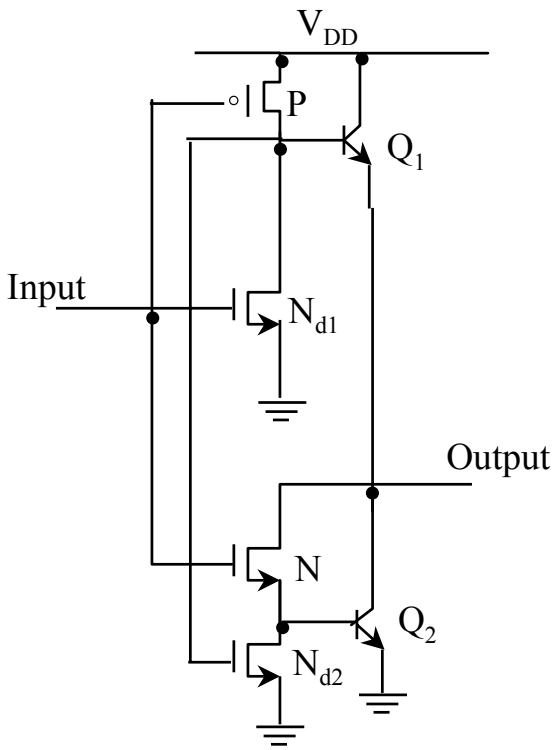
- No path to discharge the bases



- Not full swing, i.e. not (0~V_{DD})
  - swing: V_{BE}~ (V_{DD}-V_{BE})
  - Incompatible with CMOS logic
    As described in the introduction, most digital circuits of a large chip use CMOS logic instead of BiCMOS for two reasons:
    1. high density
    2. low power

BiCMOS Inverter with MOS Discharge

- Conventional BiCMOS inveretr
- First proposed by Hung-Chung Lin
- Swing : $V_{BE} \sim (V_{DD} - V_{BE})$



- Q_1 is reverse-biased when output = "low"

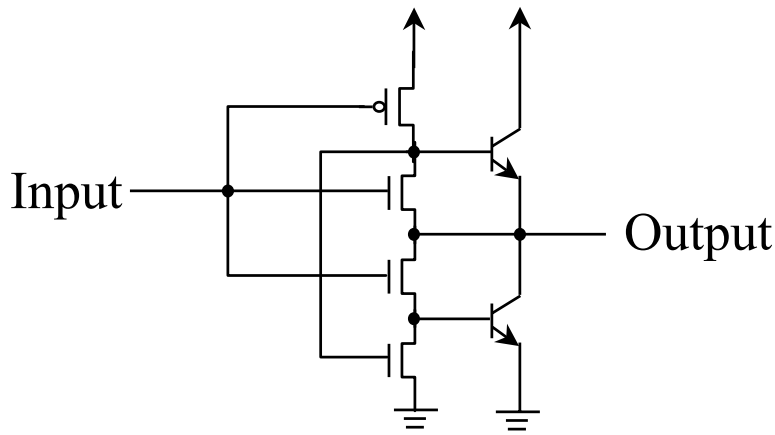
  (i.e. $V_{BE1} < 0$ when Output = V_{BE})

  => longer time to turn on Q_1

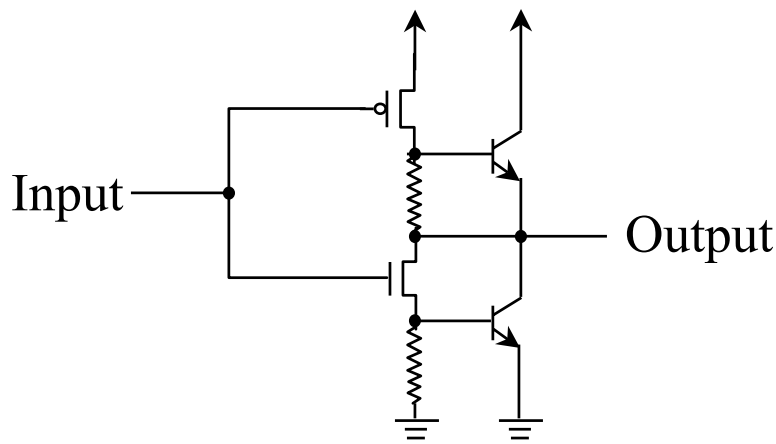
  when Output = "Low" $\longrightarrow$ "High"

Improved BiCMOS Inverters

- Discharges the bases
  - — Transistor discharge
    => Swing：V_{BE}～(V_{DD}-V_{BE})



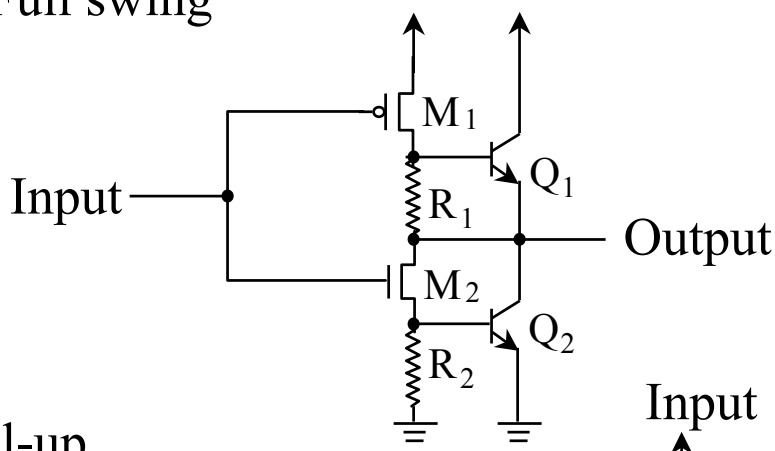
  - — Resistor discharge
    => Full swing



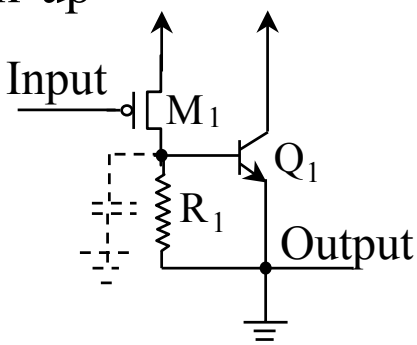
  - — Many other examples

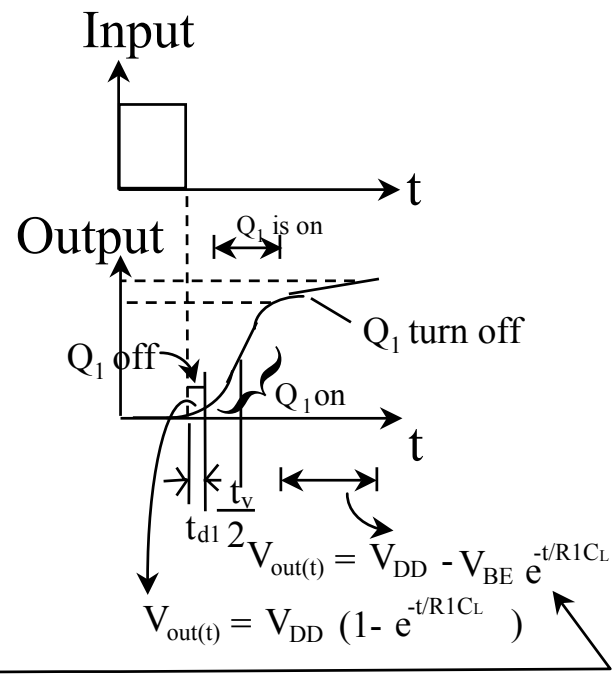
Resistor-Discharge BiCMOS Inverters

- a. Path to discharge the bases
  b. Full swing



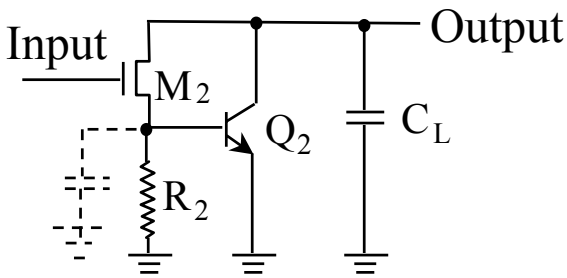
- Pull-up

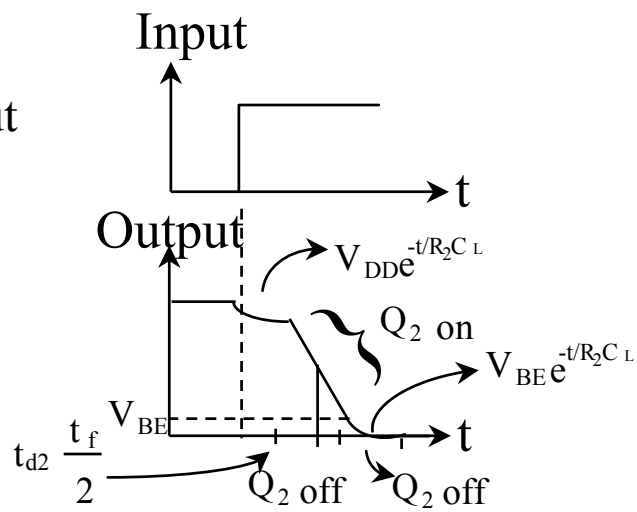




M_2 turned off by input initially
Q_2 discharged initially
Q_1 turned off during
(base is discharged through R_1)

- Pull-down





Alternative Full-Swing BiCMOS Inverters

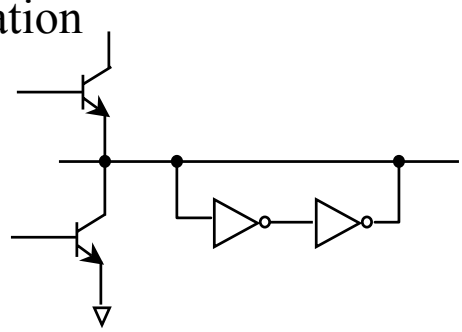
[L. Wissel CICC 1992]

CMOS-compatible BiCMOS logic

Full-swing "finisher" is required

— Latch

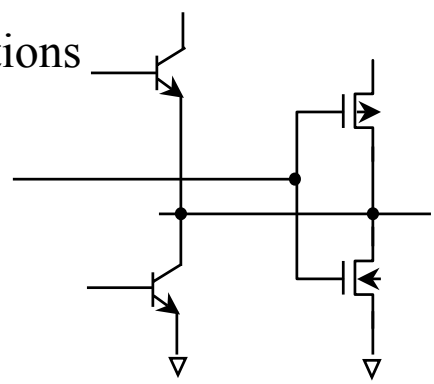
Increased power dissipation



— CMOS Parallel

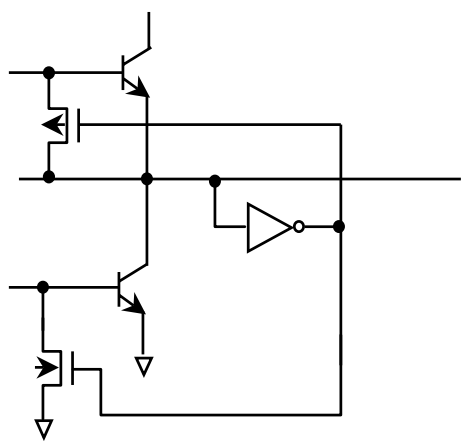
High input capacitance

Not partical for all functions



— "Feedback"

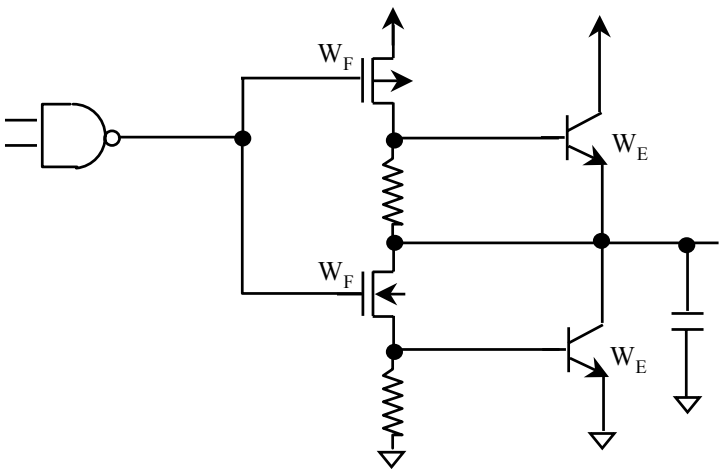
Added capacitance on base nodes



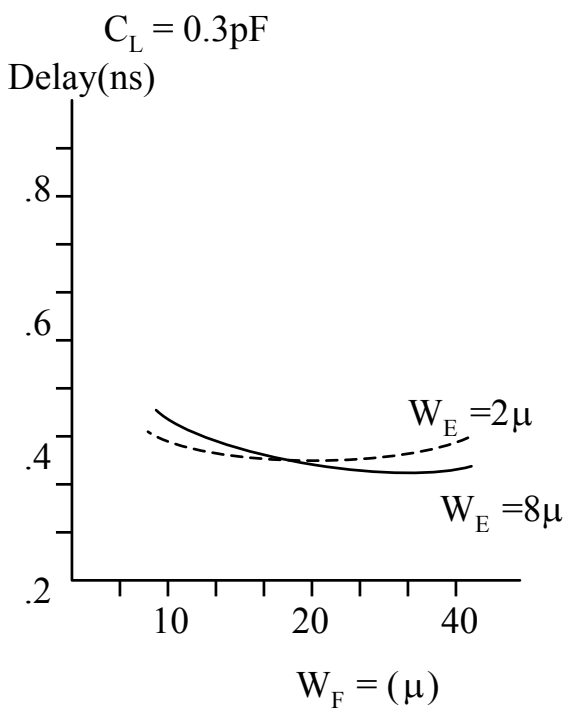
Design Example

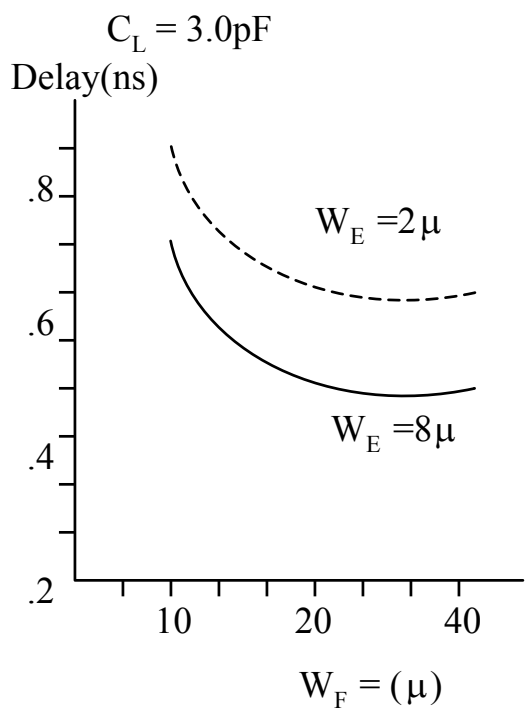
[L. Wissel CICC 1992]

- BiCMOS circuit FET vs. NPN size optimization
  - Model



  - Delay vs. FET width
    (Emitter width as parameter)

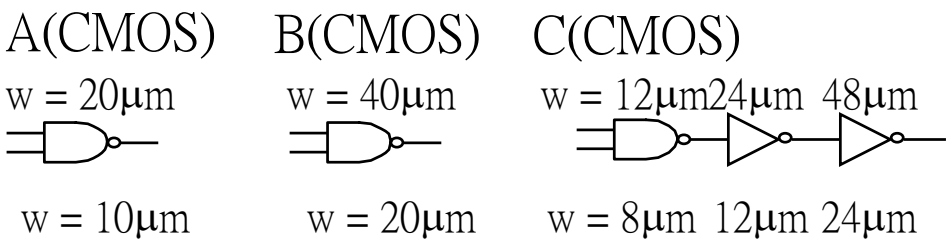




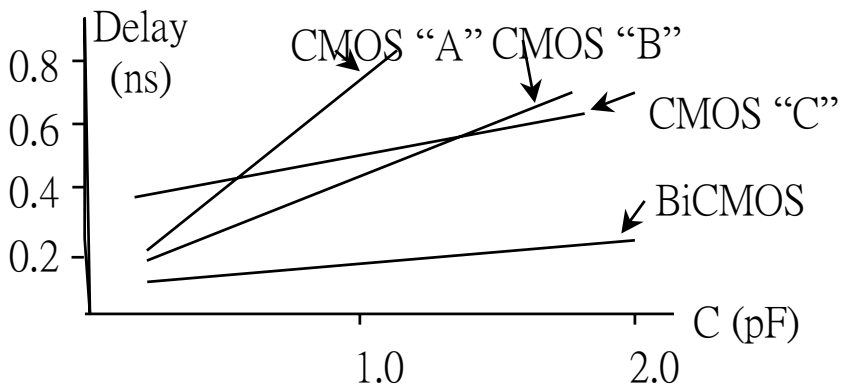
Design Example (Cont.)

[L. Wissel CICC 1992]

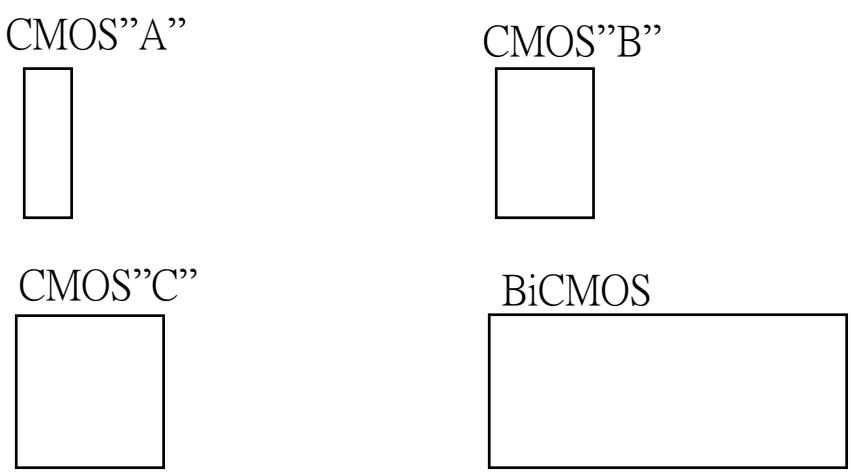
- Driving large capacitive load
  - CMOS-BiCMOS comparison
  - layout and speed



- Performance

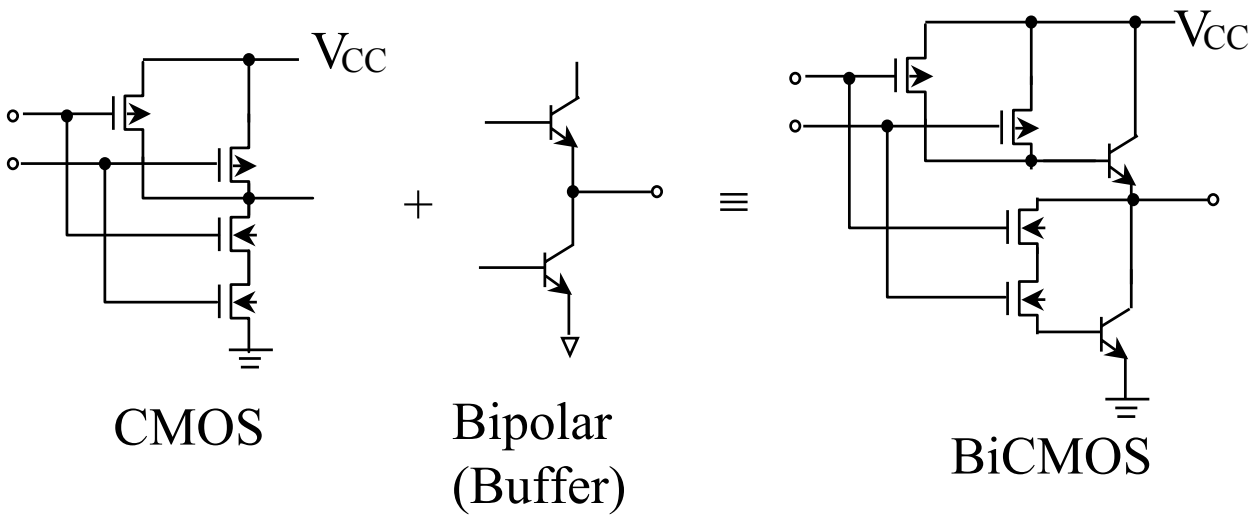


- Layout size



BiCMOS Gate

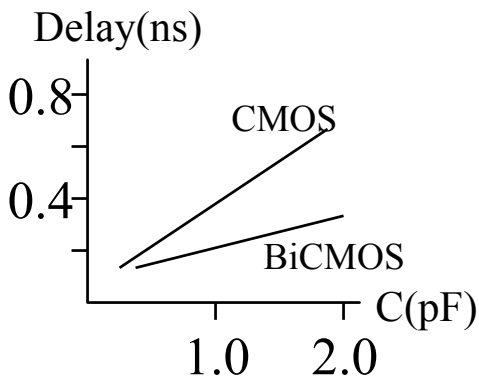
- Basic type



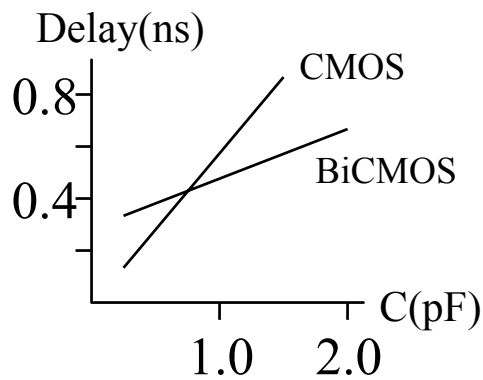
- Similar methods as used in the inverter design
  1. delay time calculation
  2. path to discharge the bases
  3. full-swing

Power-Supply Sensitivity

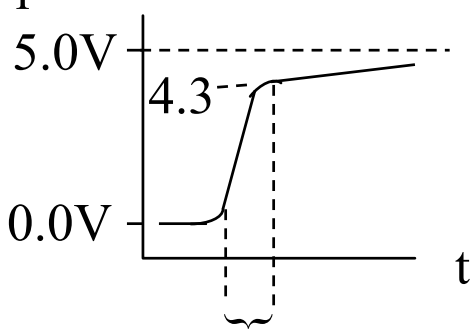
V_{DD} = 5.0V



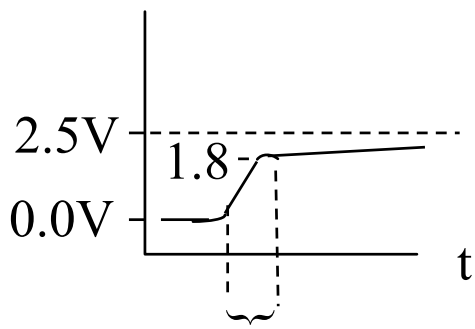
V_{DD} = 2.5V



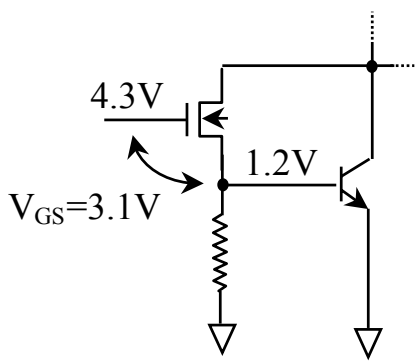
Input Waveform

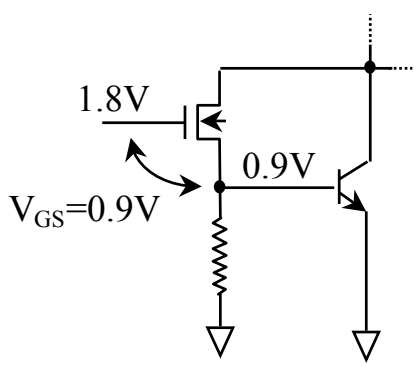


Critical switching window



Critical switching window





Voltage Scaling

- BiCMOS (full swing)
  - $\beta I_{DP} = \beta K_P (V_{DD} - V_{tp})^2 \qquad where \qquad k = \frac{\mu C_{ox}}{2}\frac{W}{L}$
  - $\beta I_{DN} = \beta K_N (V_{DD} - V_{BE} - V_{tn})^2$

    $= \beta K_n V_{DD}{}^2 (1 - \frac{V_{BE}}{V_{DD}} - \frac{V_{tn}}{V_{DD}})^2$ ------- (1)

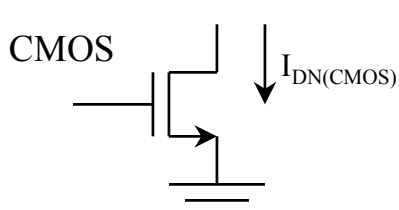
- CMOS
  - $I_{DP} = K_P (V_{DD} - V_{tp})^2$
  - $I_{DN} = K_n (V_{DD} - V_{tn})^2$

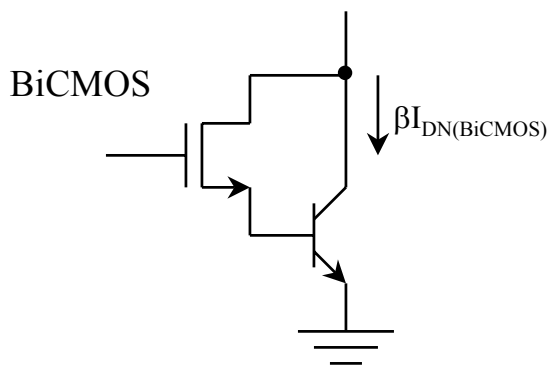
    $= K_n V_{DD}{}^2 (1 - \frac{V_{tn}}{V_{DD}})^2$ ------- (2)

- From (1) & (2)

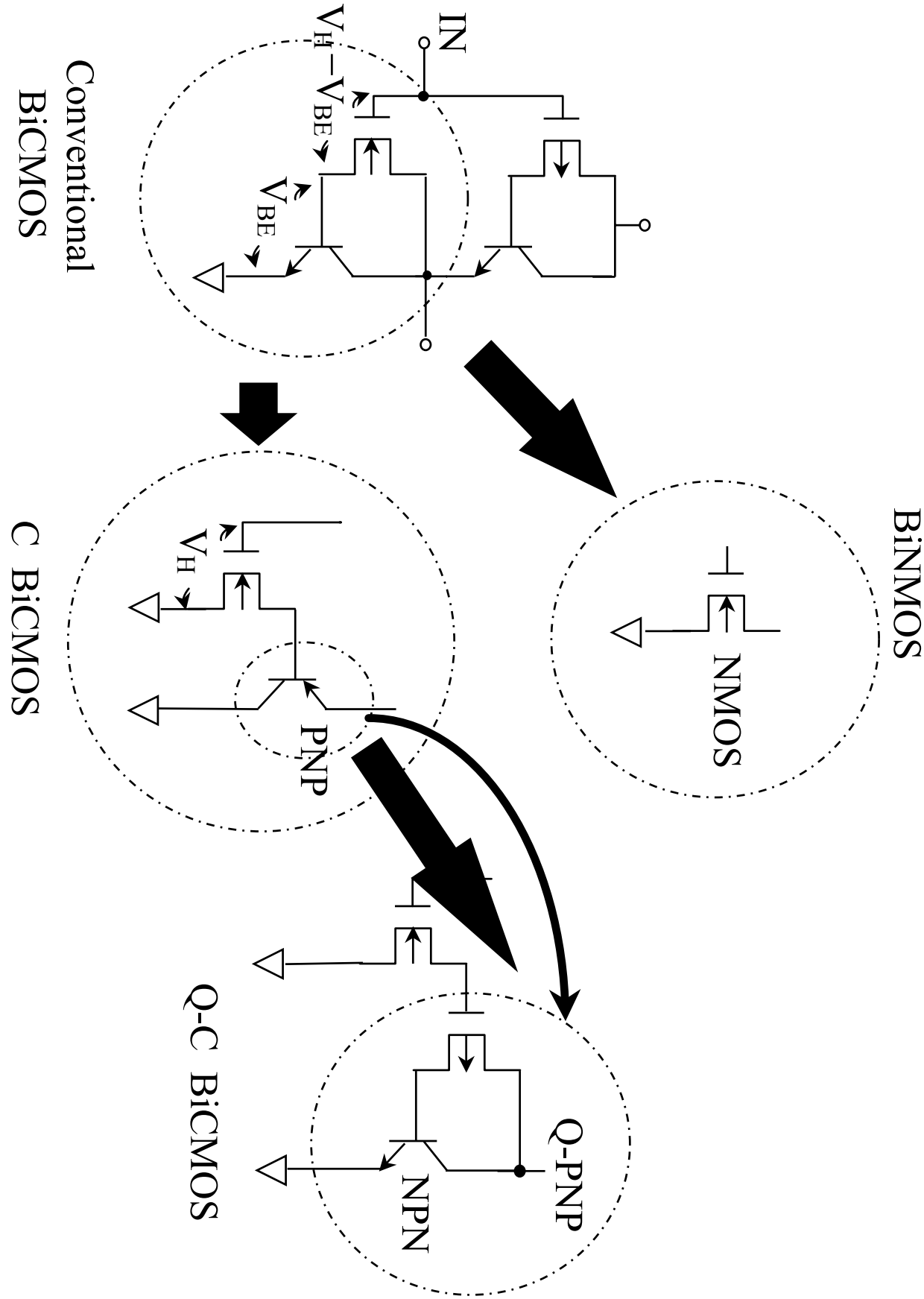
$$V_{DD}\downarrow \Rightarrow \left(\frac{1 - \frac{V_{BE}}{V_{DD}} - \frac{V_{tn}}{V_{DD}}}{1 - \frac{V_{tn}}{V_{DD}}}\right)\downarrow \Rightarrow \frac{I_{DN(BiCMOS)}}{I_{DN(CMOS)}}\downarrow$$

$$\Rightarrow \frac{\beta I_{DN(BiCMOS)}}{I_{DN(CMOS)}}\downarrow \Rightarrow \frac{t_{d(BiCMOS)}}{t_{d(CMOS)}}\downarrow$$



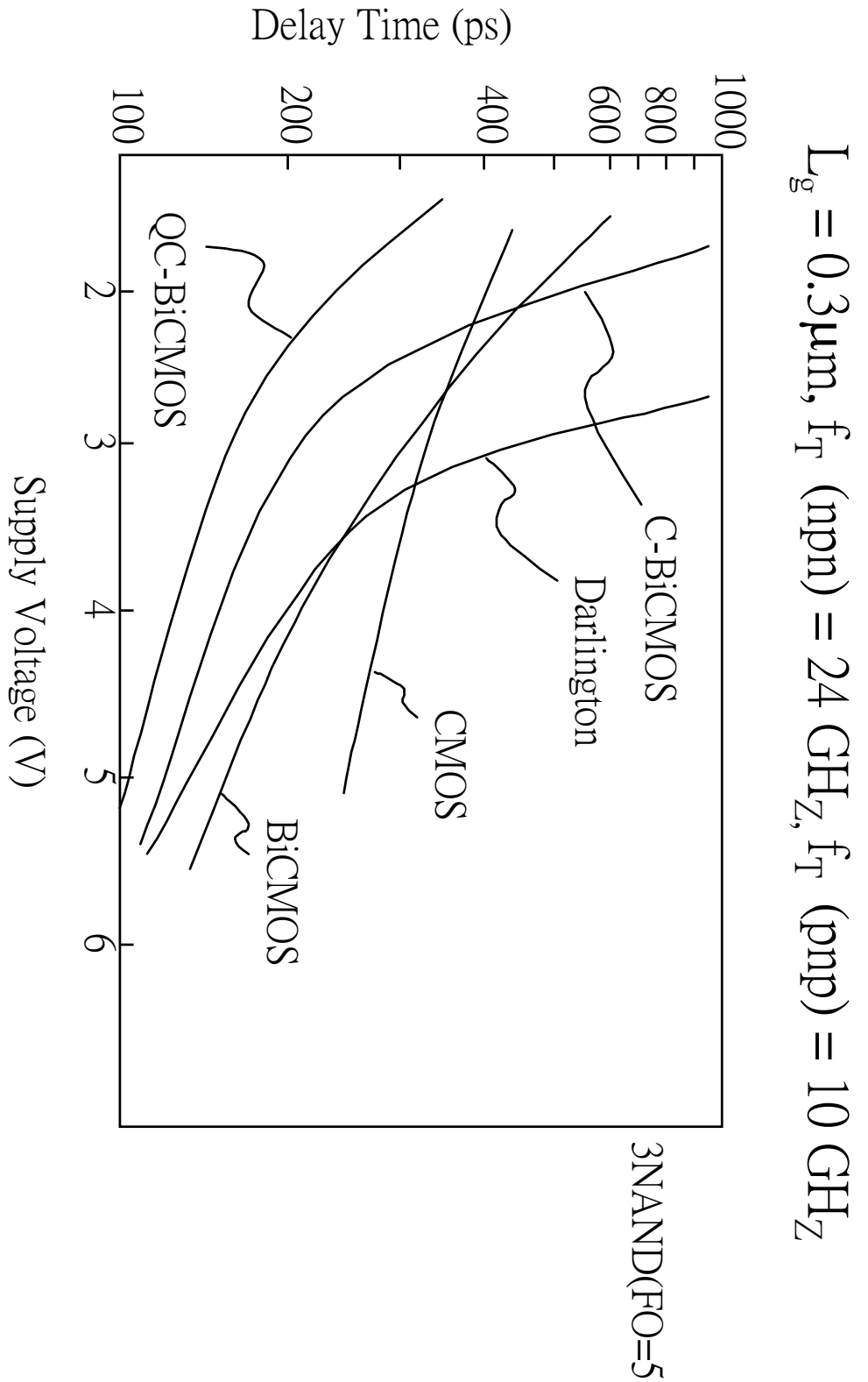


Low-Voltage BiCMOS Gates



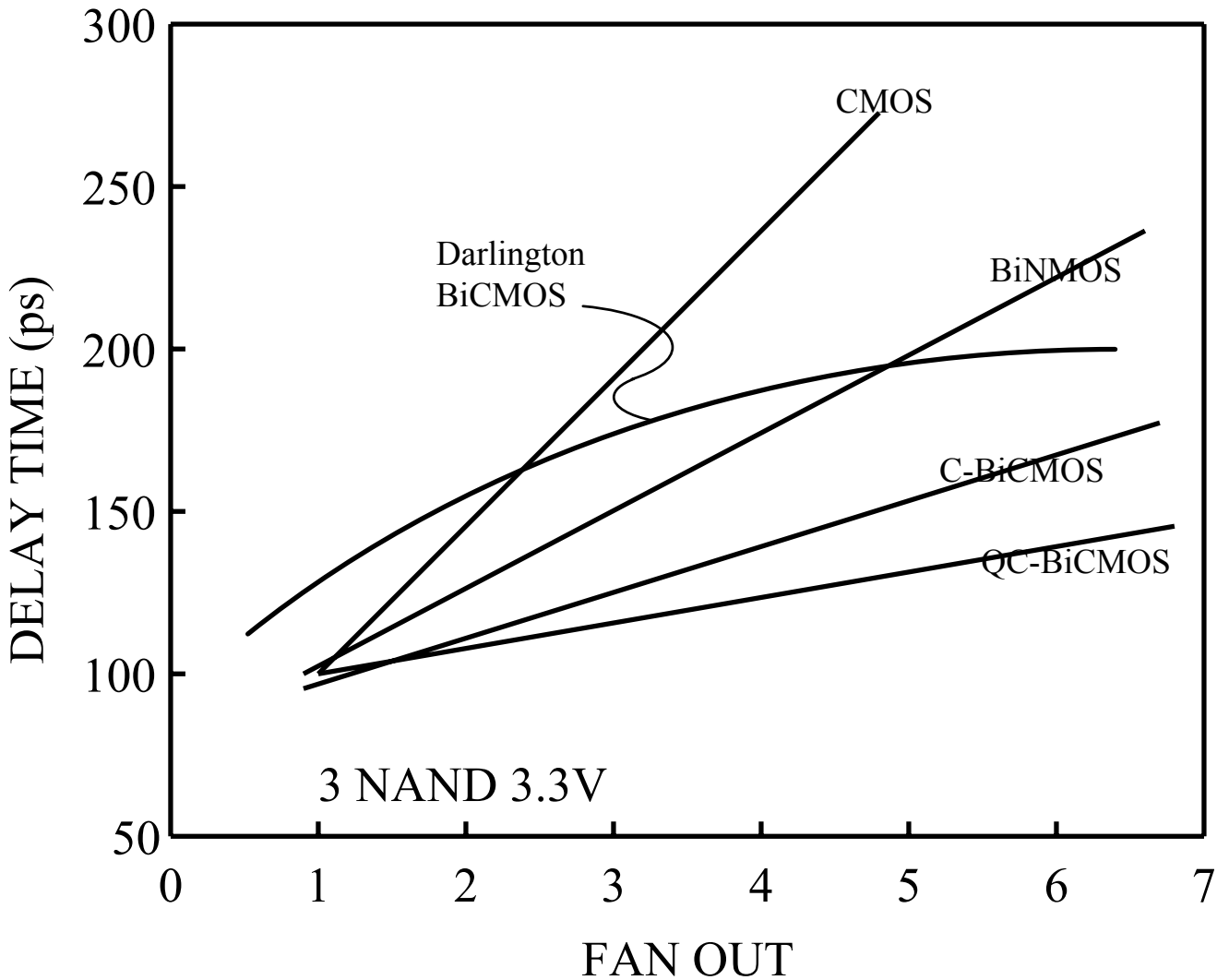
Delay Time

[Y.Kobayshi]



Delay Time (Cont.)

[Y.Kobayshi]

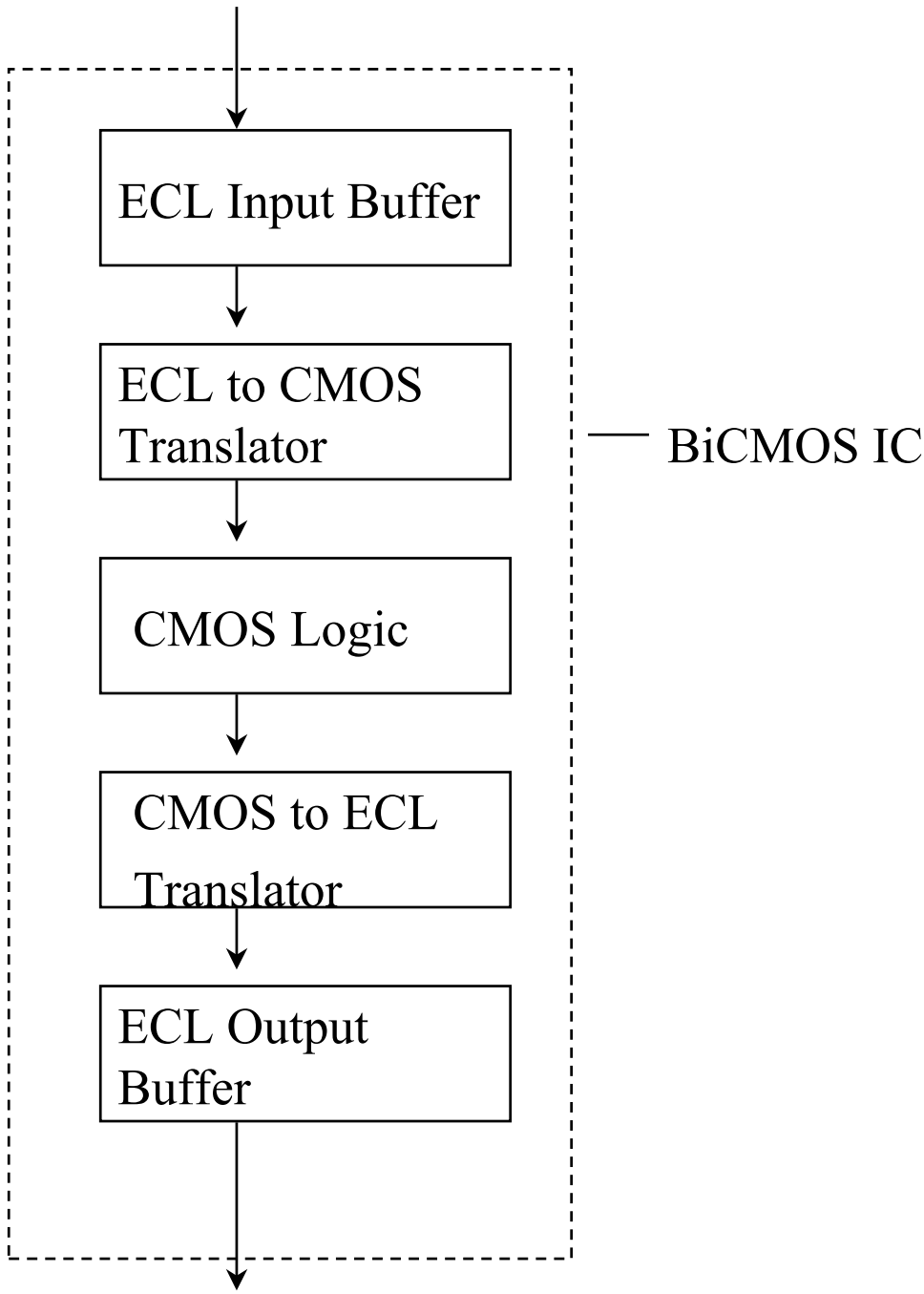


TTL, ECL and CMOS Logic

- Level conversion circuits for different logics
- Input BiCMOS buffers of various logics
- Output BiCMOS buffers of various logics
- Example : ECL-CMOS interface

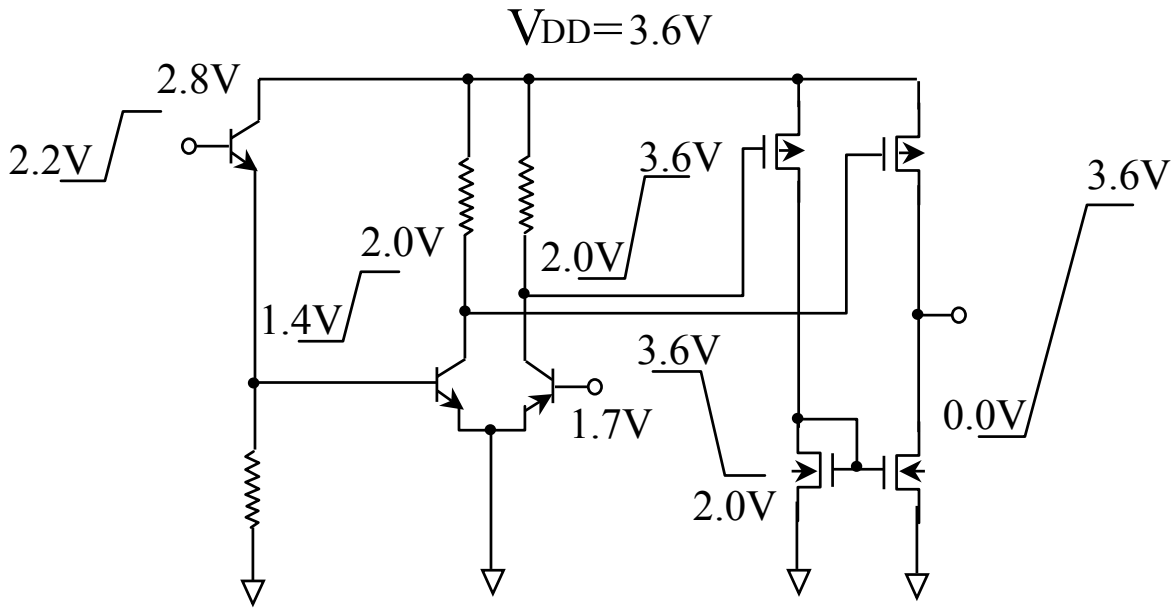
High Speed BiCMOS IC

- ECL I/O example

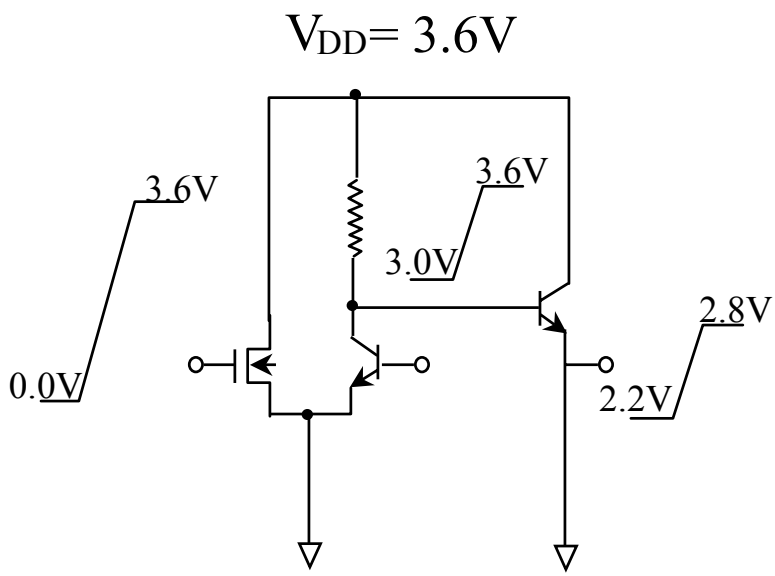


ECL-CMOS Interface

- ECL-to-CMOS converter



- CMOS-to-ECL converter

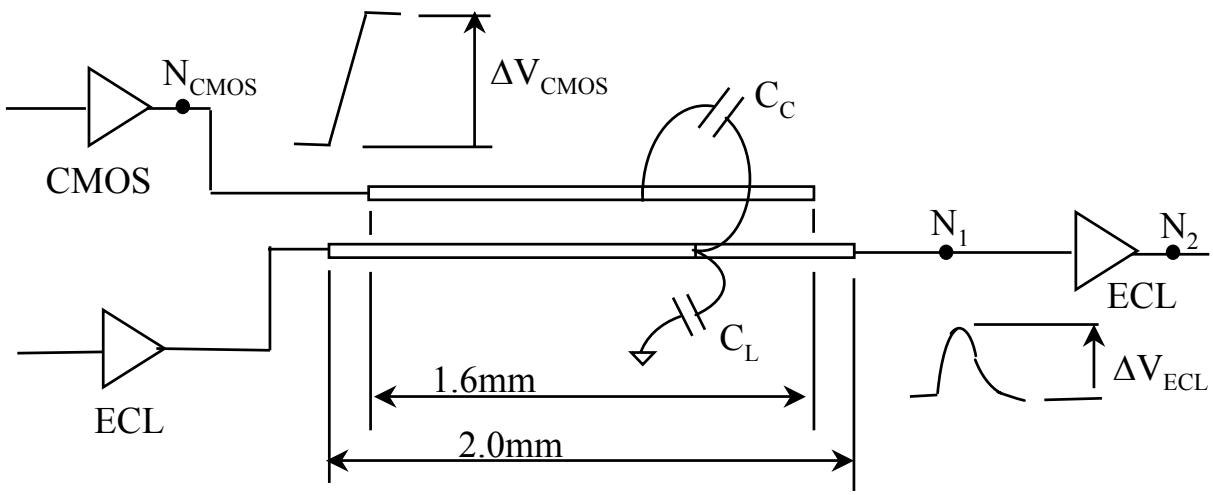


Noise Coupling of Mixed ECL/CMOS Circuits

[L.Wissel CICC 1992]

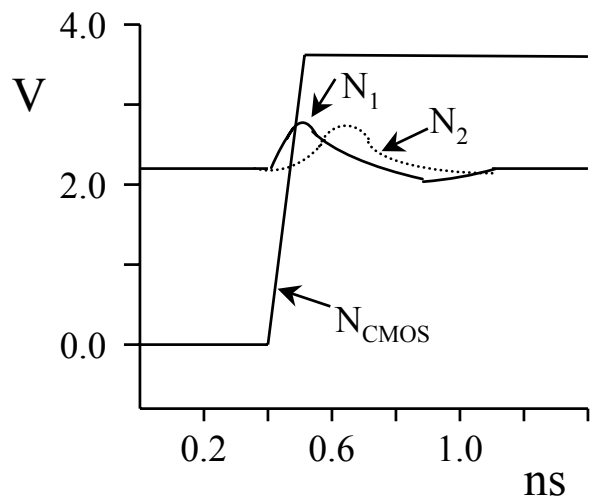
- Large CMOS waveform couples noise into ECL signal lines

- Model
  - 2 mm quiet ECL line, with partial adjacency to a switching CMOS line



C_L=0.4pF, C_C=0.07pF

$$\Delta V_{ECL} = \left(\frac{C_C}{C_L + C_C}\right) \Delta V_{CMOS}$$



  - CMOS switching can induce noise as large as ECL signal