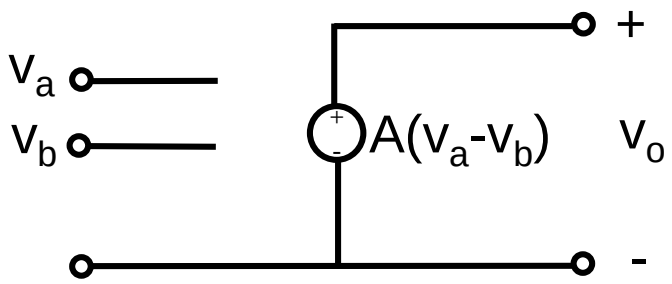
Operational Amplifiers

Operational Amplifiers

- Ideal voltage op-amp
  - Voltage-controlled voltage source
  - Infinite voltage gain
  - Infinite input impedance
  - Zero output impedance
  - No noise
  - Infinite bandwidth
  - No offset voltage
  - Infinite CMRR



- Differences between the ideal op-amp and real op-amp
  - Finite gain (practical op-amps, $A \approx 10^2 \sim 10^4$, i.e., 40~80dB)
  - Finite linear range($V_{DD} > V_o > V_{ss}$)

Operational Amplifiers (Cont.)

- Offset voltage:
  - Ideal op-amps $V_a=V_b \Rightarrow V_o=0$
  - Real op-amps

    This is not exactly true and $V_o \neq 0$ is always occurred.
  - Input offset voltage V is defined as the differential input voltage needed to restore $V_o=0$.
  - For MOS op-amps, V_{offset} is about 5-15 mV.

    For BJT op-amps, V_{offset} is about 1-2 mV.

- Common Mode Rejection Ratio(CMRR)
  - The CMRR measure how much the op-amp can suppress common-mode signal at its input.
  - Typically CMRR=60~80dB common-mode input voltage: $V_{in,c}=(V_a+V_b)/2$

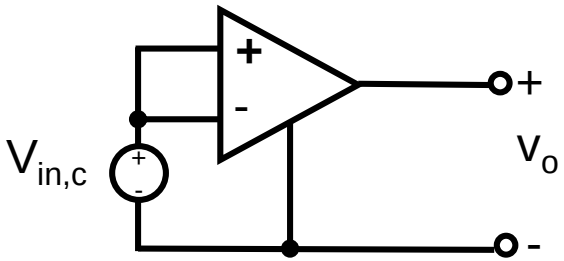
Operational Amplifiers (Cont.)

differential-mode input voltage : $V_{in,d} = V_a - V_b$

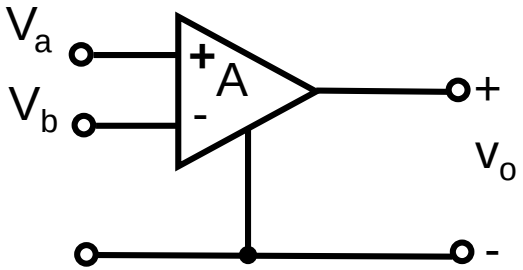
differential gain $A_d = \frac{V_o}{V_{in,d}}$

common-mode gain $A_c = \frac{V_o}{V_{in,c}}$

CMRR=(A_d/A_c) or $20\log_{10}(A_d/A_c)$ in dB



common-mode input

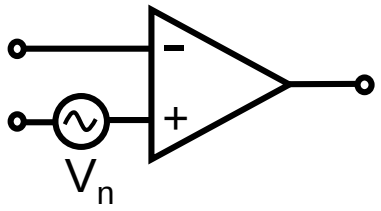


differential-mode input

- Frequency Response:
  - Limited bandwidth(100MHz unity-gain bandwidth is typical)
  - Gain decreases at high frequency, because
    - Stray capacitances
    - Finite carrier mobilities

Operational Amplifiers (Cont.)

- Slew Rate (typically, for MOS op-amps, 1~50V/μs)
  - The maximum rate of output change dV_o/dt
  - For a large input voltage, some transistors may be driven out of their saturation regions or completely cut off. As a result, the output will follow the input at a slower finite rate.
- Nonzero Output Resistance
  - 0.1~5kΩ → typical value
  - Large R will limit frequency response(i.e., speed) when a capacitor is connected to its output.
- Noise
  - Noisy transistors in op-amps give rise to a noise voltage V_{on} at the output of op-amp.
  - Equivalent input noise voltage=$V_{on}/A=V_n$

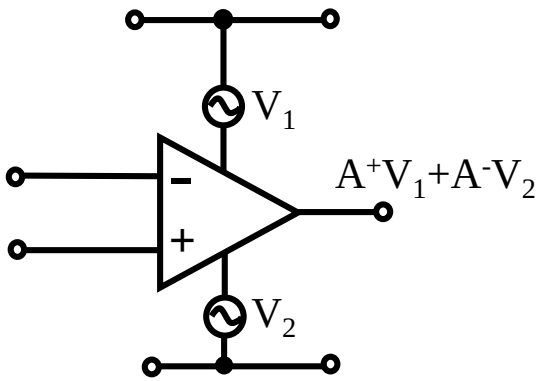


Operational Amplifiers (Cont.)

- Dynamic Range(DR) = $20\log_{10}\left(\frac{V_{in,max}}{V_{in,min}}\right)$
  - Open loop~30-40dB

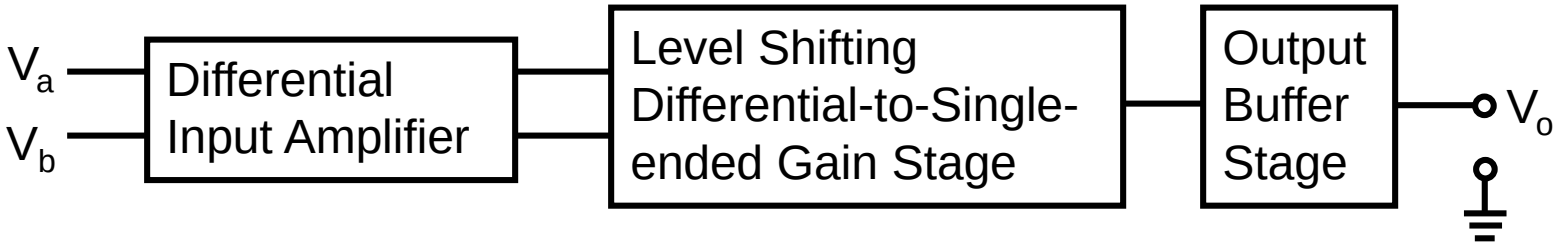
    $V_{in,min} \approx \sqrt{\overline{V_n^2}} \sim 30\mu V$

    $V_{in,max} \approx \frac{V_{dd}}{A}$
  - Close loop~100dB has larger DR than open loop.
  - Can be increased by using correlated double sampling (CDS)
- PSRR (Power supply rejection ratio)
  - $PSRR^+ = 20\log_{10}\left(\frac{A_d}{A^+}\right)$
  - $PSRR^- = 20\log_{10}\left(\frac{A_d}{A^-}\right)$



- DC Power Dissipation(0.1mW~5mW)

Practical OPAMP



- Differential amp provides
  - High input impedance
  - Large CMRR and PSRR
  - Low offset voltage
  - Low noise
  - High gain

- 2^{nd} block provides
  - Level shift
  - Added gain
  - Differential-to-single-ended conversion

Practical OPAMP (Cont.)

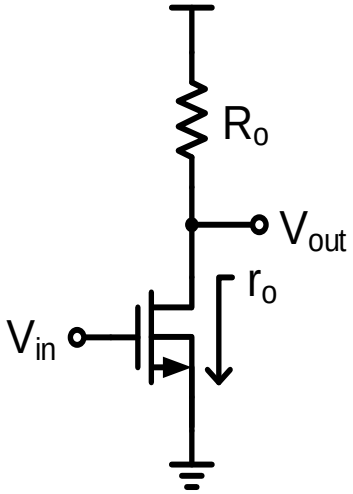
- Output stage provides
  - Low output impedance
  - Large driving capability

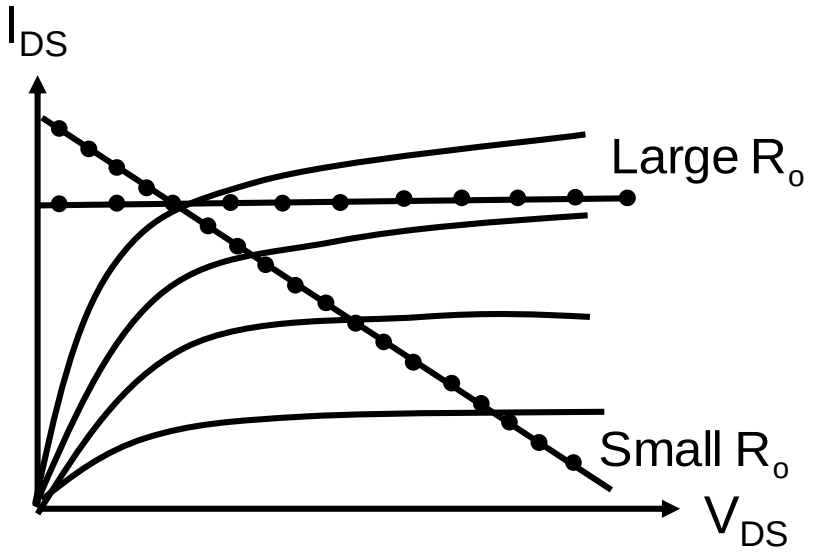
- Output stage usually consumes more power than the other stage.

CMOS Amplifier with Resistive Load

- Resistor Load

$$A = g_m\left(R_o // r_o\right)$$
$$\approx g_m R_o$$
$$\propto \frac{I_D R_o}{V_{ov}}$$

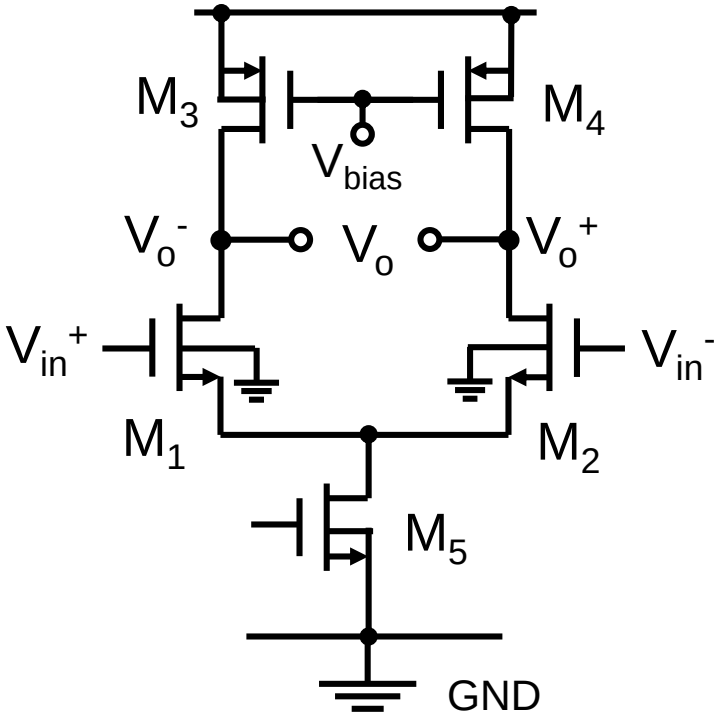


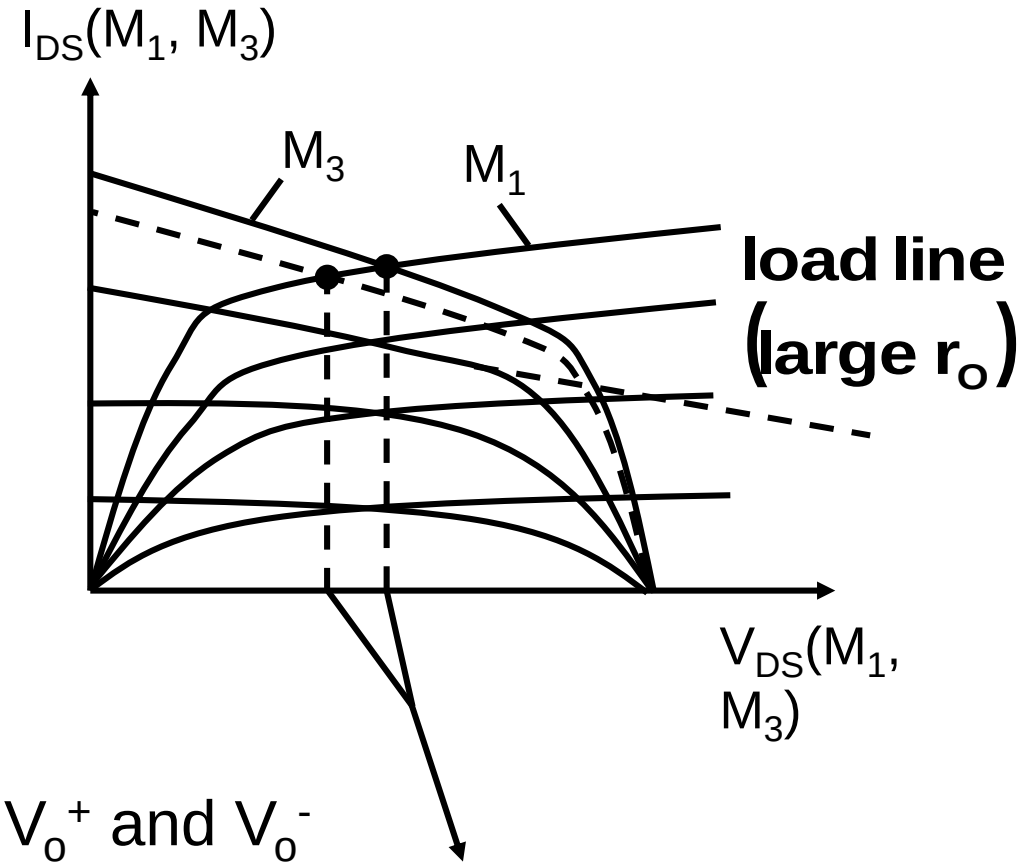


- For high gain
  - High $I_D R_o$
    - High $I_D R_o$ means large voltage drop on R_o
    - Large power supply
  - High R_o reduces speed
  - Use active loads to overcome the above problems.

CMOS Amplifier with Active Load

- With external bias





  - Why not?

    → Quiescent point of V_o^+ and V_o^- can't be determined due to process variations

CMOS Amplifier with Active Load (Cont.)

- Self-biased active load, where quiescent V_o less sensitive to $\frac{M_1}{M_2}$ variations
- Performs differential gain and differential to single-ended
- Differential gain A_{dm}

$$g_{m,M1}, g_{m,M2}, g_{m,M3}, g_{m,M4} >> \frac{1}{r_{ds}}$$

$$r_{out} \approx r_{ds2} // r_{ds4}$$

$$A_{dm} \approx g_{m1}\left(r_{ds2} // r_{ds4}\right)$$

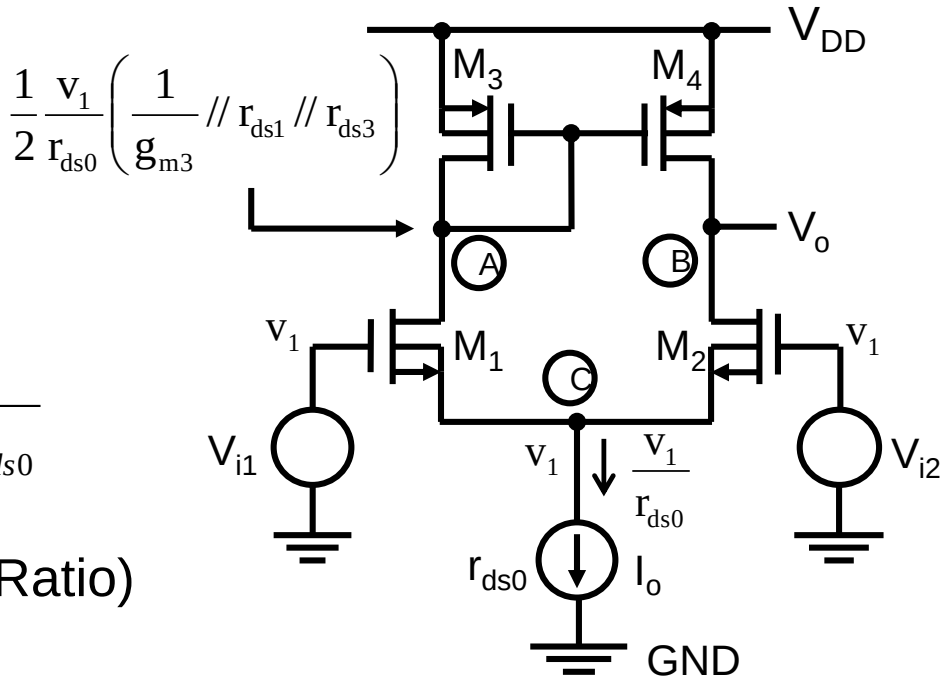
- Common-mode gain A_{cm}

$$A_{cm} \approx \frac{1}{2}\frac{1}{r_{ds0}}\left(\frac{1}{g_{m3}} // r_{ds1} // r_{ds3}\right) \approx \frac{1}{2 g_{m3} r_{ds0}}$$

- CMRR(Common-Mode Rejection Ratio)

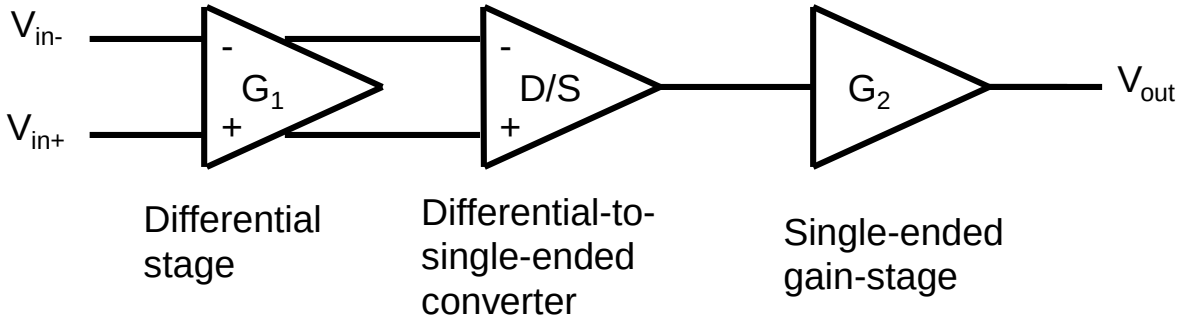
$$CMRR = \frac{A_{dm}}{A_{cm}} \approx 2 g_{m1}\left(r_{ds2} // r_{ds4}\right) g_{m3} r_{ds0}$$

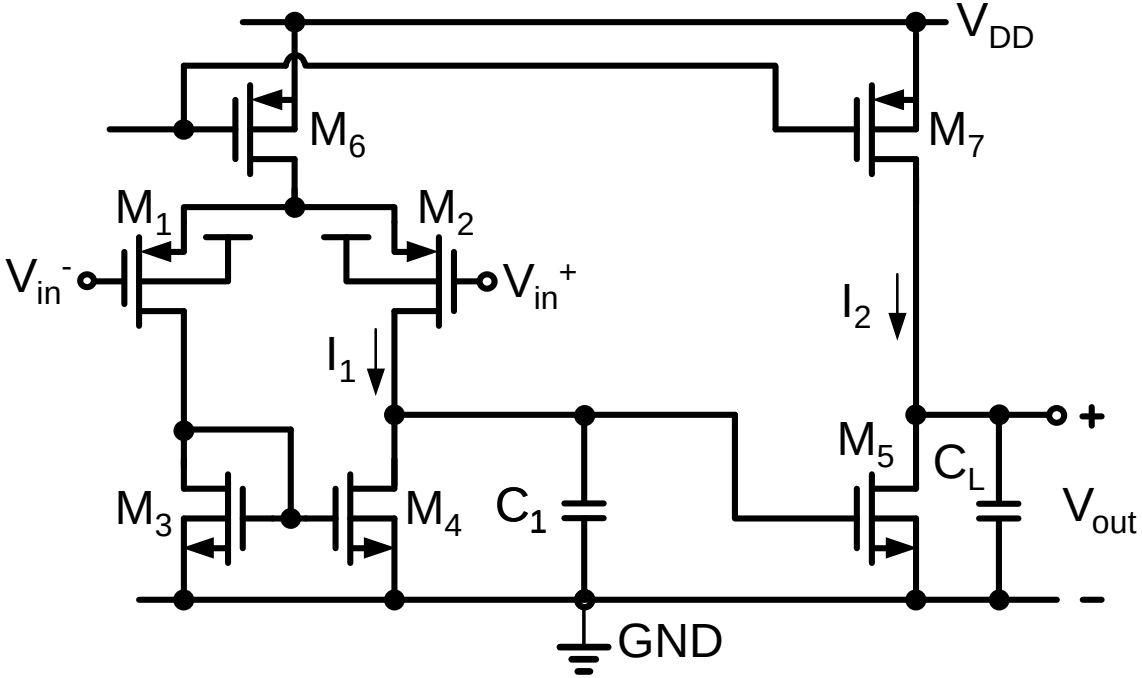
- Model of A_{cm}



Uncompensated CMOS OPAMP

- Basic building blocks of an operational amplifier





Uncompensated CMOS OPAMP (Cont.)

$$A_{V1} = -g_{m1}R_{o1} = -g_{m1}(r_{ds4} // r_{ds2})$$

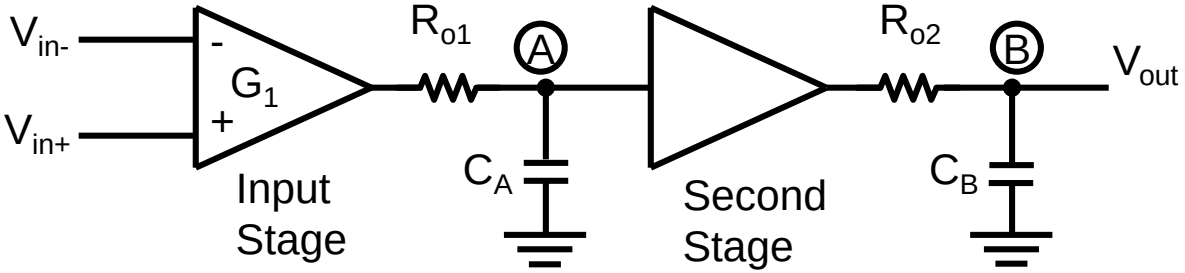
$$A_{V2} = -g_{m6}R_{o2} = -g_{m6}(r_{ds6} // r_{ds7})$$

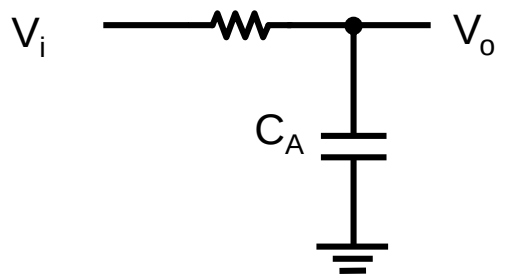
where R_{o1} is low frequency output impedance of node A

R_{o2} is low frequency output impedance of node B

$C_A(C_B)$ is capacitive loading at node A(B)

- Block diagram showing the origin of the dominant poles





$$\Rightarrow \frac{V_o(s)}{V_i(s)} = \frac{\frac{1}{sC_A}}{R_{o1} + \frac{1}{sC_A}}$$

Uncompensated CMOS OPAMP (Cont.)

$$A_V(s) = \frac{V_{out}(s)}{V_{in}^{+}(s) - V_{in}^{-}(s)} = A_v(0) \frac{\frac{1}{sC_A}}{R_{o1} + \frac{1}{sC_A}} \frac{\frac{1}{sC_B}}{R_{o2} + \frac{1}{sC_B}}$$

$$= A_v(0) \frac{1}{(1 + \frac{s}{S_A})(1 + \frac{s}{S_B})}; S_A = \frac{-1}{R_{o1}C_A}; S_B = \frac{-1}{R_{o2}C_B}$$

- S_A and S_B are dominant poles since R_{o1} and R_{o2} are normally large.
- The effects of other poles are usually negligible.

Bode Plot

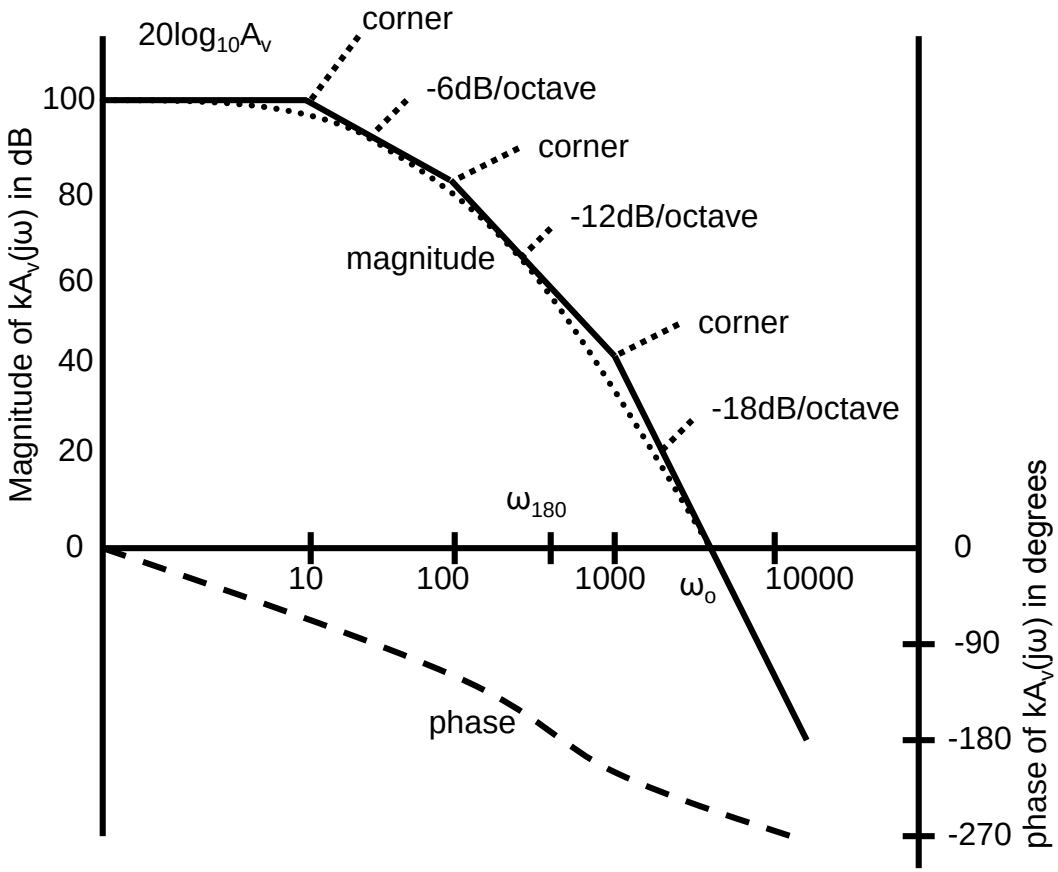
$$kA_v(j\omega) = \frac{A_o}{(1+j\frac{\omega}{s_1})(1+j\frac{\omega}{s_2})(1+j\frac{\omega}{s_3})}$$

- Example:

  $A_o=10^5$, $s_1=-10$ rad/sec

  $s_2=-10^2$ rad/sec

  $s_3=-10^3$ rad/sec



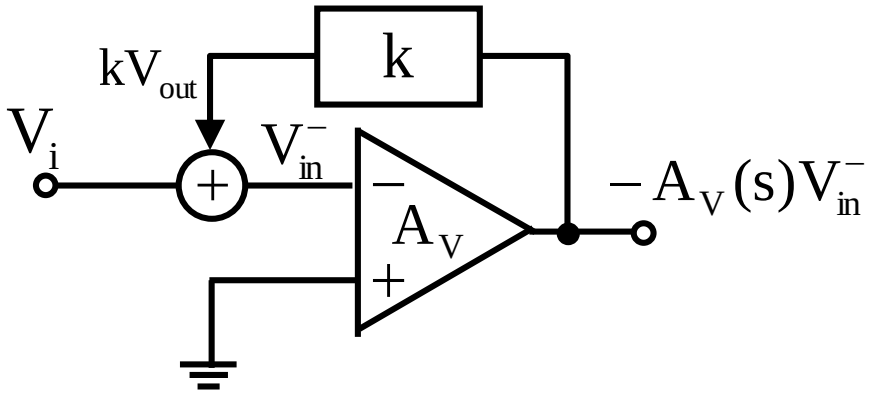
An example of a Bode plot for three real poles

Stability and Compensation of OPAMP

- Open-loop: always stable(no internal feedback)
- Closed-loop: stable when negative feedback

  unstable when positive feedback & |kA| ≥ 1

  - $V_{in}^{-} = V_I + kV_{out}$
  - $V_{out} = -A(S)V_{in}^{-}$
  - $A_{vf}(S) = \frac{V_{out}(S)}{V_I(S)} = \frac{-A_v(S)}{kA_v(S)+1}$
  - A_{vf} is closed-loop gain
  - A_v is opened-loop gain
  - kA_v is loop gain.



- Example
  - All pole: $A_v(S) = \frac{k}{(S+S_1)(S+S_2).....(S+S_n)}$

$$|A_v(j\omega)| = \frac{|k|}{\prod_{i=1}^{n}(\omega^2+|S_i|^2)^{1/2}}, \angle A_v(j\omega) = \angle k - \sum_{i=1}^{n}\tan^{-1}(\frac{\omega}{|S_i|^2})$$

  - Closed-loop poles S_p is obtained from $kA_v(S_p) + 1 = 0$

Stability and Compensation of OPAMP (Cont.)

- For stable system, the real part of all poles must be negative. Besides, if $A_v(S)$ has only poles with negative real parts, then s_o will $A_{vf}(S)$,
  - Gain margin = $20\log\left|KA_v(j\omega_{180^\circ})\right|$
  - Unity-gain frequency ω_0
  - Phase Margin=$\angle KA_v(j\omega_0)+180^\circ$ is an important measure of stability at least 60^o (and preferably larger) margin is required. This will also give a desirable (i.e., no ringing) step response for the closed-loop amplifier.

Uncompensated Two-Stage CMOS OPAMP

$$A(s) = \frac{A_0}{(1+s/\omega_{P1})(1+s/\omega_{P2})}$$

$$A_0 = g_{m1}R_{01}g_{m6}R_{02}$$

$$g_{m1} = \sqrt{2\mu C_{ox}(W/L)_{M_1} I_1}$$

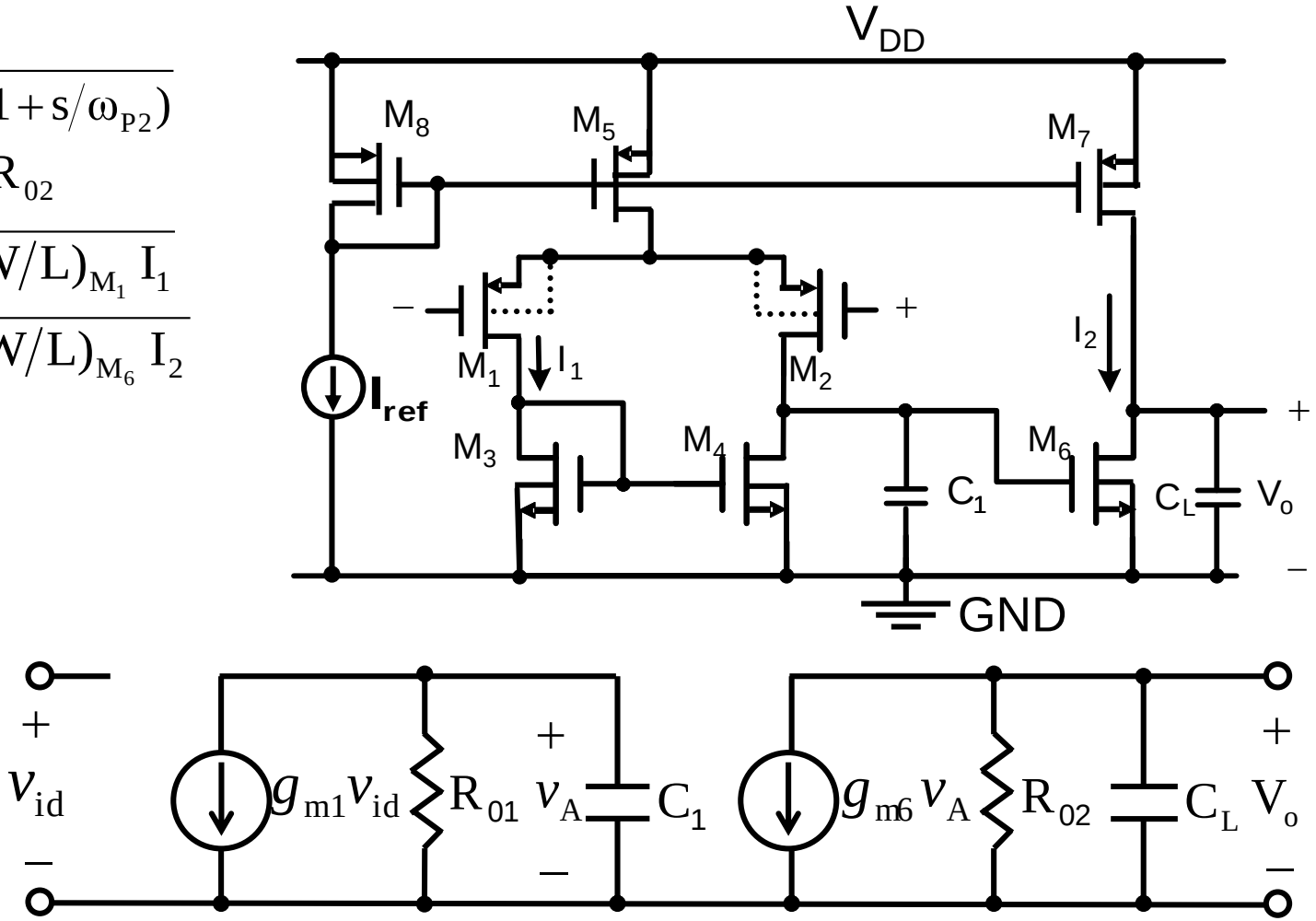
$$g_{m6} = \sqrt{2\mu C_{ox}(W/L)_{M_6} I_2}$$

$$R_{01} = r_{ds2}//r_{ds4}$$

$$R_{02} = r_{ds6}//r_{ds7}$$

$$\omega_{P1} = -1/R_{01}C_1$$

$$\omega_{P2} = -1/R_{02}C_L$$



- P_1 & P_2 are dominant poles since R_{01} and R_{02} are normally large. The effects of other poles are usually negligible.

Uncompensated CMOS OPAMP (Cont.)

- For low frequency, $A(j\omega) \approx A_V(0)$

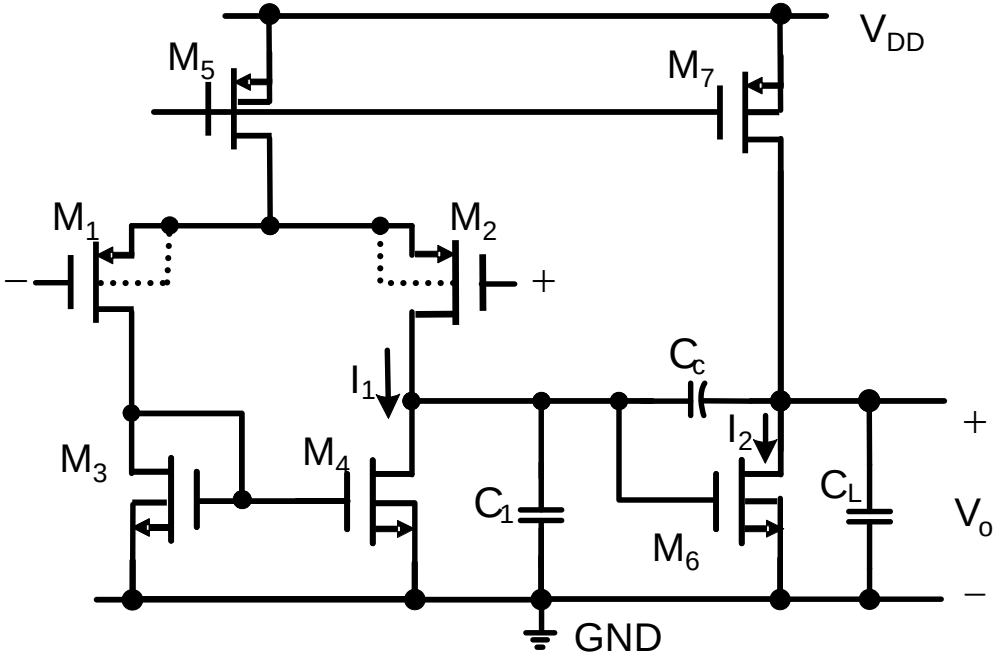
  For high frequency, $A(j\omega) \approx -\dfrac{g_{m1}g_{m5}}{\omega^2 C_1 C_L}$

  For high frequency, the amplifier inverts the input voltage. If feedback is used, then positive feedback occurs.

- Two dominant poles
  - Phase margin is not large enough
  - Pole-splitting technique to solve this problem

Pole-Splitting of Two-Stage CMOS OPAMP

- Reduce ω_{P1} and increase ω_{P2}



$$A(s) = \frac{A_0(1-s/\omega_Z)}{(1+s/\omega_{P1})(1+s/\omega_{P2})}$$

$$A_0 = g_{m1}R_{01}g_{m6}R_{02}$$

$$g_{m1} = \sqrt{2\mu C_{ox}(W/L)_{M_1} I_1}$$

$$g_{m6} = \sqrt{2\mu C_{ox}(W/L)_{M_6} I_2}$$

$$R_{01} = r_{ds2} \,//\, r_{ds4}$$

$$R_{02} = r_{ds6} // r_{ds7}$$

$$\omega_Z \approx \frac{g_{m6}}{C_C} \qquad \text{If } g_{m6}R_{02} >> 1$$

$$\omega_{P1} = \frac{-1}{(1+g_{m6}R_{02})C_C R_{01}} \approx \frac{-g_{m1}}{A_0 C_C}$$

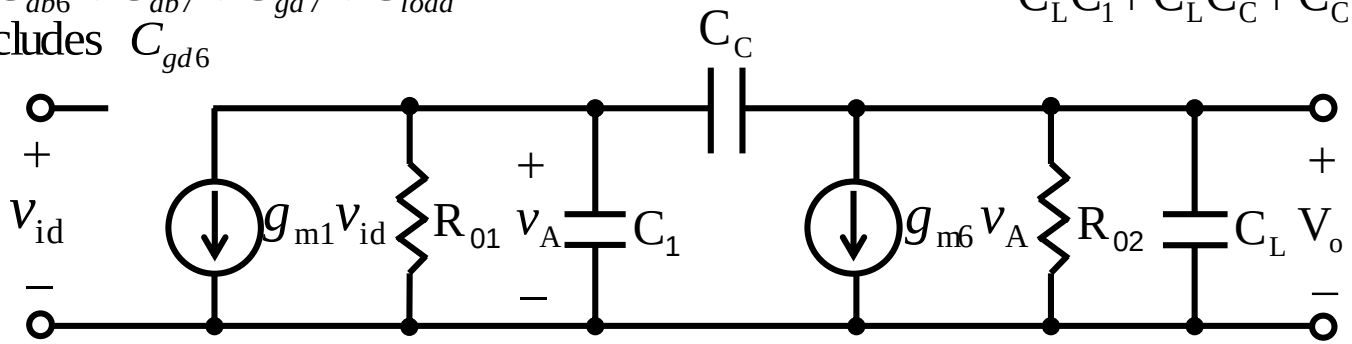
$$C_1 = C_{gd2} + C_{db2} + C_{gd4} + C_{db4} + C_{gs6}$$

$$C_L = C_{db6} + C_{db7} + C_{gd7} + C_{load}$$

C_C includes C_{gd6}

If C_C & $C_L >> C_1$

$$\omega_{P2} = \frac{-g_{m6}C_C}{C_L C_1 + C_L C_C + C_C C_1} \approx \frac{-g_{m6}}{C_L}$$

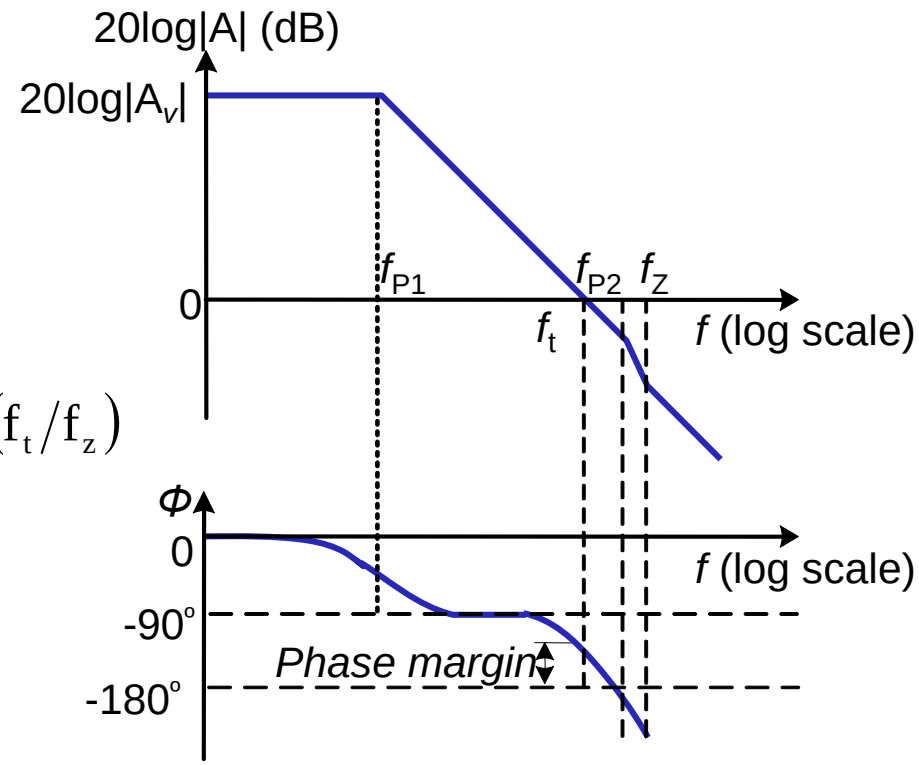


$\Rightarrow$ Right plane zero causes slower gain drop but quick phase drop

Pole-Splitting of Two-Stage CMOS OPAMP (Cont.)

- Unity-gain frequency $f_t = |A_0| \frac{\omega_{P1}}{2\pi} = \frac{1}{2\pi} \frac{g_{m1}}{C_C}$

- To achieve a uniform -20dB/dec gain rolloff down to 0dB, the following two conditions must be satisfied
  1. $f_t < f_{P2} \Rightarrow \frac{g_{m1}}{C_C} < \frac{g_{m6}}{C_L}$
  2. $f_t < f_Z \Rightarrow g_{m1} < g_{m6}$



- At unity-gain frequency f_t (or f_u)

$$\Phi_{total} = \tan^{-1}(f_t/f_{p1}) + \tan^{-1}(f_t/f_{p2}) + \tan^{-1}(f_t/f_z)$$

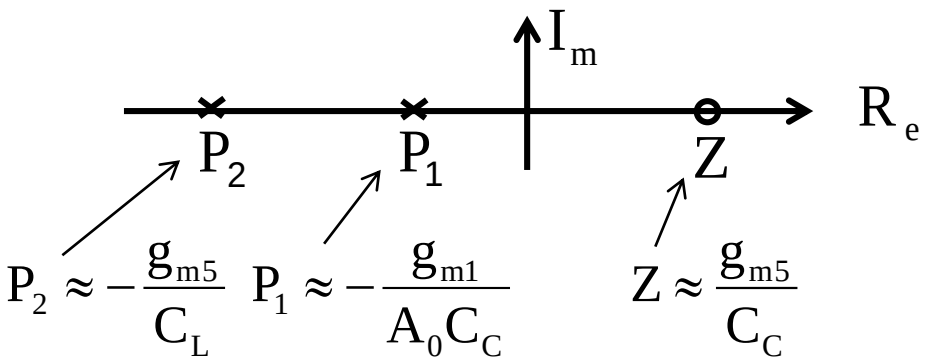
where $\tan^{-1}(f_t/f_{p1}) \cong 90^\circ$

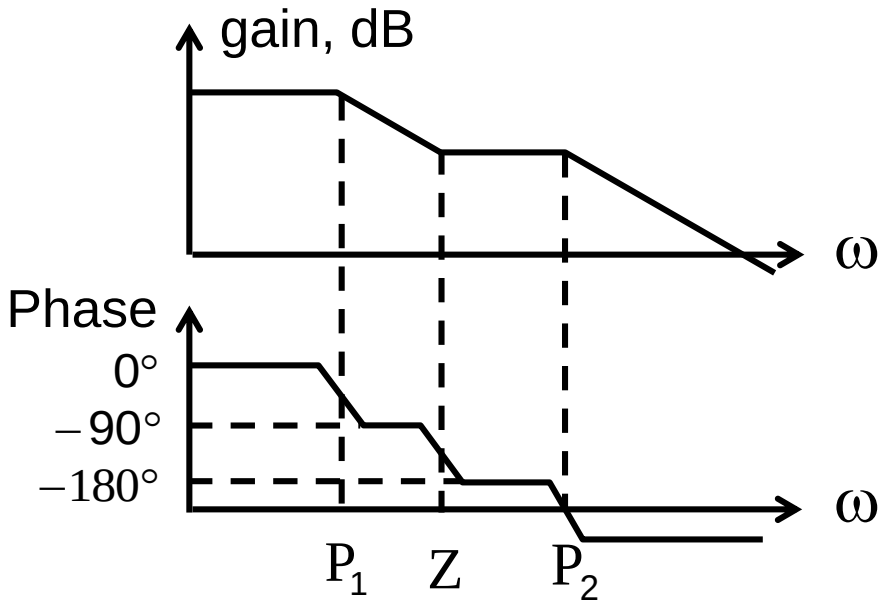
$$\text{Phase margin} = 180^\circ - \Phi_{total}$$

$$= 90^\circ - \tan^{-1}(f_t/f_{p2}) - \tan^{-1}(f_t/f_z)$$

Right Plane Zero

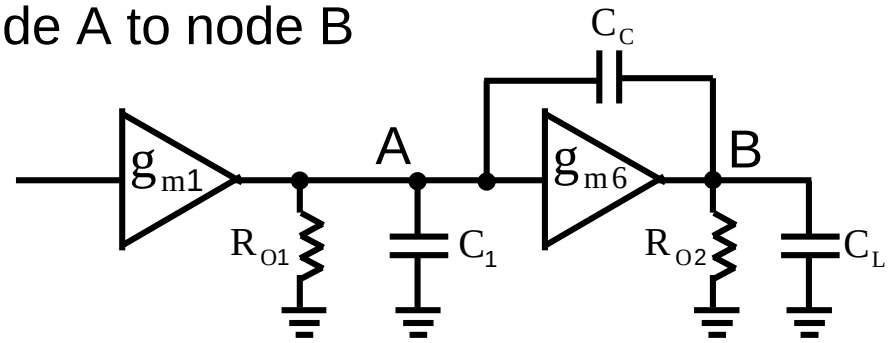
- Causes slower gain drop but quick phase drop
  Usually moved away if phase margin is not large enough





Right-Plane Zero (Cont.)

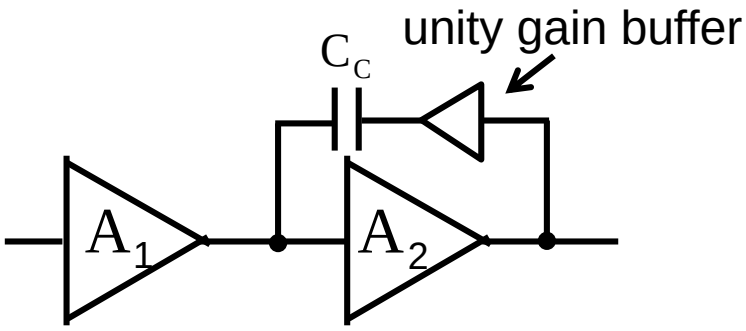
- The zero is due to the existence of two path through which the signal can propagate from node A to node B



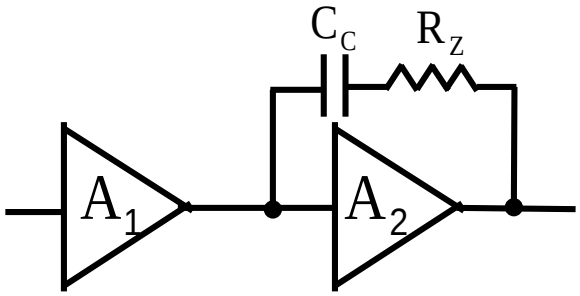
1. through C_C
2. through the controlled source $g_{m6}V_A$

- To eliminate zero ω_z

1. Method-1

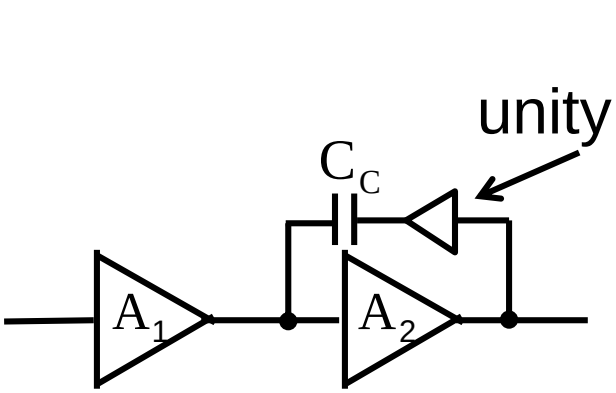


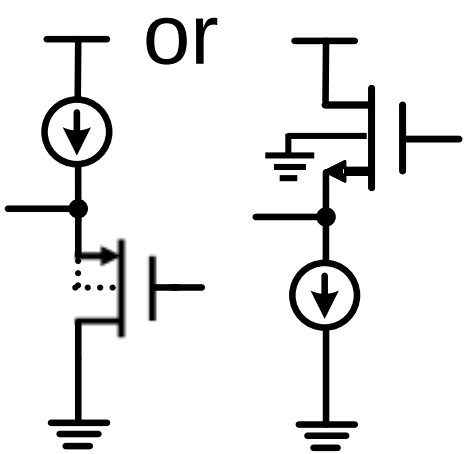
2. Method-2

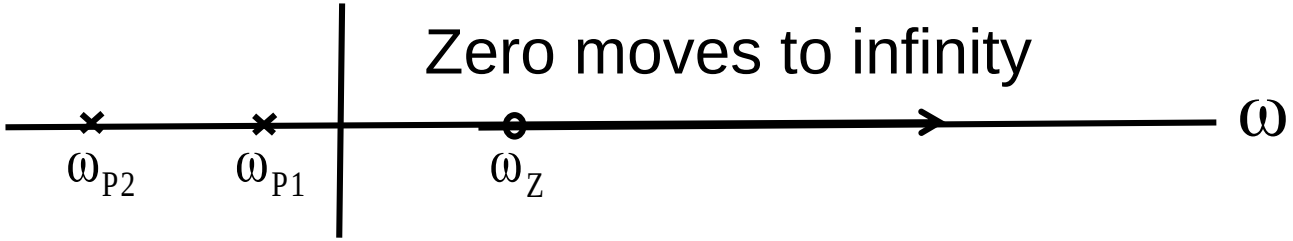


Eliminating Right-Plane Zero

- Method-1 : Using unity-gain buffer → Zero moves to infinity







$$A(s) = \frac{A_0}{(1+\frac{s}{\omega_{P1}})(1+\frac{s}{\omega_{P2}})} \text{ where } \omega_{P1} \approx \frac{-g_{m1}}{A_0 C_C}, \omega_{P2} \approx \frac{-g_{m6}}{C_L}$$

Eliminating Right-Plane Zero (Cont.)

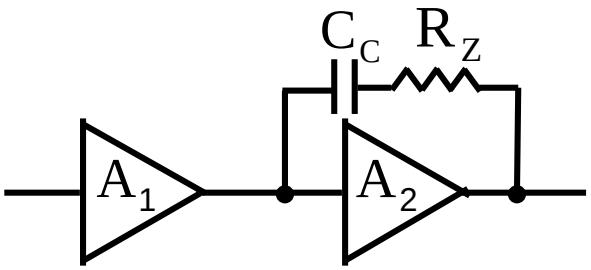
- Method-1 : Using R instead of buffer
  - Eliminating zero → Let $R_Z = \frac{1}{g_{m6}}$
  - Pole-zero cancellation → Let $\omega_Z = \omega_{P2}$

$$\omega_{P1} \approx -\frac{g_{m1}}{A_0 C_C}$$

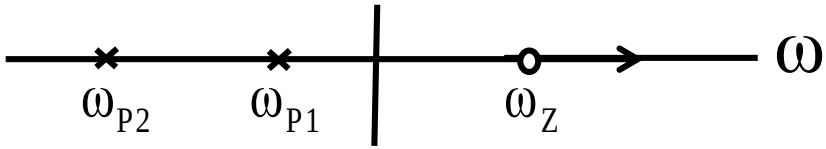
$$\omega_{P2} \approx -\frac{g_{m6}}{C_L}$$

$$\omega_{P3} \approx -\frac{1}{R_Z}\left(\frac{1}{C_C}+\frac{1}{C_1}+\frac{1}{C_L}\right)$$

$$\omega_Z = -\frac{1}{\left[R_Z - \left(\frac{1}{g_{m6}}\right)\right] C_C}$$

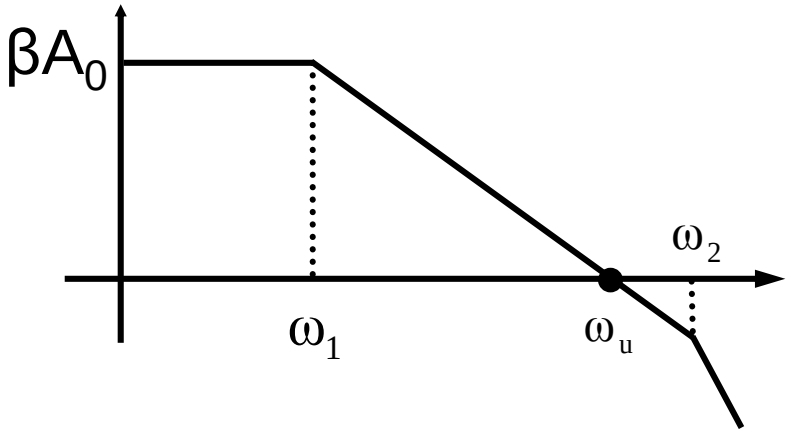


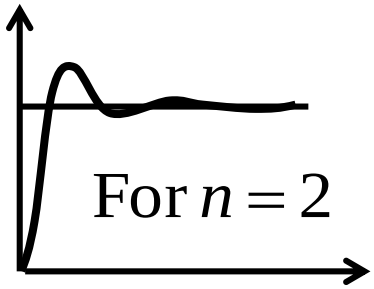
Zero moves toward the left plane

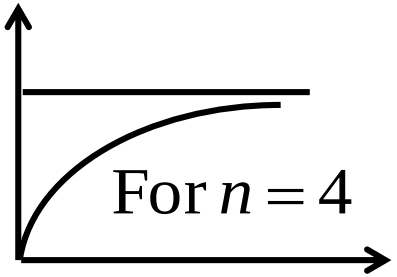


Pole Separation vs. Phase Margin and Speed

- $\omega_u = \frac{1}{n}\omega_2 = \beta A_0 \omega_1$
- For fixed ω_2
  - n=2
    - Phase margin = 63°
    - Fast (Step response)
  - n=3
    - Phase margin = 71°
  - n=4
    - Phase margin = 76°
    - Critically damped (Step response)

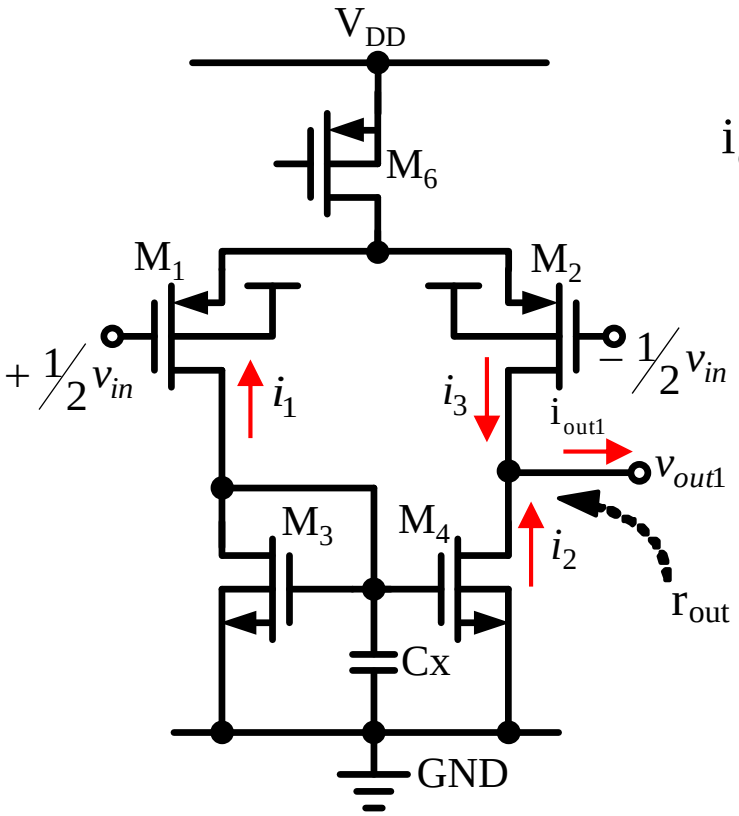






Pole-Zero Doublet

- First stage of a two-stage opamp



$$\text{Assume}: g_{m1} = g_{m2}, g_{m3} = g_{m4},$$

$$C_X = C_{gs3} + C_{gs4} + C_{db1} + C_{db3} + C_{gd1}$$

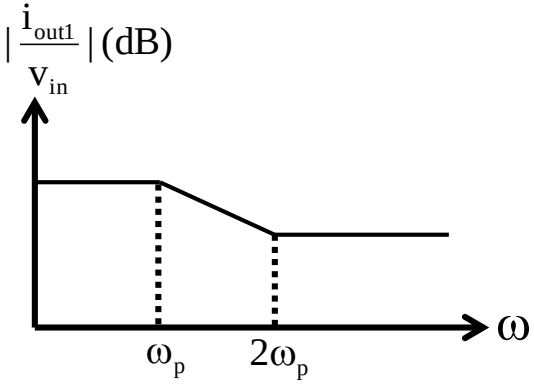
$$i_{out1} = (i_2 + i_3)$$

$$= \left[\frac{1}{2} v_{in} \cdot g_{m1} \cdot \left(\frac{1}{g_{m3}} // \frac{1}{sC_X} \right) \cdot g_{m4} + \frac{1}{2} v_{in} \cdot g_{m2} \right]$$

$$= \frac{1}{2} g_{m1} v_{in} \left(\frac{1}{1 + s/\omega_p} + 1 \right) \quad \text{where } \omega_p = \frac{g_{m3}}{C_X}$$

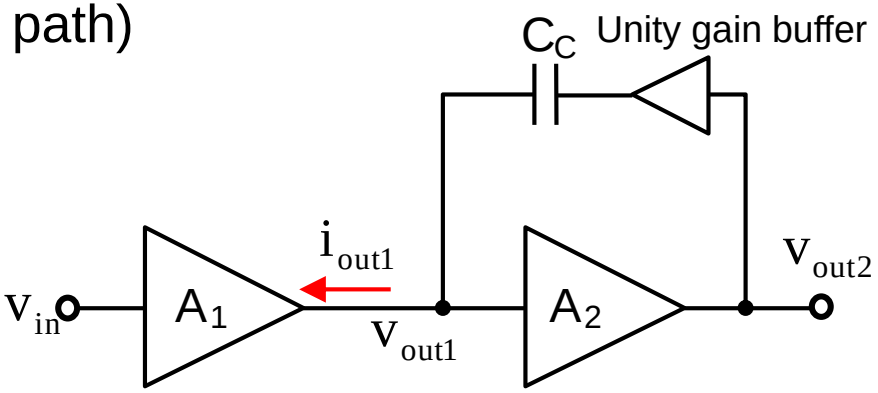
$$= g_{m1} v_{in} \cdot \left(\frac{1 + s/2\omega_p}{1 + s/\omega_p} \right)$$

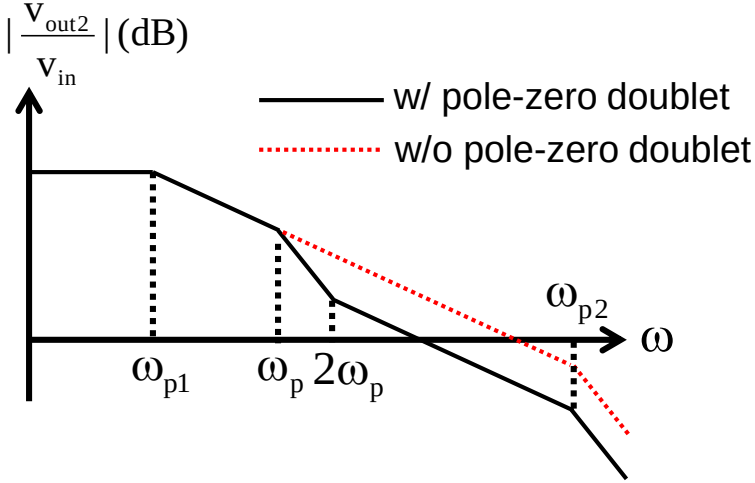
$$\Rightarrow \frac{i_{out1}}{v_{in}} = g_{m1} \cdot \left(\frac{1 + s/2\omega_p}{1 + s/\omega_p} \right)$$



Pole-Zero Doublet (Cont.)

- Equivalent circuit of two-stage opamp (example: buffer in feedback path)





$$\Rightarrow \frac{i_{out1}}{v_{in}} = g_{m1}\cdot\left(\frac{1+ s/2\omega_p}{1+ s/\omega_p}\right), \text{ and } \frac{v_{out2}}{i_{out1}} = \frac{R_{o1}g_{m5}R_{o2}}{\left(1+\frac{s}{\omega_{P1}}\right)\left(1+\frac{s}{\omega_{P2}}\right)} \text{ where } \omega_{P1} \approx \frac{1}{R_{o1}g_{m5}R_{o2}Cc} = \frac{g_{m1}}{A_0 Cc}, \omega_{P2} \approx \frac{g_{m5}}{C_L}$$

$$\Rightarrow \frac{v_{out2}}{v_{in}} = \frac{i_{out1}}{v_{in}}\cdot\frac{v_{out2}}{i_{out1}} = \frac{g_{m1}R_{o1}g_{m5}R_{o2}}{\left(1+\frac{s}{\omega_{P1}}\right)\left(1+\frac{s}{\omega_{P2}}\right)}\cdot\left(\frac{1+ s/2\omega_p}{1+ s/\omega_p}\right) = A_0\frac{\left(1+ s/2\omega_p\right)}{\left(1+\frac{s}{\omega_{P1}}\right)\left(1+\frac{s}{\omega_{P2}}\right)\left(1+ s/\omega_p\right)}$$

- The parasitic capacitance C_x creates a pole at ω_p and a zero at $2\omega_p$.
- It may affect OPAMP stability if close to unity gain frequency.

Slew Rate

- Inverting example
  - Slew rate

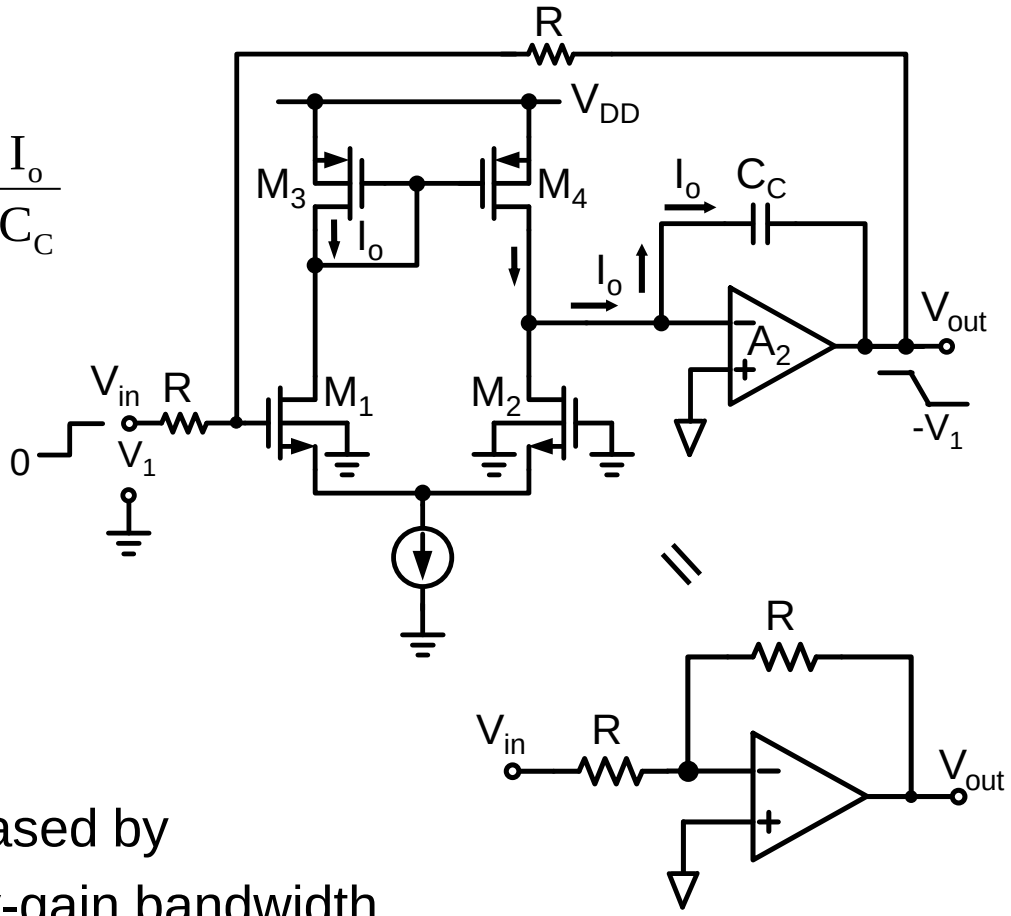
$$S_r = \left|\frac{dV_{out}}{dt}\right| = \left|-\frac{1}{C_C}\frac{dQ_c}{dt}\right| = \frac{I_o}{C_C}$$

  - Assume

$$\omega_u = \frac{g_{mi}}{C_C} \Rightarrow C_C = \frac{g_{mi}}{\omega_u}$$

$$g_{mi} = \sqrt{2uC_{ox}\frac{W}{L}I_o}$$

$$S_r = \frac{I_o\omega_u}{g_{mi}} = \omega_u\sqrt{\frac{I_o}{2uC_{ox}\frac{W}{L}}}$$

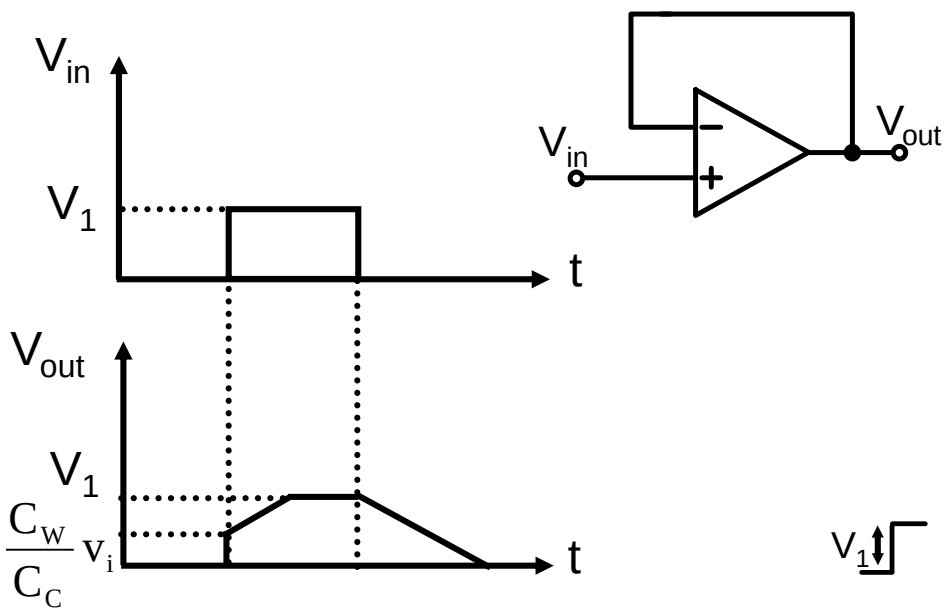


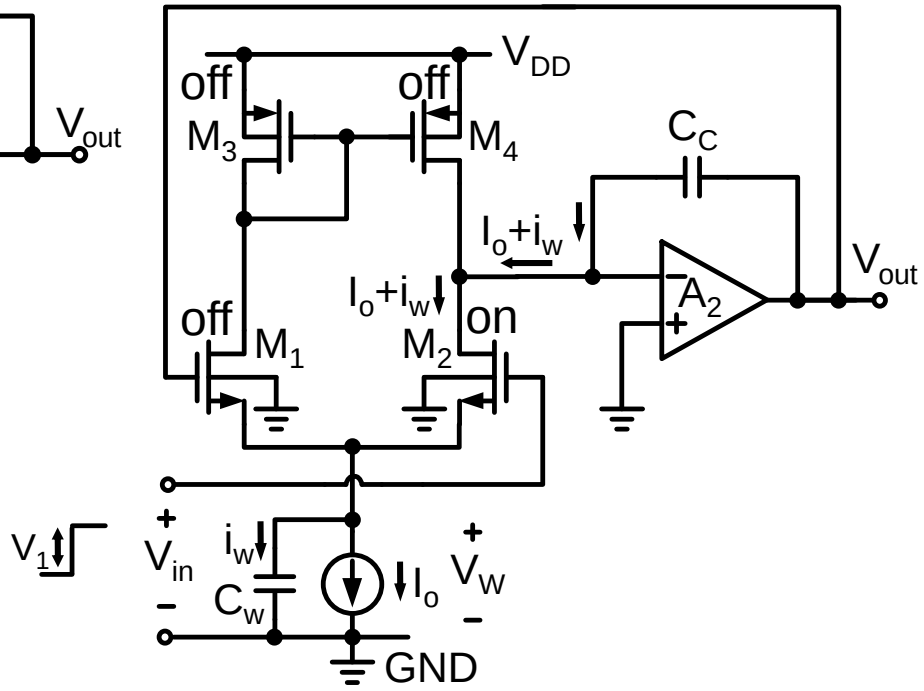
  - Slew rate can be increased by
    - Increasing the unity-gain bandwidth.
    - Increasing bias current of input stage.
    - Decreasing the W/L ratio of the input transistors.

Slew Rate of Voltage Follower

- Large positive input

  With enough A_2 output driving capability





$$V_{in}(t) = V_1 u(t)$$

$$i_W(t) = C_W \frac{dV_W(t)}{dt} \approx C_W \frac{dV_{in}(t)}{dt} = C_W V_1 \delta(t)$$

$$V_{out}(t) = \frac{1}{C_C}\int_0^t (I_o + i_W)dt = \frac{I_o t}{C_C} + \frac{C_W}{C_C}\int_0^t \frac{dV_{in}}{dt}dt = \frac{I_o}{C_C}t + \frac{C_W}{C_C}V_1 u(t)$$

Slew Rate of Voltage Follower (Cont.)

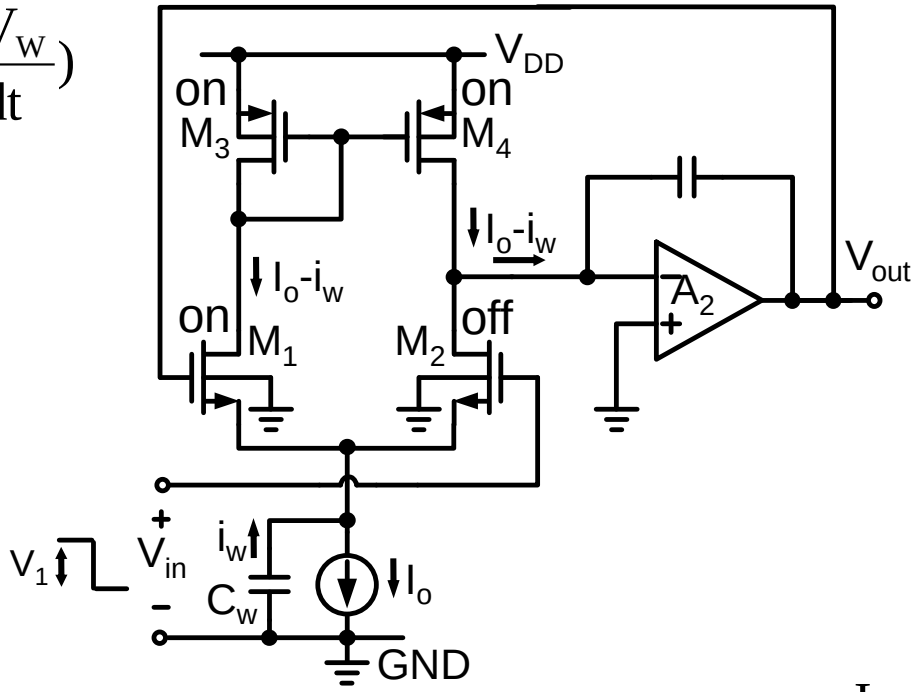
- Large negative input

  With enough A_2 output driving capability

  Because V_W follows V_{out} (Source follower), $\frac{dV_{out}}{dt} \approx \frac{dV_W}{dt}$

$$\frac{dV_{out}}{dt} = -\frac{I_o - i_W}{C_C} = -\frac{i_W}{C_W} \left(= \frac{dV_W}{dt}\right)$$

$$\frac{dV_{out}}{dt} = -\frac{I_o}{C_C + C_W}$$



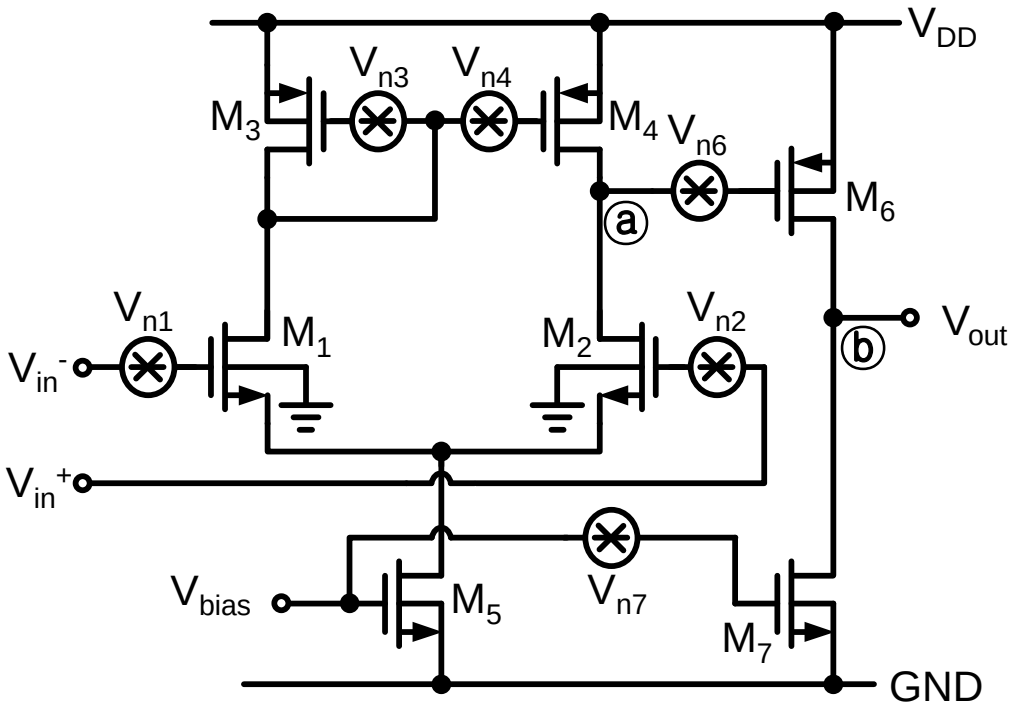
- The negative slew rate is reduced by the presence of C_W, from $\frac{I_o}{C_C}$ to $\frac{I_o}{C_C + C_W}$

Noise Performance of CMOS OPAMP

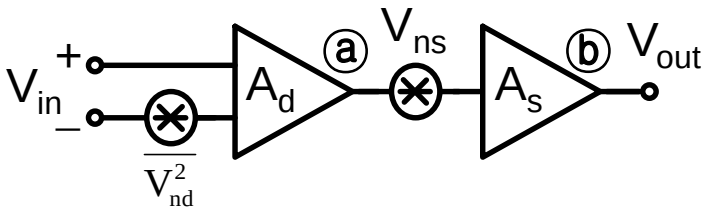
- Noise is fundamental limitation of OPAMP performance
- The equivalent noise voltage of MOS OPAMPs may be 10 times larger than that of a comparable bipolar amplifier
- Example

  $A_d = g_{m1} \cdot (r_{ds2} // r_{ds4})$ for input signal, V_{n1} and V_{n2}

  $A_v = g_{m3} \cdot (r_{ds2} // r_{ds4})$ for V_{n3} and V_{n4}



Noise Performance of CMOS OPAMP (Cont.)



Mean-square voltage at node ⓐ

$$\overline{V_A^2} = A_d^2(\overline{V_{n1}^2} + \overline{V_{n2}^2}) + A_v^2(\overline{V_{n3}^2} + \overline{V_{n4}^2})$$

$$\overline{V_{nd}^2} = \frac{\overline{V_A^2}}{A_d^2} = \overline{V_{n1}^2} + \overline{V_{n2}^2} + \left(\frac{g_{m3}}{g_{m1}}\right)^2(\overline{V_{n3}^2} + \overline{V_{n4}^2})$$

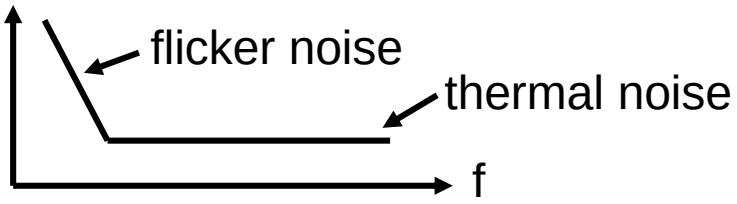
Equivalent input noise voltage

$$\overline{V_n^2} = \overline{V_{nd}^2} + \frac{\overline{V_{ns}^2}}{A_d^2}$$

$$= \overline{V_{n1}^2} + \overline{V_{n2}^2} + (\frac{g_{m3}}{g_{m1}})^2(\overline{V_{n3}^2} + \overline{V_{n4}^2}) + \frac{g_{m6}\overline{V_{n6}^2} + g_{m7}\overline{V_{n7}^2}}{A_d^2}$$

Noise Performance of CMOS OPAMP (Cont.)

- Device noise



  - 1/f noise component dominates at low frequencies
  - The equivalent input noise voltage is greatest at low frequencies (below 1kHz)

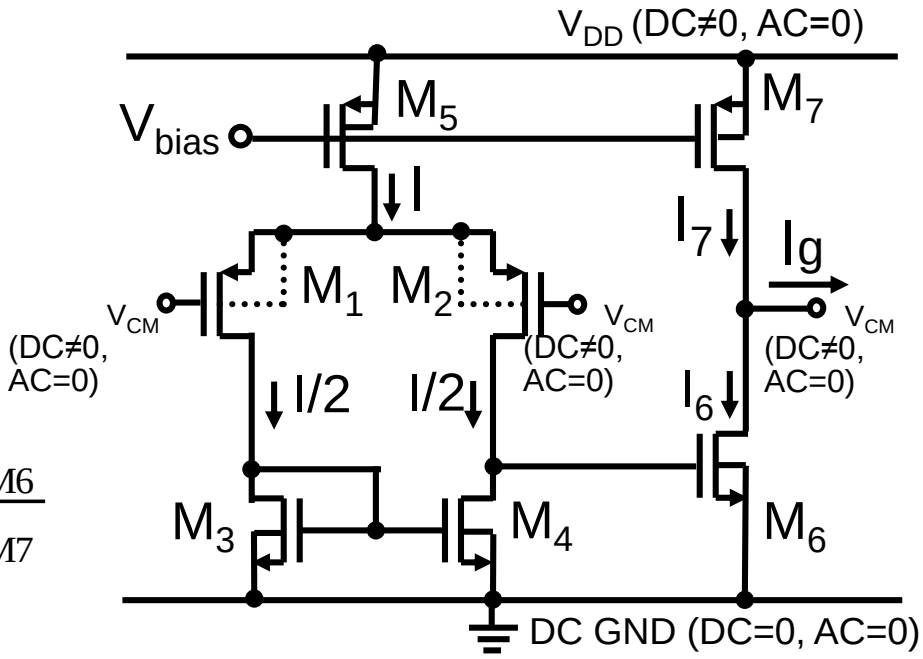
- If $|A_d(\omega)|>>1$, then the input devices M_1 and M_2 tend to be the dominant noise sources and their optimization is the key to low-noise design.

- 1/f noise of OPAMP can be cancelled using
  - Chopper-stabilized technique

    (Dynamic Range over 100dB can be obtained)
  - Correlated double sampling (CDS)

Offset Voltage of Two-Stage CMOS OPAMPs

- Input voltage need to restore the output to zero
- Two components
  - Systematic offset
  - Random offset



- To avoid systematic offset, design must follow the rule

$$\frac{(W/L)_{M3}}{(W/L)_{M5}} = \frac{(W/L)_{M4}}{(W/L)_{M5}} = \frac{1}{2}\frac{(W/L)_{M6}}{(W/L)_{M7}}$$

- To minimize random offset
  - $L_1=L_2$, $W_1=W_2$, $L_3=L_4$, $W_3=W_4$, $L_3=L_6$ and $L_5=L_7$ to minimize the offsets of channel length and channel width variations
  - Large L and W such that $\Delta L/L$ and $\Delta W/W$ can be ignored

Input Common-Mode Range and Output Swing of Two-Stage CMOS OPAMP

- Input common-mode range, V_{ICM}
  - Minimum V_{ICM}

    To keep M_1 and M_2 in saturation, $V_{dg1,2} < |V_{tp}|$. Hence,

    $V_{ICM} \geq -V_{SS} + V_{tn} + V_{OV3} - |V_{tp}|$ where V_{ov} is overdrive voltage
  - Maximum V_{ICM}

    To keep M_5 in saturation, $V_{ds5} > V_{ov5}$. Hence,

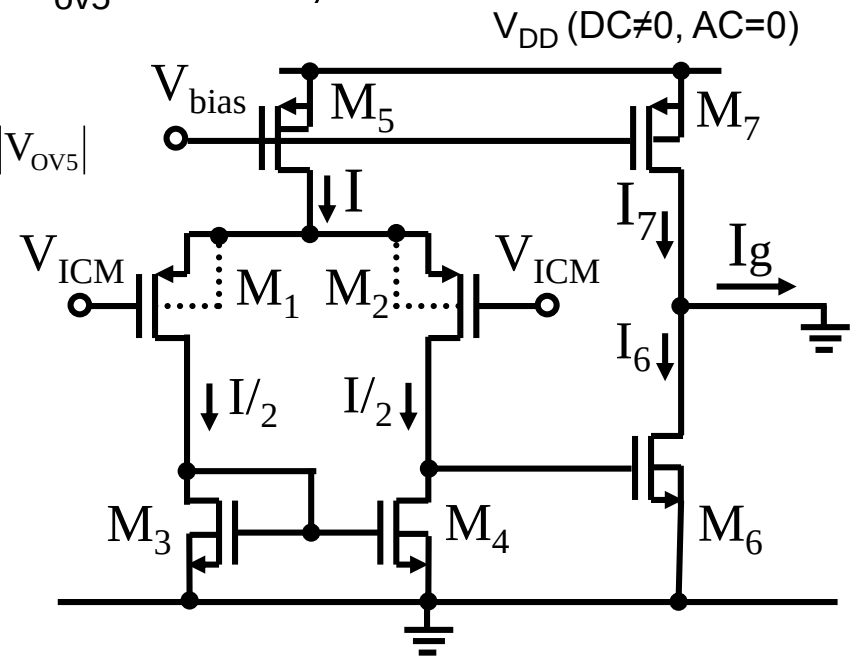
    $V_{ICM} \leq V_{DD} - |V_{OV5}| - |V_{tp}| - |V_{OV1}|$

    $\Rightarrow V_{OV3} + V_{tn} - |V_{tp}| \leq V_{ICM} \leq V_{DD} - |V_{tp}| - |V_{OV1}| - |V_{OV5}|$

- Output swing, V_O

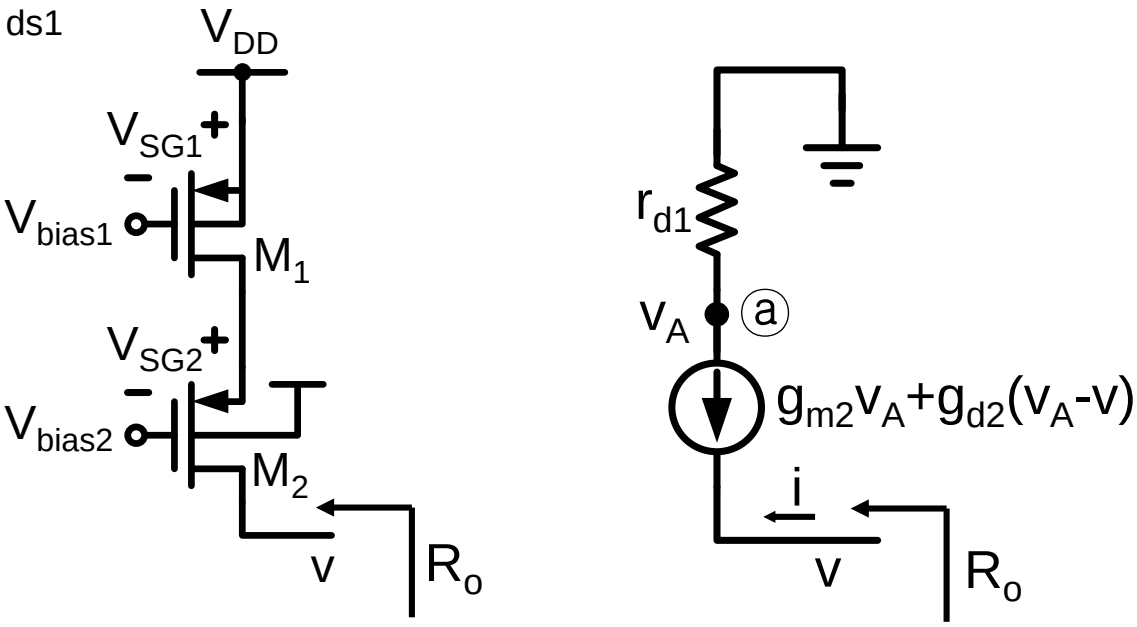
  To keep M_6 and M_7 in saturation

  $V_{OV6} \leq v_o \leq V_{DD} - |V_{OV7}|$



Cascode Circuit as a load

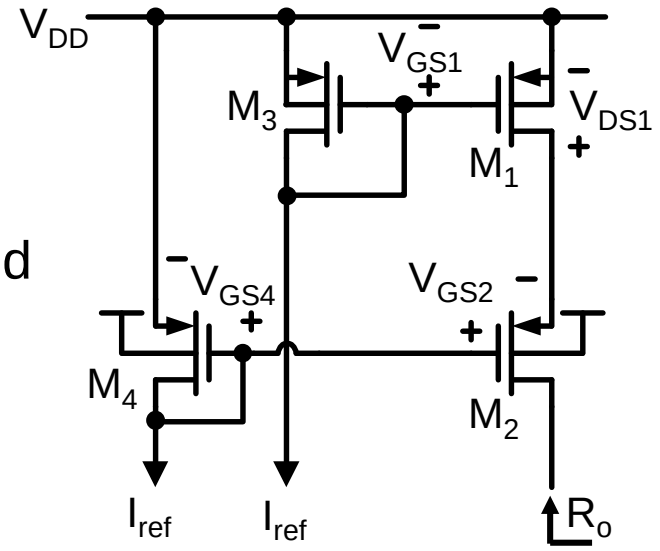
- To reduce # of stages in the design of high-gain OPAMP, cascode is used.
- $R_o=(g_{m2}r_{ds2})r_{ds1}$



- Voltage drop on the two MOSFETs must be minimized to increase voltage swing
  - Both transistors work at the voltage of $V_{DS(min)}$

Cascode Circuit as a load (Cont.)

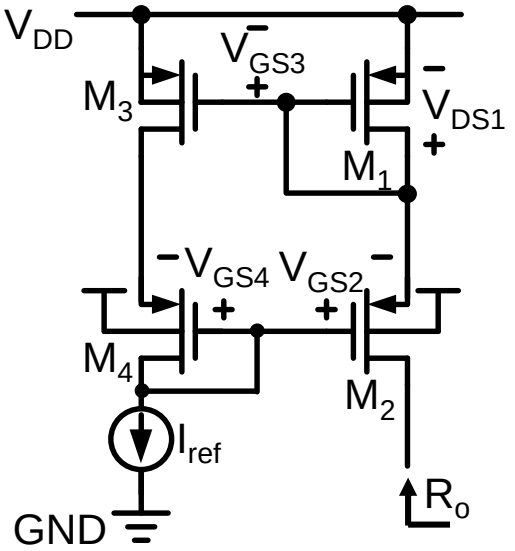
- $(W/L)_{M1}= (W/L)_{M2}= (W/L)_{M3}= 4(W/L)_{M4}$
  - $(V_{GS3}-V_{tp})=V_{DS3(sat)}= V_{DS1(sat)}$
    $= (V_{GS4}-V_{tp})/2= (V_{GS2}-V_{tp})$
    For safety, it is better to make V_{DS1} and V_{DS2} larger than saturation voltage
  - $(W/L)_{M4}< (1/4)(W/L)_{M1}$



- One of other examples is self-biased

$$R_o \approx (g_{m2}r_{ds2})\frac{g_{m3}}{g_{m1}}(r_{ds3} // r_i)$$

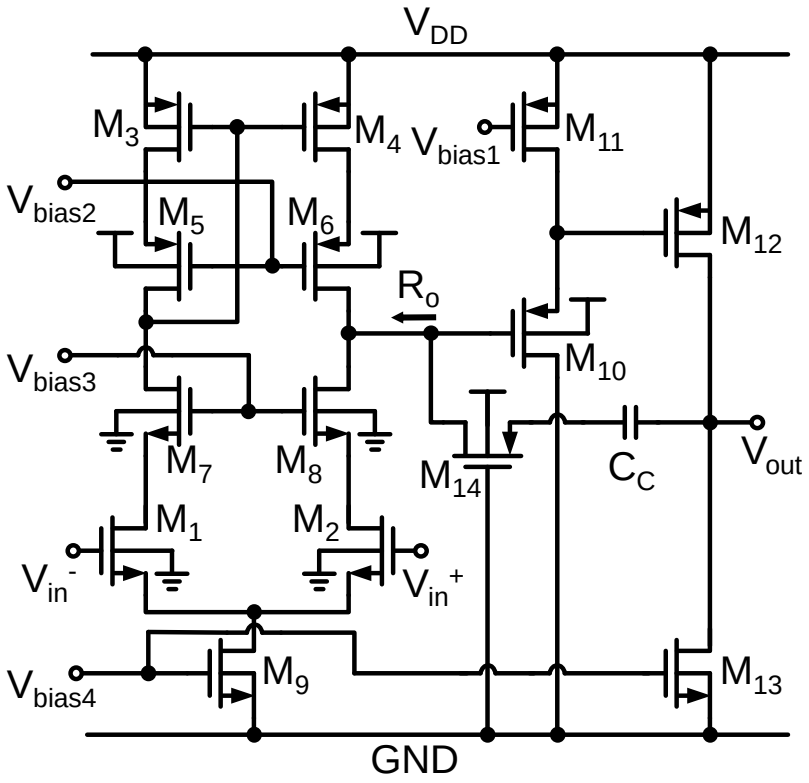
where r_i is the output resistance of I_{ref}



CMOS OPAMP Using Cascode Load

- High gain stage
- Example

$$R_0 = \frac{1}{\left(\frac{1}{g_{m6}r_{d6}r_{d4}}\right) + \left(\frac{1}{g_{m8}r_{d8}r_{d2}}\right)}$$



- Normally, the differential stage must be followed by a level shifter (usually a source follower) and often also by an output amplifier stage. It needs them to be compensated by a pole-splitting capacitor and a resistor or source follower.

CMOS OPAMP Using Cascode Load (Cont.)

- Problems
  - For large C_L, the bandwidth will be limited by nondominant pole.
  - Limited slew rate because of large C_c .
  - PSRR is reduced by pole-splitting.

- All problems can be eliminated, and the circuit made faster as well as simpler, by using “folded cascode” configuration.
- Q_3~Q_8 is disconnected from V_{DD}, folded down, and connected to GND instead.

Folded-Cascode OPAMP

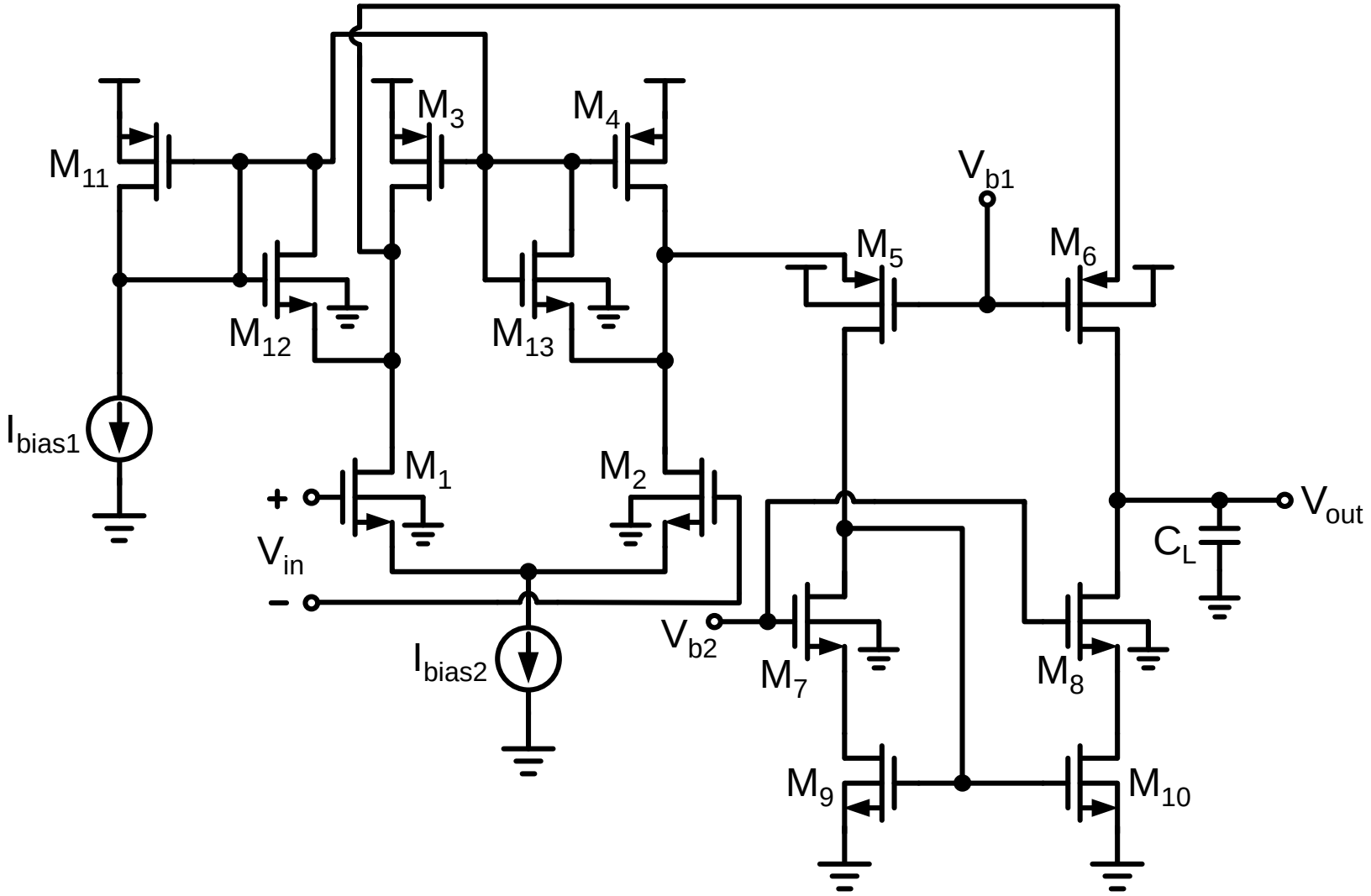
- Many modern CMOS OPAMPs are designed to drive only capacitive load.
  - It's not necessary to use a voltage buffer to obtain a low output impedance.
  - It's possible to realize OPAMPs having higher speed and larger signal swings than those that must also drive resistance loads.
    - These improvements are obtained by having only a single high-impedance node at the output of an OPAMP that drives only capacitive loads.
    - The admittance seen at all other nodes in these OPAMPs is on the order of a transistor's transconductance, and thus they have relatively low impedance.
    - By having all internal nodes of relatively low impedance, the OPAMP speed is maximized.

Folded-Cascode OPAMP (Cont.)

- These low node impedance result in reduced voltage signals at all nodes other than the output node. However, the current signals in the various transistors can be quite large.
- With these OPAMPs, the compensation is usually achieved by the load capacitance.
- As the load capacitance gets larger, the OPAMP usually becomes more stable but also slower.
- One of the most important parameters of these OPAMPs is their transconductance value. Therefore, some designers refer to these modern OPAMPs as transconductance OPAMPs, or Operational Transconductance Amplifiers (OTAs).

Folded-Cascode OPAMP (Cont.)

- A folded-cascode OPAMP



Folded-Cascode OPAMP (Cont.)

- Current mirrors are all wide-swing cascode
  - High output impedance
  - High dc gain

- Two extra transistors, Q_{12} and Q_{13}, serve two purposes
  - Increase slew rate.
  - Allow OPAMP to recover more quickly following a slew rate condition.

    (Because Q_{12} and Q_{13} prevent the drain voltages of Q_1 and Q_2 from having large transients.)

Folded-Cascode OPAMP (Cont.)

- The compensation is realized by the load capacitor, C_L, and realizes dominant pole compensation. In applications where the load capacitance is very small, it is necessary to add additional compensation capacitance in parallel with the load to guarantee stability.

- Small-signal analysis
  - $A_V = \frac{V_{out}(s)}{V_{in}(s)} = g_{m1} Z_L(s) = g_{m1}(r_{out} // C_L) = \frac{g_{m1} r_{out}}{1 + s r_{out} C_L}$
  - Unity-gain frequency

    $\omega_t = \frac{g_{m1}}{C_L}$

Folded-Cascode OPAMP (Cont.)

- Second pole is usually generated at the nodes of Q_1(or Q_3) drain and Q_2(or Q_4) drain.

$$P_2 \approx \frac{g_{mb}}{C_{total}(\text{at } Q_1 \text{ drain})}$$

In BiCMOS, Q_5(Q_6) is usually replaced by a BJT to push P_2 to higher frequency.
(In BiCMOS, ω_t can therefore be maximized.)

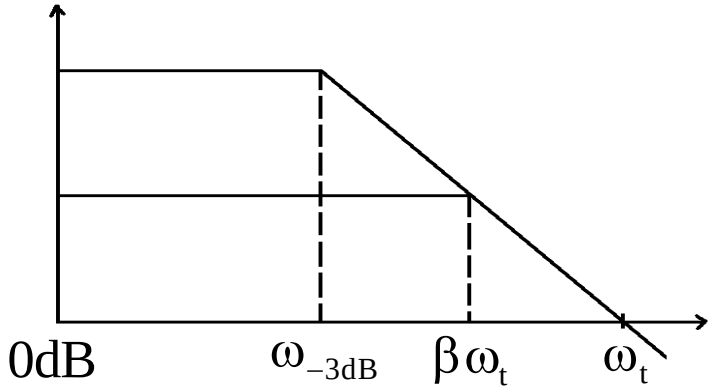
- Slew rate

$$SR = \frac{I_{D4}}{C_L}$$

  - Q_{12} and Q_{13} are included to increase SR. (These two transistors are also used to clamp the drain voltage of Q_{12} and Q_{13}.)

Linear Settling Time

- Time constant for linear settling is approximately equal to if nondominant poles are larger than $\omega_t (= \omega_u)$ $\dfrac{1}{\omega_{-3dB}}$



For closed-loop OPAMP,

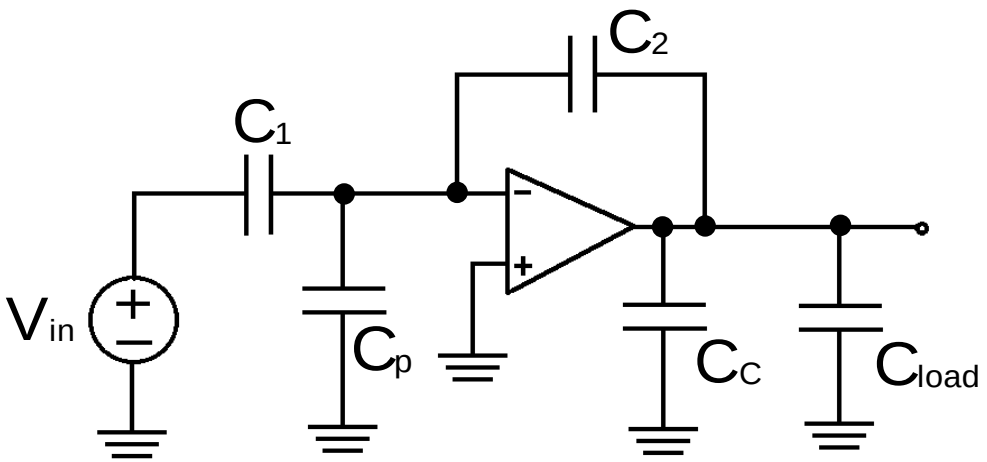
$$\omega_{-3dB} = \beta\omega_t$$

- For classical two-stage CMOS OPAMP the unity-gain frequency remains relatively constant for varying load capacitances, the unity-gain frequencies of folded-cascode and current-mirror amplifiers are strongly related to their load capacitance. As a result, their settling-time performance is affected by both the feedback factor as well as the effective load capacitance.
  - For folded-cascode OPAMP

$$\omega_t = \frac{g_{m1}}{C_L}$$

Linear Settling Time (Cont.)

- -3dB frequency of a closed-loop cascoded (or current mirror) OPAMP
  - Example



$$\beta = \frac{1/[s(C_1 + C_p)]}{1/s(C_1 + C_p) + 1/sC_2} = \frac{C_2}{C_1 + C_p + C_2}$$; C_P is parasitic capacitance

$$C_L = C_C + C_{load} + \frac{C_2(C_1 + C_p)}{C_1 + C_p + C_2}$$

Linear Settling Time (Cont.)

$$\omega_t = \frac{g_{m1}}{C_L}$$ (folded-cascode)

Time constant $\tau = \frac{1}{\beta \omega_t}$

- Step Response

$$V_{out}(t) = V_{step}(1 - e^{-t/\tau})$$

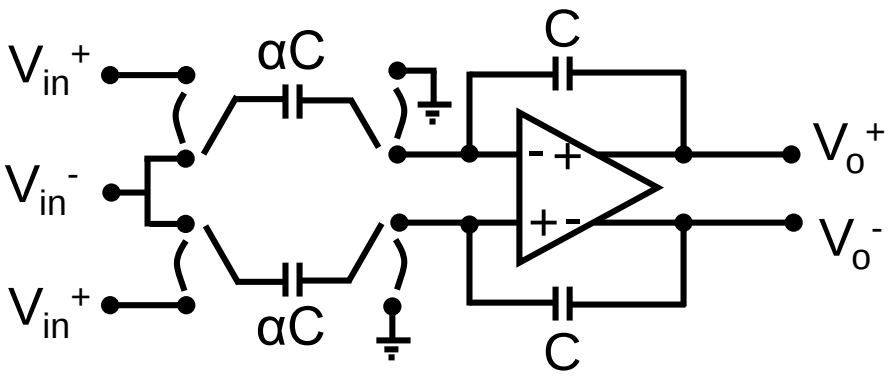
  - If 1% accuracy is required $\Rightarrow 4.6\tau$
  - If 0.1% (i.e. 10-bit) accuracy is required $\Rightarrow 7\tau$

$$\frac{d}{dt} V_{out}(t)\Big|_{t=0} = \frac{V_{step}}{\tau}$$

    - If the slew rate of the OPAMP is larger than this value, no slew-rate limiting would occur.

Fully Differential CMOS Switched-Capacitor Circuit

- Power supply rejection is high
- Larger chip area compared with single-ended output
- Output swing is doubled
  - DR is 6dB greater than single-ended OPAMPs
- The effect of clock feedthrough noise is minimized by the differential configuration since it will appear as a common-mode signal.



Fully Differential OPAMPs

- Fully differential signal paths
  - Differential input
  - Differential output
  - Used in most modern high-performance analog ICs

- Help reject noise from the substrate as well as from switches turning off in switched-capacitor applications.
  - Ideally, noise affects both signal paths identically and will then be rejected since only the difference between signals is important.
  - In reality, this rejection only partially occurs since the mechanisms introducing the noise are usually nonlinear with respect to voltage levels. For example, substrate noise will usually feed in through junction capacitances, which are nonlinear with voltage.
  - Certainly, the noise rejection of a fully differential design will be much better than that for a single-ended output design.

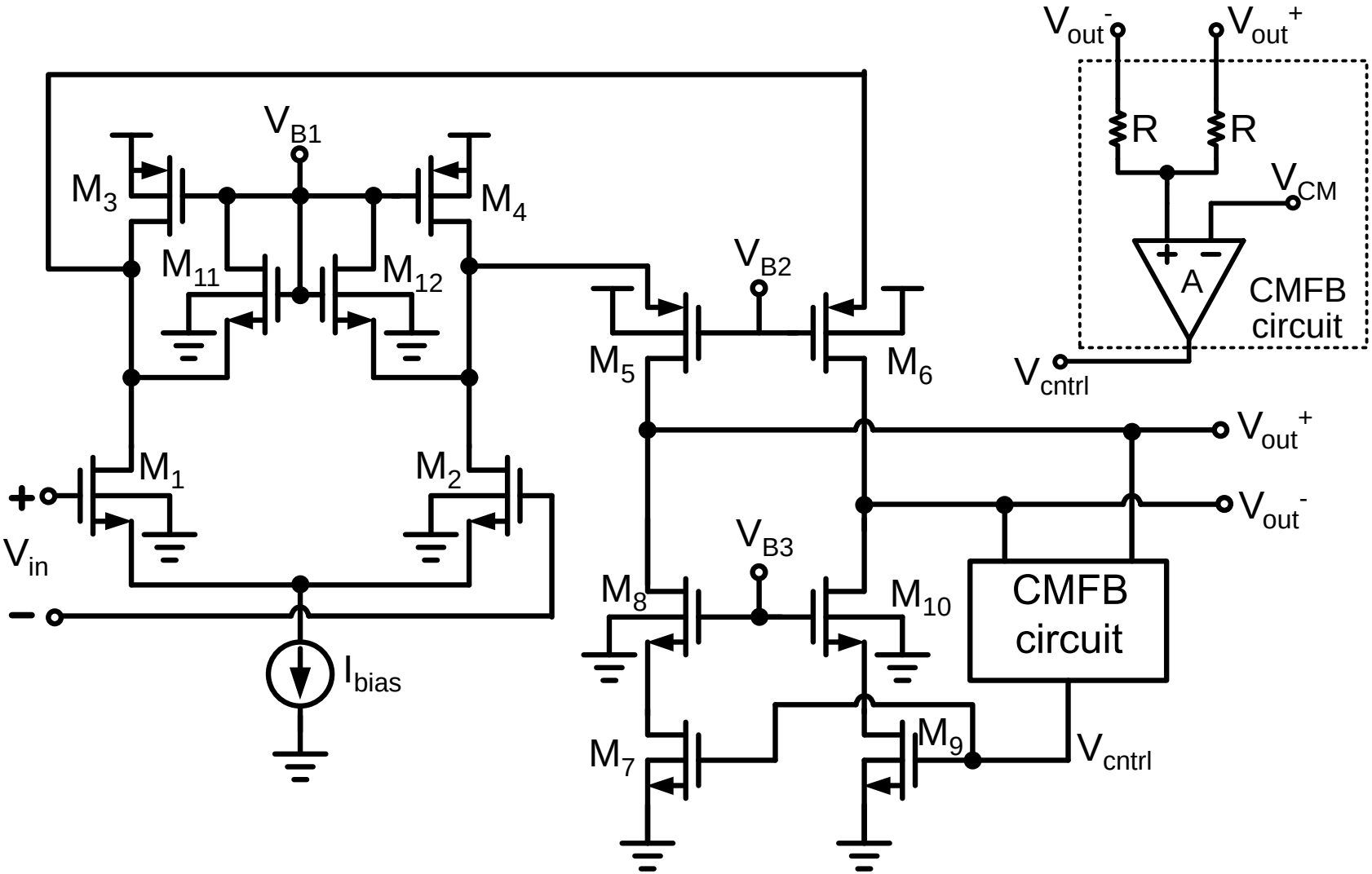
Fully Differential OPAMPs (Cont.)

- Common-mode feedback (CMFB) circuit must be added to establish the common-mode (i.e. average) output voltage.

- Reduced slew rate in one direction (compared to single-ended design)
  - Maximum current for slewing is often limited by fixed-bias currents in the output stages.

Fully Differential Folded-Cascode OPAMP

- Cascode current source (rather than self-biased current mirror)



Fully Differential Folded-Cascode OPAMP (Cont.)

- CMFB circuit forces the average of the two outputs to a predetermined value
- Maximum negative slew rate is limited by I_{D7} and I_{D9}
- Clamp transistors M_{11} and M_{12}
- Dominant pole : output node

  2nd pole : node at M_1 (or M_2) drain
  - n-channel input and p-channel for M_5 and M_6
    - High transconductance
    - High gain
  - p-channel input and n-channel for M_5 and M_6
    - Maximize 2nd pole frequency
    - Unity-gain bandwidth can be maximized.

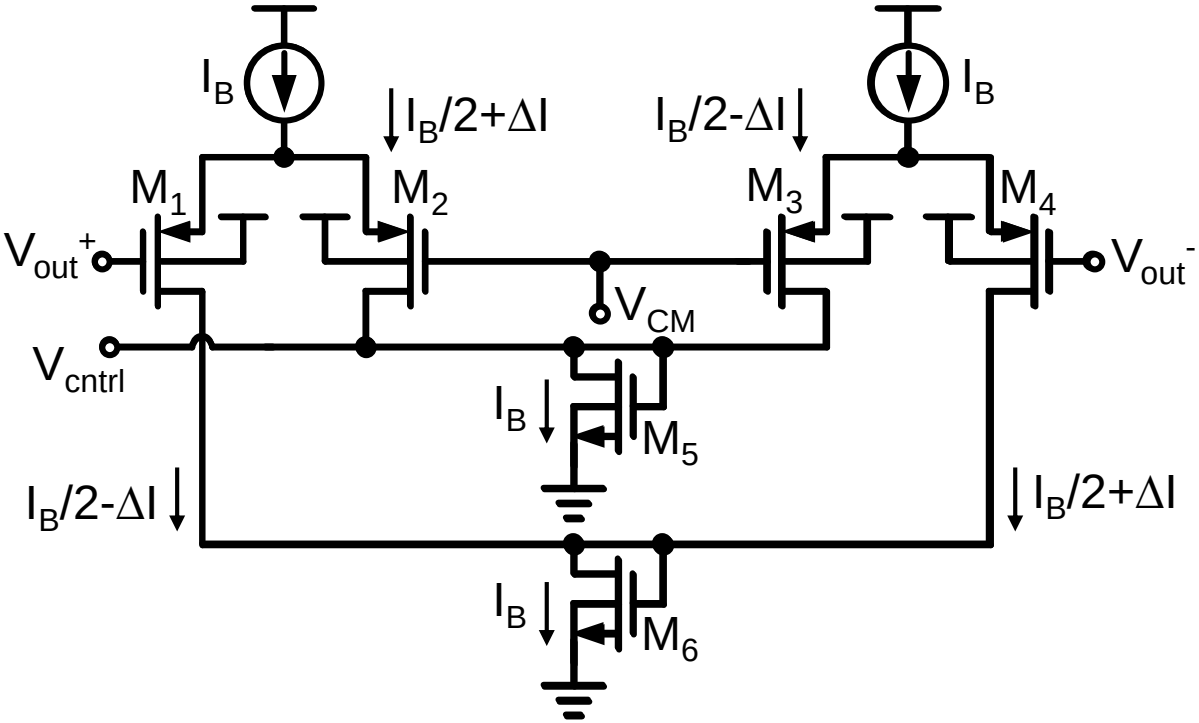
Common-Mode Feedback (CMFB) Circuits

- Force output common-mode voltage to a predetermined value
- CMFB is often the most difficult part of the OPAMP to design.
- Two typical approaches
  - Continuous-time
    - Limited signal swing
  - Switched-capacitor
    - Used in switched-capacitor circuits
    - Signal swings are not limited
    - Becomes a source of noise
    - Increases load capacitance

- By having as few nodes in the common-mode loop as is possible, compensation is simplified without having to severely limit the speed of the CMFB circuit. For this reason, the CMFB circuit is usually used to control current sources in the output stage of the OPAMP.

CMFB Circuits

- A continuous-time CMFB circuit



  - The circuit can not operate correctly if the OPAMP output voltage is so large that transistors in the differential pairs turn off.
  - When common-mode voltage is zero

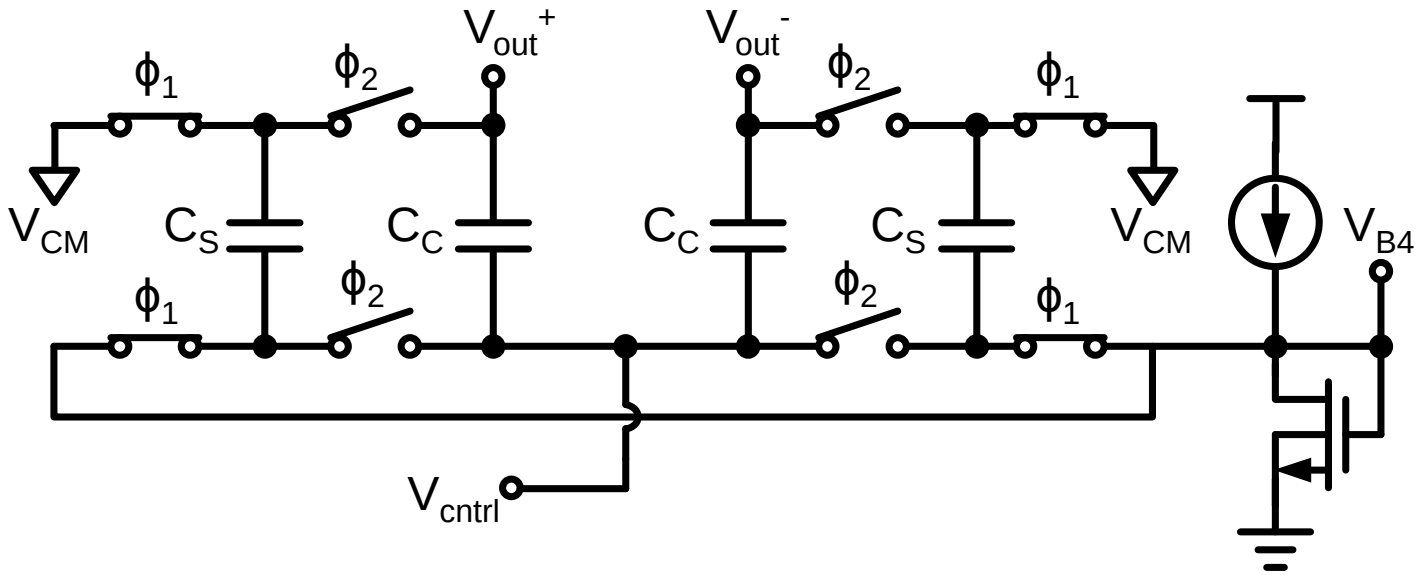
$$I_{D2} = \frac{I_B}{2} + \Delta I, \quad I_{D3} = \frac{I_B}{2} - \Delta I, \quad I_{D5} = I_B$$

CMFB Circuits (Cont.)

- Operational principle of CMFB circuits
  - When a positive common-mode signal is present
  - I_{M2} and I_{M3} increase → I_{M5} increase → V_{cntrl} increase
  - V_{cntrl} sets the current levels in the n-channel current sources at the output of the OPAMP.
  - Thus, both current sources will have larger currents pulling down to the negative rail → the common-mode voltage decrease → bringing the common-mode voltage back to V_{CM}
  - If the common-mode loop gain is large enough, and the differential signals are not so large as to cause transistors in the differential pairs to turn off, the common-mode output voltage will be kept very close to V_{CM}.

CMFB Circuits (Cont.)

- A switched-capacitor circuit



  - Using larger capacitance values overloads the OPAMP
  - Reducing the capacitors too much caused common-mode offset voltages due to charge injection of the switches.

$$\frac{V_{out}^{+} + V_{out}^{-}}{2} - V_{cntr1} \approx V_{CM} - V_{bias}$$

Appendix

- Operational-amplifier (OPAMP)
- Cascode CMOS and BiCMOS OPAMPs
- Folded-Cascode CMOS OPAMP
- Current mirror OPAMP
- Alternative fully differential OPAMPs
- BiCMOS amplifiers

Operational-Amplifier (OPAMP)

- OPAMP design
  - CMOS OPAMPs are adequate for VLSI implementation.
    - Main stream
    - Two-stage and folded-cascode OPAMPs will be introduced.
  - Bipolar OPAMPs
    - Can achieve better performance than CMOS OPAMPs.
    - Less popular
    - 741 OPAMP will be introduced.
  - BiCMOS OPAMPs
    - combine the advantages of bipolar and CMOS devices.
    - Less popular
    - First published by H. C. Lin in 1960's.
- ADCs and DACs are the most important analog ICs in many systems.

CMOS OPAMP

- Two-stage

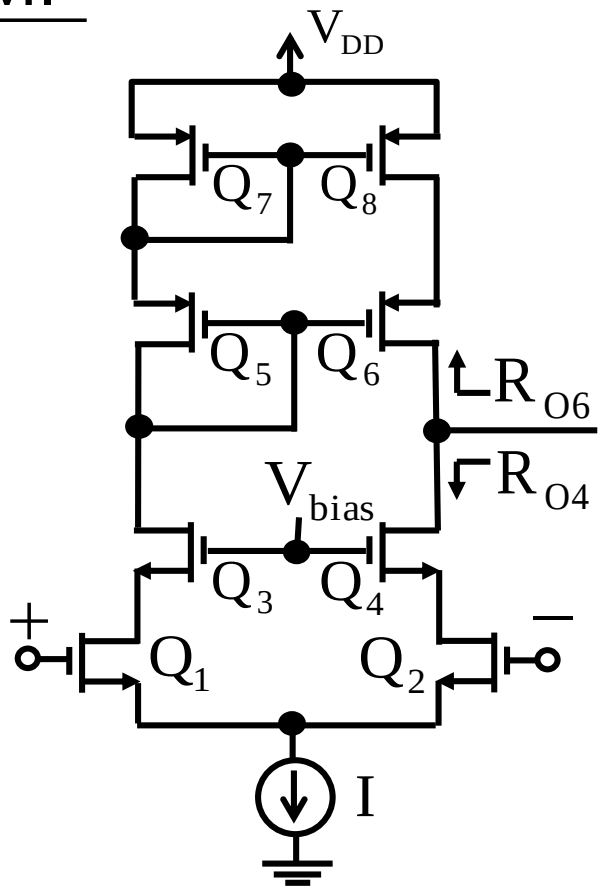
  I guess, it is suitable for 50% of applications with OPAMPs.
- Folded-cascode

  I guess, it is good for 20% applications.
- Others

Cascode CMOS and BiCMOS OPAMPs

- Cascaded two-stage CMOS OPAMP
  - most popular and works well with low capacitive load
  - problems
    - limited slew rate due to large C_c
    - limited bandwidth with large C_L
    - PSRR is reduced by pole-splitting
- If 1. low output resistance is not required,
  2. high open-loop gain is required, and
  3. large phase margin can be maintained with large C_L,
  then cascode configuration can provide attractive solutions for the above problems.
- Cascode CMOS OPAMP
  - Gain of two-stage OPAMP can be increased by adding gain stage in cascade.
    $\Rightarrow$ phase shift is increased (i.e. PM$\downarrow$)
  - Cascode configurations can be used to increase gain in the existing stage.

Cascode CMOS OPAMP



- Output resistance(Ro) is increased

$$R_{O6} \approx (g_{m6} r_{ds6}) r_{ds8}$$

$$R_{O4} \approx (g_{m4} r_{ds4}) r_{ds2}$$

$$R_O = R_{O2} // R_{O4}$$

- Voltage gain $A_1 = -g_{m1} R_O$

  $\Rightarrow$ Gain is increased .

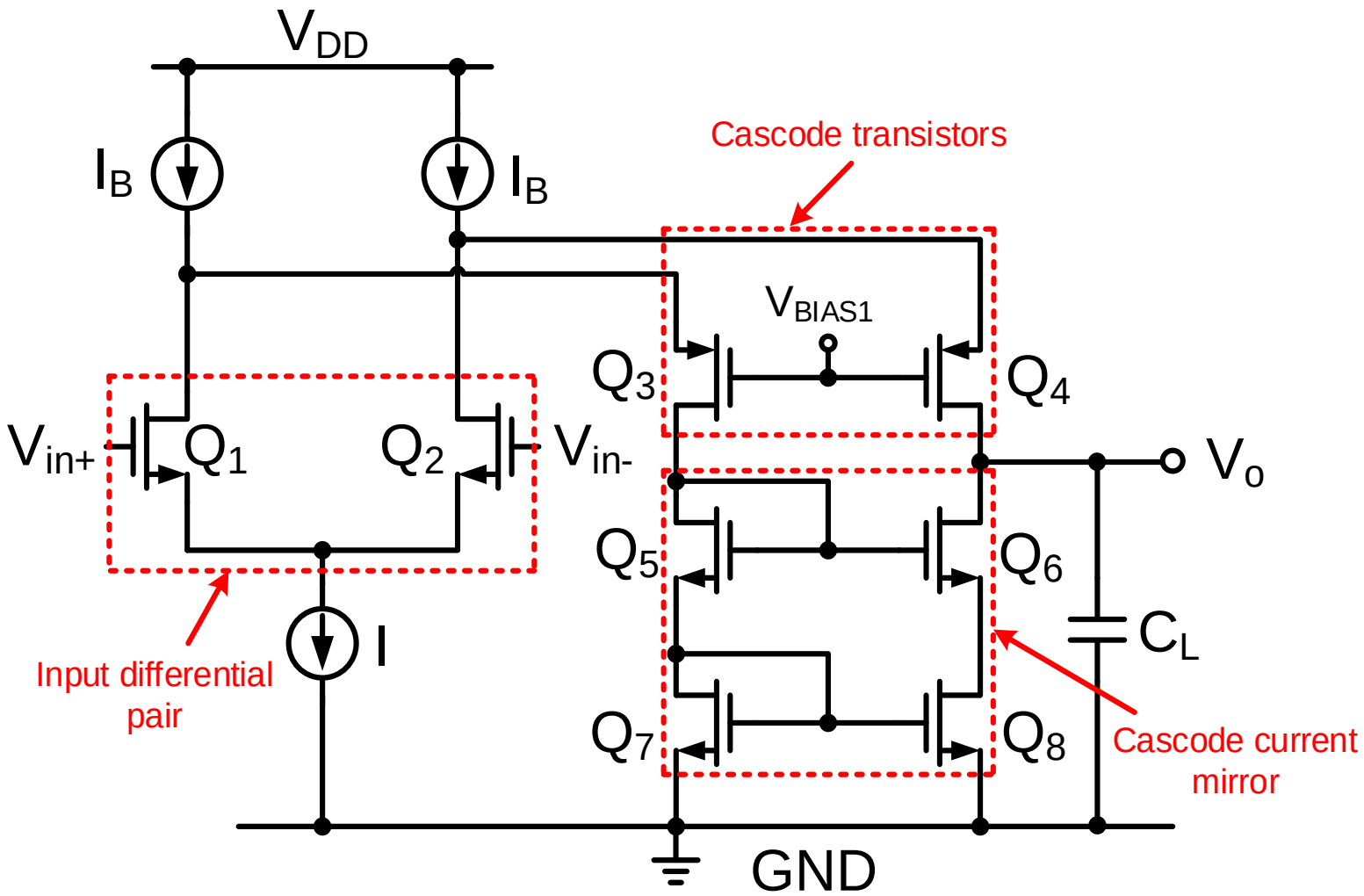
- Common-mode range is lowered and more transistors are stacked between the two power supplies.

  $\Rightarrow$ Folded-cascode has large common-mode range

- Cascode and folded-cascode OPAMPs are also named as "transconductance OPAMP" or "operational transconductance amplifier (OTA)"

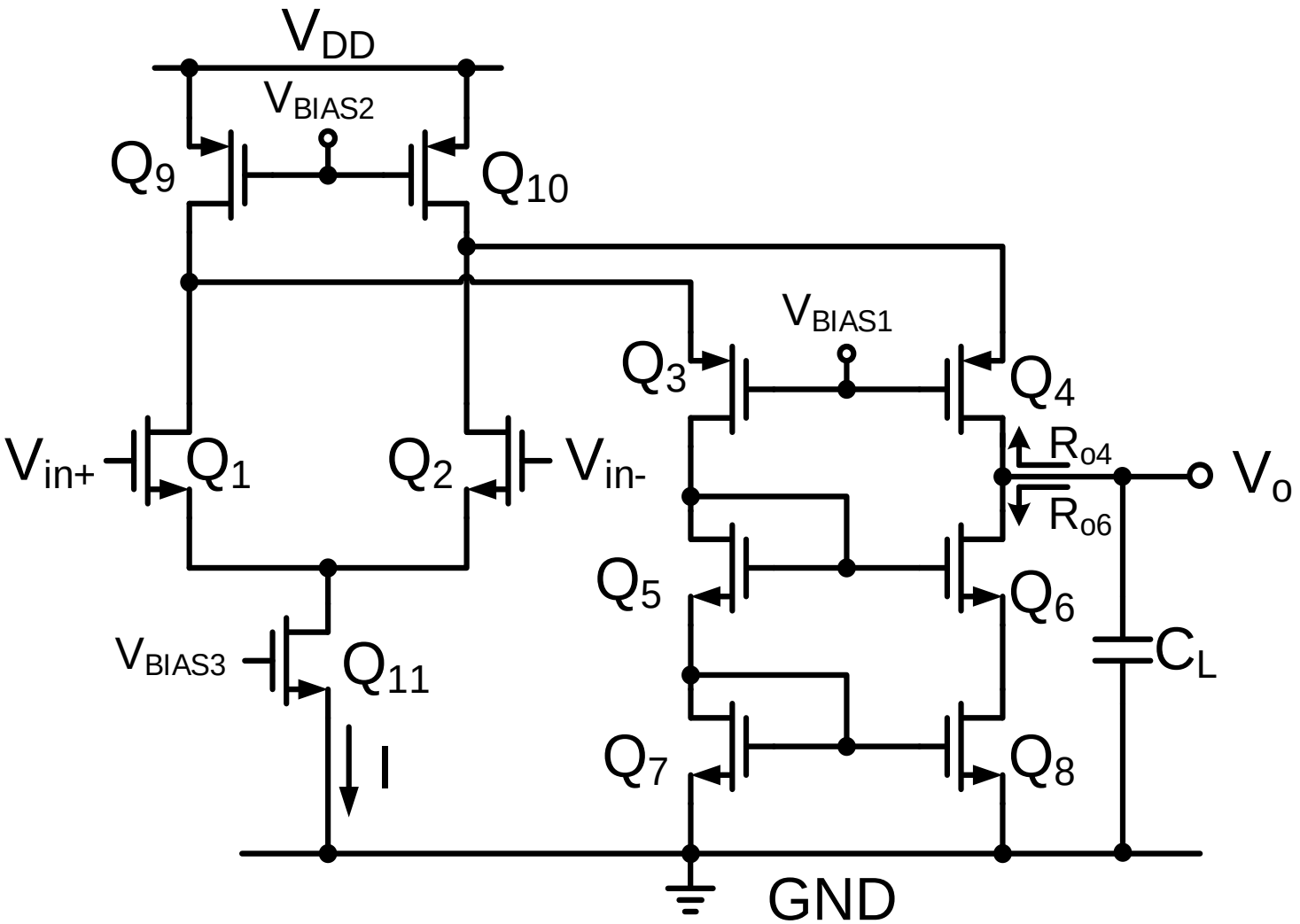
Folded-Cascode CMOS OPAMP

- Q_3 ~ Q_8 are folded and connected to GND



Folded-Cascode CMOS OPAMP (Cont.)

- Q_9 ~ Q_{11} form externally-biased current sources
  Q_5 and Q_8 form self-biased current sources



Folded-Cascode CMOS OPAMP (Cont.)

- Input common-mode range

  Common-mode range is increased (compared with cascode OPAMPs). However, it is small compared with 2-stage OPAMPs

$$V_{OV\,11} + V_{OV\,1} + V_{tn} \leq V_{ICM} \leq V_{DD} - |V_{OV\,9}| + V_{tn}$$

- Output voltage swing

$$V_{OV\,7} + V_{OV\,5} + V_{tn} \leq V_o \leq V_{DD} - |V_{OV\,10}| - |V_{OV\,4}|$$

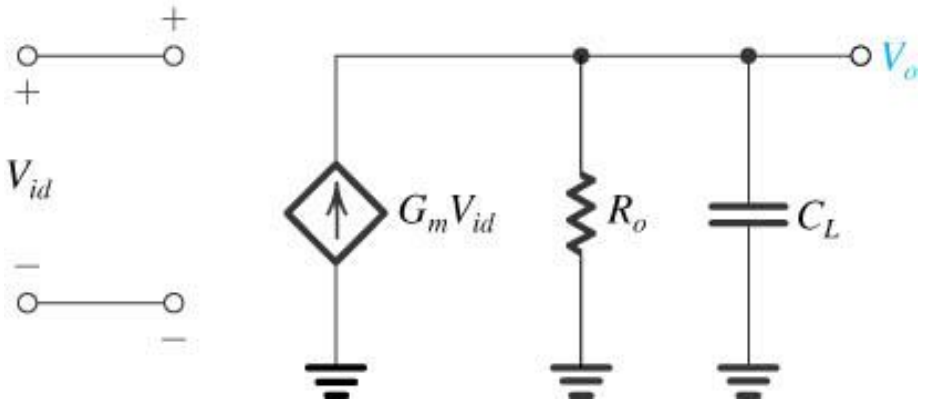
- Voltage gain

  $A = G_m R_o = g_{m1} R_o$

  where

  $R_o = R_{o4} // R_{o6}$

  $= g_{m4} r_{ds4} (r_{ds2} // r_{ds10}) \; // \; g_{m6} r_{ds6} r_{ds8}$

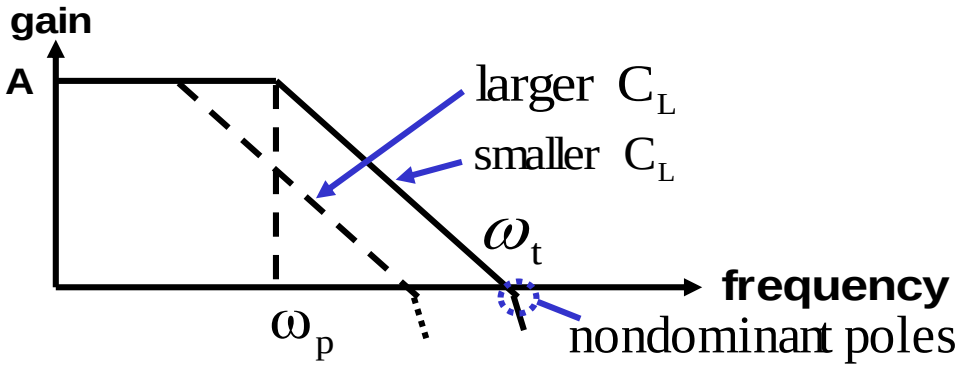


Folded-Cascode CMOS OPAMP

- Frequency response
  - Bode plot

$$\omega_p \approx \frac{1}{R_0 C_L}$$

$$\omega_t \approx \frac{g_{m1}}{C_L}$$

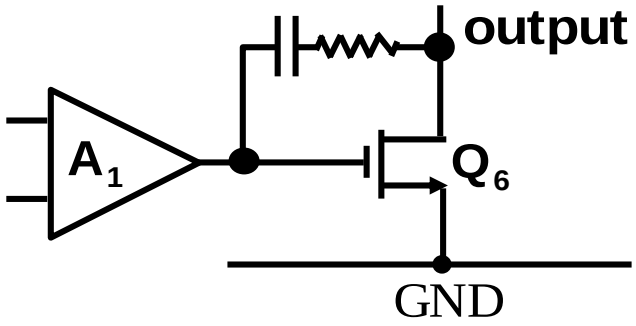


  - The only high-impedance point is the output node.
    $\Rightarrow$ Dominant pole is generated at the output node
  - The resistance of all other node at level of 1/gm
    $\Rightarrow$ Nondominant poles occur at all other nodes.
    The 2nd pole is usually at the source of Q_3 and Q_4.
  - Nondominant poles are usually at frequencies beyond ω_t
    $\Rightarrow$ If C_L is increased, then phase margin is increased.
    $\Rightarrow$ If C_L is not large enough, it can be augmented.
  - No frequency compensation is required
    $\Rightarrow$ wide bandwidth
- Slew rate SR=I/C_L= $2\pi f_t V_{OV1} = \omega_t V_{OV1}$

Folded-Cascode CMOS OPAMP(Cont.)

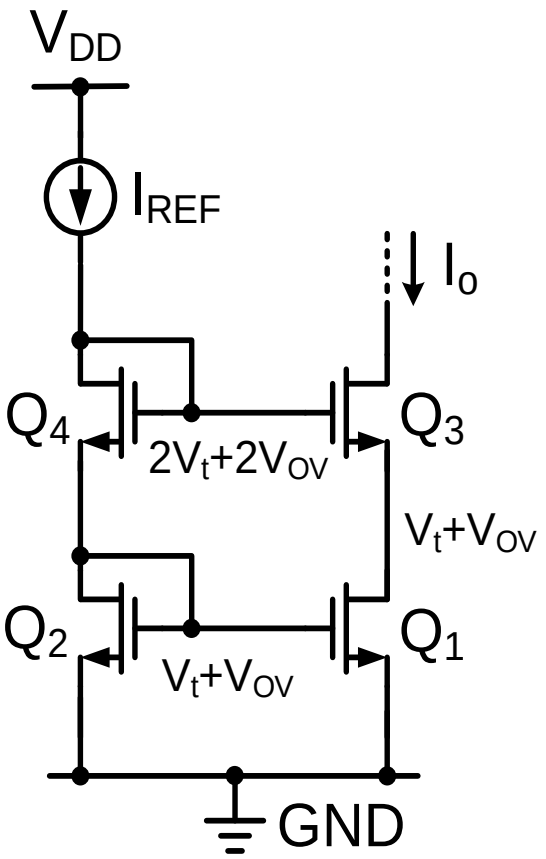
- High PSRR (to-V_{SS})
  - much less susceptible to the effect of high-frequency noise on GND
  - power supply noise may be induced from
    - logic circuit
    - switches of SC circuit
    - current switching

★ Low PSRR (to-V_{SS}) in cascaded 2-stage OPAMP
  - GND noise $\rightarrow$ Q_6 source $\rightarrow$ Q_6 gate $\rightarrow$ C,R $\rightarrow$ output
  - GND noise $\rightarrow$ Q_6 source $\rightarrow$ Q_6 V_{GS} $\rightarrow$ amplified and appear at output

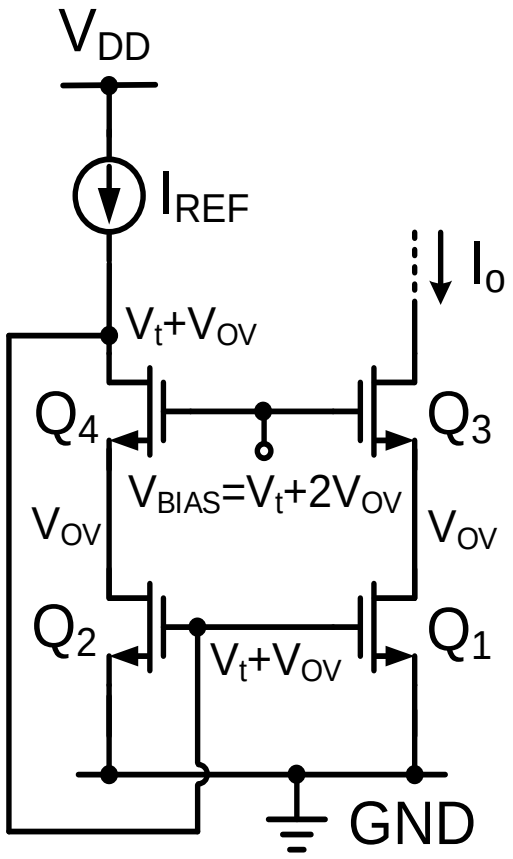


Wide-Swing Current Mirror

- Increased output voltage range
  - $v_{Omin} \geq V_{OV1} + V_{OV3} + V_{tn}$



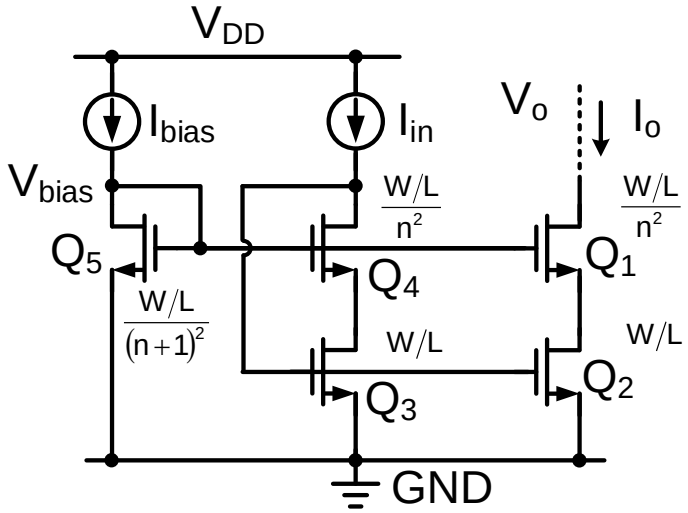
  - $v_{Omin} \geq V_{OV1} + V_{OV3}$



Wide-Swing Current Mirror (Cont.)

- Design example

  a varying signal $I_{in} \le I_{bias}$



$$V_{eff_2} = V_{eff_3} = \sqrt{\frac{2I_{D_2}}{\mu_n C_{ox}(W/L)}} = V_{eff}$$

$$(\because I_{D2} = \frac{\mu_n C_{ox}}{2}\frac{W}{L}V_{eff}{}^2)$$

Since $\left(\frac{W}{L}\right)_2 = \left(\frac{W}{L}\right)_3 = (n+1)^2\left(\frac{W}{L}\right)_5 = n^2\left(\frac{W}{L}\right)_1 = n^2\left(\frac{W}{L}\right)_4$

$V_{eff_1} = V_{eff_4} = nV_{eff}$ for the target $I_{in} = I_{bias}$

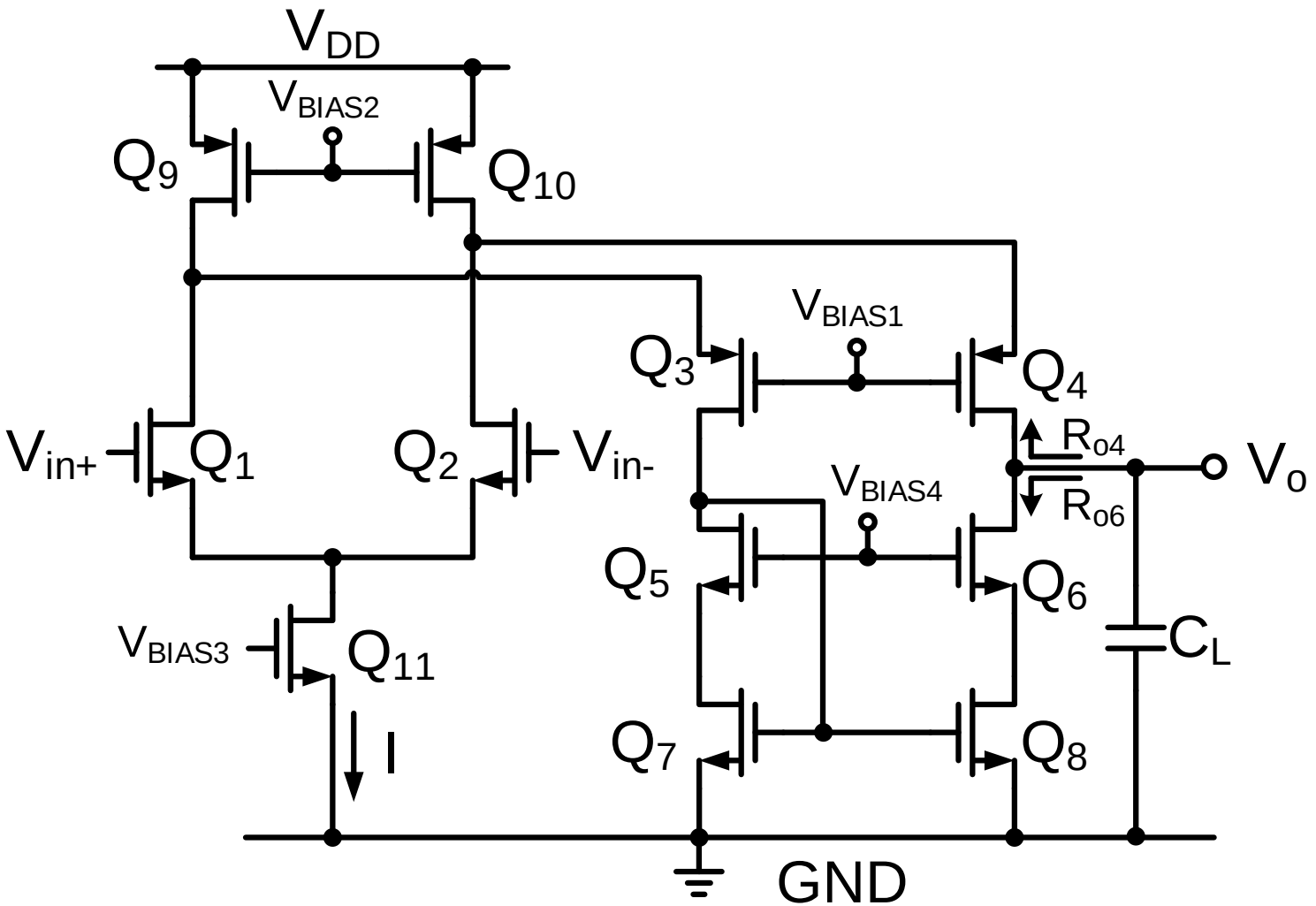
$V_{G_5} = V_{G_4} = V_{G_1} = (n+1)V_{eff} + V_{th}$

$V_{DS_2} = V_{DS_3} = V_{G_5} - V_{GS_1} = V_{G_5} - (nV_{eff} + V_{th}) = V_{eff}$

$\Rightarrow V_o > V_{eff_1} + V_{eff_2} = (n+1)V_{eff}$

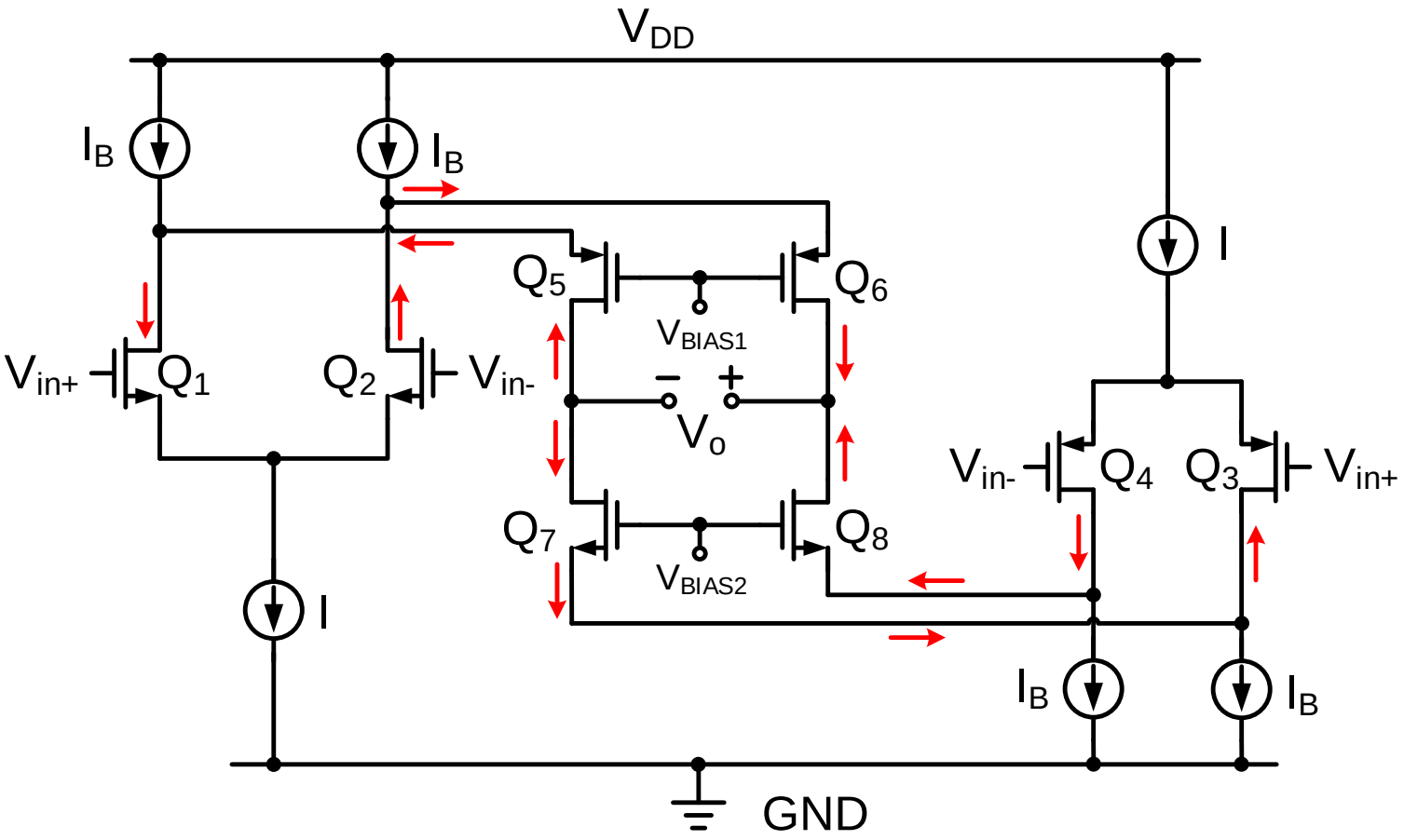
- A common choice, $n = 1,\ V_{out} > 2V_{eff}$

Folded-Cascode with Wide-Swing Current Mirror



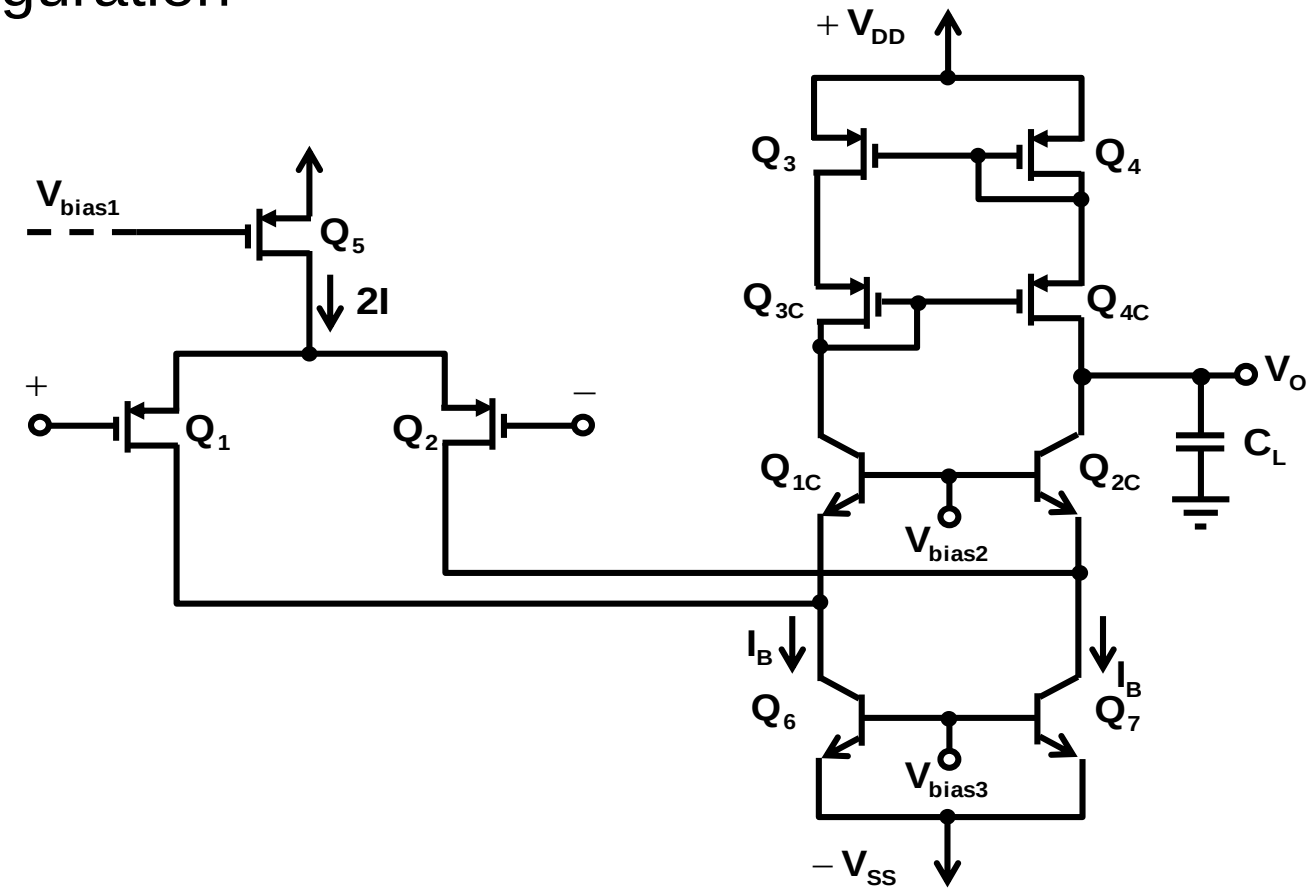
Folded-Cascode with Rail-to-Rail Input Operation

- Increased input common-mode range, rail-to-rail or even larger
- Voltage gain, if $g_{m1}=g_{m3}=G_m$
  - $A = (g_{m1}+g_{m3})R_o = 2G_mR_o$ for middle V_{ICM}
  - $A = g_{m1}R_o$ for high V_{ICM}
  - $A = g_{m3}R_o$ for low V_{ICM}



BiCMOS Folded-Cascode OPAMP

- Configuration



- When it is necessary to drive a resistive load, a low resistance output buffer is needed

BiCMOS Folded-Cascode OPAMP (Cont.)

- The largest nondominant pole is usually generated at the emitter nodes of Q_{1C} and Q_{2C}

$$\omega_{p2} \approx \frac{1}{R_{1C}C_{p1}} \approx \frac{g_{m1C}}{C_{p1}} \quad \text{where} \quad R_{1C} \approx R_{e1c}//r_{O(Q16)}//r_{O(Q1)} \approx R_{e1c} = \frac{1}{g_{m1c}}$$

  - The transconductance of BJT can be much larger than that of CMOS

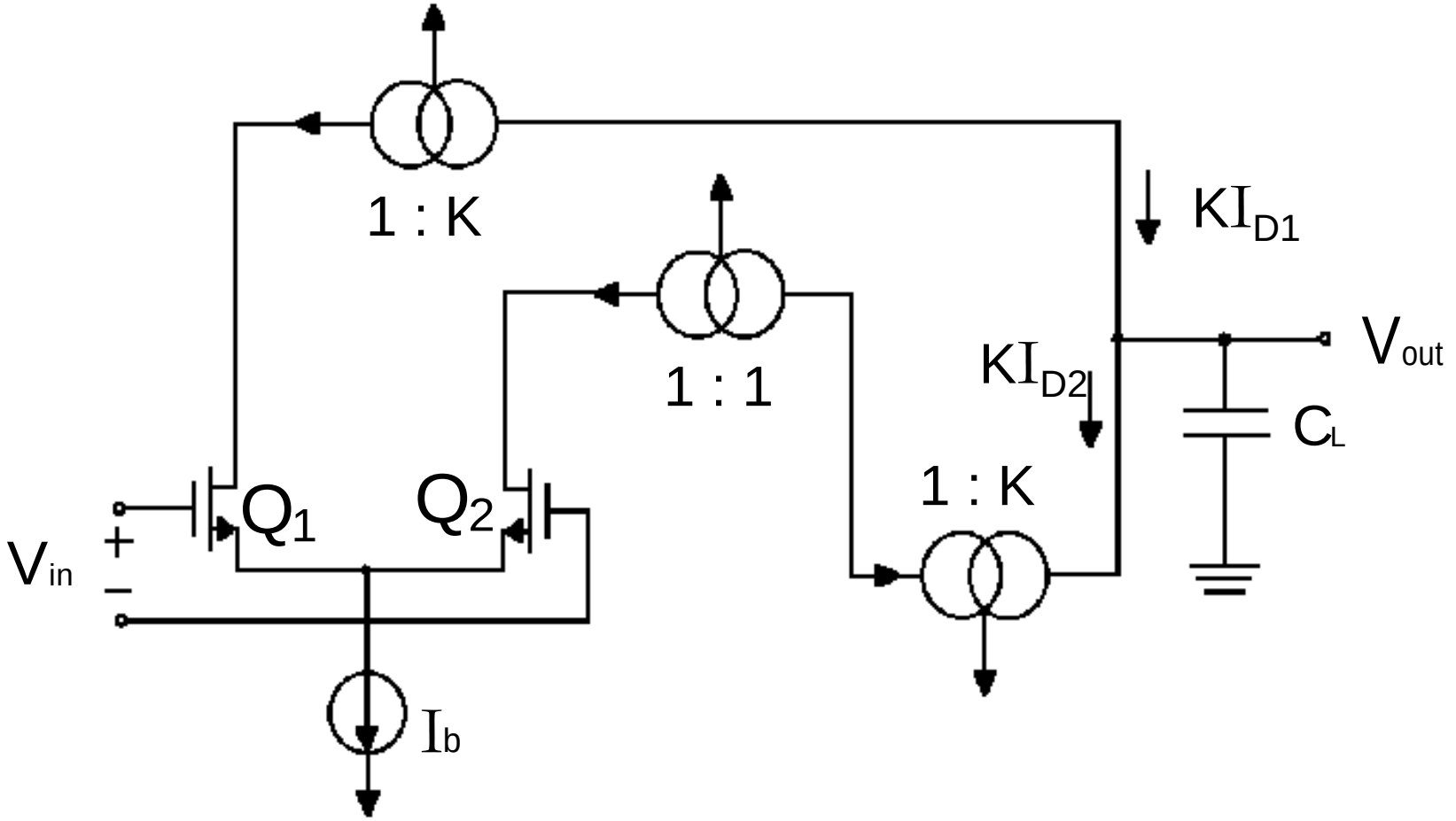
    $\Rightarrow \omega_{P2}$ can be increased

    $\Rightarrow \omega_u$ can be increased while enough phase margin is maintained

    $\Rightarrow$ Wider bandwidth than that of CMOS folded-cascode OPAMP

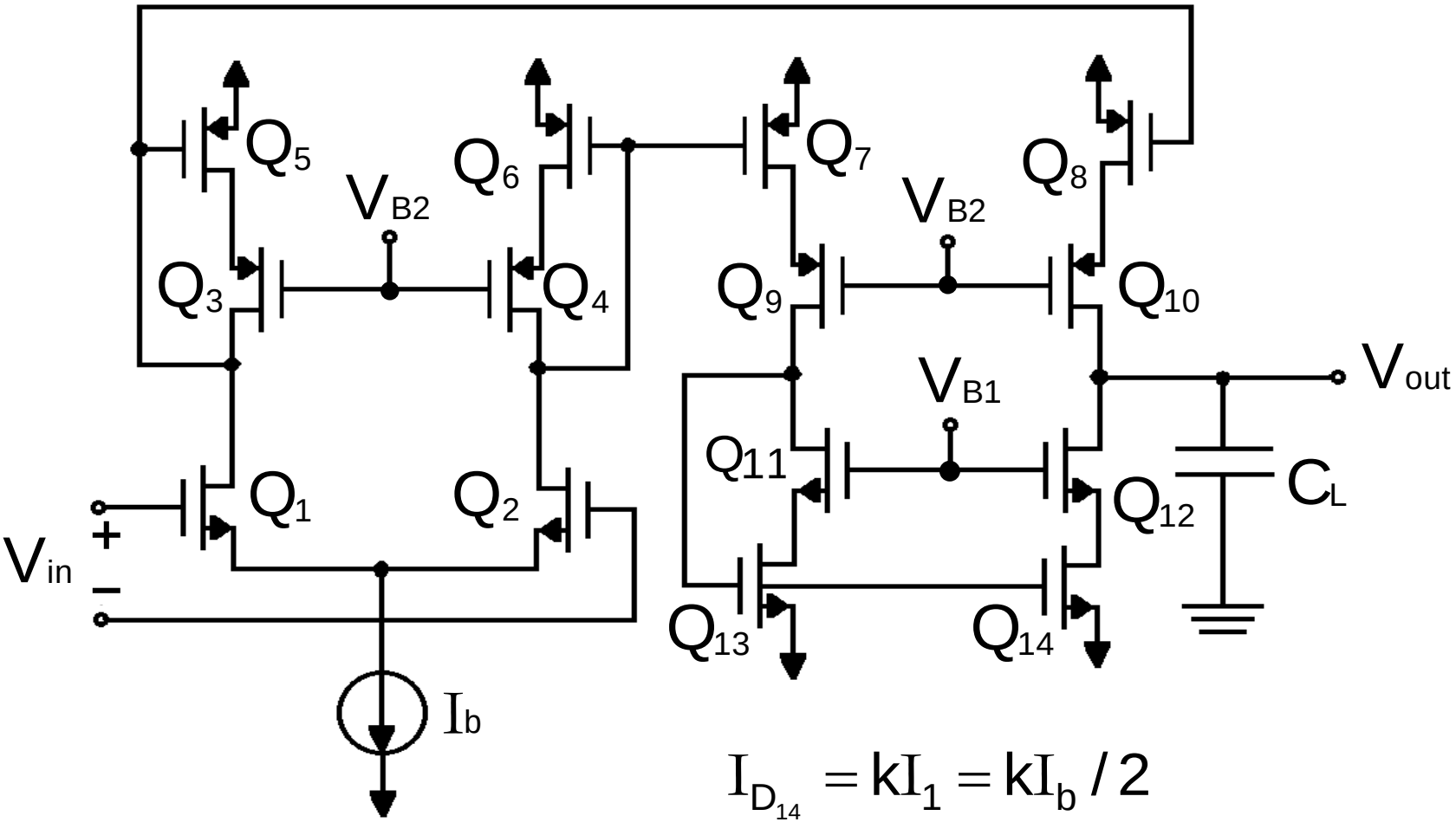
Current Mirror OPAMP

- A simplified current-mirror OPAMP



Current Mirror OPAMP (Cont.)

- A current-mirror OPAMP with wide-swing cascode current mirrors



$$I_{D_{14}} = kI_1 = kI_b / 2$$

Current Mirror OPAMP (Cont.)

$$\frac{(W/L)_8}{(W/L)_5} = k, \quad \frac{(W/L)_7}{(W/L)_6} = 1, \quad \frac{(W/L)_{12}}{(W/L)_{11}} = \frac{(W/L)_{14}}{(W/L)_{13}} = k$$

- $A_V = \dfrac{V_{out}(s)}{V_{in}(s)} = k g_{m1} z_L(s) = k g_{m1}(r_{out} // C_L) = \dfrac{k g_{m1} r_{out}}{1 + s r_{out} C_L}$

  where k is the current gain from Q_5 to Q_8

- Unity-gain frequency ω_t

$$\omega_t = \frac{k g_{m1}}{C_L} = \frac{k\sqrt{2 I_{D1} \mu_n c_{ox} (W/L)_1}}{C_L}$$

- Total OPAMP current $I_{total} = (3 + K) I_{D1}$

Current Mirror OPAMP (Cont.)

$$\omega_t = \frac{k\sqrt{2\left(\frac{I_{total}}{3+k}\right)\mu_n C_{ox}(W/L)_1}}{C_L} = \frac{k}{\sqrt{3+k}}\frac{\sqrt{2I_{total}\mu_n C_{ox}(W/L)_1}}{C_L}$$

$k \uparrow \Longrightarrow \omega_t \uparrow$ for a specified power dissipation

- The important nodes for determining the nondominant pole are the drain of Q_1, primarily, and the drains of Q_2 and Q_9, secondly.

  Increasing K increases the capacitances of these nodes while also increasing the equivalent resistances.

Current Mirror OPAMP (Cont.)

As a result, the equivalent second pole moves to lower frequencies. If K is increased too much, an increase in C_L will be required to keep ω_t below the frequency of the equivalent second pole to maintain stability. Thus, increasing K decreases the bandwidth when the equivalent second poles dominate. In the case where the load capacitance is small, the equivalent second pole will limit the unity-gain frequency of the opamp, and if it is very important that speed is maximized, K might be taken as small as one. From experience it has been found that a reasonable compromise for a general-purpose opamp might be to let K = 2.

Current Mirror OPAMP (Cont.)

- Slew rate

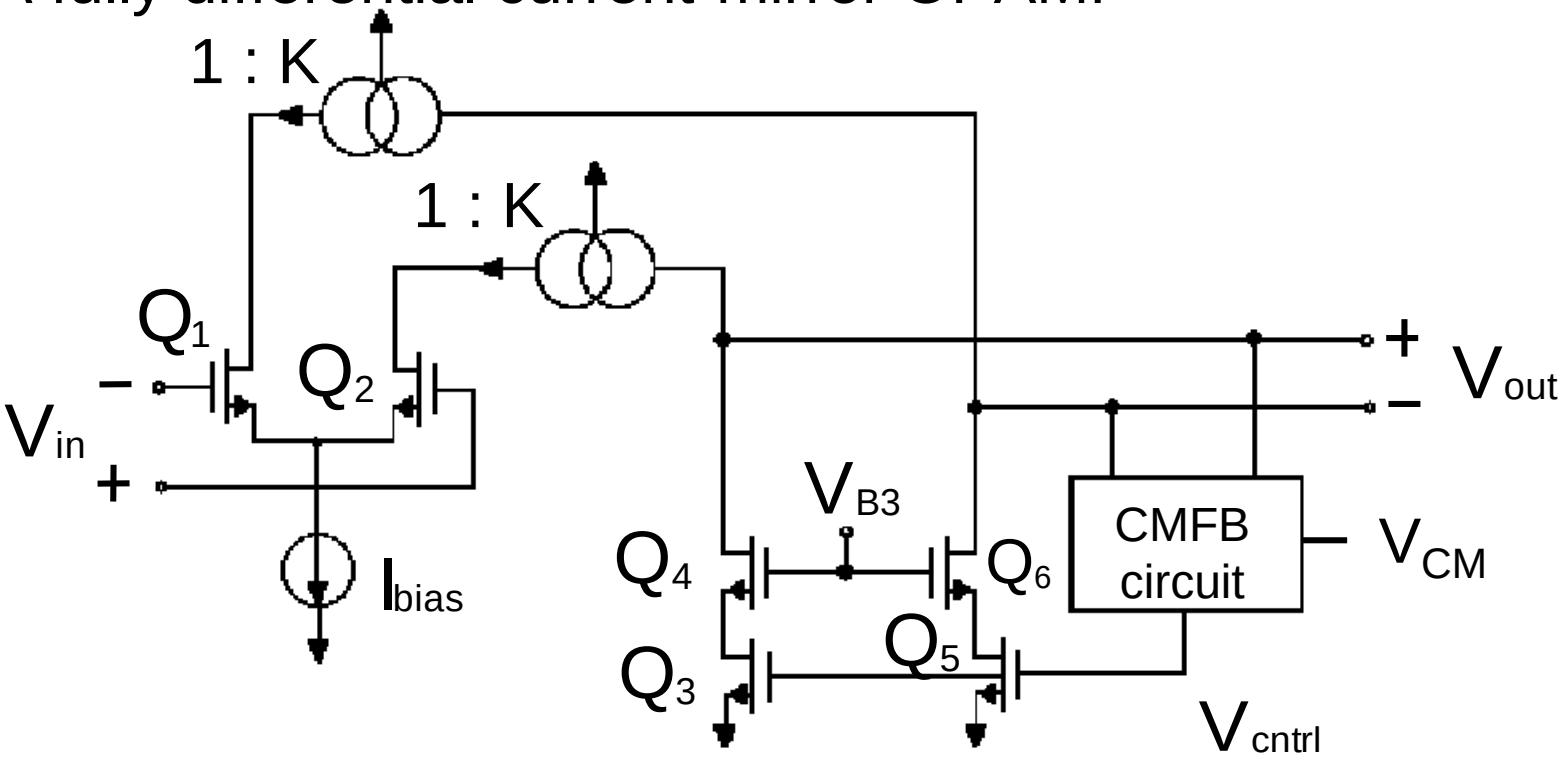
$$SR = \frac{kI_b}{C_L} \bullet\bullet\bullet$$ Larger compared to folded-cascode

- Due primarily to the larger bandwidth and slew rate, the current-mirror OPAMP is usually preferred over a folded-cascode OPAMP.

  However, it will suffer from larger thermal noise when compared to a folded-cascode amplifier because its input transistors are biased at a lower current level and therefore have a smaller transconductance.

Alternative Fully Differential OPAMPs

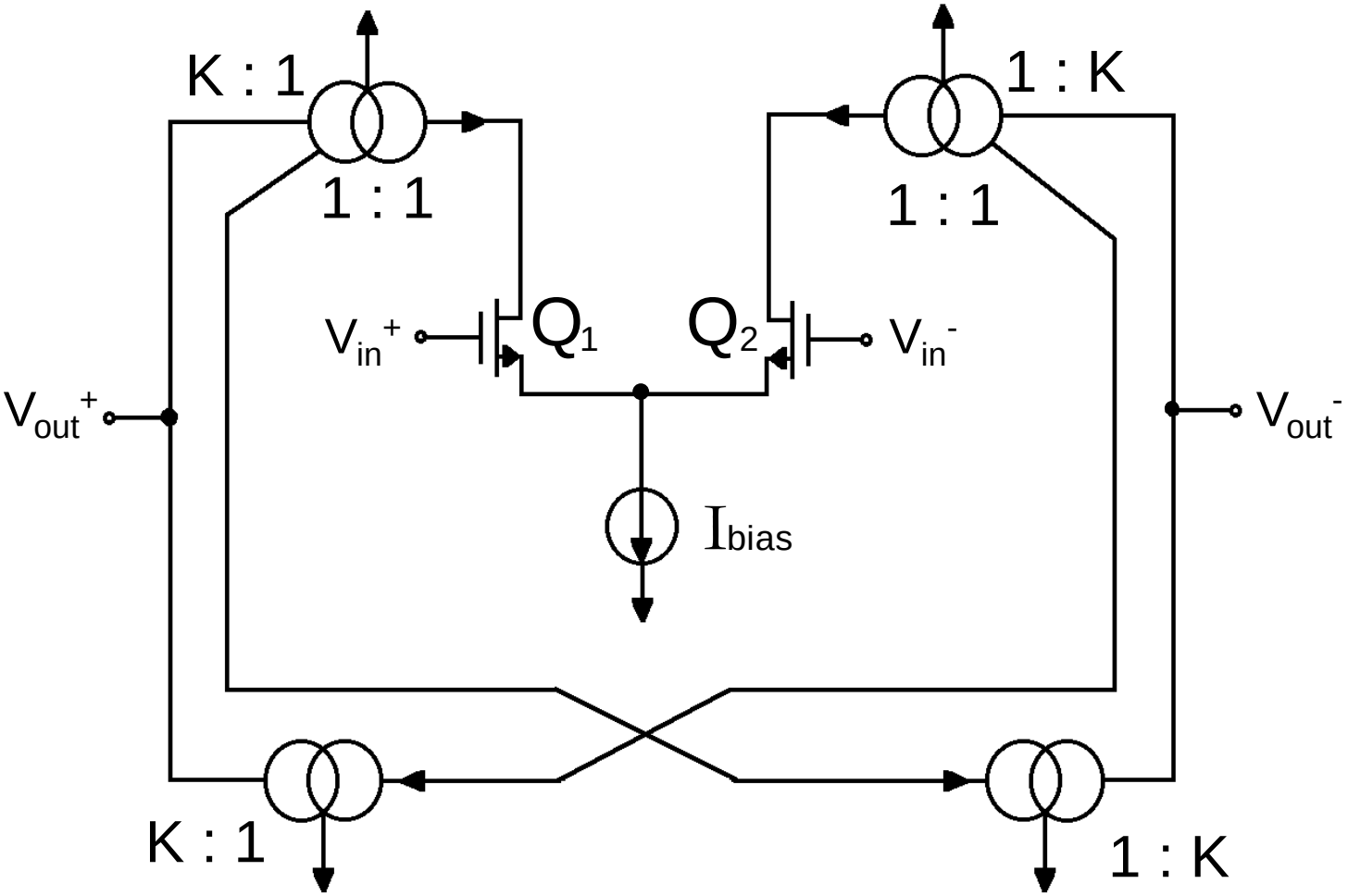
- A fully differential current-mirror OPAMP



- ◆ n-channel input { high gain; lower thermal noise
- ◆ p-channel input { wide bandwidth; low 1/f noise

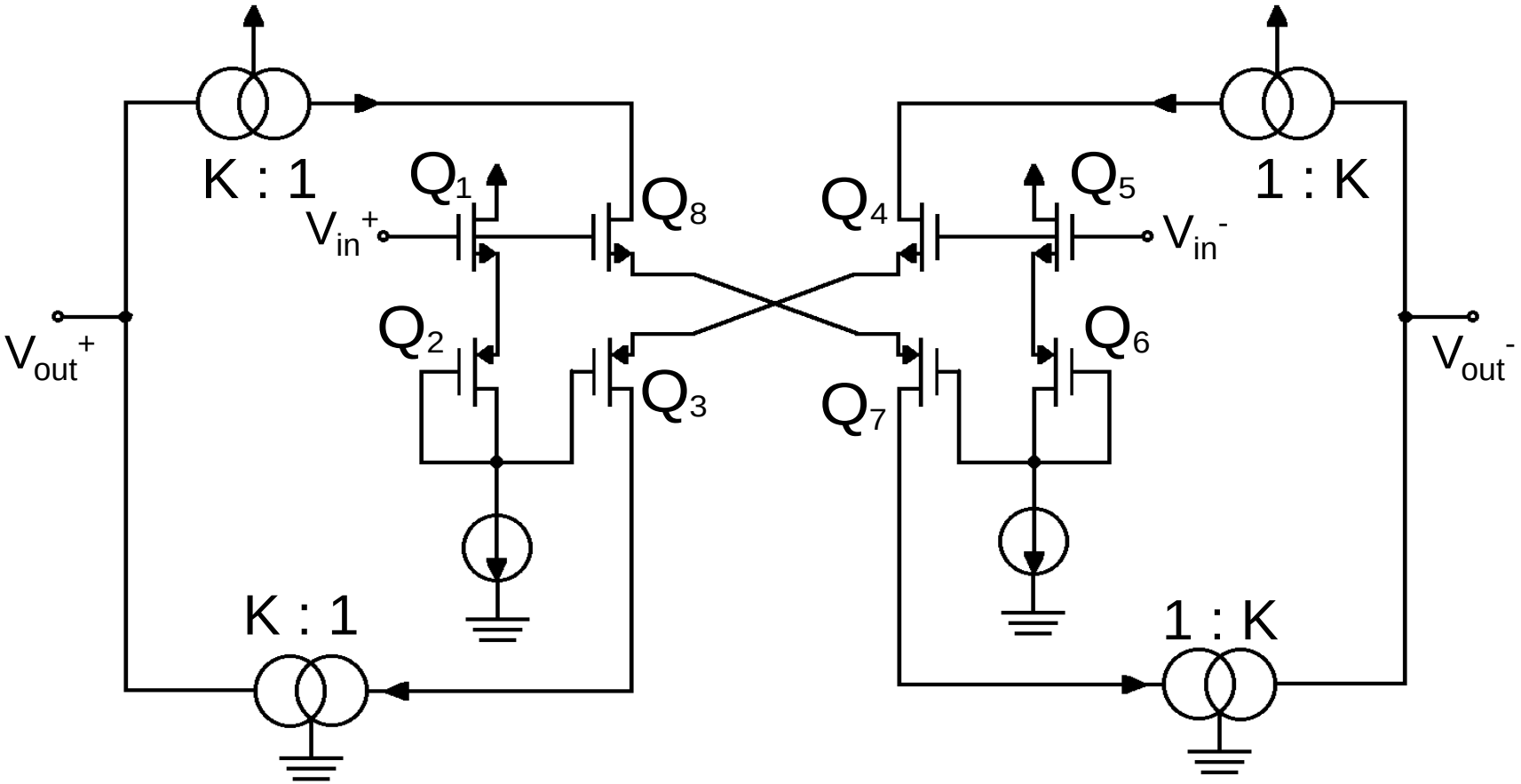
Alternative Fully Differential OPAMPs (Cont.)

- A fully differential OPAMP with bidirectional output drive



Alternative Fully Differential OPAMPs (Cont.)

- A class AB fully differential OPAMP



Alternative Fully Differential OPAMPs (Cont.)

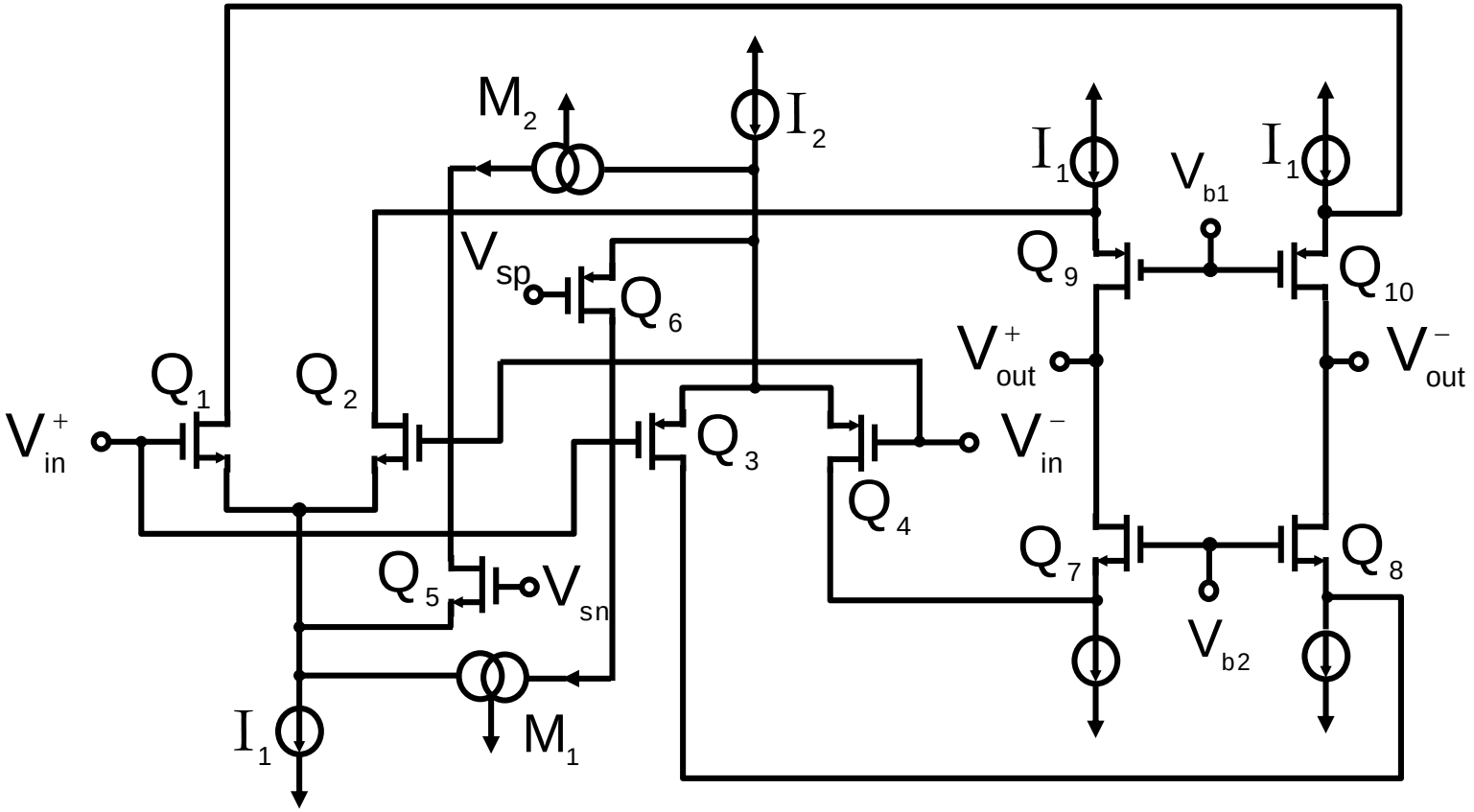
- The advantage of the input stage in this OPAMP is that during slew-rate limiting, one differential pair will turn off, but the total current in the other differential pair will dynamically increase substantially.
- The disadvantage of this design is that the level-shift circuitry required at the input increases the noise and adds additional parasitics, which contribute to the equivalent second pole. In addition, the common-mode range of the input must remain at least $2V_t + 3V_{eff}$ above the lower power supply (and typically higher for the slew-rate performance to be maintained). This is a major problem when 5-V power supplies are being used, and it effectively eliminates this design from consideration for use with 3.3-V power supply voltages. However, for applications where the power-supply voltages are large, the load capacitances are large, and the slew rate is very important, this approach is quite reasonable.

Alternative Fully Differential OPAMPs (Cont.)

- A fully differential OPAMP composed of two single-ended output current-mirror OPAMPs

  ☆ Reading Assignment p.284 ~ 286

- An OPAMP having rail-to-rail common-mode voltage range



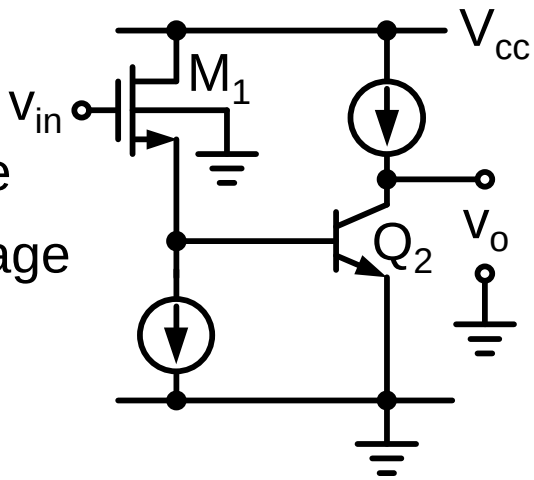
Alternative Fully Differential OPAMPs (Cont.)

- When the input common-mode voltage range is close to one of the power-supply voltages, one of the input differential pairs will turn off, but the other one will remain active.
- In an effort to keep the OPAMP gain relatively constant during this time, the bias currents of the still-active differential pair are dynamically increased. M_1, M_2, Q_5, Q_6 are added for this purpose.
- With careful design, it has been reported that the transconductance of the input stage can be held constant to within 15% of its nominal value with an input common-mode voltage range as large as the difference between the power-supply voltages.

BiCMOS Amplifiers

- Source follower–common emitter
  - $R_i = \infty$

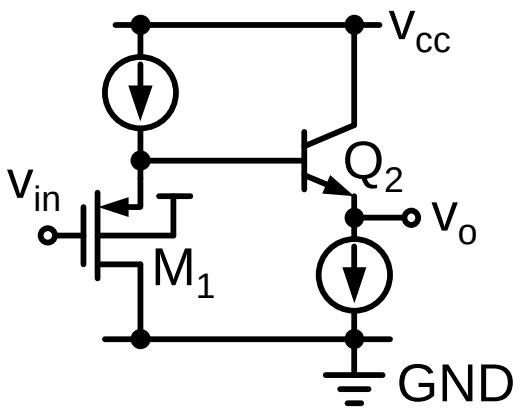
$$A_V = \frac{r_{\pi 2}}{\frac{1}{g_m} + r_{b2} + r_{\pi 2}} \cdot \frac{V_A}{V_T}$$; V_A is Early voltage ; V_T is thermal voltage



  - Advantages:
    - Infinite input resistance
    - Higher gain than MOS common source AMP
  - Drawback: pole at $\omega_p = \frac{1}{[(\frac{1}{g_{m1}} + r_{b2}) // r_{\pi 2}]C_{\pi 2}} = \frac{g_{m1}}{C_{\pi 2}}$

(Assuming $r_{b2} << 1/g_{m1} < r_\pi$)

Source Follower-Emitter Follower

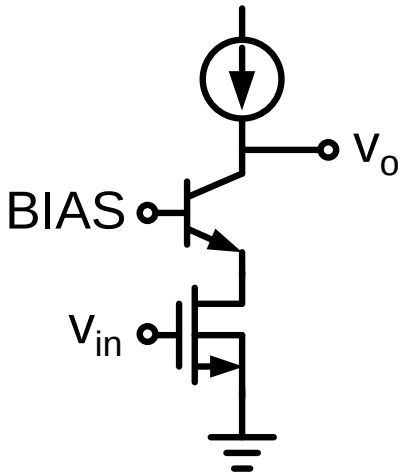


$$;\frac{V_o}{V_i}=1, R_i=\infty, R_o=\frac{1}{g_{m2}}$$

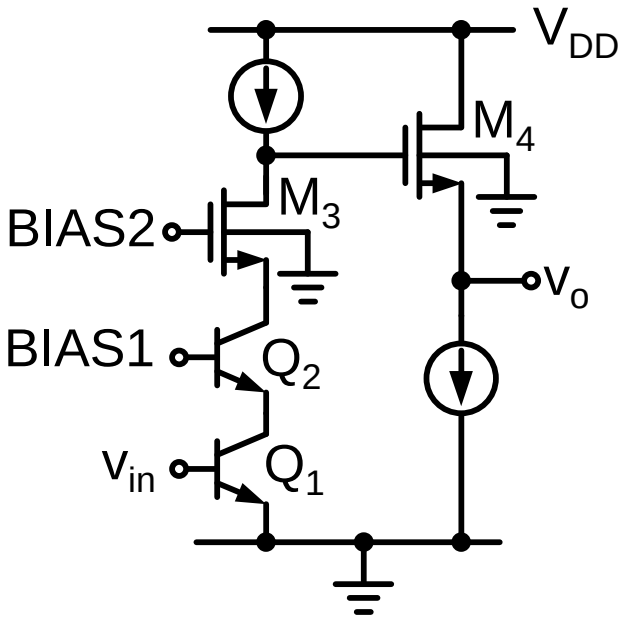
- Note: use PMOS input for better output swing no back-gate effect(N-well process).
  - Advantages: Infinite input resistance
    Low output resistance
  - Disadvantages: pole at $\frac{g_{m1}}{C_{\pi 2}}$

Cascode Amplifiers

- Cascode to increase R_o
  - $R_i = \infty$
  - $A_v = g_{m1}(\beta r_{o2})$
- Advantages:
  - Infinite input resistance
  - High gain
  - Good dynamics(2nd pole at f_T of NPN)
- The above circuit chooses BJT on MOSFET.
  - Higher R_o
  - Higher R_i
  - Wider bandwidth



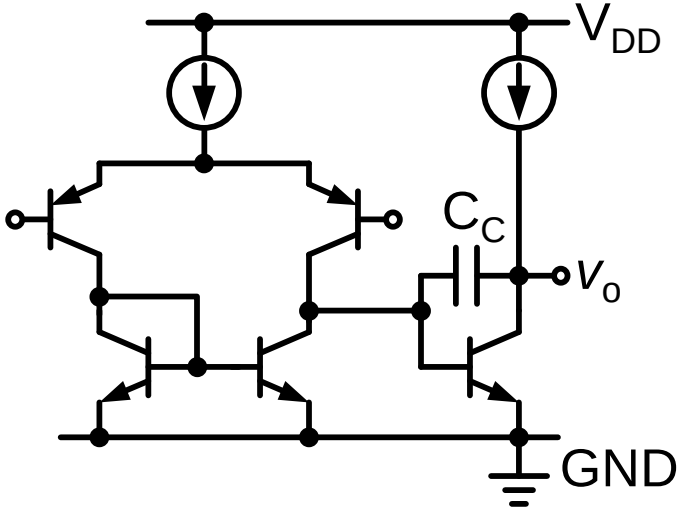
Double Cascode Amplifiers



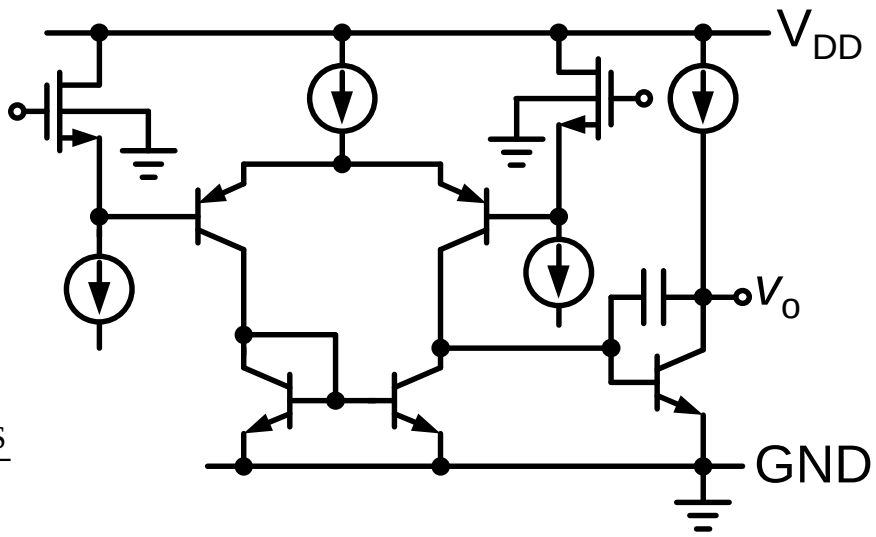
- $R_i = r_{\pi 1}$
- $A_v = g_{m1}(g_{m3}r_{o3})(\beta r_{o2})$
- Advantage: extremely high gain
  (gain of more than 10^6 achievable)
- Note: A source follower can be added
  if any resistive load is to be driven.

OPAMP Circuits

- Bipolar OPAMP



- Source follower input bipolar OPAMP

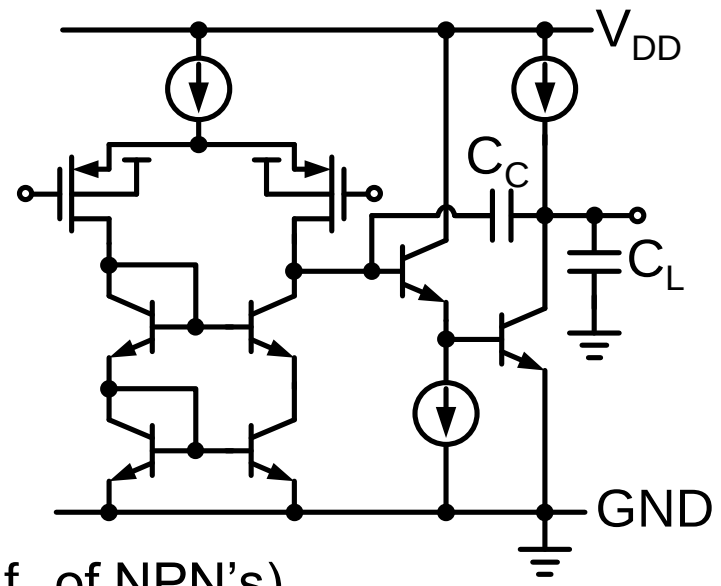


  - Drawback:
    - Additional pole at $\frac{g_{m,MOS}}{C_{\pi,PNP}}$

BiCMOS Differential Amplifier

- For high input resistance and zero input bias current
  - Use MOSFET input
- For low offset
  - Use BJT input.
- Usually, the subsequent stages utilize BJT to obtain a wide bandwidth.

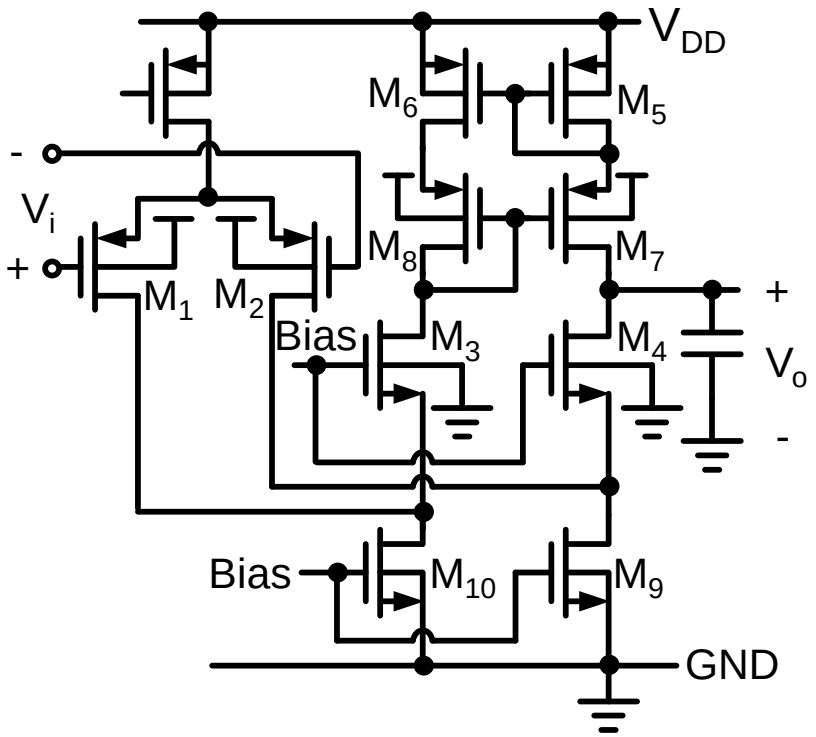
- BiCMOS OPAMP
  - $R_i = \infty$
  - $W_u < P_2 = \frac{G_{m2}}{C_L}$



  - Advantages: high W_u

(higher poles at f_T of NPN's)

CMOS Folded-Cascode OPAMP



$$P_1 \approx \frac{-1}{R_0 C_L}$$

$$P_2 \approx \frac{-g_{m3}}{C_S}$$

; C_S is the total cap. at the source of the common gate transistors

$$\omega_u \approx \frac{g_{m1}}{C_L}$$