Analog IC Design Homework 6 (1/5)

- 1. Use CIC 0.18um 1.8V Virtual Process SPICE Model (cic018.I)
- 2. Please express the steady-state output (V_{out}) of the multiplying-by-four gain amplifiers (as shown in Fig. 1 & Fig. 2) in terms of A, C₁, C₂, C₃, C₄, V_{in}, V_{CM}, and V_{offset}, and explain the difference between Fig. 1 & Fig. 2.
- 3. Please design the multiplying-by-four gain amplifiers (as shown in Fig. 1 & Fig. 2) including two-stage OPAMP, bias circuit and non-overlapped clock circuit (as shown in Fig. 3). Then verify your design with Spectre/HSPICE. Assume C₁=C₂=C₃=C₄=1pF and C_L=1.5pF
 - (a) With $V_{in}=V_{CM}+0.025V$ and $V_{offset}=0V$
 - (b) With $V_{in}=V_{CM}+0.025V$ and $V_{offset}=0.05V$
- Note
 - OPAMP and bias circuit should be included in your homework
 - > You can use the OPAMP and bias circuit designed in homework 2
 - Follow design rules of maximum and minimum transistor width and length
 - Please set the common mode voltage V_{cm} in a reasonable voltage
 - Please use Cadence Virtuoso to build schematic and export the .cir file for verification

Analog IC Design Homework 6 (2/5)



Fig. 1

Fig. 2

Fig. 3

• You should define the clock characteristics as the one shown in Fig. 3.

Accuracy = $\left[1 - \frac{|v_{OUT} - (4v_{IN} - 3V_{CM})|}{4(v_{IN} - V_{CM})}\right] \times 100\% @ t = 1.275 \mu s$

• The waveform of V_{out} , $\Phi 1$ and $\Phi 2$





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Analog IC Design Homework 6 (3/5)

- Your report should include
 - Design flow (Example: The analysis of switches and non-overlap clock circuit)
 - Spectre/HSPICE verification results
 - > The waveform of V_{out} , $\Phi 1$ and $\Phi 2$
 - > Accuracy of the multiplying-by-four gain amplifiers (Please refer to testbench)
 - Virtuoso schematic (Include the .cir file and circuit diagram)
 - Total current and power consumption
 - Area
 - > MOSFET: Please calculate the sum of the W*L for all the MOS used in the designed circuit $A_{MOS} = \sum W_i \times L_i$
 - Resistor / Capacitor: Just show the resistance / capacitance (if used)
 - Table of specifications

	Fig	g. 1	Fig	ı. 2
Area (µm²)				
Power consumption (µW)				
	w/o offset	w/ offset	w/o offset	w/ offset

 Note: The total current, power consumption and area should include bias circuits, twostage OPAMP and non-overlapped clock circuit

Analog IC Design Homework 6 (4/5)

Grading

- Customization of the .sp file will not be accepted
- Please use Virtuoso Spectre or HSPICE to verify your circuit
- Under the condition of all circuits are composed of MOS, R and C and meet the test conditions, the higher accuracy, area, and power consumption will receive higher scores
- Please clearly describe the design flow in your report and attach your calculation process (Do not copy)
- Report with simulation results only but no design flow will get deducted points according to the situation
- Report with advanced discussion and analysis will receive higher scores
- Precautions
 - ◆ Deadline: <u>12/18/2022 (Sun.) 23:59:59 pm (</u>不接受作業補交)
 - Personal work, please upload Word and Virtuoso library (or HSPICE code) to moodle
 - ◆ Please compress files into a .zip file and name it as HW#_student ID, ex: HW6_E24064088 Font size: 12pt (Chinese: 標楷體, English: Times New Roman)
 - Refer to the IEEE submission regulations, set the picture resolution to 300dpi.
 - Upload file size is recommended to be 2MB

Analog IC Design Homework 6 (5/5)

- Virtuoso library folder
 - Add virtuoso folder into the zip file (make sure your file can be opened by virtuoso)



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analogLib			schematic	29k
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• Use the resistor and capacitor in analogLib library (res, cap)

Appendix 1: Circuits for Reference (1/4)

Bias circuit & Two-stage OPAMP



• Non-overlapped clock circuit





• Step 4: 設計start up circuit

Appendix 1: Circuits for Reference (3/4)

Design Flow of Two Stage OPAMP

● Step 1: 決定C_C(一般C_C值會小於C_L,太大會增大整體面積,太小會受到雜散電容的影響)

• Step 2: 由
$$\phi_m = 90^\circ - \tan^{-1}({f_t}/{f_{P_2}}) = 63^\circ \rightarrow f_{P_2} = \frac{g_{m_{13}}}{2\pi C_L} \approx 2 f_t \perp f_t = \frac{g_{m_8}}{2\pi C_C} \rightarrow 求得 g_{m_{13}}$$

- Step 3: 由 Slew rate(SR) < $\frac{I_{11}}{C_c}$ & $\frac{I_{12}}{C_c + C_L} \rightarrow C_c$ 已知且SR須同時滿足兩公式 → 求得 $I_{11} \setminus I_{12}$
- Step 4: 由DC Gain A₀ = $\frac{\alpha I_{D_8}}{V_{eff8}}$ ($r_{o_8}||r_{o_{10}}$) $g_{m_{13}}(r_{o_{12}}||r_{o_{13}})$ → $I_{12} = I_{13}$ → 求得 V_{eff8}
- Step 5: 求出W/L (由上述條件可算出除了M₉~M₁₀跟M_C的(W/L)值)
 - ◆ Mg跟M10的size決定Vgs13的大小,調整(W/L)g~10得到先前算出的Veff13

◆
$$M_{C}$$
的size可由設計好的 R_{C} 值及公式 $R_{c} = \frac{1}{Kn'(\frac{W}{L})_{Mc}(V_{GS_{Mc}}-V_{t})}$ 求出

- Note: n3與Vout的偏壓點會決定M8、M10、M12跟M13的操作區域
 - ◆ 如果Vout的偏壓點過低,讓M13接近Linear region,會影響Gain的大小(ro變小)
 - ◆ 若往下拉力量太強,只要稍微降低V_{gs13},就可以讓V_{out}的偏壓點上升
 - ◆ 若 V_{OUT} bias 偏低,可以 M9↑, M10↑或 M13↓

Appendix 1: Circuits for Reference (4/4)

Information of Slew Rate

- 講義6-29, 6-30所推得結果: Slew rate(SR) = ^{I₁₁}/_{Cc} → 不完全適用於這次作業
 - ◆ 因為講義上之範例,第二級為ideal OP且無C_L
 - ◆ 當 I_{12} 足夠大 → Slew rate(SR) = $\frac{I_{11}}{C_C}$
 - ◆ 當 I_{12} 不夠大 → Slew rate(SR) < $\frac{I_{11}}{C_C}$ & $\frac{I_{12}}{C_C + C_L}$
- V_{DD} Rising & Falling 之 Slew rate(SR) M11 ao M12 12 To Vout **M8** in+ out M_{c} T n2 h3 M13 /110 M9 I₁₀ GND Positive slewing

Appendix 2: Virtuoso Spectre Simulator (1/12)

- Terminal: cd CIC_PDK (0.18um virtual process virtuoso library)
- Terminal: source sourceMe
- Terminal: virtuoso & \rightarrow Create a Library for CIC018 Model

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Compression enabled						OK Cancel He
	OK Cancel	Defaults Apply He	Ip			

Appendix 2: Virtuoso Spectre Simulator (2/12)

• Create Cell View



Appendix 2: Virtuoso Spectre Simulator (4/12)

- Editing Interface \rightarrow Add an Instance (Press 'i' to add instance)
- Press 'q' to edit object properties \rightarrow Please show properties in your schematic circuit

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Appendix 2: Virtuoso Spectre Simulator (5/12)

- Piece-Wise Linear Voltage Source (Cell name: vpwl)
 - In analogLib



Browse	Reset Instance Labels Display	
Property	Value	C
Library Name	analogLib	off
Cell Name	vpwl	off
View Name	symbol	- off
Instance Name	VO	off

CDF Parameter	Value
Frequency name for 1/period	
Number of pairs of points	6
Time 1	0 s
Voltage 1	0 V
Time 2	1u s
Voltage 2	0 V
Time 3	1.5u s
Voltage 3	1.8 V
Time 4	2.5u s
Voltage 4	1.8 V
Time 5	3u s
Voltage 5	0 V
Time 6	4u s
Voltage 6	0 V

Period of the PWL

4u s

Appendix 2: Virtuoso Spectre Simulator (6/12)

Global VDD and GND (Cell name: VDD and GND)

Û٥	Add Instance (on cfc5) + ×
Library	analogLib Browse
Cell	vdd
View	symbol
Names	
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Array	Rows 1 Columns 1
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	Hide Cancel Defaults Help

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Library	analogLib Browse
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View	symbol
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	Hide Cancel Defaults Help

Set VDD as $1.8V \rightarrow Add$ a 1.8-V DC voltage source (Cell name: VDC)

	0 •	Add Ins	tance (on cfc5)	↑ ×
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	Cell	vdc		
	View	symbol		
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	Number	of noise/freq pairs	0	
	DC voltag	e	1.8 V	

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Appendix 2: Virtuoso Spectre Simulator (7/12)

- Wiring and Wire Name setting
 - 'w' for wiring
 - 'I' (lower case of L) for adding wire name
 - > Attach the auxiliary line to the wire to be named

۰ 🛈	Create Wire Name (on cfc5) 🛛 🛧 🗙
	Names in out
	Expand bus names
	Attach to multiple wires
	📃 Create net alias labels
	🔲 Display bundles vertically



- Simulation by Spectre
 - Check and save it before using spectre for simulation \rightarrow Launch \rightarrow ADE XL



Appendix 2: Virtuoso Spectre Simulator (8/12)

Create a test for the schematic



Select CIC018 Model



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Appendix 2: Virtuoso Spectre Simulator (9/12)

• Choose Analysis: .tran (Transient) \rightarrow Plot Result \rightarrow Click the wire to be plotted

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Appendix 2: Virtuoso Spectre Simulator (10/12)

Run Simulation → Waveform Window

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Delete → Delete output variable



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Appendix 2: Virtuoso Spectre Simulator (11/12)

Way 1 to get power: iprobe in analogLib



點iprobe component



ADE XL Test Editor - test_lib:inv:1 (on cfc5)							
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Appendix 2: Virtuoso Spectre Simulator (12/12)

XL

Way 2 to get power: DC analysis and Annotate

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	🔾 stb	🔾 pz	◯ If	⊖ sp	
	🔾 envlp	O pss	🔾 pac	🔾 pstb	
	🔾 pnoise	⊖ pxf	🔾 psp	🔾 qpss	
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