Midterm Exam Analog IC Design NCKUEE

1. Briefly describe the following questions.

   (a) Please use cascode and ratio matching techniques to design a wide-swing current mirror, as shown in Fig. P1(a), which can generate accurate $0.6 \times I_O$. Describe your design and draw your schematic. Do not apply any DC voltages except V_{DD} and GND.

   (b) Explain pole-zero frequency doublet with the first stage of a two-stage OPAMP shown in Fig. P1(b) by showing that $\frac{i_{out}}{v_{in}} = g_{m1} \cdot \left(\frac{1 + s/2\omega_p}{1 + s/\omega_p} \right)$, where $\omega_p = \frac{g_{m3}}{C_X}$. Assume $g_{m1}=g_{m2}$, $g_{m3}=g_{m4}$, $C_X=C_{gs3} + C_{gs4} + C_{db1} + C_{db3} + C_{gd1}$.

   (c) Briefly describe mobility degradation.

   (d) Describe flicker noise and how to reduce it. Explain the correlated double sampling (CDS) circuit.

   (e) Briefly describe noise bandwidth and how kT/C noise is generated.

   (f) Briefly explain how to prevent latch-up problem.

   (g) Briefly describe device mismatch and list two major capacitor mismatch errors. How to get accurate resistor and capacitor ratios?

   (h) Briefly explain yield and what factors affect it.

   (i) Briefly explain antenna rule.

   (j) Briefly describe subthreshold operation of MOSFET.

   (k) Briefly describe how to set the input and output common mode voltage of single-ended and fully-differential ended resistive-feedback inverting amplifier with its closed loop gain = $-R_1/R_2$, respectively.

   (l) What is the full power bandwidth of an OPAMP with a rated output voltage of 1V and a slew rate of 1V/ns?

   (m) Describe the purpose of capacitor layout with equal perimeter-to-area ratio, and show a capacitor layout with **equal perimeter-to-area ratios** of 2 units and 3.35 units, where a unit-sized capacitor is 10μm x 10μm. (Hint: when a **non-unit-size** is required, it is usually set to between one and two times the unit-sized capacitor and is **rectangular in shape**, ex : 3.35units=2units+1.35units.)

   (n) Briefly describe how to design a high gain and wideband amplifier with accurate gain and bandwidth. (Hint: feedback, multi stage and switching capacitor may be used to realize such requirement)

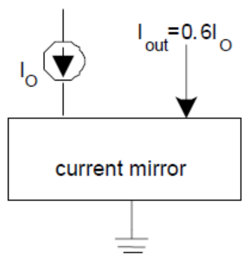


Fig. P1(a)

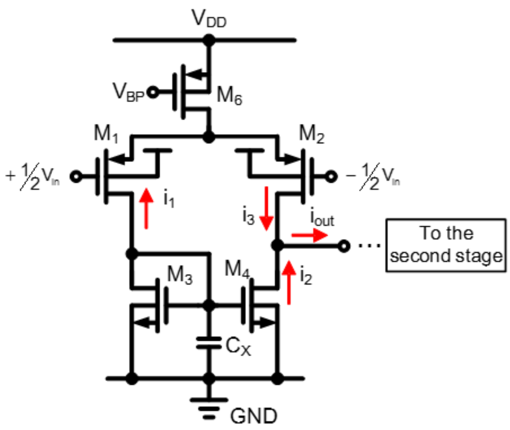


Fig. P1(b)

2. Two voltage amplifiers (each having infinite input impedance and zero output impedance) are available: one with a gain of 3V/V and 6μV_{rms} noise observed at the output; the other with a gain of 10V/V and 15μV_{rms} noise observed at its output.
   (a) What is the input-referred noise of each amplifier?
   (b) If the two amplifiers are to be placed in series to realize a gain of 30V/V, in what order should they be placed to obtain the best noise performance?
   (c) What is the resulting input-referred noise of the overall system in (b)?

3. Answer the following questions.
   (a) Find the total rms noise value if three uncorrelated noise sources having V_{n1_rms}=7μV, V_{n2_rms}=3μV and V_{n3_rms}=4μV are combined.
   (b) Consider an ideal noiseless amplifier with voltage gain of 40dB, and the load capacitor C_L, in parallel with a load resistor, R_L, as shown in Fig. P3, where $V_{RL}(f)$ is the thermal noise of R_L. Assuming T=300K, C=3pF, R=150kΩ, and $k=1.38\times10^{-23}JK^{-1}$, please calculate the squared rms noise across the capacitor, $V_{no\_rms}^2$ and the squared rms input-referred noise of the circuit.

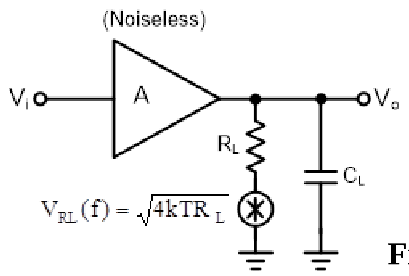


Fig. P3

4. Fig. P4(a) shows a comparator using an OPAMP, where Φ_1, Φ_{1a}, and Φ_2 is shown in Fig. P4(b) and the OPAMP is assumed to be ideal. Describe the operation of offset cancellation in Fig. P4(a).

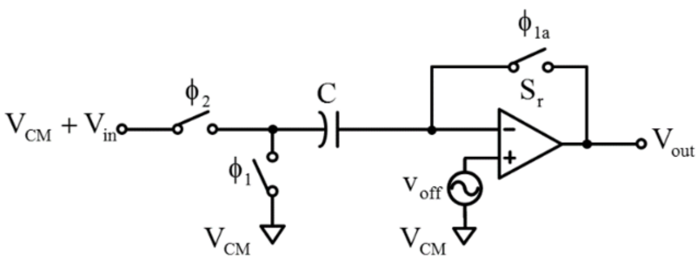


Fig. P4(a)

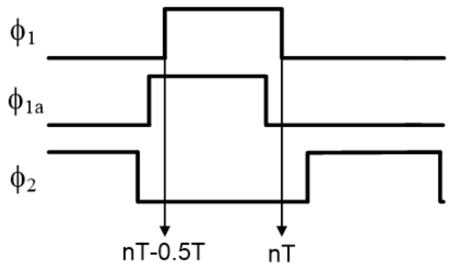


Fig. P4(b)

5. As shown in Fig. P5, there is a cascaded n-stage comparator. Derive the gain A_c of each stage to get the minimum total time constant ($\tau_{total}=\Sigma\tau i$, where $\tau i=1/\omega_{3dB}$), assuming the total gain (A_{tot}) of the comparator is a constant and corner frequency ω_{3dB} of each stage is the same. **Hint :** $\partial A^n/\partial n = A^n \cdot \ln(A)$

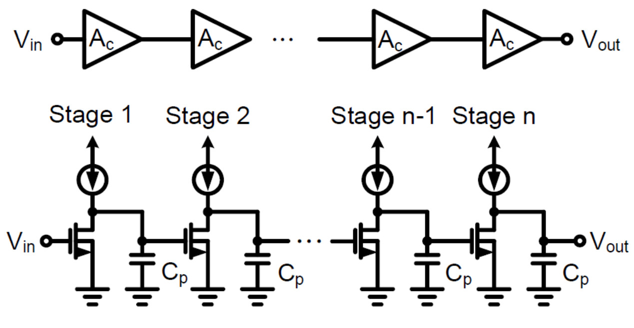


Fig. P5

6. Show the frequency response of $V_{out}(s)/V_{DD}(s)$ in Fig.P6, with the parameters of C_{gs}, g_m, r_{ds} and C_L. In addition, C_{gd}, C_{gb}, C_{sb}, and C_{db} of MOSFETs can be neglected.

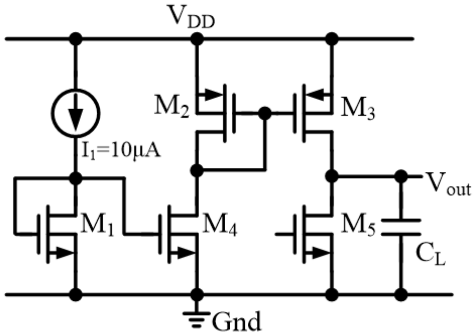


Fig. P6

7. A constant g_m bias circuit is shown in Fig. P7(a). Neglect channel length modulation and body effect.
   (a) For Fig. P7a, please find I_{REF} (non-zero solution) in terms of $\mu_p C_{ox}$、$(W/L)_p$、R and K (K>1).
   (b) According to the circuit shown in Fig. P7(b), find the DC loop gain, $A_0 = (V_o/V_i)$ in g_{m1}, g_{m2} and R.
   (c) Let K=4, what is the value of DC loop gain A_0?

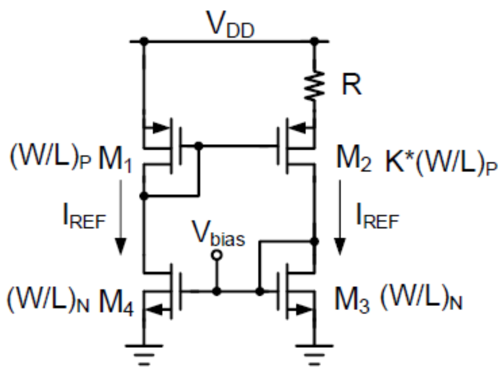


Fig. P7(a)

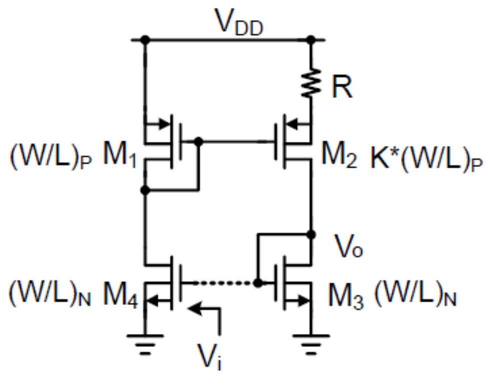


Fig. P7(b)

8. For a single-stage fully differential OPAMP and its common-mode feedback (CMFB) block diagram shown in Fig. P8, where V_{BIAS_P}, V_{BN} and V_{CM} are DC voltage, the transistor sizes are given in Table P8. Assume $\mu_n C_{OX}=100\mu A/V^2$, $\mu_p C_{OX}=40\mu A/V^2$, $V_{tn}=-V_{tp}=0.5V$, $V_{DD}=1.8V$, $\lambda_n=\lambda_p=0.05/L(\mu m)$, $I_{D\_M1}=I_{D\_M2}=10\mu A$, $a_{cms}=1$ and body effect can be neglected.
   (a) Briefly describe the operational principle of CMFB block diagram shown in Fig. P8. (5%)
   (b) Calculate the DC gain of common-mode loop gain. (10%)

   (Hint: common-mode loop gain = $\frac{V_{ctrl}(s)}{V_{oc}(s)} \cdot \frac{V_o^+(s)}{V_{ctrl}(s)}$ or $\frac{V_{ctrl}(s)}{V_{oc}(s)} \cdot \frac{V_o^-(s)}{V_{ctrl}(s)}$)

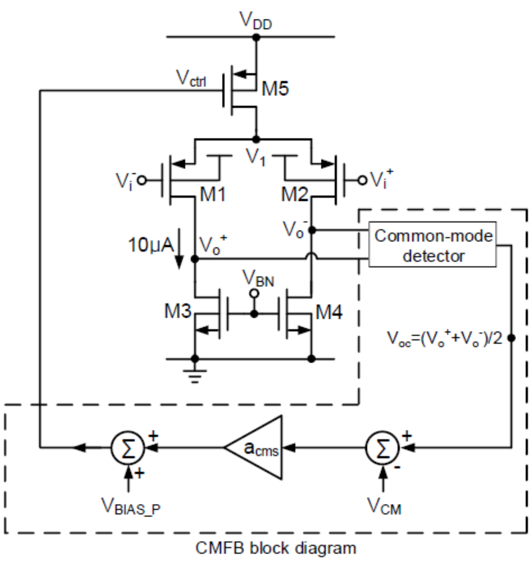


Table P8

The dimension of transistors (in μm)

M1	32/1
M2	32/1
M3	12/1
M4	12/1
M5	64/1

Fig. P8

9. Fig. P9 shows enhanced output-impedance current mirror, where the current source is ideal and the transistor sizes are in Table P9. Assume $\mu_n C_{OX}$=100μA/V^2, $\mu_p C_{OX}$=40μA/V^2, V_{tn}=-V_{tp}=0.5V, V_{DD}=1.8V, λ_n=λ_p =0.05/L(μm). Neglect λ and body effect when determining DC voltage and current.
   (a) Show that the output impedance R_O in Fig. P9 can be approximated as $(1+A)g_{m1}r_{ds1}r_{ds2}$.
   (b) Assuming A=50, calculate the output impedance in Fig. P9.

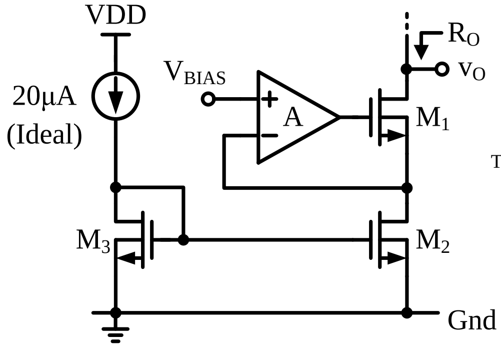


Table P9

Transistor dimension (in μm)

M1	5/0.2
M2	4/0.2
M3	4/0.2

Fig. P9

10. For a two-stage OPAMP and a bias circuit shown in Fig. P10, where C_C=0.2pF, C_L=2pF and input bias voltage=0.8V, the transistor sizes are given in Table P10. Assume V_{DD}=1.8V, $\mu_n C_{OX}$=200μA/V^2, $\mu_p C_{OX}$=80μA/V^2,V_{tn}=-V_{tp}=0.5V, λ=λ_n=-λ_p =0.06/L(μm), neglect λ effect and mismatch errors when determining DC voltage and current.
   (a) Calculate DC currents of I_1 and I_2
   (b) Calculate DC voltages of V_1, V_2 and V_3.
   (c) Calculate the input common mode range of the OPAMP.
   (d) Calculate the DC gain of the OPAMP.
   (e) Assuming the parasitic capacitance of all transistors can be neglected. To place the right-half-place zero on the 2nd pole, calculate the W of Mc. (Hint: the right-half-place zero is at
   $$\omega_z = \frac{-1}{C_c(1/g_{m7} - R_C)}$$)
   (f) Assuming the W and threshold voltage of M1 become 5.2μm and 0.45V respectively due to process variation, calculate the input offset voltage. (5%) (Hint: Input offset voltage is the voltage applied to the input to drive the small signal output voltage to zero)

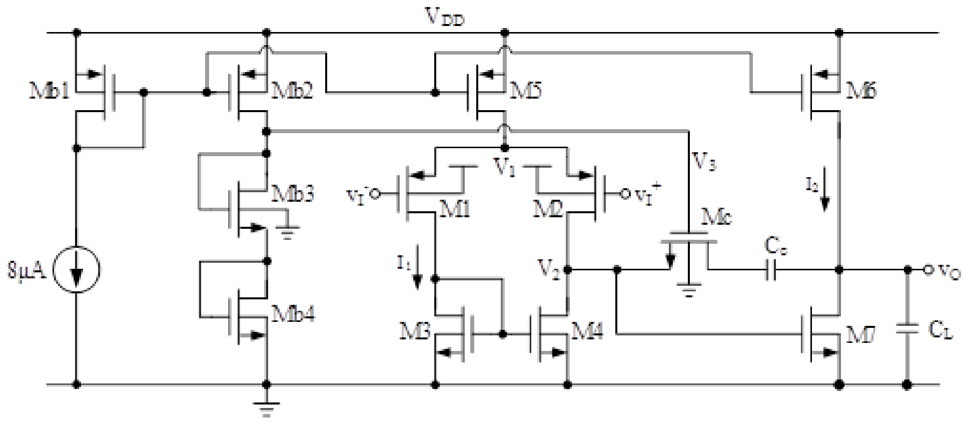


Table P10

The dimension of transistors (in μm)

M1	5.0/0.5	M7	7.5/0.5
M2	5.0/0.5	Mb1	2.0/0.5
M3	2.0/0.5	Mb2	2.0/0.5
M4	2.0/0.5	Mb3	1.5/0.5
M5	12/0.5	Mb4	1.5/0.5
M6	15/0.5	Mc	W_c/0.5

Fig. P10

11. Two structures of high output impedance current mirrors are shown in Fig.P11, where the current sources are ideal and the transistor sizes are shown in Table P11. Assume V_{DD}=1.8V, $\mu_n C_{OX}$=200μA/V^2, $\mu_p C_{OX}$=80μA/V^2, $V_{tn}=-V_{tp}$=0.4V, $\lambda=\lambda_n=-\lambda_p$ =0.2/L(μm). Neglect λ when calculating DC voltage and current.

(a) Please calculate output impedance R_{O1} and minimum output voltage v_{O1} in Fig. P11(a).

(b) Please calculate output impedance R_{O2} and minimum output voltage v_{O2} in Fig. P11(b).

(c) Please modify the circuit in Fig.P11(a) into a wide-swing cascode structure. Simply sketch your answer (use additional bias circuit if needed) and recalculate the minimum output voltage v_{O1}.

(d) If $(W/L)_{M8}$ becomes 6.3/0.5 and $(W/L)_{M7}$ becomes 5.7/0.5, please calculate minimum v_o.

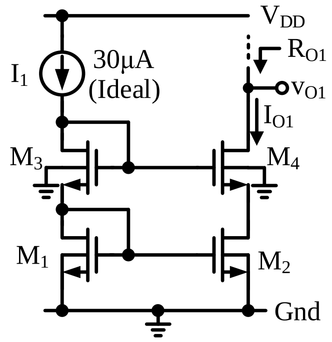


Fig. P11(a)

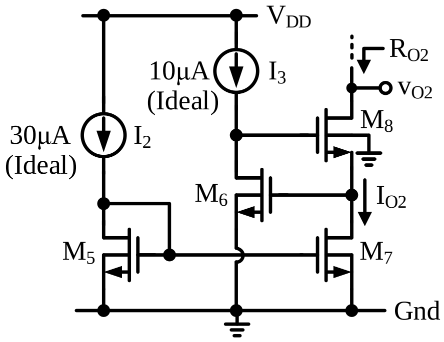


Fig. P11(b)

Table P11
Transistor dimension (in μm)

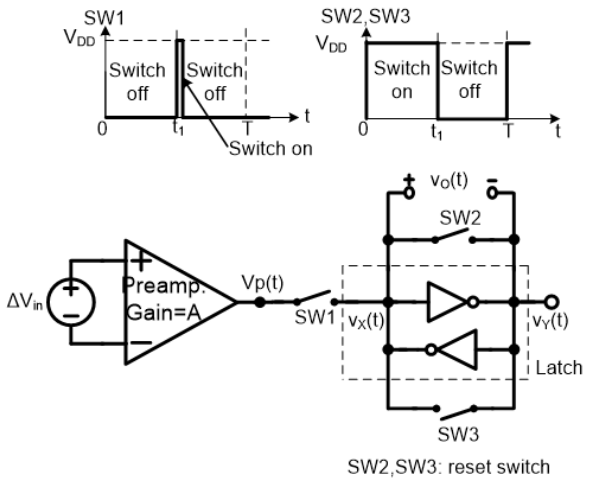
M_1	5/0.5	M_5	3/0.5
M_2	5/0.5	M_6	9/0.5
M_3	6/0.5	M_7	6/0.5
M_4	6/0.5	M_8	6/0.5

12. Fig. P12(a) shows a comparator composed of a pre-amplifier and a positive-feedback latch. The waveforms of the internal nodes are illustrated in Fig. P12(b). Assume the preamplifier output can be expressed as $v_p(t) = A_{pre} \times \Delta V_{in} [1-\exp(-t/\tau_{pre})] + V_{DD}/2$, where $V_{DD}/2$ is the common-mode voltage of the pre-amplifier, and the two inverters are identical.

(a) If $v_o(t) = v_X(t) - v_Y(t)$, and $v_o(t_1)=\Delta V_O$. Please refer to Fig.P12(b) and prove that

$$v_o(t) = \Delta V_O \times \exp\left(\frac{t - t_1}{R_L C_L / (A_{inv} - 1)}\right)$$ for $t_1 < t < t_1+t_2$,where A_{inv}, C_L and R_L are the inverter gain, total capacitance of each node v_X and v_Y, and total resistance of each node v_X and v_Y, respectively.

(b) Please refer to Fig. P12(b) and find the time interval t_2, which is the time it takes for v_O to reach 1.7V after t_1, where VDD=1.8V, t_1=50ps, ΔV_{IN}=0.7μV, τ_{pre}=2ns, R_L=10kΩ, C_L=0.5pF, A_{inv}=181 and the preamp gain A_{pre}=120. Assume the driving capability of PMOS and NMOS of the inverter are the same and $v_o(t_1)=v_p(t_1)$.



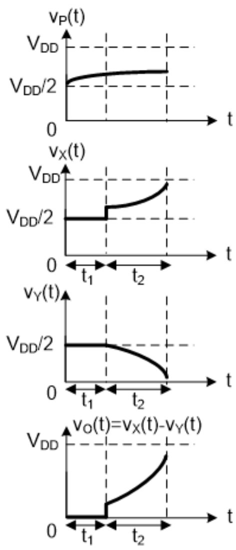


Fig. P12(a) **Fig. P12(b)**

13. A comparator design usually employs preamplifier with offset cancellation and a positive feedback latch as shown in Fig. P13(a). The internal nodal voltage waveforms of this comparator are shown in Fig. P13(b). Specifically, the gain and output time constant of this preamplifier are A and τ, respectively. The clock period of this comparator is T. The output of the preamplifier can be expressed as $V_{preamp}(t)=V_{DD}/2+A*V_{in}\{1-\exp[-(t-nT)/\tau]\}$ for $t\in[nT,nT+T_1]$ if the offset voltage (V_{off}) of the preamplifier are zero. (Assume all switches are ideal).

(a) Considering finite A, please modify the equation of $V_{preamp}(t)$ for $t\in[nT,nT+T_1]$ if V_{off} is non-zero.

(b) If the differential output $V_o(t)=V_x(t) - V_y(t)$, and $\Delta V_o= V_{preamp}(nT+T_1)-V_{DD}/2$. Please prove ,

$$V_o(t)=\Delta V_o\times\exp[\frac{t-nT-T_1}{(R_L C_L/(A_{inv}-1))}]\ \text{for}\ t\in[nT+T_1,(n+1)T]$$

where A_{inv}, C_L and R_L are the inverter gain, total capacitance of each node V_x and V_y, and total resistance of each node V_x and V_y, respectively. Assume the two inverters are identical.

(c) Let τ=4ns, T_1=1ns, R_L=5kΩ, C_L=1pF, A_{inv}=51, A=80, V_{off} =1mV and V_{in}=1.5mV. What is the minimum value of period T for this comparator to let $|V_o(t)|\geqq 0.9V_{DD}$ for $t\in[nT+T_1, (n+1)T]$?

(d) Digital circuit at the comparator differential output requires $-0.9V_{DD}$ and $0.9V_{DD}$ for valid logic "0" and "1", respectively. With parameters in (c), if T=2ns, find the range of V_{in} causing metastability.

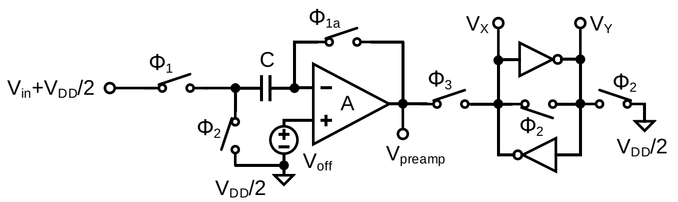


Fig. P13(a)

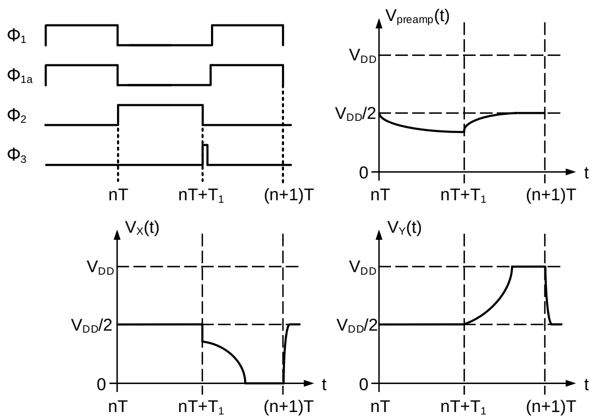


Fig. P13(b)

14. An OPAMP is shown as Fig.P14, where C_C=0.5pF, C_L=2pF and input bias voltage=0.9V. Assume V_{DD}=1.8V, $\mu_n C_{OX}=200\mu A/V^2$, $\mu_p C_{OX}=80\mu A/V^2$, $V_{tn}=-V_{tp}=0.4V$, $\lambda=\lambda_n=-\lambda_p =0.2/L(\mu m)$. Neglect λ and mismatch error when calculating DC voltage and current.

(a) Calculate I_2, V_1, V_2, and V_3.

(b) To eliminate the right-half-place zero altogether ($\omega_z \to \infty$), calculate the W of M_c.

(c) For the condition in (b), calculate the DC gain, unity-gain frequency and phase margin.

(d) Please calculate the value of rising slew rate shown in Fig.P14.

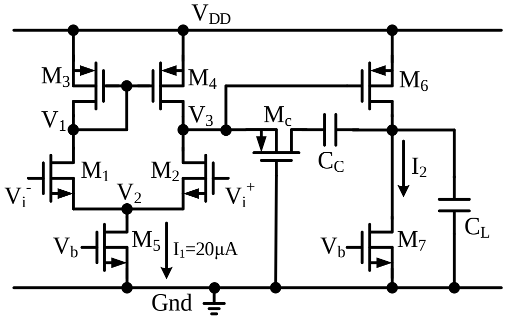


Fig. P14

Table P14
Transistor dimension
(in μm)

M_1	2/0.25	M_6	24/0.25
M_2	2/0.25	M_7	3/0.25
M_3	2/0.25	M_c	W/0.25
M_4	2/0.25		
M_5	0.5/0.25		

15. Fig. P15 shows a comparator with OPAMP and offset cancellation. In this circuit, when switch Q_3 turns off, charge injection causes two extra errors to OPAMP input V″ due to channel charge and clock feedthrough. The former can be attributed to the charge in transistor channel, which flows out from the channel region to the drain and source junctions. The latter is due to the overlap capacitance (C_{ov}) of transistor between the gate and the junctions. Assume V_{DD}=1.8V and V_{tn} =0.5V.

 (a) Derive the OPAMP input voltage change ($\Delta V''$) due to channel charge and clock feedthrough in terms of V_{DD}, GND, V_{tn}, C_{ox}, W, L, L_{ov} , C. (Hint: $C_{ov}=C_{ox}\times W\times L_{ov}$, where L_{ov} is the overlap length between gate and the junctions)

 (b) Let C=3pF, C_{ox}=5fF/(μm)^2, $(W/L)_{1\sim3}$ = 10μm/0.5μm, L_{ov}=0.2μm. Calculate the voltage change due to channel charge and clock feedthrough and total voltage change.

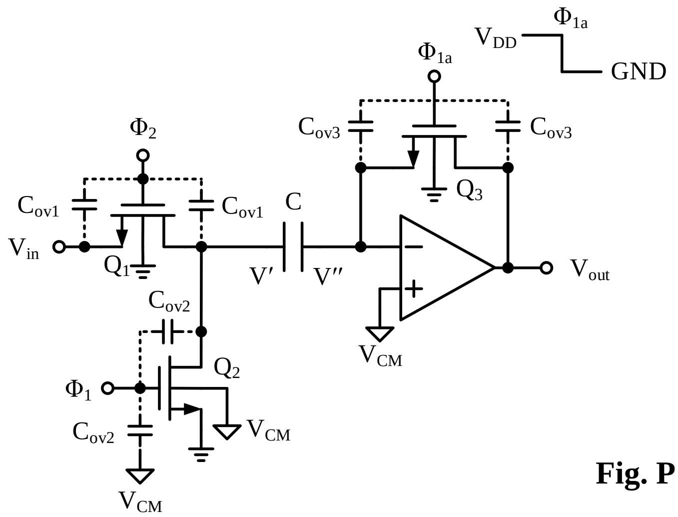


Fig. P15

16. A single-stage fully differential OPAMP and its common-mode feedback (CMFB) circuit are shown in Fig. P16, where V_{BN} and V_{CM} are DC voltage and the transistor sizes are given in Table P16. Assume $\mu_n C_{OX}$=100μA/V^2, $\mu_p C_{OX}$=40μA/V^2, $V_{tn}=-V_{tp}$=0.5V, V_{DD}=1.8V, $\lambda n=\lambda p$ =0.05/L(μm), $I_{D\_M1}=I_{D\_M2}$ =8μA and body effect is negligible. (Neglect λ and when determining DC voltage and current.)

 (a) For proper CMFB operation, briefly explain which one of A and B should be connected to v_{CTRL}?

 (b) Calculate the DC gain of the common-mode loop gain.

 (Hint: common-mode loop gain = $\frac{v_{ctrl}(s)}{v_{oc}(s)}\cdot\frac{v_o^+(s)}{v_{ctrl}(s)}$ or $\frac{v_{ctrl}(s)}{v_{oc}(s)}\cdot\frac{v_o^-(s)}{v_{ctrl}(s)}$)

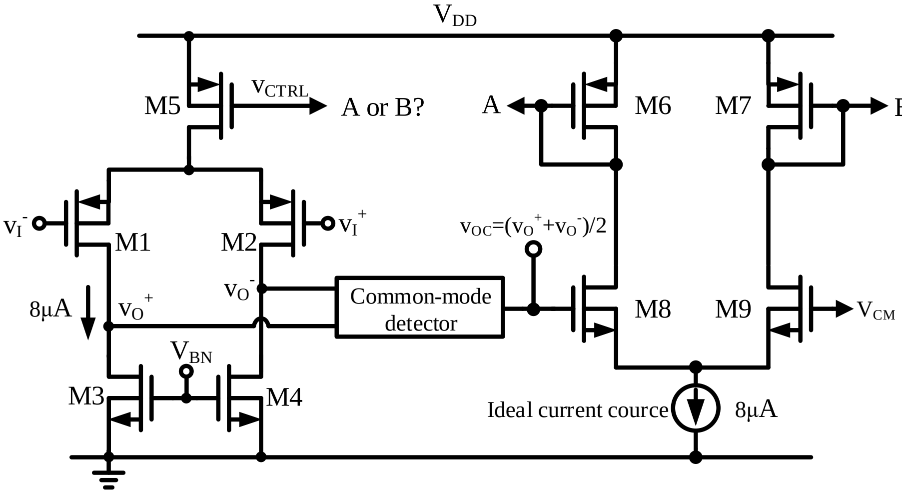


Table P16

The dimension of transistors (in μm)

M1	30/0.8	M6	15/0.8
M2	30/0.8	M7	15/0.8
M3	10/0.8	M8	6/0.8
M4	10/0.8	M9	6/0.8
M5	60/0.8		

Fig. P16

17. For the circuit shown in Fig. P17, assuming μ_nC_{OX}=100μA/V^2, μ_pC_{OX}=30μA/V^2, V_{tn}=-V_{tp}=0.6V, V_{DD}=1.8V, λ_n=λ_p =0.05/L(μm), α=2.

(a) If devices are perfectly matched, calculate V_O and I

(b) If $(W/L)_2$ becomes 3.1/0.25 and $(W/L)_4$ becomes 9.9/0.25, calculate V_O.

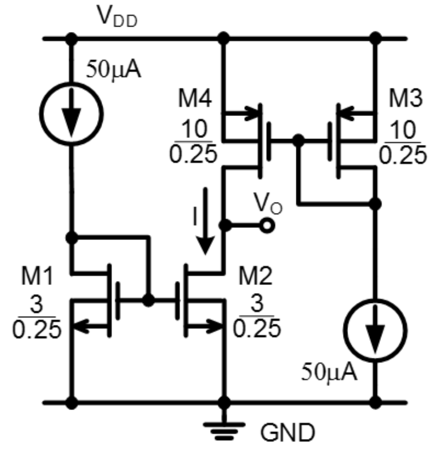


Fig. P17

18. A fully-differential folded-cascode OPAMP is shown in Fig.P18(a), where it's input bias voltage is 0.9V. Assume that V_{ov} = 0.2V for all MOSFET except M_9 & M_{10} and body effect can be neglected, and V_{DD}=1.8V, μ_nC_{OX}=200μA/V^2, μ_pC_{OX}=80μA/V^2, V_{tn}=-V_{tp}=0.4V, λ=λ_n=-λ_p =0.2/L(μm).

(a) Derive the output resistance (R_{out}) with parameter of MOSFET. (g_{mx} and r_{dsx} for M_x)

(b) Calculate the DC gain and maximum negative slew rate, all the size of MOSFET are list in Table P18. Assume that the total output capacitance is 2pF at both V_{out+} & V_{out-}.

(c) Fig.P18(b) shows a common-mode feedback circuit, derive V_{ctrl} when output common-mode voltage is stable. (Parameters you can use: V_{out+}, V_{out-}, V_{CM}, V_{B4}, C_s and C_c. Hint: charge conservation)

(d) If V_{CM}=0.9V, C_c=C_s and output common-mode voltage is stable, determine the voltage of V_{B4}.

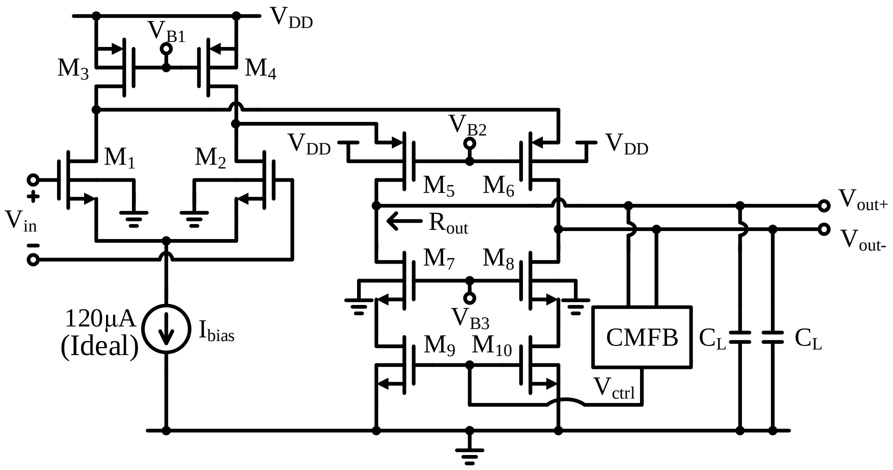
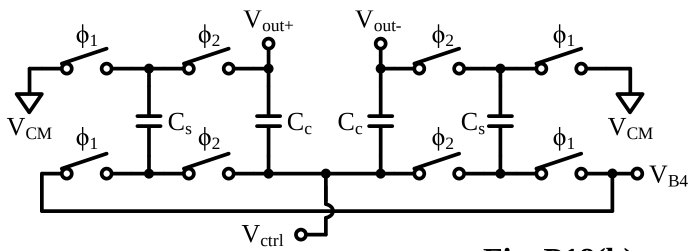


Fig. P18(a)

Table P18

Transistor dimension (in μm)

M_1	5/0.5	M_6	29/0.5
M_2	5/0.5	M_7	12/0.5
M_3	50/0.5	M_8	12/0.5
M_4	50/0.5	M_9	15/0.5
M_5	29/0.5	M_{10}	15/0.5



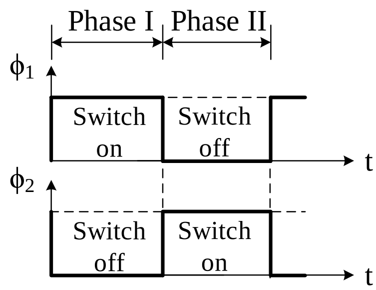


Fig. P18(b)

19. Derive the input-referred offset voltage of the circuit in Fig. P19. (Neglect channel length modulation and body effect.) Show the result in terms of $\Delta(W/L)_N$, $\Delta(W/L)_P$, $V_{t1\sim4}$, $(W/L)_N$, $(W/L)_P$, I_N, I_P, V_{OVN} , and $|V_{OVP}|$, where $V_{t1\sim4}$ are the threshold voltages of $M_{1\sim4}$.

$$\begin{cases} \Delta(W/L)_N = (W/L)_1 - (W/L)_2,\ \Delta(W/L)_P = (W/L)_3 - (W/L)_4 \\ (W/L)_N = \dfrac{(W/L)_1 + (W/L)_2}{2},\ (W/L)_P = \dfrac{(W/L)_3 + (W/L)_4}{2} \\ I_N = \dfrac{I_1 + I_2}{2},\ I_P = \dfrac{I_3 + I_4}{2} \\ V_{OVN} = \sqrt{\dfrac{2I_N}{k_n'(W/L)_N}},\ |V_{OVP}| = \sqrt{\dfrac{2|I_P|}{k_p'(W/L)_P}} \end{cases}$$

(Hint: For $\varepsilon << 1$, $\sqrt{1+\varepsilon} \approx 1+\varepsilon/2$ and $\left(\sqrt{1+\varepsilon}\right)^{-1} \approx 1-\varepsilon/2$.)

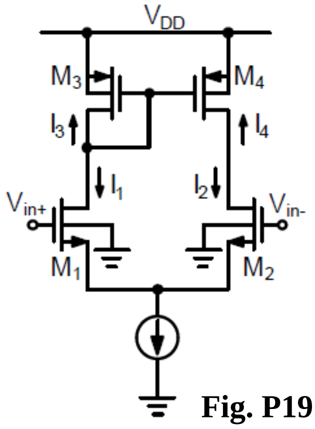


Fig. P19

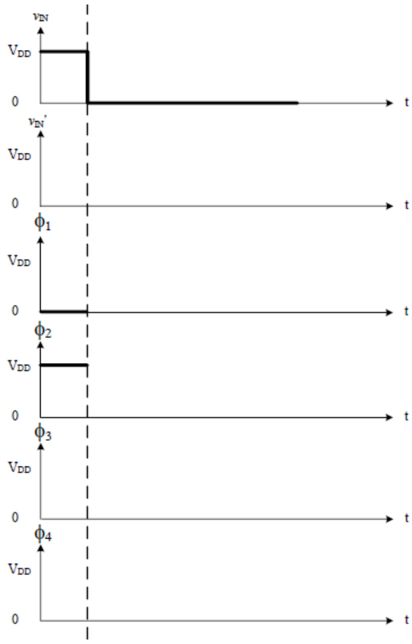
20. A non-overlapped clock circuit and its input v_{IN} are shown in Fig. P20(a) and Fig. P20(b). Assume the gate delays of NOR gate and inverter are t_{dN} and t_{dI}, respectively. The v_{IN} period $T >> t_{dN}, t_{dI}$.

(a) Please draw the waveform including all state transitions triggered by the falling edge of v_{IN} for each of v_{IN}', Φ_1, Φ_2, Φ_3 and Φ_4 and specify each edge delay relative to v_{IN} in terms of t_{dN} and t_{dI}.

(b) Fig. P20(d) shows a comparator using an OPAMP, where the switch control signal is shown in Fig. P20(c) and the OPAMP is assumed to be ideal.

(1) According to the pulses of Φ_1, Φ_2, and Φ_3, please derive the time-domain $v_{out}(nT)$ in $v_n(nT)$, $v_n(nT-T/2)$ and $v_{in}(nT)$ when the OPAMP noise(v_n) is considered.

(2) Assume the OAPMP gain A is 1000V/V (virtual short can be created at input nodes) where the noise (v_n) is white with the value of $3.2(\mu V/\sqrt{Hz})$ and the sampling frequency is 2MHz. Please find the noise power in a bandwidth of 0 to 20kHz using noise shaping function of correlated double sampling. (Hint: $z=e^{j\omega T}$)



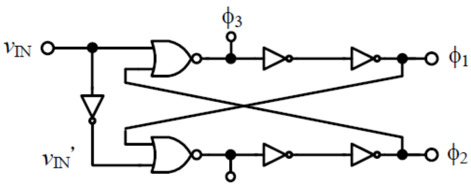


Fig. P20(a)

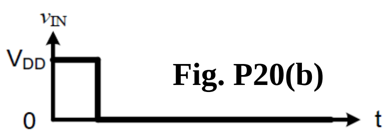


Fig. P20(b)

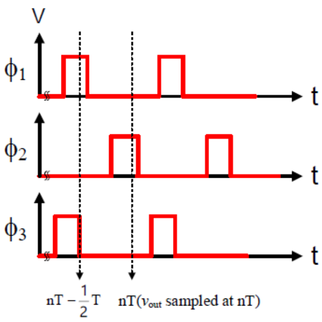


Fig. P20(c)

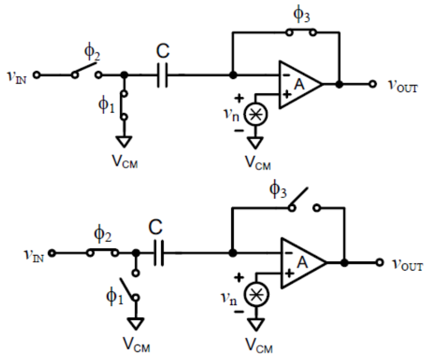


Fig. P20(d)

21. For the fully-differential folded-cascode OPAMP shown in Fig. P21(a), the transistor sizes are given in Table P21. Assume $\mu_n C_{OX}$=90μA/V^2, $\mu_p C_{OX}$=30μA/V^2, V_{tn}=$-V_{tp}$=0.7V, V_{DD}=1.8V, I_{D2}= 3×I_{D6} =90μA, C_L=4.5pF, and junction capacitances and body effect can be ignored.

(a) Design a bias circuit for generating the required bias voltages.

(b) Calculate the power consumption of the OPAMP, the unity-gain frequency, phase margin, and slew rate excluding the common-mode feedback (CMFB) circuit.

(c) Estimate the frequency of the second pole caused by parasitic capacitances at the drains of M1 and M2 using $C_{gs(overlap)-i}$, $C_{gd(overlap)-i}$ and C_{ox}. (Hint: Assume C_{gs-i} = 2/3*WLC_{ox} + W*$C_{gs(overlap)-i}$.)

(d) Briefly explain operational principle of the CMFB circuit shown in Fig. P21(b)?

(e) Why CMFB circuit is required in fully-differential amplifier circuit? (10%)

(f) From Fig. P21(c), assume $g_{m,12} = g_{m,13} = g_{m,14} = g_{m,15}$, please calculate the common-mode loop gain in term of $r_{ds,i}$ and $g_{m,i}$. (Hint: common-mode loop gain = $\frac{v_{cntrl}}{v_{cm}} \cdot \frac{v_{out}}{v_{cntrl}}$)

(g) Could nodes from V_{B2} to V_{B5} be connected with the control voltage, V_{cntrl}, of a general CMFB circuit, which doesn't specifically refer to the CMFB circuit shown in Fig. P21(b), for achieving common-mode voltage control as well? Give explanations on your answer. (10%)

(h) Assume thermal noise power of the input transistor M1 is V_n^2. Calculate the total input-referred thermal noise power excluding the CMFB and bias circuits. (15%)

Table P21

Table P5. The transistor dimensions (in um) of the OPAMP of Fig.P5(a)

M1	300/1.6	M6	60/1.6
M2	300/1.6	M7	60/1.6
M3	300/1.6	M8	20/1.6
M4	300/1.6	M9	20/1.6
M5	80/1.6	M10	20/1.6
		M11	20/1.6

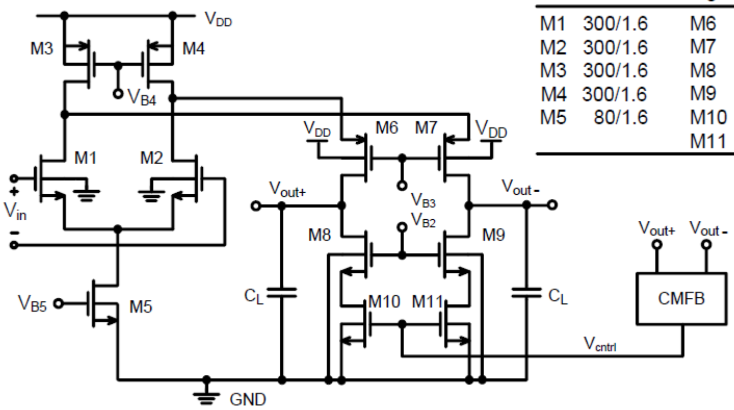


Fig. P21(a)

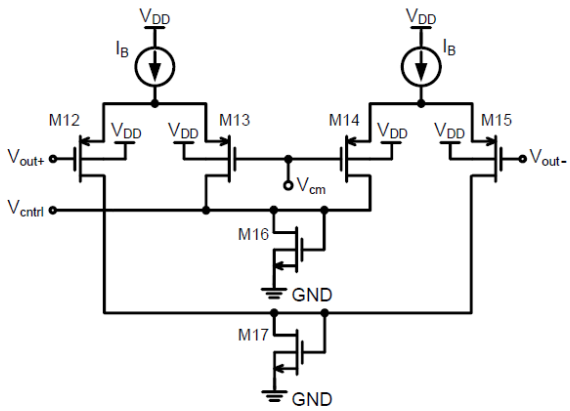


Fig. P21(b)

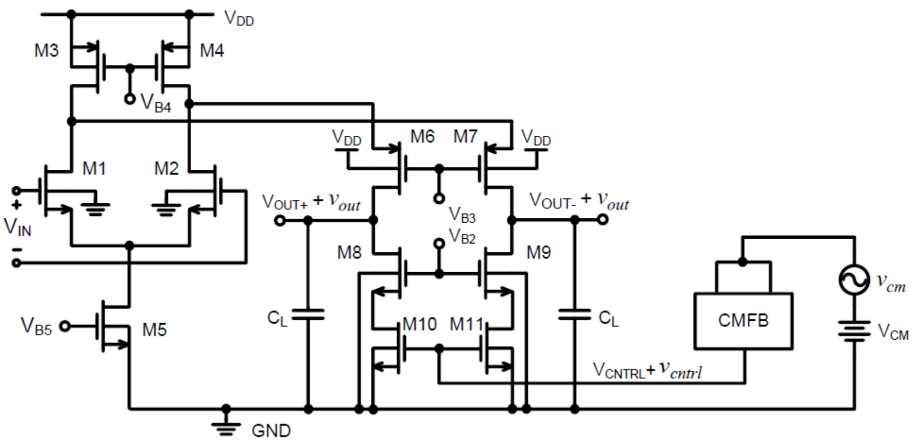


Fig. P21(c)