

HSPICE® Reference Manual: MOSFET Models

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SYNOPSYS®

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About This Manual

This manual describes available MOSFET models that you can use when simulating your circuit designs in HSPICE or HSPICE RF.

The material covered includes:

- Design model and simulation aspects of MOSFET models.
- Parameters of each model level, and associated equations.
- Parameters and equations for MOSFET diode and MOSFET capacitor models.

In addition, Synopsys has introduced LEVELs that are compatible with models developed by UC Berkeley, The University of Florida, Rensselaer Polytechnic Institute, and other institutions, developers, and foundries.

Inside This Manual

This manual contains the chapters described below. For descriptions of the other manuals in the HSPICE documentation set, see the next section, [The HSPICE Documentation Set](#).

Chapter	Description
Chapter 1, Overview of MOSFET Models	Provides an overview of MOSFET model types and general information on using and selecting MOSFET models.
Chapter 2, Common MOSFET Model Parameters	Lists and describes parameters that are common to several or all MOSFET model levels.
Chapter 3, MOSFET Models: LEVELs 1 through 40	Lists and describes standard MOSFET models (Levels 1 to 40).
Chapter 4, MOSFET Models: LEVELs 50 through 74	Lists and describes standard MOSFET models (Levels 50 to 74).

Chapter	Description
Chapter 5, MOSFET Models (BSIM): Levels 13 through 39	Lists and describes three of the earliest BSIM-type MOSFET models supported by HSPICE.
Chapter 6, MOSFET Models (BSIM): Levels 47 through 72	Lists and describes seven of the newest MOSFET models supported by HSPICE.
Chapter 7, MOSFET Capacitance Models	Discusses use of available capacitance models and CAPOP parameter values.
Chapter 8, MOSFET Diode Models	Discusses use of available MOSFET diode models.
Chapter 9, CMC MOS Varactor Model (Level 7)	Introduces and discusses Level 7 CMC MOS Varactor Model parameters.
Chapter 10, MOSFET Noise Models	Discusses use of available MOSFET noise model parameters.
Appendix A, Finding Device Libraries	Describes how to use the HSPICE automatic model selector to find the proper model for each transistor size.
Appendix B, Technology Summary for HSPICE MOSFET Models	Describes the technology used in all HSPICE MOSFET models.

The HSPICE Documentation Set

This manual is a part of the HSPICE documentation set, which includes the following manuals:

Manual	Description
HSPICE User Guide: Simulation and Analysis	Describes how to use HSPICE to simulate and analyze your circuit designs, and includes simulation applications. This is the main HSPICE user guide.
HSPICE User Guide: Signal Integrity	Describes how to use HSPICE to maintain signal integrity in your chip design.

Manual	Description
HSPICE User Guide: RF Analysis	Describes how to use special set of analysis and design capabilities added to HSPICE to support RF and high-speed circuit design.
HSPICE Reference Manual: Commands and Control Options	Provides reference information for HSPICE and HSPICE RF commands and options.
HSPICE Reference Manual: Elements and Device Models	Describes standard models you can use when simulating your circuit designs in HSPICE, including passive devices, diodes, JFET and MESFET devices, and BJT devices.
HSPICE Integration to Cadence® Virtuoso® Analog Design Environment User Guide	Describes use of the HSPICE simulator integration to the Cadence tool.
AMS Discovery Simulation Interface Guide for HSPICE	Describes use of the Simulation Interface with other EDA tools for HSPICE.
AvanWaves User Guide	Describes the AvanWaves tool, which you can use to display waveforms generated during HSPICE circuit design simulation.

Searching Across the HSPICE Documentation Set

You can access the PDF format documentation from your install directory for the current release by entering `-docs` on the terminal command line when the HSPICE tool is open.

Synopsys includes an index with your HSPICE documentation that lets you search the entire HSPICE documentation set for a particular topic or keyword. In a single operation, you can instantly generate a list of hits that are hyper-linked to the occurrences of your search term. For information on how to perform searches across multiple PDF documents, see the HSPICE release notes.

Note: To use this feature, the HSPICE documentation files, the Index directory, and the index.pdx file must reside in the same directory. (This is the default installation for Synopsys documentation.) Also, Adobe Acrobat must be invoked as a standalone application rather than as a plug-in to your web browser.

You can also invoke HSPICE and RF documentation in a browser-based help system by entering `-help` on your terminal command line when the HSPICE tool is open. This provides access to all the HSPICE manuals with the exception of the *AvanWaves User Guide* which is available in PDF format only.

Known Limitations and Resolved STARs

You can find information about known problems and limitations and resolved Synopsys Technical Action Requests (STARs) in the *HSPICE Release Notes* shipped with this release. For updates, go to SolvNet.

To access the *HSPICE Release Notes*:

1. Go to <https://solvnet.synopsys.com/ReleaseNotes>. (If prompted, enter your user name and password. If you do not have a Synopsys user name and password, follow the instructions to register with SolvNet.)
2. Select Download Center> HSPICE> version number> Release Notes.

Conventions

The following typographical conventions are used in Synopsys HSPICE documentation.

Convention	Description
Courier	Indicates command syntax.
<i>Italic</i>	Indicates a user-defined value, such as <i>object_name</i> .
Bold	Indicates user input—text you type verbatim—in syntax and examples.

Convention	Description
[]	Denotes optional parameters, such as: <code>write_file [-f filename]</code>
...	Indicates that parameters can be repeated as many times as necessary: <code>pin1 pin2 ... pinN</code>
	Indicates a choice among alternatives, such as <code>low medium high</code>
+	Indicates a continuation of a command line.
/	Indicates levels of directory structure.
Edit > Copy	Indicates a path to a menu command, such as opening the Edit menu and choosing Copy.
Control-c	Indicates a keyboard combination, such as holding down the Control key and pressing c.

Customer Support

Customer support is available through SolvNet online customer support and through contacting the Synopsys Technical Support Center.

Accessing SolvNet

SolvNet includes an electronic knowledge base of technical articles and answers to frequently asked questions about Synopsys tools. SolvNet also gives you access to a wide range of Synopsys online services, which include downloading software, viewing Documentation on the Web, and entering a call to the Support Center.

To access SolvNet:

1. Go to the SolvNet Web page at <http://solvnet.synopsys.com>.

2. If prompted, enter your user name and password. (If you do not have a Synopsys user name and password, follow the instructions to register with SolvNet.)

If you need help using SolvNet, click Help on the SolvNet menu bar.

Contacting the Synopsys Technical Support Center

If you have problems, questions, or suggestions, you can contact the Synopsys Technical Support Center in the following ways:

- Open a call to your local support center from the Web by going to <http://solvet.synopsys.com/EnterACall> (Synopsys user name and password required).
- Send an e-mail message to your local support center.
 - E-mail support_center@synopsys.com from within North America.
 - Find other local support center e-mail addresses at http://www.synopsys.com/support/support_ctr.
- Telephone your local support center.
 - Call (800) 245-8005 from within the continental United States.
 - Call (650) 584-4200 from Canada.
 - Find other local support center telephone numbers at http://www.synopsys.com/support/support_ctr.

Overview of MOSFET Models

Provides an overview of MOSFET model types and general information on using and selecting MOSFET models.

HSPICE ships numerous of examples for your use; see [Listing of Demonstration Input Files](#) for paths to demo files.

The following topics are discussed in these sections:

- [MOSFET Model Usage](#)
- [MOSFET Device Definition](#)
- [General MOSFET Model Statement](#)
- [MOSFET Models \(LEVELs\)](#)
- [MOSFET Model LEVEL Descriptions](#)
- [MOSFET Capacitors](#)
- [MOSFET Diodes](#)
- [MOSFET Control Options](#)
- [MOSFET Output Templates](#)
- [Safe Operating Area Voltage Warning](#)
- [Model Pre-Processing and Parameter Flattening](#)
- [Use of Example Syntax](#)

MOSFET Model Usage

A circuit netlist describes the basic functionality of an electronic circuit that you are designing. In HSPICE format, a netlist consists of a series of elements that

define the individual components of the overall circuit. You can use your HSPICE-format netlist to help you verify, analyze, and debug your circuit design, before you turn that design into actual electronic circuitry.

Synopsys provides a series of standard models. Each model is like a template that defines various versions of each supported element type used in an HSPICE-format netlist. Individual elements in your netlist can refer to these standard models for their basic definitions. When you use these models, you can quickly and efficiently create a netlist and simulate your circuit design. Referring to standard models this way reduces the amount of time required to:

- Create the netlist
- Simulate and debug your circuit design
- Turn your circuit design into actual circuit hardware.

Within your netlist, each element that refers to a model is known as an *instance* of that model. When your netlist refers to predefined device models, you reduce both the time required to create and simulate a netlist, and the risk of errors, compared to fully defining each element within your netlist.

One type of model that you can use as a template to define an element in your netlist is a Metal Oxide Semiconductor Field Effect Transistor (MOSFET) device. This manual describes the MOSFET models supplied for use with HSPICE.

A MOSFET device is defined by the MOSFET model and element parameters, and two submodels selected by the `CAPOP` and `ACM` model parameters.

- The `CAPOP` model parameter specifies the model for the MOSFET gate capacitances.
- The Area Calculation Method (`ACM`) parameter selects the type of diode model to use for the MOSFET bulk diodes.

Parameters in each submodel define the characteristics of the gate capacitances and bulk diodes.

MOSFET models are either p-channel or n-channel models; they are classified according to level, such as LEVEL 1 or LEVEL 50.

HSPICE and MOSFET Libraries

The [Figure 1 on page 3](#) diagrams a generic flow of creating a MOSFET library-based circuit simulation. The `.LIB` call statement is used to call portions or all

of a model file from a model library (see [.LIB](#) in the *HSPICE Reference Manual: Command and Control Options* and [Invoking MOSFET Library Files](#), below).

Support for Parameter Extraction

The accuracy and a support for industry standard models makes HSPICE a strong option as an external circuit simulator in a parameter extraction flow. HSPICE built-in models are viable alternatives for any parameter extraction tool, such as the Agilent Technologies Integrated Circuits Characterization and Analysis Program (IC-CAP).

Note: Run HSPICE in client-server mode for best performance in a parameter extraction flow (See [Using HSPICE in Client-Server Mode](#)).

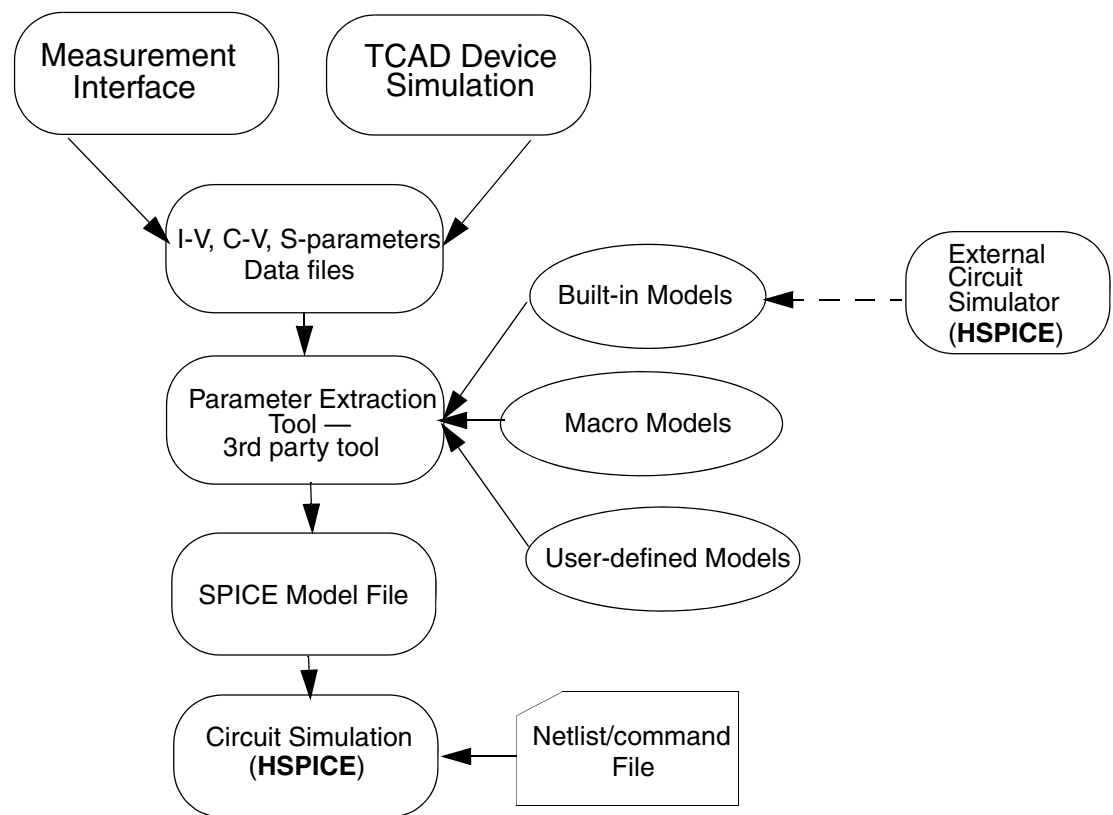


Figure 1 Model library creation and simulation flow

MOSFET Device Definition

To define a MOSFET device in your netlist, use both an element statement and a `.MODEL` statement.

The element statement defines the connectivity of the transistor and references the `.MODEL` statement. The `.MODEL` statement specifies either an n- or p-channel device, the level of the model, and several user-selectable model parameters.

Example

The following example specifies a PMOS MOSFET. PCH is the model reference name. The transistor is modeled using the LEVEL 13 BSIM model. Select the parameters from the MOSFET model parameter lists in this chapter.

```
M3 3 2 1 0 PCH <parameters>
.MODEL PCH PMOS LEVEL=13 <parameters>
```

Invoking MOSFET Library Files

You can use the `.LIB` command to create and read from libraries of commonly used commands, device models, subcircuit analyses, and statements.

Use the following syntax for library calls:

```
.LIB '<filepath> filename' entryname
```

Use the following syntax to define library files:

```
.LIB entryname1
. $ ANY VALID SET OF HSPICE STATEMENTS
.ENDL entryname1
.LIB entryname2
.
. $ ANY VALID SET OF HSPICE STATEMENTS
.ENDL entryname2
.LIB entryname3
.
. $ ANY VALID ET OF HSPICE STATEMENTS
.ENDL entryname3
```

To build libraries (library file definition), use the `.LIB` statement in a library file. For each macro in a library, use a library definition statement (`.LIB entryname`) and an `.ENDL` statement. The `.LIB` statement begins the library macro and the `.ENDL` statement ends the library macro. The text after a library file entry name must consist of HSPICE RF statements. Library calls can call

other libraries (nested library calls) if they are different files. You can nest library calls to any depth. Use nesting with the `.ALTER` statement to create a sequence of model runs. Each run can consist of similar components by using different model parameters without duplicating the entire input file.

The simulator uses the `.LIB` statement and the `.INCLUDE` statement to access the models and skew parameters. The library contains parameters that modify `.MODEL` statements.

Reliability Analysis for HSPICE MOSFET Devices

As CMOS technology scales down, reliability requirements become more challenging and important in maintaining the long-term reliability of these devices. Two of the most critical reliability issues, the hot carrier injection (HCI) and the negative bias temperature instability (NBTI) effects have been demonstrated to change the characteristics of the MOS devices.

Introduced in HSPICE Z-2007.03 release, the HSPICE reliability analysis feature allows circuit designers to be able to predict the reliability of their designs such that there are enough margins for their circuits to function correctly over the entire lifetime.

Refer to [MOSFET Model Reliability Analysis \(MOSRA\)](#) in the *HSPICE User Guide: Simulation and Analysis* for more information. In addition, a unified custom reliability modeling MOSRA API is available with an application note. Consult your Synopsys support team for full information.

HSPICE Custom Common Model Interface (CMI)

HSPICE or HSPICE RF can use a dynamically-linked shared library to integrate models with the Custom CMI with use of the `cmiflag` global option to load the dynamically linked Custom CMI library. Consult your HSPICE technical support team for access to the HSPICE CMI application note and source code.

TSMC Model Interface (TMI)

You can invoke the TMI flow using proprietary TSMC model files and compiled libraries. Jointly developed by Synopsys and TSMC the TMI technology and API is a compact model with additional instance parameters and equations for an advanced modeling approach to support TSMC's extension of the standard

BSIM4 model. Modeling API code is written in C and available in a compiled format for HSPICE and HSI-M to link to during the simulation. TMI-required settings to invoke the flow and the location of a .so file are set by TSMC. The API also performs automatic platform selection on the .so file. Both HSPICE and HSI-M provide the tool binaries and support the same .so file.

Use the existing HSPICE and HSI-M commands to run the simulation. (Contact Synopsys Technical Support for further information.) See also the *HSPICE Reference Manual: Commands and Control Options* for [.OPTION TMI FLAG](#) and [.OPTION TMIPATH](#).

General MOSFET Model Statement

You can use the `.MODEL` statement to include a MOSFET model in your HSPICE netlist. For a general description of the `.MODEL` statement, see [.MODEL](#) in the *HSPICE Reference Manual: Commands and Control Options*.

The following syntax applies to all MOSFET model specifications. All related parameter levels are described in their respective sections.

Note: The `ENCMODE` parameter can only be set in BSIM4 (Level 54) to suppress warning messages. The `TMIMODEL` and `CMIMODEL` parameters avoid potential conflicts when the TMI or custom CMI model and other standard models are used together in a shared object file.

Syntax

```
.MODEL mname [PMOS|NMOS] [ENCMODE=0|1]
+ ([LEVEL=val keyname1=val1 keyname2=val2...])
+ [VERSION=version_number]
+ [TMIMODEL=0|1] [CMIMODEL=0|1]
```

Parameter	Description
mname	Model name. Elements refer to the model by this name. See Model Name Identification Rule below.
PMOS	Identifies a p-channel MOSFET model.
NMOS	Identifies an n-channel MOSFET model.

Parameter	Description
ENCMODE	Applicable to BSIM4 (level 54 only); use to suppress warning messages originating in CMI code while inside encrypted code. Default is 0 (off). Set to off if this parameter is not present. This parameter cannot be overwritten through the instance line.
LEVEL	Use the LEVEL parameter to select from several MOSFET model types. Default=1.0.
VERSION	Specifies the version number of the model for LEVEL=13 BSIM and LEVEL=39 BSIM2 models only. See the .MODEL statement description for information about the effects of this parameter.
TMIMODEL	This parameter takes effect when .option tmiflag is on. If you set it to 1, the simulator seeks models from a shared object file to avoid potential conflicts. TMIMODEL default (1) with TMI model cards. Set it to 'zero' in non-TMI models when both TMI and non-TMI models are used in a design. When 0, the flag directs the simulator to ignore models in compiled TMI libraries.
CMIMODEL	This parameter takes effect when .option cmiflag is on. If you set it to 1, the simulator seeks models from a shared object file to avoid potential conflicts.

Example

```
.MODEL MODP PMOS LEVEL=7 VTO=-3.25 GAMMA=1.0)
.MODEL MODN NMOS LEVEL=2 VTO=1.85 TOX=735e-10)
.MODEL MODN NMOS LEVEL=39 TOX=2.0e-02 TEMP=2.5e+01
+ VERSION=95.1
```

Model Name Identification Rule

MOSFETs can support up to 7 nodes. HSPICE model name identification uses the following rule:

If the model names 'nch' and 'pch' appear at the same time, then 'nch' is regarded as a node name and 'pch' is considered the model. However, after the 4th node, HSPICE regards 'nch' as the model name instead of 'pch'.

For example:

```
m1 n1 n2 n3 n4 nch pch p1 p2 p3
```

Measuring the Value of MOSFET Model Card Parameters

The keywords `val()` and `valm()` are supported by `.MEAS/.PRINT/.PROBE` commands (only).

The syntax for instance parameters is: `val(element.parameter)`

The syntax for model parameters is: `valm(elem_name.model_param)`

The parameters currently supported for `valm()` include: `vth0`, `lmin`, `lmax`, `wmin`, `wmax`, `lref`, `wref`, `xl`, `dl`, `dell`, `xw`, `dw`, `delw`, `scalm`, `lmlt`, `wmlt`, and levels 54, 57, and 70. If the modelcard in `valm()` is not a valid model parameter for the level, an error is reported.

For example:

```
.meas delvto1 param='val(m1.l) '  
.meas tran m_vth0 param='valm(m1.vth0) '
```

For cmi models, `valm()` only supports levels 54, 57, and 70 and model card parameters: `vth0`, `lmin`, `lmax`, `wmin`, `wmax`, `lref`, `wref`, `xl`, `dl`, `dll`, `xw`, `dw`, `delw`, `scalm`, `lmlt`, `wmlt`.

MOSFET Models (LEVELs)

Before you can select the appropriate MOSFET model level to use in analysis, you need to know the electrical parameters that are critical to your application. LEVEL 1 models are most often used to simulate large digital circuits in situations where detailed analog models are not needed. LEVEL 1 models offer low simulation time and a relatively high level of accuracy for timing calculations. If you need more precision (such as for analog data acquisition circuitry), use the more detailed models, such as the LEVEL 6 IDS model or one of the BSIM models (LEVEL 13, 28, 39, 47, 49, 53, 54, 57, 59, and 60).

For precision modeling of integrated circuits, the BSIM models consider the variation of model parameters as a function of sensitivity of the geometric parameters. The BSIM models also reference a MOS charge conservation model for precision modeling of MOS capacitor effects.

- Use the SOSFET model (LEVEL 27) to model silicon-on-sapphire MOS devices. You can include photocurrent effects at this level.
- Use LEVEL 5 and LEVEL 38 for depletion MOS devices.

- LEVEL 2 models consider bulk charge effects on current.
- LEVEL 3 models require less simulation time, provides as much accuracy as LEVEL 2, and have a greater tendency to converge.
- LEVEL 6 models are compatible with models originally developed using ASPEC. Use LEVEL 6 models to model ion-implanted devices.

MOSFET Model LEVEL Descriptions

The MOSFET model is defined by the `LEVEL` parameter. MOSFET models consist of private client and public models. [Table 1 on page 9](#) describes the Model LEVELs that Synopsys has developed or adapted. You can select a specific model (See [Table 1](#)) using the `LEVEL` parameter in the `.MODEL` statement.

Note: Synopsys frequently adds new LEVELs to the MOSFET device models.

Table 1 MOSFET Model Descriptions

LEVEL	MOSFET Model Description
1	Schichman-Hodges model
2	MOS2 Grove-Frohman model (SPICE 2G)
3	MOS3 empirical model (SPICE 2G)
4 #	Grove-Frohman: LEVEL 2 model derived from SPICE 2E.3
5 #	AMI-ASPEC depletion and enhancement (Taylor-Huang)
6 #	Lattin-Jenkins-Grove (ASPEC style parasitics)
7 #	Lattin-Jenkins-Grove (SPICE style parasitics)
8 #	advanced LEVEL 2 model
9 **	AMD

Chapter 1: Overview of MOSFET Models

MOSFET Model LEVEL Descriptions

Table 1 MOSFET Model Descriptions

LEVEL	MOSFET Model Description
10 **	AMD
11	Fluke-Mosaid model
12 **	CASMOS model (GTE style)
13	BSIM model
14 **	Siemens LEVEL 4
15	user-defined model based on LEVEL 3
16	not used
17	Cypress model
18 **	Sierra 1
19 ***	Dallas Semiconductor model
20 **	GE-CRD FRANZ
21 **	STC-ITT
22 **	CASMOS (GEC style)
23	Siliconix
24 **	GE-Intersil advanced
25 **	CASMOS (Rutherford)
26 **	Sierra 2
27	SOSFET
28	BSIM derivative; Synopsys proprietary model
29 ***	not used

Table 1 MOSFET Model Descriptions

LEVEL	MOSFET Model Description
30 ***	VTI
31 ***	Motorola
32 ***	AMD
33 ***	National Semiconductor
34 *	(EPFL) not used
35 **	Siemens
36 ***	Sharp
37 ***	TI
38	IDS: Cypress depletion model
39	BSIM2
41	TI Analog
46 **	SGS-Thomson MOS LEVEL 3
47	BSIM3 Version 2.0
49	BSIM3 Version 3 (Enhanced)
50	Philips MOS9
53	BSIM3 Version 3 (Berkeley)
54	UC Berkeley BSIM4 Model
55	EPFL-EKV Model Ver 2.6, R 11
57	UC Berkeley BSIM3-SOI MOSFET Model Ver 2.0.1
58	University of Florida SOI Model Ver 4.5 (Beta-98.4)

Chapter 1: Overview of MOSFET Models

MOSFET Capacitors

Table 1 MOSFET Model Descriptions

LEVEL	MOSFET Model Description
59	UC Berkeley BSIM3-501 FD Model
61	RPI a-Si TFT Model
62	RPI Poli-Si TFT Model
63	Philips MOS11 Model
64	STARC HiSIM Model
65	SSIMOI Model
66**	HSPICE HVMOS Model
70	BSIMOI4.0 Model
71	TFT Model
#	Not supported in HSPICE RF
*	not officially released
**	equations are proprietary – documentation not provided
***	requires a license and equations are proprietary – documentation not provided

MOSFET Capacitors

CAPOP is the MOSFET capacitance model parameter. This parameter determines which capacitor models to use when modeling the MOS gate capacitance; that is, the gate-to-drain capacitance, the gate-to-source capacitance, and the gate-to-bulk capacitance. Using the CAPOP parameter, you can select a specific version of the Meyer and charge conservation model.

Some capacitor models are tied to specific DC models; they are stated as such. Others are for general use by any DC model.

Parameter	Description
CAPOP=0	SPICE original Meyer gate-capacitance model (general)

Parameter	Description
CAPOP=1	Modified Meyer gate-capacitance model (general)
CAPOP=2	Modified Meyer gate-capacitance model with parameters (general default)
CAPOP=3	Modified Meyer gate-capacitance model with parameters and Simpson integration (general)
CAPOP=4	Charge conservation capacitance model (analytic), LEVELs 2, 3, 6, 7, 13, 28, and 39 only
CAPOP=5	No capacitor model
CAPOP=6	AMI capacitor model (LEVEL 5)
CAPOP=9	Charge conservation model (LEVEL 3)
CAPOP=11	Ward-Dutton model specialized (LEVEL 2)
CAPOP=12	Ward-Dutton model specialized (LEVEL 3)
CAPOP=13	Generic BSIM Charge-Conserving Gate Capacitance model (Default for Levels 13, 28, and 39)
CAPOP=39	BSIM2 Charge-Conserving Gate Capacitance Model (LEVEL 39)

CAPOP=4 selects the recommended charge-conserving model (from among CAPOP=11, 12, or 13) for the specified DC model.

Table 2 CAPOP=4 Selections

MOS Level	Default CAPOP	CAPOP=4 selects:
2	2	11
3	2	12
13, 28, 39	13	13
others	2	11

LEVELs 49 and 53 use the Berkeley `CAPMOD` capacitance-model parameter. Proprietary models, and LEVELs 5, 17, 21, 22, 25, 27, 31, 33, 49, 53, 55, and 58, use built-in capacitance routines.

MOSFET Diodes

The `ACM` (Area Calculation Method) model parameter controls the geometry of the source and drain diffusions, and selects the modeling of the bulk-to-source and bulk-to-drain diodes of the MOSFET model. The diode model includes the diffusion resistance, capacitance, and DC currents to the substrate.

For details about ACM, see [MOSFET Diode Model Parameters on page 695](#).

MOSFET Control Options

Specific control options (set in the `.OPTION` statement) used for MOSFET models include the following. For flag options, 0 is unset (off) and 1 is set (on).

Option	Description
ASPEC	This option uses ASPEC MOSFET model defaults and set units. Default=0.
BYPASS	This option avoids recomputing nonlinear functions that do not change with iterations. Default=1.
MBYPASS	BYPASS tolerance multiplier ($BYTOL = MBYPASS \times VNTOL$). Default=1 if $DVDT=0, 1, 2$, or 3 . Default=2 if $DVDT=4$.
DEFAD	Default drain diode area. Default=0.
DEFAS	Default source diode area. Default=0.
DEFL	Default channel length. Default=1e-4m.
DEFNRD	Default number of squares for drain resistor. Default=0.
DEFNRS	Default number of squares for source resistor. Default=0.

Option	Description
DEFPD	Default drain diode perimeter. Default=0.
DEFPS	Default source diode perimeter. Default=0.
DEFW	Default channel width. Default=1e-4m.
GMIN	Pn junction parallel transient conductance. Default=1e-12mho.
GMINDC	Pn junction parallel DC conductance. Default=1e-12mho.
SCALE	Element scaling factor. Default=1.
SCALM	Model scaling factor. Default=1. Note: the SCALM parameter is only available in some models below Level 49. At Level 49 and higher, it is ignored.
WL	Reverses order in VSIZE MOS element from the default order (length-width) to width-length. Default=0.

- The AD element statement overrides the DEFAD default.
- The AS element statement overrides the DEFAS default.
- The L element statement overrides the DEFL default.
- The NRD element statement overrides the DEFNRD default.
- The NRS element statement overrides the DEFNRS default.
- The PD element statement overrides the DEFPD default.
- The PS element statement overrides the DEFPS default.
- The W element statement overrides the DEFW default.

The following sections discuss additional options:

- [Scale Units](#)
- [Bypass Option for Latent Devices](#)
- [Searching Models as Function of W, L](#)
- [Number of Fingers, WNFLAG Option](#)

Scale Units

The `SCALE` and `SCALM` options control the units.

- `SCALE` scales element statement parameters.
- `SCALM` scales model statement parameters. It also affects the MOSFET gate capacitance and diode model parameters.

Note: `SCALM` is ignored in Level 49 and higher.

In this chapter, scaling applies only to parameters that you specify as scaled. If you specify `SCALM` as a parameter in a `.MODEL` statement, it overrides the `SCALM` option. In this way, you can use models with different `SCALM` values in the same simulation. MOSFET parameter scaling follows the same rules as for other model parameters, for example:

Table 3 Model Parameter Scaling

Parameter Units	Parameter Value
meter	multiplied by <code>SCALM</code>
meter ²	multiplied by <code>SCALM</code> ²
meter ⁻¹	divided by <code>SCALM</code>
meter ⁻²	divided by <code>SCALM</code> ²

To override global model size scaling for individual MOSFET, diode, and BJT models that use the `.OPTION SCALM=<val>` statement, include `SCALM=<val>` in the `.MODEL` statement. `.OPTION SCALM=<val>` applies globally for JFETs, resistors, transmission lines, and all models other than MOSFET, diode, and BJT models. You cannot override `SCALM` in the model.

Scaling for LEVEL 25 and 33

When using the proprietary LEVEL 25 (Rutherford CASMOS) or LEVEL 33 (National) models, the `SCALE` and `SCALM` options are automatically set to 1e-6. However, if you use these models with other scalable models, you must explicitly set the `SCALE=1e-6` and `SCALM=1e-6` options.

Bypass Option for Latent Devices

Use the `BYPASS` (latency) option to decrease simulation time in large designs. To speed simulation time, this option does not recalculate currents, capacitances, and conductances, if the voltages at the terminal device nodes have not changed. The `BYPASS` option applies to MOSFETs, MESFETs, JFETs, BJTs, and diodes. Use `.OPTION BYPASS` to set `BYPASS`.

`BYPASS` might reduce simulation accuracy for tightly-coupled circuits such as op-amps, high gain ring oscillators, and others. Use `.OPTION MBYPASS` to set `MBYPASS` to a smaller value for more accurate results.

Searching Models as Function of W, L

Model parameters are often the same for MOSFETs that have width and length dimensions within specific ranges. To take advantage of this, create a MOSFET model for a specific range of width and length. These model parameters help the simulator to select the appropriate model for the specified width and length.

The automatic model selection program searches a data file for a MOSFET model where the width and length are within the range specified in the MOSFET element statement. Simulation then uses this model statement.

To search a data file for MOSFET models within a specified range of width and length:

- Provide a root extension for the model reference name (in the `.MODEL` statement).
- Use the model geometric range parameters (`LMIN`, `LMAX`, `WMIN`, and `WMAX`). These model parameters define the range of physical length and width dimensions to which the MOSFET model applies.

Example 1

If the model reference name in the element statement is `NCH`, the model selection program examines the models with the same root model reference name (`NCH`), such as `NCH.1`, `NCH.2` or `NCH.A`.

The model selection program selects the first MOSFET model statement whose geometric range parameters include the width and length specified in the associated MOSFET element statement.

Example 2

The following example shows how to call the MOSFET model selection program from a data file. The model selector program examines the .MODEL statements where the model reference names have the root extensions NCHAN.2, NCHAN.3, NCHY.20, and NCHY.50.

Note: The `scaln` parameter is ignored in Level 49 and higher.

The following example is based on demonstration netlist *selector.sp*, which is available in directory `$<installdir>/demo/hspice/mos`:

```
file: selector.sp test of mos model selector
.option post list wl scale=1u scaln=1u nomod
.op
.probe i(m1)
v1 1 0 5
v2 2 0 4
v3 3 0 1
v4 4 0 -1
m1 1 2 3 4 nchan 10 2
m2 1 2 3 4 nchan 10 3
m3 1 2 3 4 nch 10 4
m4 1 2 3 4 nchx 10 5
m5 1 2 3 4 nchy 20 5
m6 1 2 3 4 nchy 50 5
$$$$$$ for channel length selection
.model nchan.2 nmos level=2 vto=2.0 uo=800 tox=500 nsub=1e15
+ rd=10 rs=10 capop=5
+ lmin=1 lmax=2.5 wmin=2 wmax=15
.model nchan.3 nmos level=2 vto=2.2 uo=800 tox=500 nsub=1e15
+ rd=10 rs=10 capop=5
+ lmin=2.5 lmax=3.5 wmin=2 wmax=15
$$$$$$ no selection for channel length and width
.model nch nmos level=2 vto=2.3 uo=800 tox=500 nsub=1e15
+ rd=10 rs=10 capop=5
$+ lmin=3.5 lmax=4.5 wmin=2 wmax=15
.model nchx nmos level=2 vto=2.4 uo=800 tox=500 nsub=1e15
+ rd=10 rs=10 capop=5
$+ lmin=4.5 lmax=100 wmin=2 wmax=15
$$$$$$ for channel width selection
.model nchy.20 nmos level=2 vto=2.5 uo=800 tox=500 nsub=1e15
+ rd=10 rs=10 capop=5
+ lmin=4.5 lmax=100 wmin=15 wmax=30
.model nchy.50 nmos level=2 vto=2.5 uo=800 tox=500 nsub=1e15
+ rd=10 rs=10 capop=5
+ lmin=4.5 lmax=100 wmin=30 wmax=500
.end
```

Number of Fingers, WNFLAG Option

This section discusses number of fingers, categorization bin, channel currents and NF vs. M parameter.

Number and Width of Fingers

Specify the number of fingers for fingered MOSFETs in HSPICE by using the instance parameter NF. The resultant width is explained below.

Example:

```
M1 out in vdd vdd pmos w=10u l=1u nf=5
```

M1 has a total drawn width of 10um with 5 fingers, each having a finger gate width of 2um. Both HSPICE and UCB BSIM4 models employ the same, consistent definition.

Categorizing Bins in Model File for MOSFETs

By default, HSPICE uses W/nf for model selection of the MOSFET. This is the default behavior because the parameter `wnflag` has been set to 1. If `wnflag = 1`, then HSPICE uses the ratio W/nf for model selection. If `wnflag = 0`, then HSPICE uses W for model selection. If you want to use the total width for binning model selection, you need to explicitly set `wnflag` to 0.

Only BSIM4-based models can have `wnflag` as an instance parameter. But the netlist option, `.option wnflag`, is not strictly for BSIM4 model usage, it is for all levels of MOSFETs. For example,

For BSIM4 models only:

```
M1 out in vdd vdd pmos w=10u l=1u nf=5 wnflag=1
```

For all other levels:

```
.option wnflag  
M1 out in vdd vdd pmos w=10u l=1u nf=5
```

Values for IDs with Different Values of NF

While one might expect the MOSFET to have the same value of channel current even if you layout a device with a different number of fingers, you get different values of channel current (IDs).

Example:

```
M1 out in vdd vdd pmos w=10u l=1u nf=1  
M2 out in vdd vdd pmos w=10u l=1u nf=5
```

Ideally, M1 (one finger) and M2 (five fingers) should have same values of channel current since their W and L values are same, but these values are different because for the fingered MOSFETs, the channel current, effective width, and effective resistance of source and drain are functions of nf .

Hence, the channel current value also differs slightly. Refer to the BSIM4.5 manual for detailed expressions. (http://www-device.eecs.berkeley.edu/~bsim3/bsim4_get.html)

How NF Differs from Multiplication Parameter M

'M' stands for multiplicity factor. It means that 'M' identical transistors are in parallel. For example,

```
M1 out in vdd vdd pmos w=10u l=1u m=5
```

indicates that 5 identical transistors are connected in parallel with a total width of 50um.

MOSFET Output Templates

Many MOSFET models produce an output template, consisting of a set of parameters that specify the output of state variables, stored charges, capacitances, parasitic diode current, and capacitor currents. Different MOSFET model levels support different subsets of these output parameters.

For example, if your netlist contains four transistors $m0$, $m1$, $m2$, and $m3$, you can print the parameter values during the transient analysis using the following `.print` statement:

```
.print tran lx3(m1) lx4(m1) lx7(m1) lx8(m1)
```

This command prints the values of V_{ds} , I_{ds} , G_m and G_{ds} to the `*.lis` file

Wildcards are also supported, so you can also use the following which prints the V_{ds} of all transistors:

```
.print tran lx3(m*)
```

[Table 4](#) lists all parameters in the MOSFET output templates, and indicates which model levels support each parameter. See also: [Output Template for](#)

Parameters in HiSIM-HVMOS v.1.2.0 and Higher (level=73) and New Output Templates for PSP and Other Models on page 38.

Table 4 Parameters in MOSFET Output Templates

Name	Alias	Description	MOSFET Level
L	LV1	Channel length (L) (also the effective channel length for all MOSFET models except Levels 54, 57, 69 and 70)	All
W	LV2	Channel width (W) (also the effective channel width for all MOSFET models except Levels 54, 57, 69 and 70)	All
AD	LV3	Area of the drain diode (AD)	All
AS	LV4	Area of the source diode (AS)	All
ICVDS	LV5	Initial condition for the drain-source voltage (VDS)	All
ICVGS	LV6	Initial condition for the gate-source voltage (VGS)	All
ICVBS	LV7	Initial condition for the bulk-source voltage (VBS)	All except 57, 58, 59, 70, 71
ICVES	LV7	Initial condition for the substrate-source voltage (VES)	57, 58, 59, 70, 71
–	LV8	Device polarity: <ul style="list-style-type: none"> ▪ 1 = forward ▪ -1 = reverse (not used after HSPICE release 95.3). 	All
VTH	LV9	Threshold voltage (bias dependent)	All
VDSAT	LV10	Saturation voltage (VDSAT)	All
PD	LV11	Drain diode periphery (PD)	All
PS	LV12	Source diode periphery (PS)	All
RDS	LV13	Drain resistance (squares) (RDS) (equals the value of instance parameter nrd/nrs)	All

Chapter 1: Overview of MOSFET Models

MOSFET Output Templates

Table 4 Parameters in MOSFET Output Templates (Continued)

Name	Alias	Description	MOSFET Level
RSS	LV14	Source resistance (squares) (RSS) (equals the value of instance parameter nrd/nrs)	All
XQC	LV15	Charge-sharing coefficient (XQC).	All
GDEFF	LV16	Effective drain conductance (1/RDeff), rgeoMod is not 0	All
GSEFF	LV17	Effective source conductance (1/RSeff), rgeoMod is not 0	All
CDSAT	LV18	Drain-bulk saturation current, at -1 V bias.	All
CSSAT	LV19	Source-bulk saturation current, at -1 V bias.	All
VDBEFF	LV20	Effective drain bulk voltage.	All
BETAEFF	LV21	BETA effective	All
GAMMAEFF	LV22	GAMMA effective	All
DELTAL	LV23	ΔL (MOS6 amount of channel length modulation)	1, 2, 3, 6
UBEFF	LV24	UB effective	1, 2, 3, 6
VG	LV25	VG drive	1, 2, 3, 6
VFBEFF	LV26	VFB effective.	All
–	LV31	Drain current tolerance (not used in HSPICE releases after 95.3)	All
IDSTOL	LV32	Source-diode current tolerance	All
IDDTOL	LV33	Drain-diode current tolerance	All
COVLGS	LV36	Gate-source overlap and fringing capacitances	All
COVLGD	LV37	Gate-drain overlap and fringing capacitances	All
COVLGB	LV38	Gate-bulk overlap capacitances	All except 57, 59, 70, 71

Table 4 Parameters in MOSFET Output Templates (Continued)

Name	Alias	Description	MOSFET Level
COVLGE	LV38	Gate-substrate overlap capacitances	57, 59, 70, 71
VBD	L0	Bulk-drain voltage	All
VBS	LX1	Bulk-source voltage (VBS)	All except 57, 59, 70, 71
VES	LX1	Substrate-source voltage (VES)	57, 59, 70, 71
VGS	LX2	Gate-source voltage (VGS)	All
VDS	LX3	Drain-source voltage (VDS)	All
CDO	LX4	Channel current (IDS)	All
CBSO	LX5	DC source-bulk diode current (CBSO)	All
CBDO	LX6	DC drain-bulk diode current (CBDO)	All
GMO	LX7	DC MOSFET gate transconductance (GMO) ▪ Current is I_{ds} , from drain-to-source, ▪ Voltage is v_{gs}	All
GDSO	LX8	DC drain-source conductance (GDSO)	All
GMBSO	LX9	DC substrate transconductance (GMBSO)	All except 57, 58, 59, 70, 71
GMESO	LX9	DC substrate transconductance (GMBSO/ GMESO)	57, 58, 59, 70, 71
GBDO	LX10	Conductance of the drain diode (GBDO)	All
GBSO	LX11	Conductance of the source diode (GBSO)	All
QB	LX12	Total bulk (body) charge (QB)—Meyer and Charge Conservation	All
CQB	LX13	Bulk (body) charge current (CQB)—Meyer and Charge Conservation	All

Chapter 1: Overview of MOSFET Models
MOSFET Output Templates

Table 4 Parameters in MOSFET Output Templates (Continued)

Name	Alias	Description	MOSFET Level
QG	LX14	Total Gate charge (QG)—Meyer and Charge Conservation	All
CQG	LX15	Gate charge current (CQG)—Meyer and Charge Conservation	All
QD	LX16	Total Drain charge (QD)	49, 53
QD	LX16	Channel charge (QD)—Meyer and Charge Conservation	All except 49 and 53
CQD	LX17	Drain charge current (CQD)	49, 53
CQD	LX17	Channel charge current (CQD)—Meyer and Charge Conservation	All except 49 and 53
CGGBO	LX18	$CGGBO = dQg/dVg = CGS + CGD + CGB$ - Meyer and Charge Conservation	All except 54, 57, 59, 60, 70, 71
CGGBO	LX18	Intrinsic gate capacitance	54, 57, 59, 60, 66, 70, 71
CGDBO	LX19	$CGDBO = -dQg/dVd$ - Meyer and Charge Conservation; this cap is the total capacitance, including derivative of charge (dQg/dVd) and overlap capacitance.	All except 54, 57, 59, 60, 66, 70, 71
CGDBO	LX19	Intrinsic gate-to-drain capacitance	54, 57, 59, 60, 66, 70, 71
CGSBO	LX20	$CGSBO = -dQg/dVd$ - Meyer and Charge Conservation	All except 54, 57, 59, 60, 66, 70, 71
CGSBO	LX20	Intrinsic gate-to-source capacitance	54, 57, 59, 60, 66, 70, 71
CBGBO	LX21	$CBGBO = -dQb/dVg$ - Meyer and Charge Conservation	All except 54, 57, 59, 60, 66, 70, 71

Table 4 Parameters in MOSFET Output Templates (Continued)

Name	Alias	Description	MOSFET Level
CBGBO	LX21	Intrinsic bulk-to-gate capacitance	54, 66
CBGBO	LX21	Intrinsic floating body-to-gate capacitance	57, 59, 60, 70, 71
CBDBO	LX22	CBDBO = $-dQ_b/dV_d$ - Meyer and Charge Conservation	All except 54, 57, 59, 60
CBDBO	LX22	Intrinsic bulk-to-drain capacitance	54, 66
CBDBO	LX22	Intrinsic floating body-to-drain capacitance	57, 59, 60, 70, 71
CBSBO	LX23	CBSBO = $-dQ_b/dV_s$ - Meyer and Charge Conservation	All except 54, 57, 59, 60, 66, 70, 71
CBSBO	LX23	Intrinsic bulk-to-source capacitance	54, 66
CBSBO	LX23	Intrinsic floating body-to-source capacitance	57, 59, 60, 70, 71
QBD	LX24	Drain-bulk charge (QBD)	All
–	LX25	Drain-bulk charge current (CQBD), (not used in HSPICE releases after 95.3).	All
QBS	LX26	Source-bulk charge (QBS)	All
–	LX27	Source-bulk charge current (CQBS), (not used after HSPICE release 95.3).	All
CAP_BS	LX28	Extrinsic drain to substrate Capacitances—Meyer and Charge Conservation. $CAP_BS = csbox + csesw$ <ul style="list-style-type: none"> ▪ csbox is the substrate-to-source bottom capacitance ▪ csesw is the substrate-to-source sidewall capacitance 	57, 58, 70, 71

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MOSFET Output Templates

Table 4 Parameters in MOSFET Output Templates (Continued)

Name	Alias	Description	MOSFET Level
CAP_BS	LX28	Bias dependent bulk-source capacitance	All except 57, 58, 70, 71
CAP_BD	LX29	Extrinsic source to substrate Capacitances—Meyer and Charge Conservation. $CAP_BD = cdbox + cdesw$ <ul style="list-style-type: none"> ▪ $cdbox$ is the substrate-to-drain bottom capacitance ▪ $cdesw$ is the substrate-to-drain sidewall capacitance 	57, 58, 70, 71
CAP_BD	LX29	Bias dependent bulk-drain capacitance	All except 57, 58, 70, 71
CQS	LX31	Channel-charge current (CQS).	All
CDGBO	LX32	$CDGBO = -dQd/dVg$ - Meyer and Charge Conservation	All except 54, 57, 59, 60, 66, 70
CDGBO	LX32	Intrinsic drain-to-gate capacitance	54, 57, 59, 60, 66, 70
CDDBO	LX33	$CDDBO = dQd/dVd$ - Meyer and Charge Conservation	All except 54, 57, 59, 60, 66, 70, 71
CDDBO	LX33	Intrinsic drain capacitance	54, 57, 59, 60, 66, 70, 71
CDSBO	LX34	$CDSBO = -dQd/dVs$	All
		Drain-to-source capacitance - Meyer and Charge Conservation	
QE	LX35	Substrate charge (QE)—Meyer and Charge Conservation	57, 58, 59, 70, 71
CQE	LX36	Substrate charge current (CQE)—Meyer and Charge Conservation	57, 58, 59, 70, 71

Table 4 Parameters in MOSFET Output Templates (Continued)

Name	Alias	Description	MOSFET Level
CDEBO	LX37	CDEBO = $-dQ_d/dV_e$ intrinsic drain-to-substrate capacitance	57, 59, 70, 71
CBEBO	LX38	CBEBO = $-dQ_b/dV_e$ intrinsic floating body-to-substrate capacitance	59, 70, 71
igso	LX38	Gate-to-Source Current	54, 69
CEEBO	LX39	CEEBO = dQ_e/dV_e intrinsic substrate capacitance	59, 70, 71
igdo	LX39	Gate-to-Drain Current	54, 69
CEGBO	LX40	CEGBO = $-dQ_e/dV_g$ intrinsic substrate-to-gate capacitance	57, 59, 70, 71
CEDBO	LX41	CEDBO = $-dQ_e/dV_d$ intrinsic substrate-to-drain capacitance	57, 59, 70, 71
CESBO	LX42	CESBO = $-dQ_e/dV_s$ intrinsic substrate-to-source capacitance	57, 59, 70, 71
VBSI	LX43	Body-source voltage (VBS)—Meyer and Charge Conservation	57, 58, 59, 70, 71
ICH	LX44	Channel current—Meyer and Charge Conservation	57, 58, 59, 70, 71
IBJT	LX45	Parasitic BJT collector current—Meyer and Charge Conservation	57, 58, 59, 70, 71
III	LX46	Impact ionization current—Meyer and Charge Conservation	57, 58, 59, 70, 71
IGIDL	LX47	GIDL current—Meyer and Charge Conservation	57, 58, 59, 70, 71
ITUN	LX48	Tunneling current—Meyer and Charge Conservation	57, 58, 59, 70, 71
Qbacko	LX49	Back gate charge	57, 59, 70, 71

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MOSFET Output Templates

Table 4 Parameters in MOSFET Output Templates (Continued)

Name	Alias	Description	MOSFET Level
lbp	LX50	Body contact current	57, 59, 70, 71
Sft	LX51	Value of the temperature node with shmod=1	57, 59, 70, 71
VBFLOAT	LX52	Internal body node voltage, if you do not specify the terminal	57, 59, 70, 71
Rbp	LX53	Combination of rbody and rhalo	57, 59, 70, 71
IGB	LX54	Gate tunneling current	57, 59, 70, 71
QSRCO	LX55	Total Source charge (Charge Conservation: $QS = -(QG + QD + QB)$)	49, 53
QSRCO	LX55	Total Source charge (Charge Conservation: $QS = -(QG + QD + QB + QE)$)	57, 59, 70, 71
CQs	LX56	Source charge current	57, 59, 70, 71
CGEBO	LX57	$CGEBO = -dQg/dVe$ intrinsic gate-to-substrate capacitance	57, 59, 70, 71
CSSBO	LX58	$CSSBO = dQs/dVs$ intrinsic source capacitance	57, 59, 70, 71
CSGBO	LX59	$CSGBO = -dQs/dVg$ intrinsic source-to-gate capacitance	57, 59, 70, 71
CSDBO	LX60	$CSDBO = -dQs/dVd$ intrinsic source-to-drain capacitance	57, 59, 70, 71
CSEBO	LX61	$CSEBO = -dQs/dVe$ intrinsic source-to-substrate capacitance	57, 59, 70, 71
weff	LX62	Effective channel width	54, 57, 66, 69, 70
leff	LX63	Effective channel length	54, 57, 66, 69, 70
weffcv	LX64	Effective channel width for CV	54, 66, 69
leffcv	LX65	Effective channel length for CV	54, 66, 69

Table 4 Parameters in MOSFET Output Templates (Continued)

Name	Alias	Description	MOSFET Level
igbo	LX66	Gate-to-Substrate Current ($I_{gb} = I_{gbacc} + I_{gbinv}$)	54, 69
igcso	LX67	Source Partition of I_{gc}	54, 69
igcdo	LX68	Drain Partition of I_{gc}	54, 69
iimi	LX69	Impact ionization current	54, 69
igidlo	LX70	Gate-induced drain leakage current	54, 69
igdt	LX71	Gate Dielectric Tunneling Current ($I_g = I_{gs} + I_{gd} + I_{gcs} + I_{gcd} + I_{gb}$)	54, 69
igc	LX72	Gate-to-Channel Current at zero V_{ds}	54, 69
igbacc	LX73	Determined by ECB (Electron tunneling from the Conduction Band); significant in the accumulation	54
igbinv	LX74	Determined by EVB (Electron tunneling from the Valence Band); significant in the inversion	54
vfbsd	LX75	Flat-band Voltage between the Gate and S/D diffusions	54, 66
vgse	LX76	Effective Gate-to-Source Voltage	54, 66
vox	LX77	Voltage Across Oxide	54, 66
rdv	LX78	Asymmetric and Bias-Dependent Source Resistance, ($r_{dsMod} = 1$)	54, 66
rsv	LX79	Asymmetric and Bias-Dependent Drain Resistance, ($r_{dsMod} = 1$)	54, 66
cap_bsz	LX80	Zero voltage bias bulk-source capacitance	54, 66
cap_bdz	LX81	Zero voltage bias bulk-drain capacitance	54, 66
CGGBM	LX82	Total gate capacitance (including intrinsic), and all overlap and fringing components	54, 57, 59, 60, 66, 70, 69, 71

Table 4 Parameters in MOSFET Output Templates (Continued)

Name	Alias	Description	MOSFET Level
CGDBM	LX83	Total gate-to-drain capacitance (including intrinsic), and overlap and fringing components	54, 57, 59, 60, 66, 69, 70, 71
CGSBM	LX84	Total gate-to-source capacitance (including intrinsic), and overlap and fringing components	54, 57, 59, 60, 66, 69, 70, 71
CDDBM	LX85	Total drain capacitance (including intrinsic), overlap and fringing components, and junction capacitance	54, 57, 59, 60, 66, 69, 70, 71
CDSBM	LX86	Total drain-to-source capacitance	54, 57, 60, 66, 69, 70, 71
CDGBM	LX87	Total drain-to-gate capacitance (including intrinsic), and overlap and fringing components	54, 57, 59, 60, 66, 69, 70, 71
CBGBM	LX88	Total bulk-to-gate (floating body-to-gate) capacitance, including intrinsic and overlap components	54, 57, 59, 60, 66, 70, 71
CBDBM	LX89	Total bulk-to-drain capacitance (including intrinsic), and junction capacitance	54, 66
CBDBM	LX89	Total floating body-to-drain capacitance (including intrinsic), and junction capacitance.	57, 59, 60, 70, 71
CBSBM	LX90	Total bulk-to-source capacitance (including intrinsic), and junction capacitance	54, 66
CBSBM	LX90	Total floating body-to-source capacitance (including intrinsic), and junction capacitance.	57, 59, 60, 70, 71
CAPFG	LX91	Fringing capacitance	54, 66
CDEBM	LX92	Total drain-to-substrate capacitance (including intrinsic), and junction capacitance.	57, 59, 60, 70, 71
CSGBM	LX93	Total source-to-gate capacitance (including intrinsic), and overlap and fringing components.	57, 59, 60, 70, 71

Table 4 Parameters in MOSFET Output Templates (Continued)

Name	Alias	Description	MOSFET Level
CSSBM	LX94	Total source capacitance (including intrinsic), overlap and fringing components, and junction capacitance.	57, 59, 60, 70, 71
CSEBM	LX95	Total source-to-substrate capacitance (including intrinsic), and junction capacitance.	57, 59, 60, 70, 71
CEEBM	LX96	Total substrate capacitance (including intrinsic), overlap and fringing components, and junction capacitance.	57, 59, 60, 70, 71
QGI	LX97	Intrinsic Gate charge	49, 53
QSI	LX98	Intrinsic Source charge	49, 53
QDI	LX99	Intrinsic Drain charge	49, 53
QBI	LX100	Intrinsic Bulk charge (Charge Conservation: $QBI = -(QGI + QSI + QDI)$)	49, 53
CDDBI	LX101	Intrinsic drain capacitance; only includes derivative of charge	49, 53
CBDBI	LX102	Intrinsic bulk-to-drain capacitance; only includes derivative of charge	49, 53
CBSBI	LX103	Intrinsic bulk-to-source capacitance; only includes derivative of charge	49, 53
VBDI	LX109	Body-drain voltage(VBD)—Meyer and Charge Conservation	57, 58, 59, 70, 71
IGISLO	LX110	Gate-induced source leakage current	54
GRII	LX118	Intrinsic channel reflected gate conductance	54
GRGELTD	LX119	Gate electrode conductance	54
bs1	LX120	Bulk to source diffusion current	57, 59, 60
lbd1	LX121	Bulk to drain diffusion current	57, 59, 60

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Table 4 Parameters in MOSFET Output Templates (Continued)

Name	Alias	Description	MOSFET Level
lbs2	LX122	Bulk to source recombination/trap-assisted tunneling current	57, 59, 60
lbd2	LX123	Bulk to drain recombination/trap-assisted tunneling current	57, 59, 60
lbs3	LX124	Bulk to source recombination current in neutral body	57, 59, 60
lbd3	LX125	Bulk to drain recombination current in neutral body	57, 59, 60
lbs4	LX126	Bulk to source reversed bias tunneling leakage current	57, 59, 60
lbd4	LX127	Bulk to drain reversed bias tunneling leakage current	57, 59, 60
b4_sca	LX128	sca for WPE effect	54
b4_scb	LX129	scb for WPE effect	54
b4_scc	LX130	scc for WPE effect	54
b4_sc	LX131	sc for WPE effect	54
Ueff	LX132	Effective mobility at the specified analysis temperature	66
VGB	LX133	Gate to bulk voltage	All
VDG	LX134	Drain to gate voltage	All
mult	LX135	Prints value of multiplier (M) for a specified MOSFET	All
b4_sa	LX136	sa for STI or LOD-induced mechanical stress-effects	54
b4_sb	LX137	sb for STI or LOD-induced mechanical stress-effects	54

Table 4 Parameters in MOSFET Output Templates (Continued)

Name	Alias	Description	MOSFET Level
b4_sd	LX138	sd for STI or LOD-induced mechanical stress-effects	54
b4_nf	LX139	nf for STI or LOD-induced mechanical stress-effects	54
b4_saeff	LX140	saeff for STI or LOD-induced mechanical stress-effects	54
b4_sbeff	LX141	sbeff for STI or LOD-induced mechanical stress-effects	54
ivth(m*)	LX142 (m*)	New vth output, based on the monotony Id/Vgs curve obtained through .OPTION IVTH; ivthn and ivthp support NMOS and PMOS, respectively	54, 69, 70
soiq0	LX143 (bqi)	Initial floating body charge at t=0 for BQI. If it is not given, 1e35 will be printed. For tran analysis (t>0), the floating body charge will be printed. This parameter only supports BQI.	57, 60, 70

Additional MOSFET Output templates include:

- [Output Template for Parameters in HiSIM-HVMOS v.1.2.0 and Higher \(level=73\)](#)
- [New Output Templates for PSP and Other Models](#)

Output Template for Parameters in HiSIM-HVMOS v.1.2.0 and Higher (level=73)

HSPICE supports parameter output templates for HiSIM-HV beginning with version 1.2.0 model (version=1.20 level=73).

Table 5 Output Templates for HiSIM LDMOS/HVMOS Model -1.2.0

Name	Alias	Description
L	LX291	Channel Length (L)

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Table 5 Output Templates for HiSIM LDMOS/HVMOS Model -1.2.0 (Continued)

Name	Alias	Description
W	LX292	Channel Width (W)
AD	LX293	Area of the drain diode (AD)
AS	LX294	Area of the source diode (AS)
ICVDS	LX295	Initial condition for the drain-source voltage (VDS)
ICVGS	LX296	Initial condition for the gate-source voltage (VGS)
ICVBS	LX297	Initial condition for the bulk-source voltage (VBS)
PD	LX298	Drain diode periphery (PD)
PS	LX299	Source diode periphery (PS)
RSS	LX301	Source resistance (squares) (RSS)
WEFF	LX302	Effective channel width
LEFF	LX303	Effective channel length
CAPFG	LX304	Fringing capacitance
VTH	LX305	Threshold voltage (bias dependent)
VDSAT	LX306	Saturation voltage (VDSAT)
GDEFF	LX307	Effective drain conductance (1/RDeff)
GSEFF	LX308	Effective source conductance (1/RSeff)
VDBEFF	LX309	Effective drain bulk voltage.
BETAEFF	LX310	BETA effective
GAMMAEFF	LX311	GAMMA effective
VFBEFF	LX312	VFB effective
COVLGS	LX313	Gate-source overlap and fringing capacitances

Table 5 Output Templates for HiSIM LDMOS/HVMOS Model -1.2.0 (Continued)

Name	Alias	Description
COVLGD	LX314	Gate-drain overlap and fringing capacitances
COVLGB	LX315	Gate-bulk overlap capacitances
VBD	LX316	Bulk-drain voltage
VBS	LX317	Bulk-source voltage (VBS)
VGS	LX318	Gate-source voltage (VGS)
VDS	LX319	Drain-source voltage (VDS)
CDO	LX320	Channel current (IDS)
CBSO	LX321	DC source-bulk diode current (CBSO)
CBDO	LX322	DC drain-bulk diode current (CBDO)
GMO	LX323	DC MOSFET gate transconductance (GMO)
GDSO	LX324	DC drain-source conductance (GDSO)
GMBSO	LX325	DC substrate transconductance (GMBSO)
GBDO	LX326	Conductance of the drain diode (GBDO)
GBSO	LX327	Conductance of the source diode (GBSO)
QB	LX328	Total bulk (body) charge (QB)—Meyer and Charge Conservation
CQB	LX329	Bulk (body) charge current (CQB)—Meyer and Charge Conservation
QG	LX330	Total Gate charge (QG)—Meyer and Charge Conservation
CQG	LX331	Gate charge current (CQG)—Meyer and Charge Conservation
QD	LX332	Channel charge (QD)
CQD	LX333	Channel charge current (CQD)
CGGBO	LX334	Intrinsic gate capacitance

Table 5 Output Templates for HiSIM LDMOS/HVMOS Model -1.2.0 (Continued)

Name	Alias	Description
CGDBO	LX335	Intrinsic gate-to-drain capacitance
CGSBO	LX336	Intrinsic gate-to-source capacitance
CBGBO	LX337	Intrinsic bulk-to-gate capacitance
CBDBO	LX338	Intrinsic bulk-to-drain capacitance
CBSBO	LX339	CBSBO = $-dQ_b/dV_s$
QBD	LX340	Drain-bulk charge (QBD)
QBS	LX341	Source-bulk charge (QBS)
CAP_BS	LX342	Bias dependent bulk-source capacitance
CAP_BD	LX343	Bias dependent bulk-drain capacitance
CDGBO	LX344	Intrinsic drain-to-gate capacitance
CDDBO	LX345	Intrinsic drain capacitance
CDSBO	LX346	CDSBO = $-dQ_d/dV_s$, Drain-to-source capacitance
SFT	LX347	Value of the temperature node
weffcv	LX348	Effective channel width for CV
leffcv	LX349	Effective channel length for CV
igso	LX350	Gate-to-Source Current
igdo	LX351	Gate-to-Drain Current
igbo	LX352	Gate-to-Substrate Current
igcso	LX353	Source Partition of I_{gc}
igcdo	LX354	Drain Partition of I_{gc}
iimi	LX355	Impact ionization current

Table 5 Output Templates for HiSIM LDMOS/HVMOS Model -1.2.0 (Continued)

Name	Alias	Description
igidlo	LX356	Gate-induced drain leakage current
igislo	LX357	Gate-induced source leakage current
igdt	LX358	Gate Dielectric Tunneling Current ($I_g = I_{gs} + I_{gd} + I_{gcs} + I_{gcd} + I_{gb}$)
vgse	LX359	Effective Gate-to-Source Voltage
rdv	LX360	Asymmetric and Bias-Dependent Source Resistance
rsv	LX361	Asymmetric and Bias-Dependent Drain Resistance
cap_bsz	LX362	Zero voltage bias bulk-source capacitance
cap_bdz	LX363	Zero voltage bias bulk-drain capacitance
CGGBM	LX364	Total gate capacitance (including intrinsic), and overlap and fringing components
CGDBM	LX365	Total gate-to-drain capacitance (including intrinsic), and overlap and fringing components
CGSBM	LX366	Total gate-to-source capacitance (including intrinsic), and overlap and fringing components
CDDBM	LX367	Total drain capacitance (including intrinsic), overlap and fringing components, and junction capacitance
CDSBM	LX368	Total drain-to-source capacitance
CDGBM	LX369	Total drain-to-gate capacitance (including intrinsic), and overlap and fringing components
CBGBM	LX370	Total bulk-to-gate (floating body-to-gate) capacitance, including intrinsic and overlap components
CBDBM	LX371	Total bulk-to-drain capacitance (including intrinsic) and junction capacitance
CBSBM	LX372	Total bulk-to-source capacitance (including intrinsic), and junction capacitance

Table 5 Output Templates for HiSIM LDMOS/HVMOS Model -1.2.0 (Continued)

Name	Alias	Description
Ueff	LX373	Effective mobility at the specified analysis temperature
VGB	LX374	Gate to bulk voltage
VDG	LX375	Drain to gate voltage
mult	LX376	Prints value of multiplier (M) for a specified MOSFET
sa	LX377	sa for STI or LOD-induced mechanical stress-effects
sb	LX378	sb for STI or LOD-induced mechanical stress-effects
sd	LX379	sd for STI or LOD-induced mechanical stress-effects
hsmhv_nf	LX380	nf for STI or LOD-induced mechanical stress-effects

New Output Templates for PSP and Other Models

The following output templates do not require an HSPICE alias and are all in support of the PSP model. Note that LPOLY and WPOLY also support BSIM3, BSIM4, BSIM3-SOI, and BSIM4-SOI models.

The output templates of HiSIM-HVMOS (available beginning with version=1.20, level=73) are found in [Table 104 on page 327](#).

Table 6 New Output Templates for PSP MOSFETs

Name	Description	Model Level
LPOY	POLY Length	49,53,54,57, 69, 70
WPOLY	POLY Width	49,53,54,57, 69,70
VFB	Flat-band voltage at TR after geometry scaling	69
STVFB	Temperature dependence of VFB after geometry scaling	69
TOX	Gate oxide thickness after geometry scaling	69

Table 6 New Output Templates for PSP MOSFETs (Continued)

Name	Description	Model Level
EPSROX	Relative permittivity of gate dielectric)after geometry scaling	69
NEFF	Substrate doping after geometry scaling	69
VNSUB	Effective doping bias-dependence parameter)after geometry scaling	69
NSLP	Effective doping bias-dependence parameter after geometry scaling	69
DNSUB	Effective doping bias-dependence parameter after geometry scaling	69
DPHIB	Offset of ϕ_B) after geometry scaling	69
NP	NP Gate poly-silicon doping after geometry scaling	69
CT	Interface states factor after geometry scaling	69
TOXOV	Overlap oxide thickness after geometry scaling	69
NOV	Effective doping of overlap region after geometry scaling	69
CF	DIBL parameter after geometry scaling	69
CFB	Back-bias dependence of CF after geometry scaling	69
BETN	Product of channel aspect ratio and zero field mobility at TR after geometry scaling	69
STBET	Temperature dependence of BETN after geometry scaling	69
MUE	Mobility reduction coefficient at TR after geometry scaling	69
STMUE	Temperature dependence of MUE after geometry scaling	69
THEMU	Mobility reduction exponent at TR after geometry scaling	69
STTHEMU	Temperature dependence of THEMU after geometry scaling	69
CS	Coulomb scattering parameter at TR after geometry scaling	69

Chapter 1: Overview of MOSFET Models

MOSFET Output Templates

Table 6 New Output Templates for PSP MOSFETs (Continued)

Name	Description	Model Level
STCS	Temperature dependence of CS after geometry scaling	69
XCOR	Non-universality parameter after geometry scaling	69
STXCOR	Temperature dependence of XCOR after geometry scaling	69
FETA	Effective field parameter after geometry scaling	69
RS	Source/drain series resistance at TR after geometry scaling	69
STRS	Temperature dependence of RS after geometry scaling	69
RSB	Back-bias dependence of RS after geometry scaling	69
RSG	Gate-bias dependence of RS) after geometry scaling	69
THESAT	Velocity saturation parameter at TR after geometry scaling	69
STTHESAT	Temperature dependence of THESAT after geometry scaling	69
THESATB	Back-bias dependence of velocity saturation after geometry scaling	69
THESATG	Gate-bias dependence of velocity saturation) after geometry scaling	69
AX	Linear/saturation transition factor after geometry scaling	69
ALP	CLM pre-factor after geometry scaling	69
ALP1	CLM enhancement factor above threshold) after geometry scaling	69
ALP2	CLM enhancement factor below threshold) after geometry scaling	69
VPO	CLM logarithmic dependence parameter) after geometry scaling	69
A1	Impact-ionization pre-factor after geometry scaling	69
A2	Impact-ionization exponent at TR after geometry scaling	69
STA2	Temperature dependence of A2 after geometry scaling	69
A3	Saturation-voltage dependence of II after geometry scaling	69

Table 6 New Output Templates for PSP MOSFETs (Continued)

Name	Description	Model Level
A4	Back-bias dependence of I_l after geometry scaling	69
GCO	Gate tunneling energy adjustment after geometry scaling	69
IGINV	Gate channel current pre-factor after geometry scaling	69
IGOV	Gate overlap current pre-factor after geometry scaling	69
STIG	Temperature dependence of gate current after geometry scaling	69
GC2	Gate current slope factor after geometry scaling	69
GC3	Gate current curvature factor after geometry scaling	69
CHIB	Tunneling barrier height) after geometry scaling	69
AGIDL	GIDL pre-factor after geometry scaling	69
BGIDL	GIDL probability factor at TR after geometry scaling	69
STBGIDL	Temperature dependence of BGIDL after geometry scaling	69
CGIDL	Back-bias dependence of GIDL after geometry scaling	69
COX	Oxide capacitance for intrinsic channel after geometry scaling	69
CGOV	Oxide capacitance for gate-drain/source overlap after geometry scaling	69
CGBOV	Oxide capacitance for gate-bulk overlap after geometry scaling	69
CFR	Outer fringe capacitance after geometry scaling	69
NFA	First coefficient of flicker noise after geometry scaling	69
NFB	Second coefficient of flicker noise) after geometry scaling	69
NFC	Third coefficient of flicker noise after geometry scaling	69
KVTHOWE	Threshold shift parameter after geometry scaling	69
KUOWE	Mobility degradation factor after geometry scaling	69

Chapter 1: Overview of MOSFET Models

MOSFET Output Templates

Table 6 New Output Templates for PSP MOSFETs (Continued)

Name	Description	Model Level
TOXOVD	Overlap oxide thickness for drain side after geometry scaling	69
NOVD	Effective doping of overlap region for drain side after geometry scaling	69
IGOVD	Gate overlap current pre-factor for drain side after geometry scaling	69
AGIDLD	GIDL pre-factor for drain side after geometry scaling	69
BGIDLD	GIDL probability factor at TR for drain side after geometry scaling	69
STBGIDLD	Temperature dependence of BGIDL for drain side after geometry scaling	69
CGIDLD	Back-bias dependence of GIDL for drain side after geometry scaling	69
CGOVD	Oxide capacitance for gate-drain/source overlap for drain side after geometry scaling	69
CFRD	Outer fringe capacitance for drain side after geometry scaling	69
EF	Flicker noise frequency exponent after geometry scaling	69
FACNEFFAC	Pre-factor for effective substrate doping in separate charge calculation when SWDELVTAC = 1 after geometry scaling	69
GFACNUD	Body factor change due to NUD-effect after geometry scaling	69
VSBNUD	Lower VSB-value for NUD-effect after geometry scaling	69
DVSBNUD	VSB-range for NUD-effect after geometry scaling	69
DELVTAC	Offset of ϕ_B in separate charge calculation when SWDELVTAC=1 after geometry scaling	69
MOBEFF	Effective mobility at the specified analysis temperature. Note: For PSP, the effective mobility calculation considers geometry and temperature scaling, plus mechanical stress and electrical field-induced mobility change.	54, 69, 70

Safe Operating Area Voltage Warning

The following warning message is issued when terminal voltages of a device (MOSFET, BJT, Diode, Resistor, Capacitor, etc.) exceed their safe operating area (SOA):

```
**warning** (filename:line number) resulted during SOA check  
<node voltage name> (=val) of <device/element name> has exceeded  
<node voltage name>_max (=val)
```

To turn it off use `.option WARN=0`

Example Warnings

```
**Warning** (res1 : r1): Vr = 1.00      has exceeded Bv_max =      0.900  
**Warning** (cap1 : c1): Vr = 1.00      has exceeded Bv_max =      0.900  
**Warning** (dio1 : d1): Vr = 1.00      has exceeded Bv_max =      0.900  
**Warning** (bjt1: q_gp1): Vbe = 1.00 has exceeded Vbe_max =      0.800  
**Warning** (mos49 : m1): Vgs =  1.00 has exceeded Vgs_max =      0.900  
**Warning** (mos49 : m1): Vgb =  1.00 has exceeded Vgs_max =      0.900  
**Warning** (mos49 : m1): Vds =  1.00 has exceeded Vds_max =      0.900  
**Warning** (mos49 : m1): Vbd = -1.00 has exceeded Vbd_max =      0.900
```

See the following control options for details:

- [.OPTION WARN](#)
- [.OPTION MAXWARNS](#)

For details on the warnings issued, see [Safe Operating Area \(SOA\) Warnings](#) in the *HSPICE User Guide: Simulation and Analysis*.

Model Pre-Processing and Parameter Flattening

You can invoke model pre-processing and parameter flattening by using `.OPTION MODPRT=1`. For details, see [.OPTION MOD PRT](#) in the *HSPICE Reference Manual: Commands and Control Options*.

Use of Example Syntax

To copy and paste proven syntax use the demonstration files shipped with your installation of HSPICE (see [Listing of Demonstration Input Files](#)). Attempting to

Chapter 1: Overview of MOSFET Models

Use of Example Syntax

copy and paste from the book or help documentation may present unexpected results, as text used in formatting may include hidden characters, white space, etc. for visual clarity.

Common MOSFET Model Parameters

Lists and describes parameters that are common to several or all MOSFET model levels.

HSPICE ships hundreds of examples for your use; see [Listing of Demonstration Input Files](#) for paths to demo files.

Parameters that are unique to a specific MOSFET model level are described in later chapters, as part of the description of the specific model level that uses the parameter.

The common MOSFET parameters are presented in the following sections:

- [Basic MOSFET Model Parameters](#)
- [Effective Width and Length Parameters](#)
- [Threshold Voltage Parameters](#)
- [Mobility Parameters](#)

Note: MOSFET LEVELs 4 through 8 are not supported in HSPICE RF.

Basic MOSFET Model Parameters

Table 7 lists the basic MOSFET model parameters.

Table 7 Basic MOSFET Model Parameters

Name (Alias)	Units	Default	Description	Level
LEVEL		1.0	DC model selector: <ul style="list-style-type: none"> LEVEL=1 (default) is the Schichman-Hodges model. LEVEL=2 is the Grove-Frohmman model. LEVEL=3 is an empirical model. LEVEL=4 is a modified version of Level 2. LEVEL=5 is the IDS model with enhancement and depletion modes. LEVEL=6 is the Lattin-Jenkins-Grove model us using ASPEC-style parasitics. LEVEL=7 is the Lattin-Jenkins-Grove model us using SPICE-style parasitics. LEVEL=8 is an advanced model using finite differences. LEVEL=13 is the University of California (UC) Berkeley BSIM1 model. LEVEL=27 is the SOSFET model. LEVEL=28 is a Synopsys proprietary model, based on the UC Berkeley BSIM1 model, Level 13. LEVEL=38 is the Cypress Depletion model. LEVEL=39 is the UC Berkeley BSIM2 model. LEVEL=40 is the Hewlett-Packard amorphous-silicon Thin-Film Transistor (a-Si TFT) model. LEVEL=47 is the UC Berkeley BSIM3 version 2 model LEVEL=49 is a Synopsys proprietary model, based on the UC Berkeley BSIM3 version 3 model, Level 53. 	All

Table 7 Basic MOSFET Model Parameters

Name (Alias)	Units	Default	Description	Level
LEVEL (continued)			<ul style="list-style-type: none"> LEVEL=50 is the Philips MOS9 model. LEVEL=53 is the original UC Berkeley BSIM3 version 3 model, not modified as Level 49 is. LEVEL=54 is the UC Berkeley BSIM4 model LEVEL=55 is the EPFL-EKV model. LEVEL=57 is the UC Berkeley BSIM3-SOI Partially-Depleted (PD) model. LEVEL=58 is the University of Florida SOI model LEVEL=59 is the UC Berkeley BSIM3-SOI Fully-Depleted (FD) model LEVEL=60 is the UC Berkeley BSIM3-SOI Dynamically-Depleted (DD) model LEVEL=61 is the Rensselaer Polytechnic Institute (RPI) a-Si TFT model LEVEL=62 is the Rensselaer Polytechnic Institute (RPI) poly-silicon Thin-Film Transistor (Poli-Si TFT) model LEVEL=63 is the Philips MOS11 model LEVEL=64 is the Hiroshima University Semiconductor Technology Academic Research Center (STARC) IGFET (HiSIM) model. LEVEL=69 is Pennsylvania State University and Philips Research PSP100 model 	All
ACM	-	0	Selects MOS S/D parasitics. ACM=0 is SPICE style. Use ACM=2 or 3 for LDD.	39
ALPHA	V^{-1}	0	Impact ionization coefficient. This parameter includes geometry-sensitivity parameters. Choose between BSIM2 (A10>0 and HSPICE (ALPHA>0) impact ionization modeling. <i>Do not use both.</i>	39

Chapter 2: Common MOSFET Model Parameters

Basic MOSFET Model Parameters

Table 7 Basic MOSFET Model Parameters

Name (Alias)	Units	Default	Description	Level
CAPOP	-	*	MOS gate cap model selector: CAPOP=39 for BSIM2 or CAPOP=13 for BSIM1. CAPOP=4 is the same as CAPOP=13. <ul style="list-style-type: none"> ▪ If SPICE3=0, default CAPOP=13 ▪ If SPICE3=1, default CAPOP=39 	4, 13 39
CGBO	F/m	-	Gate-to-bulk overlap capacitance. If you specify WD and TOX, but you do not specify CGBO, then simulation calculates CGBO.	39
CGDO	F	1.0p	TFT gate-to-drain overlap capacitance.	40
	F/m	-	Gate-to-drain overlap capacitance. If you specify TOX, and you specify either LD or METO, but you do not specify CGDO, then simulation calculates CGDO.	39
CGSO	F	1.0p	TFT gate-to-source overlap capacitance.	40
	F/m	-	Gate-to-source overlap capacitance. If you specify TOX, but you do not specify either LD or METO, and you do not specify CGSO, then simulation calculates CGSO.	39
CHI		0.5	Temperature exponential part.	40
CJ	F/m ²	0	Source/drain bulk zero-bias junction capacitance.	39
CJSW	F/m	0	Sidewall junction capacitance.	39
CLM (GDS)		0.0	Selects a channel length modulation equation.	6, 7, 8

Table 7 Basic MOSFET Model Parameters

Name (Alias)	Units	Default	Description	Level
COX	F/m ²	3.453e-4	Oxide capacitance per unit gate area. If you do not specify COX, simulation calculates it from TOX.	1, 2, 3, 8
CSC	F/m ²	10μ	Space charge capacitance.	40
DEFF		2.0	Drain voltage effect for the TFT leakage current.	40
DERIV		1	Derivative method selector: <ul style="list-style-type: none"> DERIV=0: analytic DERIV=1: finite difference 	3, 39
DP	μm	1.0	Implant depth (depletion model only).	5, 38
ECRIT (ESAT)	V/cm	0.0	Critical electric field for the carrier velocity saturation. From Grove: <ul style="list-style-type: none"> electrons 6e4 holes 2.4e4. <p>Zero indicates an infinite value. The ECRIT equation is more stable than VMAX. Simulation estimates ECRIT as:</p> $ECRIT = 100 \cdot (VMAX / UO)$	2, 8
	V/cm	0.0	Drain-source critical field. Zero indicates an infinite value, typically 40,000 V/cm.	6, 7
ECV	V/μm	1000	Critical field.	5, 38
FEFF		0.5	Frequency effect constant.	40
FREQ	Hz	400	Frequency of the device.	40
GO	ohm ⁻¹	10e-15	Conductance of the TFT leakage current.	40

Chapter 2: Common MOSFET Model Parameters

Basic MOSFET Model Parameters

Table 7 Basic MOSFET Model Parameters

Name (Alias)	Units	Default	Description	Level
IIRAT	-	0	Impact ionization source bulk current partitioning factor. One corresponds to 100% source. Zero corresponds to 100% bulk.	39
JS	A/m ²	0	Source/drain bulk diode reverse saturation current density.	39
K2		2.0	Temperature exponential part.	40
KAPPA	V ⁻¹	0.2	Saturation field factor. The channel length modulation equation uses this parameter.	3
KCS		2.77	Implant capacitance integration constant.	38
KP (BET, BETA)	A/V ²		<p>Intrinsic transconductance parameter. If you specify U0 and TOX, but you do not specify KP, simulation computes the parameter from:</p> $KP = UO \cdot COX.$ <ul style="list-style-type: none"> Level 1 default=2.0718e-5 (NMOS), 8.632e-6 (PMOS). Level 2, 3 default=2.0e-5 	1, 2, 3
LAMBDA (LAM, LA)	V ⁻¹	0.0	Channel length modulation.	2, 8
MJ	-	0.5	Source/drain bulk junction grading coefficient.	39
MJSW		0.33	Sidewall junction grading coefficient.	39
NEFF		1.0	Total channel charge (fixed and mobile) coefficient.	2
NI	cm ⁻²	2e11	Implant doping (depletion model only).	5, 38
NU		0.0	First order temperature gradient.	40
PB	V	0.8	Source/drain bulk junction potential.	39

Table 7 Basic MOSFET Model Parameters

Name (Alias)	Units	Default	Description	Level
PBSW	V	PB	Sidewall junction potential.	39
PSI		1e-20	Temperature exponential part.	40
RD	ohm	1.0K	(External) drain resistance.	40
RS	ohm	1.0K	(External) source resistance.	40
RSH	ohm/sq	0	Source/drain sheet resistance.	39
SNVB	1/(V· cm3)	0.0	Slope of the doping concentration versus vsb (element parameter). (Multiplied by 1e6).	8
SPICE3	-	0	Selects SPICE3 model compatibility. For accurate SPICE3 BSIM2, set SPICE3=1.	39
TAU	s	10n	Relaxation time constant.	40
TCV	V/C	0	Zero-bias threshold voltage temperature coefficient. The sign of TCV adjusts automatically for NMOS and PMOS to decrease the magnitude of the threshold with rising temperature.	39
TOX	m	1e-7	Gate oxide thickness.	1, 2, 3, 8
	Å	0.0	Oxide thickness.	5, 38
	m	7.0e-8	Oxide thickness.	27
TRD	1/K	0.0	Temperature coefficient for the Rd drain diffusion and contact resistances.	54
TREF		1.5	Temperature gradient of UO.	40
TRS	1/K	0.0	Temperature coefficient for the Rs source diffusion and contact resistances.	54

Chapter 2: Common MOSFET Model Parameters

Basic MOSFET Model Parameters

Table 7 Basic MOSFET Model Parameters

Name (Alias)	Units	Default	Description	Level
TUH		1.5	Implant channel mobility temperature exponent (depletion model only).	5
UO	$\text{cm}^2/(\text{V} \cdot \text{s})$		Carrier mobility. Default for LEVEL 40 is 1.0.	1, 40
UO (UB, UBO)	$\text{cm}^2/(\text{V} \cdot \text{s})$	600 (N) 250 (P)	Low-field bulk mobility. Simulation calculates this parameter from the KP value that you specify.	2
VB0 (VB)	V	0.0	Reference voltage for the GAMMA switch. <ul style="list-style-type: none"> ▪ If $v_{sb} < VB0$, the equation uses GAMMA. ▪ If $v_{sb} > VB0$, the equation uses LGAMMA. 	6, 7
VCR	V	0	Impact ionization critical voltage. This parameter includes geometry-sensitivity parameters.	39
VMAX (VMX, VSAT)	m/s	0.0	Maximum drift velocity of the carriers. Zero indicates an infinite value. Default VMAX value for Level 40 is 1e6.	2, 3, 8, 40
VMAX (VMX)	cm/s	0.0	Maximum drift velocity of the carriers. Selects a calculation scheme to use for vdsat. Zero indicates an infinite value. Typical values: <ul style="list-style-type: none"> ▪ electrons 8.4e6 cm/s ▪ holes 4.3e6 cm/s 	6, 7
VTIME	s	10m	Voltage stress.	40
ZENH		1.0	Mode flag (enhancement). Set ZENH=0.0 for the depletion mode.	5

Effective Width and Length Parameters

Table 8 lists effective width and length parameters.

Table 8 Effective Width and Length Parameters

Name (Alias)	Units	Default	Description	Level
DEL	m	0.0	Channel length reduction on each side: $DEL_{scaled} = DEL \cdot SCALM$ MOSFET Level 13 does not support DEL.	1, 2, 3, 6, 7, 8, 38
DEL (WDEL)	μm	0.0	Channel length reduction on each side	5
DELVTO	V	0	Threshold voltage shift. This parameter is type sensitive. For example, DELVTO>0 increases the magnitude of the n-channel threshold, decreases the magnitude of the p-channel threshold, and adds to the element-line DELVTO parameter.	39
LATD (LD)	μm	$1.7 \cdot XJ$	Lateral diffusion on each side	5, 38
LDAC	m		This parameter is the same as LD, but if you specify LDAC in the .MODEL statement, it replaces LD in the Leff calculation for the AC gate capacitance.	1, 2, 3, 6, 7, 8, 13, 28, 38, 39
LMLT		1.0	Gate length shrink factor.	1, 2, 3, 5, 6, 7, 8, 13, 28, 38, 39
			Scale MOSFET drawn length	54

Chapter 2: Common MOSFET Model Parameters

Effective Width and Length Parameters

Table 8 Effective Width and Length Parameters

Name (Alias)	Units	Default	Description	Level
LD (DLAT, LATD)	m		<p>Lateral diffusion into the channel from the source and the drain diffusion.</p> <ul style="list-style-type: none"> ▪ If you do not specify LD and XJ: LD Default=0.0 ▪ If you specify XJ, but you do not specify LD, simulation calculates LD as: LD default=0.75 · XJ LD_{scaled}=LD · SCALM 	1, 2, 3, 6, 7, 8, 13, 28
LD	m	0	<p>Lateral diffusion under the gate (per side) of the S/D junction. Use this parameter to calculate L_{eff} only if DL=0:</p> <p>LD_{scaled}=LD · SCALM</p>	39
LREF	m	0.0	<p>Channel length reference:</p> <p>LREF_{scaled}=LREF · SCALM</p> <p>If the Level 13 model does not define LREF and WREF, their value is infinity.</p>	2, 3, 6, 7, 8, 13, 28
	m	0 (∞)	<p>Reference channel length to adjust the length of the BSIM model parameters. For Berkeley compatibility (LREF-> ∞), use: LREF=0. LREF_{scaled}=LREF · SCALM</p>	39
OXETCH	μm	0.0	Oxide etch	5, 38
Px	[x]· μm ²	0	Px is a Synopsys proprietary, WL-product sensitivity parameter, where x is a model parameter with length and width sensitivity.	39
WD	m	0.0	<p>Lateral diffusion into the channel from the bulk along the width:</p> <p>WD_{scaled}=WD · SCALM</p>	1, 2, 3, 6, 7, 8, 13

Chapter 2: Common MOSFET Model Parameters

Effective Width and Length Parameters

Table 8 Effective Width and Length Parameters

Name (Alias)	Units	Default	Description	Level
	m	0	Channel stop lateral diffusion under the gate (per side). Use this parameter to calculate W_{eff} only if DW=0. $WD_{scaled}=WD \cdot SCALM$	39
WDAC	m		This parameter is the same as WD, but if you specify WDAC in the .MODEL statement, it replaces WD in the W_{eff} calculation for the AC gate capacitance.	1, 2, 3, 6, 7, 8, 13, 28, 39
WMLT		1.0	Diffusion layer and width shrink factor.	1, 2, 3, 5, 6, 7, 8, 13, 28, 38, 54
	-	1.0	Diffusion and gate width shrink factor.	39
			Scale MOSFET drawn width	54
WREF	m	0.0	Channel width reference: $WREF_{scaled}=WREF \cdot SCALM$ If the Level 13 model does not define LREF and WREF, their value is infinity.	2, 3, 6, 7, 8, 13, 28
	m	0 (∞)	Reference device width to adjust the width of the BSIM model parameters. For Berkeley compatibility ($WREF \rightarrow \infty$), use $WREF=0$: $WREF_{scaled}=WREF \cdot SCALM$	39
XJ	m	0.0	Metallurgical junction depth: $XJ_{scaled}=XJ \cdot SCALM$	1, 2, 3, 6, 7, 8
	μm	1.5	Junction depth	5, 38

Chapter 2: Common MOSFET Model Parameters

Effective Width and Length Parameters

Table 8 Effective Width and Length Parameters

Name (Alias)	Units	Default	Description	Level
XL (DL, LDEL)	m	0.0	Length bias accounts for the masking and etching effects (length): $XL_{scaled} = XL \cdot SCALM$	1, 2, 3, 6, 7, 8, 13, 28, 39
XL	m	0	Difference between the physical (on the wafer) and the drawn reference channel length. Use this parameter to calculate L_{eff} only if DL=0: $XL_{scaled} = XL \cdot SCALM$ Note: SCALM is ignored for Level 54.	39, 54
XLREF	m	0.0	Difference between the physical (on the wafer) and the drawn reference channel length: $XLREF_{scaled} = XLREF \cdot SCALM$	28, 39
XW (DW, WDEL)	m	0.0	Width bias accounts for the masking and etching effects (width): $XW_{scaled} = XW \cdot SCALM$	1, 2, 3, 6, 7, 8, 13, 28
XW	m	0	Difference between the physical (on the wafer) and the drawn S/D active width. Use this parameter to calculate W_{eff} only if DW=0: $XW_{scaled} = XW \cdot SCALM$ Note: SCALM is ignored for Level 54.	39, 54
XWREF	m	0.0	Difference between the physical (on the wafer) and the drawn reference channel width: $XWREF_{scaled} = XWREF \cdot SCALM$	28, 39

Threshold Voltage Parameters

Table 9 lists threshold voltage parameters.

Table 9 Threshold Voltage Parameters

Name (Alias)	Units	Default	Description	Level
BetaGam		1.0	Body effect transition ratio.	38
CAV		0.0	Thermal voltage multiplier for the weak inversion equation.	8
DELTA		0.0	Narrow width factor for adjusting the threshold.	2, 3, 8
DNB (NSUB)	cm ⁻³	0.0	Surface doping density.	5, 38
	1/cm ³	1.0e15	Substrate doping.	6, 7
DNS (NI)	1/cm ³	0.0	Surface substrate doping.	6, 7
DVIN	V	0.0	Adjusts the empirical surface inversion voltage.	38
DVSBC	V	0.0	Adjusts the empirical body effect transition voltage.	38
E1		3.9	Dielectric constant of first film.	40
E2		0.0	Dielectric constant of second film.	40
ETA	V ⁻¹ (Level 40)	0.0	Static feedback factor for adjusting the threshold voltage (difficulty of band bending).	3, 40
		0.0	Drain-induced barrier lowering (DIBL) effect coefficient for the threshold voltage.	8
		0.0	Channel-length independent drain-induced barrier lowering.	38

Chapter 2: Common MOSFET Model Parameters

Threshold Voltage Parameters

Table 9 Threshold Voltage Parameters

Name (Alias)	Units	Default	Description	Level
FDS		0.0	Field, drain to source. Controls the threshold reduction due to the source-drain electric field.	6, 7
FSS (NFS)	$\text{cm}^{-2} \cdot \text{V}^{-1}$	0.0	Number of fast surface states	5, 38
GAMMA	$\text{V}^{1/2}$	0.5276	Body effect factor. If you do not specify GAMMA, simulation calculates it from NSUB.	1, 2, 3, 8
	$\text{V}^{1/2}$		Body effect factor. <ul style="list-style-type: none"> ▪ If you do not specify GAMMA, simulation calculates it from DNB. ▪ GAMMA is the body effect, if $v_{sb} < V_{B0}$. ▪ If $v_{sb} > V_{B0}$, simulation uses LGAMMA. GAMMA, LGAMMA, and V_{B0} perform a two-step approximation of a non-homogeneous substrate.	6, 7
LBetaGam.	μm	0.0	BetaGam dependence on the channel length.	38
LDVSBC	$\text{V} \cdot \mu\text{m}$	0.0	Adjusts the L-dependent body effect transition voltage.	38
LETA(DIBL)	μm	0.0	Channel-length dependent drain-induced barrier lowering.	38
LGAMMA	$\text{V}^{1/2}$	0.0	This parameter is the body effect factor if $v_{sb} > V_{B0}$. If you use the Poon-Yau GAMMA expression, LGAMMA is the junction depth in microns. Simulation multiplies LGAMMA by SCALM.	6, 7
LND	$\mu\text{m}/\text{V}$	0.0	ND length sensitivity.	2, 3, 6, 7, 8

Table 9 Threshold Voltage Parameters

Name (Alias)	Units	Default	Description	Level
LNO	μm	0.0	N0 length sensitivity.	2, 3, 6, 7, 8
LVT (LVTO)	$V \cdot \mu\text{m}$	0.0	VT dependence on the channel length.	38
ND	V^{-1} (1/V)	0.0	Drain subthreshold factor. Typical value=1.	2, 3, 6, 7, 8
N0		0.0	Gate subthreshold factor. Typical value=1.	2, 3, 6, 7, 8
NFS (DFS, NF, DNF)	$\text{cm}^{-2} \cdot V^{-1}$	0.0	Fast surface state density.	1, 2, 3, 6, 7, 8
NFS	cm^2	0.0	Fast surface state density.	40
NSS	cm^2	0.0	Surface state density.	40
NSUB (DNB, NB)	cm^{-3}	1e15	Bulk surface doping. If you do not specify NSUB, simulation calculates it from GAMMA.	1, 2, 3, 8
NWE	m	0.0	Narrow width effect, direct compensation of VTO: $NWE_{\text{scaled}} = NWE \cdot SCALM$	6, 7
NWM		0.0	Narrow width modifier.	5, 38
		0.0	Narrow width modulation of GAMMA.	6, 7
PHI	V	0.576	Surface inversion potential. If you do not specify PHI, HSPICE calculates it from NSUB.	1, 2, 3, 8
	V	0.8	Built-in potential.	5, 38
	V	0.0	Surface potential.	40
SCM		0.0	Short-channel drain source voltage multiplier	5, 38
		0.0	Short-channel modulation of GAMMA.	6, 7

Chapter 2: Common MOSFET Model Parameters

Threshold Voltage Parameters

Table 9 Threshold Voltage Parameters

Name (Alias)	Units	Default	Description	Level
T1	m	280n	First thin film thickness.	40
T2	m	0.0	Second thin film thickness.	40
TDVSBC	V/K	0.0	Body effect transition voltage shift due to the temperature.	38
UFDS		0.0	High field FDS.	6, 7
UPDATE		0.0	Selects different versions of the LEVEL 6 model. For the UPDATE=1 or 2 alternate saturation voltage, simulation modifies the MOB=3 mobility equation and the RS and RD series resistances so they are compatible with ASPEC. UPDATE=1 is a continuous Multi-Level GAMMA model.	6, 7
VFDS	V	0.0	Reference voltage for selecting FDS or UFDS: <ul style="list-style-type: none"> ▪ Uses FDS if $v_{ds} \leq VFDS$. ▪ Uses UFDS if $v_{ds} > VFDS$. 	6, 7
VSH	V	0.0	Threshold voltage shifter for reducing the zero-bias threshold voltage (VTO) as a function of the ratio of LD to Leff.	6, 7
VT (VTO)	V	0.0	Extrapolated threshold voltage	5, 38
VTO (VT)	V	0.0	Zero-bias threshold voltage. If you do not specify VTO, simulation calculates it.	1, 2, 3, 6, 7, 8, 40
WBetaGam	μm	0.0	BetaGam dependence on the channel width.	38
WDVSBC	V · μm	0.0	Adjusts the W-dependent body effect transition voltage.	38
WETA	μm	0.0	Channel-width dependent drain-induced barrier lowering.	38

Table 9 Threshold Voltage Parameters

Name (Alias)	Units	Default	Description	Level
WEX			Weak inversion exponent.	6, 7
WIC		0.0	Subthreshold model selector.	2, 3, 6, 7, 8
WND	$\mu\text{m}/\text{V}$	0.0	ND width sensitivity.	2, 3, 6, 7, 8
WNO	μm	0.0	N0 width sensitivity.	2, 3, 6, 7
WVT (WVTO)	$\text{V} \cdot \mu\text{m}$	0.0	VT dependence on the channel width.	38

Mobility Parameters

Use curve fitting to determine the mobility parameters. Generally, you should set $UTRA$ between 0.0 and 0.5. Nonzero values for $UTRA$ can result in negative resistance regions at the onset of saturation.

[Table 10](#) lists mobility parameters.

Table 10 Mobility Parameters

Name (Alias)	Units	Default	Description	Level
BEX	-	-1.5	Surface channel mobility temperature exponent.	38, 39
BFRC	$\text{\AA} \cdot \text{s}/(\text{cm}^2 \cdot \text{V})$	0.0	Field reduction coefficient variation due to the substrate bias.	38
FACTOR			Mobility degradation factor. Default=1.0.	6, 7
FEX	-	0	Temperature exponent for velocity saturation.	39

Chapter 2: Common MOSFET Model Parameters

Mobility Parameters

Table 10 Mobility Parameters

Name (Alias)	Units	Default	Description	Level
FRC	$\text{\AA} \cdot \text{s}/\text{cm}^2$	0.0	Field reduction coefficient.	5, 38
FRCEX (F1EX)		0.0	Temperature coefficient for FRC .	38
FSB	$\text{V}^{1/2} \cdot \text{s}/\text{cm}^2$	0.0	Lateral mobility coefficient.	5, 38
HEX(TUH)		-1.5	Implant channel mobility temperature exponent.	38
KBeta1		1.0	Effective implant-channel mobility modifier.	38
KI0(KIO)		1.0	Residue current coefficient.	38
LBFR	$10^{-4} \text{\AA} \cdot \text{s}/(\text{cm} \cdot \text{V})$	0.0	BFRC sensitivity to the effective channel length.	38
LFRC	$10^{-4} \text{\AA} \cdot \text{s}/\text{cm}$	0.0	FRC sensitivity to the effective channel length.	38
LKBeta1	μm	0.0	Length-dependent implant-channel mobility modifier.	38
LKI0(LKIO)	μm	0.0	Length-dependent residue current coefficient.	38
LUO(LUB)	$\text{cm}^2 \cdot \mu\text{m}/(\text{V} \cdot \text{s})$	0.0	UO sensitivity to the effective channel length.	38
LVFR	$10^{-4} \text{\AA} \cdot \text{s}/(\text{cm} \cdot \text{V})$	0.0	VFRC sensitivity to the effective channel length.	38
LFSB	$10^{-4} \text{V}^{1/2} \cdot \text{s}/\text{cm}$	0.0	FSB sensitivity to the effective channel length.	38

Table 10 Mobility Parameters

Name (Alias)	Units	Default	Description	Level
MOB		0.0	<p>Selects a mobility equation. You can set this parameter to MOB=0 or MOB=7. MOB=7 changes both the model and the channel length calculation.</p> <p>The MOB=7 flag invokes the channel length modulation and mobility equations in MOSFET LEVEL 3.</p> <p>In MOSFET Level 8, you can set MOB to 2, 3, 6, or 7.</p>	2, 6, 7, 8
THETA	V^{-1}	0.0	Mobility modulation. MOSFET models use THETA only if MOB=7. A typical value is THETA=5e-2.	2, 40
	V^{-1}	0.0	Mobility degradation factor.	3
UB (UO)	$cm^2/(V \cdot s)$	0.0	Low field bulk mobility	5
UCRIT	V/cm	1.0e4	Critical field for mobility degradation, UCRIT. This parameter is the limit where UO surface mobility begins to decrease as specified in the empirical relation.	2
	V/cm	1e4	<ul style="list-style-type: none"> MOB=6, UEXP>0 Critical field for the mobility degradation. UEXP operates as a switch. MOB=6, UEXP≤0 Critical field for mobility degradation. Typical value is 0.01 V^{-1}. 	8

Chapter 2: Common MOSFET Model Parameters

Mobility Parameters

Table 10 Mobility Parameters

Name (Alias)	Units	Default	Description	Level
UEFF			Effective mobility at the specified analysis temperature.	6, 7
UEXP (F2)		0.0	Critical field exponent in the empirical formula that characterizes the surface mobility degradation. Typical value in MOSFET Level 8 with MOB=6 is 0.01 V ⁻¹ .	2, 8
UH	cm ² /(V·s)	900 (N) 300 (P)*	Implant - channel mobility * (For depletion model only)	5, 38
UHSAT	μm/V	0.0	Implant-channel mobility saturation factor.	38
UO (UB, UBO)	cm ² /(V·s)	600 (N) 250 (P)	Low-field bulk mobility. Simulation calculates this parameter from the KP value that you specify.	2, 3, 6, 7, 8, 38
UTRA		0.0	Transverse field coefficient (mobility). Traditional SPICE does not use UTRA. HSPICE can use UTRA, but simulation issues a warning, because UTRA can hinder convergence.	2, 8
VFRC	Å·s/(cm ² ·V)	0.0	Field reduction coefficient variation due to the drain bias.	38
VST	cm/s	0.0	Saturation velocity.	5, 38
WBFRC	10 ⁻⁴ Å·s/(cm·V)	0.0	BFRC sensitivity to the effective channel width.	38
WFRC	10 ⁻⁴ Å·s/cm	0.0	FRC sensitivity to the effective channel width.	38

Table 10 Mobility Parameters

Name (Alias)	Units	Default	Description	Level
WFSB	$10^{-4} V^{1/2} \cdot s/cm$	0.0	FSB sensitivity to the effective channel width.	38
WKBeta1	μm	0.0	Width-dependent implant-channel mobility modifier.	38
WKIO (WKIO)	μm	0.0	Width-dependent residue current coefficient.	38
WUO(WUB)	$cm^2 \cdot \mu m/(V \cdot s)$	0.0	UO sensitivity to the effective channel width.	38
WVFRC	$10^{-4} \text{\AA} \cdot s/(cm \cdot V)$	0.0	VFRC sensitivity to the effective channel width.	38

Chapter 2: Common MOSFET Model Parameters

Mobility Parameters

MOSFET Models: LEVELs 1 through 40

Lists and describes standard MOSFET models (Levels 1 to 40).

Note: MOSFET Levels 4 through 8 are not supported in HSPICE RF.

HSPICE ships hundreds of examples for your use; see [Listing of Demonstration Input Files](#) for paths to demo files.

This chapter describes the following standard MOSFET models (Levels 1 to 40):

- [LEVEL 1 IDS: Schichman-Hodges Model](#)
- [LEVEL 2 IDS: Grove-Frohmman Model](#)
- [LEVEL 3 IDS: Empirical Model](#)
- [LEVEL 4 IDS: MOS Model](#)
- [LEVEL 5 IDS Model](#)
- [LEVEL 6/LEVEL 7 IDS: MOSFET Model](#)
- [LEVEL 7 IDS Model](#)
- [LEVEL 8 IDS Model](#)
- [LEVEL 27 SOSFET Model](#)
- [LEVEL 38 IDS: Cypress Depletion Model](#)
- [LEVEL 40 HP a-Si TFT Model](#)

For information about standard MOSFET Models Levels 50 to 64, see [Chapter 4, MOSFET Models: LEVELs 50 through 74](#). For information on BSIM MOSFET models (based on models developed by the University of California at Berkeley), see [Chapter 6, MOSFET Models \(BSIM\): Levels 47 through 72](#) and [Chapter 6, MOSFET Models \(BSIM\): Levels 47 through 72](#).

LEVEL 1 IDS: Schichman-Hodges Model

Use the LEVEL 1 MOSFET model if accuracy is less important to you than simulation turn-around time. For digital switching circuits, especially if you need only a “qualitative” simulation of the timing and the function, LEVEL 1 run-time can be about half that of a simulation using the LEVEL 2 model. The agreement in timing is approximately 10%. The LEVEL 1 model, however, results in severe inaccuracies in DC transfer functions of any TTL-compatible input buffers in the circuit.

The LAMBDA channel-length modulation parameter is equivalent to the inverse of the Early voltage for the bipolar transistor. LAMBDA measures the output conductance in the saturation. If you specify this parameter, the MOSFET has a finite but constant output conductance in saturation. If you do not specify LAMBDA, the LEVEL 1 model assumes zero output conductance.

LEVEL 1 Model Parameters

MOSFET Level 1 uses only the generic MOSFET model parameters described in [Chapter 2, Common MOSFET Model Parameters](#).

LEVEL 1 Model Equations

The LEVEL 1 model equations follow.

IDS Equations

The LEVEL 1 model does not include the carrier mobility degradation, the carrier saturation effect, or the weak inversion model. This model determines the DC current:

Cutoff Region,

$$v_{gs} \leq v_{th}, I_{ds} = 0.0$$

Linear Region, $v_{ds} < v_{gs} - v_{th}$

$$I_{ds} = KP \cdot \frac{W_{eff}}{L_{eff}} \cdot (1 + LAMBDA \cdot v_{ds}) \cdot \left(v_{gs} - v_{th} - \frac{v_{ds}}{2} \right) \cdot v_{ds}$$

Saturation Region, $v_{ds} \geq v_{gs} - v_{th}$

$$I_{ds} = \frac{KP}{2} \cdot \frac{W_{eff}}{L_{eff}} \cdot (1 + LAMBDA \cdot v_{ds}) \cdot (v_{gs} - v_{th})^2$$

Effective Channel Length and Width

The Level 1 model calculates the effective channel length and width from the drawn length and width:

$$L_{eff} = L_{scaled} \cdot LMLT + XL_{scaled} - 2 \cdot (LD_{scaled} + DEL_{scaled})$$

$$W_{eff} = M \cdot (W_{scaled} \cdot WMLT + XW_{scaled} - 2 \cdot WD_{scaled})$$

Threshold Voltage, v_{th}

$$v_{sb} \geq 0, v_{th} = v_{bi} + GAMMA \cdot (PHI + v_{sb})^{1/2}$$

$$v_{sb} < 0, v_{th} = v_{bi} + GAMMA \cdot \left(PHI^{1/2} + 0.5 \frac{v_{sb}}{PHI^{1/2}} \right)$$

The preceding equations define the built-in voltage (v_{bi}) as:

$$v_{bi} = v_{fb} + PHI, v_{bi} = VTO - GAMMA \cdot PHI^{1/2}$$

See [Common Threshold Voltage Equations on page 742](#) for calculation of VTO , $GAMMA$, and PHI if you do not specify them.

Saturation Voltage, v_{sat}

The saturation voltage for the LEVEL 1 model is due to the channel pinch-off at the drain side. The following equation computes this voltage:

$$v_{sat} = v_{gs} - v_{th}$$

The LEVEL 1 model does not include the carrier velocity saturation effect.

LEVEL 2 IDS: Grove-Frohmman Model

This section describes the parameters and equations for the LEVEL 2 IDS: Grove-Frohmman model.

LEVEL 2 Model Parameters

MOSFET Level 2 uses only the generic MOSFET model parameters described in [Chapter 2, Common MOSFET Model Parameters](#).

LEVEL 2 Model Equations

The LEVEL 2 model equations follow.

IDS Equations

This section describes how the LEVEL 2 MOSFET model calculates the drain current of n-channel and p-channel MOSFETs.

Cutoff Region, $v_{gs} < v_{th}$, $I_{ds} = 0$ (see subthreshold current)

On Region, $v_{gs} > v_{th}$

$$I_{ds} = \beta \cdot \left\{ \left(v_{gs} - v_{bi} - \frac{\eta \cdot v_{de}}{2} \right) \cdot v_{de} - \frac{2}{3} \left[(\phi_i + v_{de} + v_{sb})^{3/2} - (\phi_i + v_{sb})^{3/2} \right] \right\}$$

The following equations calculate values used in the preceding equation:

$$v_{de} = \min(v_{ds}, v_{dsat})$$

$$\eta = 1 + DELTA \cdot \frac{\pi \cdot \epsilon_{si}}{4 \cdot COX \cdot W_{eff}}, \quad \beta = KP \cdot \frac{W_{eff}}{L_{eff}}$$

Effective Channel Length and Width

The Level 2 model calculates effective channel length and width from the drawn length and width:

$$L_{eff} = L_{scaled} \cdot LMLT + XL_{scaled} - 2 \cdot (LD_{scaled} + DEL_{scaled})$$

$$W_{eff} = M \cdot (W_{scaled} \cdot WMLT + XW_{scaled} - 2 \cdot (WD_{scaled}))$$

$$LREF_{eff} = LREF_{scaled} \cdot LMLT + XL_{scaled} - 2 \cdot (LD_{scaled} + DEL_{scaled})$$

$$WREF_{eff} = M \cdot (WREF_{scaled} \cdot WMLT + XW_{scaled} - 2 \cdot (WD_{scaled}))$$

Threshold Voltage, v_{th}

The V_{TO} model parameter is an extrapolated zero-bias threshold voltage for a large device. The following equation calculates the effective threshold voltage, including the device size effects and the terminal voltages:

$$v_{th} = v_{bi} + \gamma \cdot (PHI + v_{sb})^{1/2}$$

The following equation calculates the v_{bi} value used in the preceding equation:

$$v_{bi} = V_{TO} - GAMMA \cdot (PHI)^{1/2} + (\eta - 1) \cdot (PHI + v_{sb})$$

To include the narrow width effect, use v_{bi} and η . To include the narrow width effect, specify the Δ model parameter. The effective γ specifies the short-channel effect. To include short-channel effects, the XJ model parameter must be greater than zero.

$$\gamma = GAMMA \cdot \left\{ 1 - \frac{XJ_{scaled}}{2 \cdot L_{eff}} \left[\left(1 + \frac{2 \cdot W_s}{XJ_{scaled}} \right)^{1/2} + \left(1 + \frac{2 \cdot W_d}{XJ_{scaled}} \right)^{1/2} - 2 \right] \right\}$$

The following equations determine the W_s and W_d depletion widths:

$$W_s = \left[\frac{2 \cdot E_{si}}{q \cdot NSUB} \cdot (PHI + v_{sb}) \right]^{1/2}$$

$$W_d = \left[\frac{2 \cdot E_{si}}{q \cdot NSUB} \cdot (PHI + v_{ds} + v_{sb}) \right]^{1/2}$$

If you do not specify parameters such as V_{TO} , $GAMMA$, and PHI , simulation calculates them automatically. The Level 2 model uses these parameters to calculate the threshold voltage. (See [Common Threshold Voltage Equations on page 742](#)).

Saturation Voltage, v_{dsat}

If you do not specify the V_{MAX} model parameter, the program computes the saturation voltage due to channel pinch off at the drain side. If you specify the corrections for small-size effects, then:

$$v_{sat} = \frac{v_{gs} - v_{bi}}{\eta} + \frac{1}{2} \left(\frac{\gamma}{\eta} \right)^2 \cdot \left\{ 1 - \left[1 + 4 \cdot \left(\frac{\eta}{\gamma} \right)^2 \cdot \left(\frac{v_{gs} - v_{bi}}{\eta} + PHI + v_{sb} \right) \right]^{1/2} \right\}$$

$$v_{dsat} = v_{sat}$$

If you specify **ECRIT**, the program modifies v_{sat} to include carrier velocity saturation effect:

$$v_{dsat} = v_{sat} + v_c - (v_{sat}^2 + v_c^2)^{1/2}$$

The following equation calculates the v_c value used in the preceding equation:

$$v_c = ECRIT \cdot L_{eff}$$

Note: If you specify **VMAX**, simulation calculates a different v_{dsat} value. Refer to the Vladimirescu document[\[1\]](#) for details.

Mobility Reduction, u_{eff}

The mobility of carriers in the channel decreases as speeds of the carriers approach their scattering limited velocity. The mobility degradation for the LEVEL 2 MOS model uses two different equations, depending on the **MOB** mobility equation selector value.

If **MOB**=0, (default):

$$u_{eff} = UO \cdot \left[\frac{UCRIT \cdot E_{si}}{COX \cdot (v_{gs} - v_{th} - UTRA \cdot v_{ds})} \right]^{UEXP}$$

Because u_{eff} is less than UO , the program uses the above equation if the bracket term is less than one; otherwise the program uses $u_{eff}=UO$.

If **MOB**=7, **THETA** $\neq 0$

$$u_{eff} = \frac{UO}{1 + THETA \cdot (v_{gs} - v_{th})}$$

$v_{gs} < v_{th}$, $u_{eff}=UO$

If **MOB**=7, **THETA**=0

$$u_{eff} = UO \cdot \left[\frac{UCRIT \cdot E_{si}}{COX \cdot (v_{gs} - v_{th})} \right]^{UEXP}$$

If **MOB**=7, **VMAX**>0

$$u_{eff} = \frac{u_{eff}}{1 + u_{eff} \cdot \frac{v_{de}}{V_{MAX} \cdot L_{eff}}}$$

Channel Length Modulation

To include the channel length modulation effect, the LEVEL 2 MOS model modifies the I_{ds} current:

$$I_{ds} = \frac{I_{ds}}{1 - \lambda \cdot v_{ds}}$$

If you do not specify the LAMBDA model parameter, the model calculates the λ value.

LAMBDA>0:

$\lambda = \text{LAMBDA}$

$V_{MAX} > 0$, $NSUB > 0$, and $LAMBDA < 0$

$$\lambda = \frac{X_d}{NEFF^{1/2} \cdot L_{eff} \cdot v_{ds}} \cdot \left\{ \left[\left(\frac{V_{MAX} \cdot X_d}{2 \cdot NEFF^{1/2} \cdot u_{eff}} \right)^2 + v_{ds} - v_{dsat} \right]^{1/2} - \frac{V_{MAX} \cdot X_d}{2 \cdot NEFF^{1/2} \cdot u_{eff}} \right\}$$

$V_{MAX} = 0$, $NSUB > 0$, and $LAMBDA < 0$

If $MOB = 0$

$$\lambda = \frac{X_d}{L_{eff} \cdot v_{ds}} \cdot \left\{ \frac{v_{ds} - v_{dsat}}{4} + \left[1 + \left(\frac{v_{ds} - v_{dsat}}{4} \right)^2 \right]^{1/2} \right\}^{1/2}$$

This equation does not include the effect of the field between the gate and the drain. It also tends to overestimate the output conductance in the saturation region.

If $MOB = 7$

$$\lambda = \frac{X_d}{L_{eff} \cdot v_{ds}} \cdot \left\{ \left[\frac{v_{ds} - v_{dsat}}{4} + \left(1 + \left(\frac{v_{ds} - v_{dsat}}{4} \right)^2 \right)^{1/2} \right]^{1/2} - 1 \right\}$$

This equation does not include the effect of the field between the gate and the pinch-off point. It also tends to overestimate the output conductance in the saturation region.

The following equation calculates the X_d value used in the two preceding equations:

$$X_d = \left(\frac{2 \cdot E_{si}}{q \cdot NSUB} \right)^{1/2}$$

Modifying I_{ds} by a factor of $(1 - \lambda \cdot v_{ds})$ is equivalent to replacing L_{eff} with:

$$L_e = L_{eff} - \lambda \cdot v_{ds} \cdot L_{eff}$$

To prevent the channel length (L_e) from becoming negative, the value of L_e is limited.

If $L_e < xwb$, then simulation replaces L_e with:

$$\frac{xwb}{1 + \frac{xwb - L_e}{xwb}}$$

The following equation calculates the xwb value used in the preceding equation:

$$xwb = X_d \cdot PB^{1/2}$$

Subthreshold Current, I_{ds}

The fast surface states model parameter (NFS) characterizes this region of operation. For $NFS > 0$ the model determines the modified threshold voltage (v_{on}):

$$v_{on} = v_{th} + fast$$

The following equation calculates the fast value used in the preceding equation:

$$fast = v_t \cdot \left[\eta + (PHI + v_{sb})^{1/2} \cdot \frac{\partial \gamma}{\partial v_{sb}} + \frac{\gamma}{2 \cdot (PHI + v_{sb})^{1/2}} + \frac{q \cdot NFS}{COX} \right]$$

In the preceding equations, v_t is the thermal voltage.

The following equation calculates the I_{ds} current for $v_{gs} < v_{on}$:

$$I_{ds} = I_{ds}(v_{on}, v_{de}, v_{sb}) \cdot e^{\frac{v_{gs} - v_{on}}{fast}}$$

$v_{gs} > v_{on}$:

$$I_{ds} = I_{ds}(v_{gs}, v_{de}, v_{sb})$$

The following equation calculates the v_{de} value used in the preceding equation:

$$v_{de} = \min(v_{ds}, v_{dsat})$$

Note: The modified threshold voltage (v_{on}), due to NFS specification, is also used in strong inversion instead of v_{th} , mostly in the mobility equations.

If $WIC=3$, the Level 2 model calculates the subthreshold current differently. In this case the I_{ds} current is:

$$I_{ds} = I_{ds}(v_{gs}, v_{de}, v_{sb}) + isub(N0_{eff}, ND_{eff}, v_{gs}, v_{ds})$$

$N0_{eff}$ and ND_{eff} are functions of effective device width and length.

LEVEL 3 IDS: Empirical Model

This section describes the LEVEL 3 IDS: Empirical model parameters and equations.

LEVEL 3 Model Parameters

MOSFET Level 3 uses only the generic MOSFET model parameters described in [Chapter 2, Common MOSFET Model Parameters](#).

LEVEL 3 Model Equations

The LEVEL 3 model equations follow.

IDS Equations

The following equations describe how the LEVEL 3 MOSFET model calculates the I_{ds} drain current.

Cutoff Region, $v_{gs} < v_{th}$

$$I_{ds} = 0 \text{ (See subthreshold current)}$$

On Region, $v_{gs} > v_{th}$

$$I_{ds} = \beta \cdot \left(V_{gs} - V_{th} - \frac{1+fb}{2} \cdot v_{de} \right) \cdot v_{de}$$

The following equations calculate values used in the preceding equation:

$$\beta = K \cdot P \cdot \frac{W_{eff}}{L_{eff}} = u_{eff} \cdot COX \cdot \frac{W_{eff}}{L_{eff}}$$

Since

$$K \cdot P = u_{eff} \cdot COX$$

$$v_{de} = \min(v_{ds}, v_{dsat})$$

$$fb = f_n + \frac{GAMMA \cdot f_s}{4 \cdot (PHI + v_{sb})^{1/2}}$$

Note: In the above equation, the factor 4 should be 2, but because SPICE uses a factor of 4, this model uses a factor of 4 as well.

The f_n parameter specifies the narrow width effect:

$$f_n = \frac{DELTA}{W_{eff}} \cdot \frac{1}{4} \cdot \frac{2\pi \cdot E_{si}}{COX}$$

The f_s term expresses the effect of the short channel:

$$f_s = 1 - \frac{XJ_{scaled}}{L_{eff}} \Rightarrow \left[\frac{LD_{scaled} + W_c}{XJ_{scaled}} \cdot \left[1 - \left(\frac{W_p}{XJ_{scaled} + W_p} \right)^2 \right]^{1/2} - \frac{LD_{scaled}}{XJ_{scaled}} \right]$$

$$W_p = X_d \cdot (PHI + v_{sb})^{1/2}$$

$$X_d = \left(\frac{2 \cdot E_{si}}{q \cdot NSUB} \right)^{1/2}$$

$$W_c = XJ_{scaled} \cdot \left[0.0631353 + 0.8013292 \cdot \left(\frac{W_p}{XJ_{scaled}} \right) - 0.01110777 \cdot \left(\frac{W_p}{XJ_{scaled}} \right)^2 \right]$$

Effective Channel Length and Width

The following equations determine the effective channel length and width in the LEVEL 3 model:

$$L_{eff} = L_{scaled} \cdot LMLT + XL_{scaled} - 2 \Rightarrow LD_{scaled} + DEL_{scaled}$$

$$W_{eff} = M \cdot (W_{scaled} \cdot WMLT + XW_{scaled} - 2 \Rightarrow WD_{scaled})$$

$$LREF_{eff} = LREF_{scaled} \cdot LMLT + XL_{scaled} - 2 \Rightarrow LD_{scaled} + DEL_{scaled}$$

$$WREF_{eff} = M \cdot (WREF_{scaled} \cdot WMLT + XW_{scaled} - 2 \Rightarrow WD_{scaled})$$

Threshold Voltage, v_{th}

The following equation calculates the effective threshold voltage, including the device size and terminal voltage effects:

$$v_{th} = v_{bi} - \frac{8.14e-22 \Rightarrow ETA}{COX \cdot L_{eff}^3} \Rightarrow ds + GAMMA \cdot f_s \cdot (PHI + v_{sb})^{1/2} + f_n \cdot (PHI + v_{sb})$$

The following equation calculates the v_{bi} value used in the preceding equation:

$$v_{bi} = v_{fb} + PHI \text{ or } v_{bi} = VTO - GAMMA \Rightarrow PHI^{1/2}$$

VTO is the extrapolated zero-bias threshold voltage of a large device. If you do not specify VTO, GAMMA, or PHI, simulation computes these values (see [Common Threshold Voltage Equations on page 742](#)).

Saturation Voltage, v_{dsat}

The LEVEL 3 model determines the saturation voltage due to the channel pinch-off at the drain side. The v_{MAX} parameter specifies the reduction of the saturation voltage due to the carrier velocity saturation effect.

$$v_{sat} = \frac{v_{gs} - v_{th}}{1 + f_b}$$

$$v_{dsat} = v_{sat} + v_c - (v_{sat}^2 + v_c^2)^{1/2}$$

The following equation calculates the v_c value used in the preceding equations:

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$$v_c = \frac{V_{MAX} \cdot L_{eff}}{u_s}$$

The next section defines the u_s surface mobility parameter. If you do not specify the V_{MAX} model parameter, then:

$$v_{dsat} = v_{sat}$$

Effective Mobility, u_{eff}

The Level 3 model defines the carrier mobility reduction due to the normal field as the effective surface mobility (u_s).

$$v_{gs} > v_{th}$$

$$u_s = \frac{UO}{1 + THETA \cdot (v_{gs} - v_{th})}$$

The V_{MAX} model parameter model determines the degradation of mobility due to the lateral field and the carrier velocity saturation.

$$V_{MAX} > 0:$$

$$u_{eff} = \frac{u_s}{1 + \frac{v_{de}}{v_c}}$$

$$\text{Otherwise, } u_{eff} = u_s$$

Channel Length Modulation

For $v_{ds} > v_{dsat}$, this model computes the channel length modulation factor. The V_{MAX} model parameter value determines the amount of channel length reduction (ΔL).

$$V_{MAX} = 0$$

$$\Delta L = X_d \cdot [KAPPA \cdot (v_{ds} - v_{dsat})]^{1/2}$$

$$V_{MAX} > 0$$

$$\Delta L = -\frac{E_p \cdot X_d^2}{2} + \left[\left(\frac{E_p \cdot X_d^2}{2} \right)^2 + KAPPA \cdot X_d^2 \cdot (v_{ds} - v_{dsat}) \right]^{1/2}$$

In the preceding equation, E_p is the lateral electric field at the pinch off point. The following equation approximates its value:

$$E_p = \frac{v_c \cdot (v_c + v_{dsat})}{L_{eff} \cdot v_{dsat}}$$

The LEVEL 3 model modifies the I_{ds} current to include the channel length modulation effect:

$$I_{ds} = \frac{I_{ds}}{1 - \frac{\Delta L}{L_{eff}}}$$

To prevent a zero denominator, the ΔL value is limited:

$$\text{If } \Delta L > \frac{L_{eff}}{2} \text{ then } \Delta L = L_{eff} - \frac{\left(\frac{L_{eff}}{2}\right)^2}{\Delta L}$$

Subthreshold Current, I_{ds}

This region of operation is characterized by the model parameter for the fast surface state (NFS). The following equation determines the modified threshold voltage (v_{on}):

$$NFS > 0 \quad v_{on} = v_{th} + fast$$

The following equation calculates the fast value used in the preceding equation:

$$fast = v_{tm} \cdot \left[1 + \frac{q \cdot NFS}{COX} + \frac{GAMMA \cdot f_s \cdot (PHI + v_{sb})^{1/2} + f_n \cdot (PHI + v_{sb})}{2 \cdot (PHI + v_{sb})} \right]$$

The following equations calculate the I_{ds} current:

$v_{gs} < v_{on}$:

$$I_{ds} = I_{ds}(v_{on}, v_{de}, v_{sb}) \cdot e^{\frac{v_{gs} - v_{on}}{fast}}$$

$v_{gs} > v_{on}$:

$$I_{ds} = I_{ds}(v_{gs}, v_{de}, v_{sb})$$

Note: Strong inversion does not use the modified threshold voltage.

If $WIC=3$, the model calculates subthreshold current differently. In this case, the I_{ds} current is:

$$I_{ds} = I_{ds}(v_{gs}, v_{de}, v_{sb}) + isub(NO_{eff}, ND_{eff}, v_{gs}, v_{ds})$$

The $isub$ subthreshold current for $LEVEL=3$ is the same as for $LEVEL=13$ (see [ids Subthreshold Current on page 356](#)).

NO_{eff} and ND_{eff} are functions of the effective device width and length.

Compatibility Notes

Synopsys Device Model versus SPICE3

Differences between the Synopsys Level 3 MOSFET device model and Berkeley $SPICE3$ can arise in the following situations:

Small XJ

$LEVEL 3$ and $SPICE3$ differ for small XJ values, typically >0.05 microns. Do not use such small values for XJ ; they are physically unreasonable. XJ calculates the short-channel reduction of the $GAMMA$ effect:

$$GAMMA \rightarrow f_s \cdot GAMMA$$

f_s is normally less than or equal to 1. For very small values of XJ , f_s can be greater than one. The Synopsys Level 3 model imposes the limit $f_s \leq 1.0$, but $SPICE3$ allows $f_s > 1.0$.

ETA

In this model, 8.14 is the constant in the ETA equation, which varies the v_{ds} threshold. Berkeley $SPICE3$ uses 8.15.

Solution: To convert a $SPICE3$ model to the Synopsys Level 3 MOSFET device model, multiply ETA by 815/814.

NSUB Missing

If you do not specify $NSUB$ in $SPICE3$, the $KAPPA$ equation becomes inactive. The Synopsys Level 3 MOSFET model generates a default $NSUB$ from $GAMMA$, and the $KAPPA$ equation is active.

Solution: If you do not specify $NSUB$ in the $SPICE3$ model, set $KAPPA=0$ in the Synopsys Level 3 MOSFET model.

LD Missing

If you do not specify LD, simulation uses the default (0.75XJ). The SPICE3 default for LD is zero.

Solution: If you do not specify LD in the SPICE3 model, set LD=0 in the Level 3 MOSFET model.

Name	Symbol	Value
Boltzmann constant	k	=1.3806226e-23J· K ⁻¹
Electron charge	e	=1.6021918e-19C
Permittivity of silicon dioxide	ϵ_{ox}	=3.45314379969e-11F/m
Permittivity of silicon	ϵ_{si}	=1.035943139907e-10F/m

Temperature Compensation

This example is based on demonstration netlist tempdep.sp, which is available in directory \$<installdir>/demo/hspice/mos:

```
$ test of temp dependence for LEVEL=3 Tlevc=0 Tlev=1
.option ingold=2 numdgt=6 post=2
.temp 25 100
vd d 0 5
vg g 0 2
m1 d g 0 0 nch w=10u L=1u
.op
.print id=lx4(m1) vdsat=lv10(m1)
.model nch nmos LEVEL=3 tlev=1 tlevc=0 acm=3
+ uo=600 tox=172.6572
+ vto=0.8 gamma=0.8 phi=0.64
+ kappa=0 xj=0
+ nsub=1e16 rsh=0
+ tcv=1.5e-3 bex=-1.5
.end
```

This simple model, with XJ=0 and KAPPA=0, has a saturation current:

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$$I_{ds} = \frac{\beta \cdot 0.5 \cdot (v_{gs} - v_{tm})^2}{1 + fb}$$

$$\beta = COX \cdot \left(\frac{W}{L}\right) \cdot UO(t), fb = \frac{GAMMA}{(4 \cdot \sqrt{\phi(t)})}$$

Using the model parameters in the input file, and the preceding equations, produces these results:

$$\beta = (1.2e-3) \cdot \left(\frac{t}{t_{ref}}\right)^{BEX}$$

$$v_{tm} = 0.8 - TCV \cdot (t - t_{ref})$$

$$\phi(t) = 0.64 \cdot \left(\frac{t}{t_{ref}}\right)^{-v_{therm}} \cdot \left(egarg + 3 \cdot \log\left(\frac{t}{t_{ref}}\right)\right)$$

At room temperature:

$$\beta = (1.2e-3)$$

$$v_{tm} = 0.8$$

$$\phi(t) = 0.64$$

$$I_{ds} = (1.2e-3) \cdot 0.5 \cdot \frac{(2-0.8)^2}{1 + \frac{0.2}{\sqrt{0.64}}} = 6.912e-4$$

At T=100:

$$\beta = 1.2e-3 \cdot (1.251551)^{-1.5} = 0.570545e-4$$

$$v_{tm} = 0.8 - (1.5e-3) \cdot 75 = 0.6875$$

$$egarg = 9.399920, v_{therm} = 3.215466e-2$$

$$\phi(t) = 0.64 \cdot 1.251551 - 0.3238962 = 0.4770964$$

$$I_{ds} = \beta \cdot 0.5 \cdot \frac{(2 - vt)^2}{1 + \frac{0.2}{\sqrt{\phi(t)}}} = 5.724507e-4$$

Simulation results:

T=25, id=6.91200e-04
T=100, id=5.72451e-04

These results agree with the hand calculations.

LEVEL 4 IDS: MOS Model

The LEVEL 4 MOS model is the same as the LEVEL 2 model with the following exceptions:

- No narrow width effects: $h=1$
- No short-channel effects: $\gamma=\text{GAMMA}$
- For lateral diffusion, $LD_{\text{scaled}}=LD \cdot XJ \cdot \text{SCALM}$. If you specify XJ , the LD default=0.75. If you do not specify XJ , the default is 0.
- TPG , the model parameter for type of gate materials, defaults to zero (AL gate). The default is 1 for other levels. If you do not specify VTO , this parameter computes VTO (see [Common Threshold Voltage Equations on page 742](#)).
- Starting in 2001.4.2, MOSFET LEVEL 4 and LEVEL 9 support both M and AREA scaling.

LEVEL 5 IDS Model

This section describes the LEVEL 5 IDS model parameters and equations.

Note: This model uses micrometer units rather than the typical meter units. Units and defaults are often unique in LEVEL 5. Level 5 does not use the SCALM option.

LEVEL 5 Model Parameters

MOSFET Level 5 uses the generic MOSFET model parameters described in [Chapter 2, Common MOSFET Model Parameters](#). It also uses the parameters described in this section, which apply only to MOSFET LEVEL 5.

Table 11 Capacitance Parameters for MOSFET Level 5

Name (Alias)	Units	Default	Description
AFC		1.0	Area factor for MOSFET capacitance
CAPOP		6	Gate capacitance selector
METO	μm	0.0	Metal overlap on gate

Use the ZENH flag mode parameter to select one of two modes: enhancement or depletion.

Parameter	Description
ZENH=1	This enhancement model (default mode) is a portion of the Synopsys MOS5 device model, and is identical to AMI SPICE MOS LEVEL 4.
ZENH=0	This depletion model is revised in the Synopsys MOS5 device model (from previous depletion mode) and is identical to AMI SPICE MOS LEVEL 5.

The Synopsys enhancement and depletion modes are basically identical to the AMI models. However, the Synopsys enhancement and depletion modes let you choose either SPICE or ASPEC temperature compensation.

- TLEV=1 (default) uses ASPEC-style temperature compensation.
- TLEV=0 uses SPICE-style temperature compensation.

CAPOP=6 represents AMI Gate Capacitance in the Synopsys device models. CAPOP=6 is the default setting for LEVEL 5 only. LEVEL 5 models can also use CAPOP=1, 2, and 3.

The `ACM` parameter defaults to 0 in LEVEL 5, invoking SPICE-style parasitics. You can also set `ACM` to 1 (`ASPEC`) or to 2 (Synopsys device models). All MOSFET models follow this convention.

You can use `.OPTION SCALE` with the LEVEL 5 model; however, you cannot use the `SCALM` option, due to the difference in units.

You *must* specify the following parameters for MOS LEVEL 5: `VTO` (`VT`), `TOX`, `UO` (`UB`), `FRC`, and `NSUB` (`DNB`).

IDS Equations

Cutoff Region, $v_{gs} < v_{th}$

$I_{ds} = 0$ (See [Subthreshold Current, \$I_{ds}\$ on page 88](#))

On Region, $v_{gs} > v_{th}$

$$I_{ds} = \beta \cdot \left\{ \left(v_{gs} - v_{bi} - \frac{v_{de}}{2} \right) \cdot v_{de} - \frac{2}{3} \left[(\Phi_f + v_{de} + v_{sb})^{3/2} - (\Phi_f + v_{sb})^{3/2} \right] \right\}$$

The following equations calculate values used in the preceding equation:

$$v_{de} = \min(v_{ds}, v_{dsat})$$

$$\beta = UB_{eff} \cdot cox \cdot \frac{W_{eff}}{L_{eff}}$$

$$\Phi_f = 2 \cdot v_{tm} \cdot \ln\left(\frac{DNB}{ni}\right)$$

The following equation calculates the gate oxide capacitances per unit area:

$$cox = \frac{E_{ox}}{TOX \cdot 1E-10} \text{ F/m}$$

Effective Channel Length and Width

The following equations determine the effective channel length and width in the LEVEL 5 model:

$$W_{eff} = W_{scaled} \cdot WMLT + OXETCH$$

$$L_{eff} = L_{scaled} \cdot LMLT - 2 \Rightarrow (LATD + DEL)$$

Threshold Voltage, v_{th}

The V_{TO} model parameter is an extrapolated zero-bias threshold voltage for a large device. The following equation calculates the effective threshold voltage, including the device size effects and the terminal voltages:

$$v_{th} = v_{bi} + \gamma \cdot (\Phi_f + v_{sb})^{1/2}$$

The following equations calculate values used in the preceding equation:

$$v_{bi} = v_{fb} + \Phi_f = V_{TO} - \gamma_0 \Rightarrow \Phi_f^{1/2}$$

$$\gamma_0 = \frac{(2 \cdot E_{si} \cdot q \cdot DNB)^{1/2}}{cox}$$

Note: You must specify DNB and V_{TO} parameters for the LEVEL 5 model. The Synopsys device model uses DNB to compute γ_0 , and ignores the $GAMMA$ model parameter.

The following equation computes the γ effective body effect, including the device size effects:

$$\gamma = \gamma_0 \cdot (1 - scf) \cdot (1 + ncf)$$

If $SCM < 0$, then $scf=0$.

$$\text{Otherwise, } scf = \frac{XJ}{L_{eff}} \cdot \left\{ \left[1 + \frac{2x_d}{XJ} \cdot (SCM \cdot v_{ds} + v_{sb} + \Phi_f)^{1/2} \right]^{1/2} - 1 \right\}$$

If $NWM < 0$, then $ncf=0$.

$$\text{Otherwise, } ncf = \frac{NWM \cdot X_d \cdot (\Phi_f)^{1/2}}{W_{eff}}$$

The following equation calculates the x_d value used in the preceding equations:

$$X_d = \left(\frac{2 \cdot E_{si}}{q \cdot DNB} \right)^{1/2}$$

Saturation Voltage, v_{dsat}

The following equation computes the saturation voltage due to the channel pinch-off at the drain side:

$$v_{sat} = v_{gs} - v_{bi} + \frac{\gamma^2}{2} \cdot \left\{ 1 - \left[1 + \frac{4}{\gamma^2} \cdot (v_{gs} - v_{bi} + \Phi_f + v_{sb}) \right]^{1/2} \right\}$$

$$v_{dsat} = v_{sat}$$

If ECV does not equal 1000, the program modifies v_{sat} to include the carrier velocity saturation effect:

$$v_{dsat} = v_{sat} + v_c - (v_{sat}^2 + v_c^2)^{1/2}$$

, where

$$v_c = ECV \cdot L_{eff}$$

Mobility Reduction, UB_{eff}

The following equation computes the mobility degradation effect in the LEVEL 5 MOSFET model:

$$UB_{eff} = \frac{1}{\frac{1}{UB} + \frac{FRC \cdot (v_{gs} - v_{th})}{TOX} + \frac{vde}{VST \cdot L_e} + FSB \cdot v_{sb}^{1/2}}$$

The following equations calculate the L_e value used in the preceding equation:

$$L_e = L_{eff} \text{ linear region}$$

$$L_e = L_{eff} - \Delta L \text{ saturation region}$$

The next section describes the ΔL channel length modulation effect.

Channel Length Modulation

The LEVEL 5 model modifies the I_{ds} current to include the channel length modulation effect:

$$I_{ds} = \frac{I_{ds}}{1 - \frac{\Delta L}{L_{eff}}}$$

The following equation calculates the ΔL value used in the preceding equation:

$$\Delta L = 1e4 \cdot \left[\frac{2.73e3 \cdot XJ}{DNB \cdot \ln\left(\frac{1e20}{DNB}\right)} \right]^{1/3} \cdot [(v_{ds} - v_{dsat} + PHI)^{1/3} - PHI^{1/3}]$$

ΔL is in microns, if XJ is in microns and DNB is in cm^{-3} .

Subthreshold Current, I_{ds}

The Fast Surface State (FSS) characterizes this region of operation if it is greater than $1e10$. The following equation then calculates the effective threshold voltage, separating the strong inversion region from the weak inversion region:

$$v_{on} = v_{th} + fast$$

The following equation calculates the fast value used in the preceding equation:

$$fast = v_{tm} \cdot \left[1 + \frac{q \cdot FSS}{cox} + \frac{\gamma}{2 \cdot (\Phi_f + v_{sb})^{1/2}} \right]$$

In the preceding equations, v_t is the thermal voltage.

The following equations calculate I_{ds} .

Weak Inversion Region, $v_{gs} < v_{th}$

$$I_{ds} = (v_{on}, v_{de}, v_{sb}) \cdot e^{\frac{v_{gs} - v_{on}}{fast}}$$

Strong Inversion Region, $v_{gs} > v_{th}$

$$I_{ds} = I_{ds}(v_{gs}, v_{de}, v_{sb})$$

Note: Strong inversion also use the modified threshold voltage (v_{on}) that FSS produces; that is, the mobility equations use v_{on} instead of v_{th} .

Depletion Mode DC Model ZENH=0

The LEVEL 5 MOS model uses depletion mode devices as the load element in contemporary standard n-channel technologies[2]. This model assumes a silicon gate construction with an ion implant used to obtain the depletion characteristics. A special model is required for depletion devices, because the implant used to create the negative threshold also results in a complicated impurity concentration profile in the substrate. The implant profile changes the basis for the traditional calculation of the QB bulk charge. The additional charge from the implant, QBI, must be calculated.

This implanted layer also forms an additional channel, offering a conductive pathway through the bulk silicon as well as through the surface channel. This second pathway can cause difficulties when trying to model a depletion device using existing MOS models.

The surface channel partially shields the bulk channel from the oxide interface, and the mobility of the bulk silicon can be substantially higher. Yet with all of these differences, a depletion model still can share the same theoretical basis as the Ithantola and Moll gradual channel model.

The depletion model differs from the Ithantola and Moll model:

- Implant charge accounted for.
- Finite implant thickness (DP).
- Assumes two channels: a surface channel and a bulk channel.
- Bulk channel has a bulk mobility (UH).
- Assumes that the bulk gain is different from the surface gain.

In the depletion model, the gain is lower at low gate voltages and higher at high gate voltages. Due to this variation in gain, the enhancement models cannot accurately represent a depletion device. The physical model for a depletion device is basically the same as an enhancement model, except that a one-step profile with DP depth approximates the depletion implant.

Due to the implant profile, simulation calculates the drain current equation by region. The MOSFET Level 5 model has three regions: depletion, enhancement, and partial enhancement.

Depletion Region, $v_{gs} - v_{fb} < 0$

The bulk channel dominates the low gate voltage region.

Enhancement Region, $v_{gs} - v_{fb} > 0$, $v_{ds} < v_{gs} - v_{fb}$

High gate voltage and low drain voltage define the enhancement region. In this region, both channels are fully turned on.

Partial enhancement region, $v_{gs} - v_{fb} > 0$, $v_{ds} > v_{gs} - v_{fb}$

The region has high gate and drain voltages so the surface region is partially turned on and the bulk region is fully turned on.

IDS Equations, Depletion Model LEVEL 5

Depletion, $v_{gs} - v_{fb} < 0$

$$I_{ds} = \beta_1 \cdot \left\{ q \cdot NI \cdot v_{de} + c_{av} \cdot \left[(v_{gs} - v_{fb}) \cdot v_{de} - \frac{v_{de}^2}{2} \right] \right. \\ \left. - \frac{2}{3} \cdot c_{av} \cdot \gamma \cdot [(v_{de} + v_{sb} + \Phi_d)^{3/2} - (v_{sb} + \Phi_d)^{3/2}] \right\}$$

Enhancement, $v_{gs} - v_{fb} > v_{de} > 0$

$$I_{ds} = \beta_1 \cdot \left\{ q \cdot NI \cdot v_{de} - \frac{2}{3} \beta_{cav} \beta_{\gamma} [(v_{de} + v_{sb} + \Phi_d)^{3/2} - (v_{sb} + \Phi_d)^{3/2}] \right\} \\ \beta \cdot \left[(v_{gs} - v_{fb}) \cdot v_{de} - \frac{v_{de}^2}{2} \right]$$

Partial Enhancement, $v_{gs} - v_{fb} < v_{de}$

$$I_{ds} = \beta_1 \cdot \left\{ q \cdot NI \cdot v_{de} + c_{av} \cdot \left[(v_{gs} - v_{fb}) \cdot v_{de} - \frac{v_{de}^2}{2} \right] \right. \\ \left. - \frac{2}{3} \cdot c_{av} \cdot \gamma \cdot [(v_{de} + v_{sb} + \Phi_d)^{3/2} - (v_{sb} + \Phi_d)^{3/2}] \right\} \\ \left(\frac{1}{2} \beta - \beta_1 \beta_{cav} \right) \cdot (v_{gs} - v_{fb})^2$$

The following equations calculate values used in the preceding equations:

$$\beta_1 = UH \cdot \frac{W_{eff}}{L_{eff}}$$

$$\beta = UB_{eff} \cdot cox \cdot \frac{W_{eff}}{L_{eff}}$$

$$cav = \frac{cox \cdot cs}{cox + cs}$$

$$cs = \frac{2.77E_{si}}{DP \cdot 1e-4}$$

$$\Phi_d = v_{tm} \cdot \ln\left(\frac{DNB \cdot nd}{ni^2}\right)$$

$$nd = \frac{NI \cdot 1e4}{DP}$$

$$v_{de} = \min(v_{ds}, v_{dsat})$$

The following sections describe the saturation voltage, threshold voltage, and effective γ .

Threshold Voltage, v_{th}

The V_{TO} model parameter is an extrapolated zero-bias threshold voltage for a large device. The following equations calculate the effective threshold voltage, including the device size effects and the terminal voltages:

$$v_{th} = v_{fb} - \beta_d \cdot [v_{ch} - \gamma \cdot (\Phi_d + v_{sb})^{1/2}]$$

The following equations calculate values used in the preceding equation:

$$v_{fb} = V_{TO} + \beta_d \cdot (v_{ch} - \gamma_0 \cdot \Phi_d^{1/2})$$

$$\beta_d = \frac{UH \cdot cav}{UB \cdot cox}$$

$$v_{ch} = \frac{q \cdot NI}{cav}$$

$$\gamma_0 = \frac{(2 \cdot E_{si} \cdot q \cdot na1)^{1/2}}{cav}$$

$$na1 = \frac{nd \cdot DNB}{nd + DNB}$$

$$nd = \frac{NI}{DP \cdot 1e-4}$$

The following equation computes the effective γ , including the small device size effects:

$$\gamma = \gamma_0 \cdot (1 - scf) \cdot (1 + ncf)$$

The following equations calculate values used in the preceding equation:

If SCM $\neq 0$, then scf=0. Otherwise,

$$scf = \frac{XJ}{L_{eff}} \cdot \left\{ \left[1 + \frac{2xd}{XJ} \cdot (SCM \cdot v_{ds} + v_b + \Phi_d)^{1/2} \right]^{1/2} - 1 \right\}$$

If NWM $\neq 0$, then ncf=0. Otherwise,

$$ncf = \frac{NWM \cdot X_d \cdot \Phi_d^{1/2}}{W_{eff}}$$

The following equation calculates the x_d value used in the preceding equation:

$$X_d = \left(\frac{2 \cdot E_{si}}{q \cdot DNB} \right)^{1/2}$$

Note: If $v_{gs} \leq v_{th}$, the surface is inverted and a residual DC current exists. If v_{sb} is large enough to make $v_{th} > vin_{th}$, then v_{th} is the inversion threshold voltage. To determine the residual current, this model inserts vin_{th} into the I_{ds} , v_{sat} , and mobility equation in place of v_{gs} (except for v_{gs} in the exponential term of the subthreshold current).

The inversion threshold voltage at a specified v_{sb} is vin_{th} , which the following equation computes:

$$vinth = v_{fb} - \frac{q \cdot NI}{cox} - v_{sb}$$

Saturation Voltage, v_{dsat}

The following equation computes the saturation voltage (v_{sat}):

$$v_{sat} = v_{gs} - v_{fb} + v_{ch} + \frac{\gamma^2}{2} \cdot \left\{ 1 - \left[1 + \frac{4}{\gamma^2} \cdot (v_{gs} - v_{fb} + v_{ch} + v_{sb} + \Phi_d) \right]^{1/2} \right\}$$

$$v_{dsat} = v_{sat}$$

IF ECV is not equal to 1000 (V/ μ m), the Synopsys device models modify v_{sat} to include the carrier velocity saturation effect:

$$v_{dsat} = v_{sat} + v_c - (v_{sat} + v_c^2)^{1/2}$$

The following equation calculates the v_c value used in the preceding equation:

$$v_c = ECV \cdot L_{eff}$$

Mobility Reduction, UB_{eff}

The surface mobility (UB) depends on terminal voltages as follows:

$$UB_{eff} = \frac{1}{\frac{1}{UB} + \frac{FRC \cdot (v_{gs} - v_{th})}{TOX} + \frac{v_{de}}{VST \cdot l_e} + FSB \cdot v_{sb}^{1/2}}$$

The following equations calculate values used in the preceding equation:

$$L_e = L_{eff} \text{ Linear region}$$

$$L_e = L_{eff} - \Delta L \text{ Saturation region}$$

The next section describes the ΔL channel length modulation effect.

Channel Length Modulation

Modify the I_{ds} current to model the channel length modulation effect:

$$I_{ds} = \frac{I_{ds}}{1 - \frac{\Delta L}{L_{eff}}}$$

The following equation calculates the ΔL value used in the preceding equation:

$$\Delta L = 1e4 \cdot \left[\frac{2.73e3 \cdot XJ}{na1 \cdot \ln\left(\frac{1e20}{na1}\right)} \right]^{1/3} \cdot [(v_{ds} - v_{dsat} + PHI)^{1/3} - PHI^{1/3}]$$

The ΔL parameter is in microns, if XJ is in microns and $na1$ is in cm^{-3} .

Subthreshold Current, I_{ds}

If device leakage currents become important for operation near or below the normal threshold voltage, then this model considers the subthreshold characteristics. The Level 5 MOSFET model uses the subthreshold model only if the number of fast surface states (FSS) is greater than $1e10$. The following equation determines the effective threshold voltage (von):

$$von = v_{th} + fast$$

The following equation calculates the fast value used in the preceding equation:

$$fast = v_{tm} \cdot \left[1 + \frac{q \cdot FSS}{cox} + \frac{\gamma}{2 \cdot (\Phi_d + v_{sb})^{1/2}} \right]$$

If $von < vin_{th}$, then simulation substitutes vin_{th} for von .

Note: The Level 5 MOSFET device model uses the following subthreshold model only if $v_{gs} < von$, and if the device is either in partial or full enhancement mode. Otherwise, it uses the model in enhancement mode ($ZENH=1$). The subthreshold current calculated below includes the residual DC current.

If $v_{gs} < von$ then:

Partial Enhancement, $v_{gs} - v_{fb} < v_{de}$

$$I_{ds} = \beta 1 \cdot \left\{ q \cdot NI \cdot v_{de} + cav \cdot \left[(von - v_{fb}) \cdot v_{de} - \frac{v_{de}^2}{2} \right] - \frac{2}{3} \cdot cav \cdot \gamma \cdot [(v_{de} + v_{sb} + \Phi_d)^{3/2} - (v_{sb} + \Phi_d)^{3/2}] \right\}$$

$$\frac{1}{2} \cdot \left(\beta \cdot e^{\frac{v_{gs} - v_{on}}{fast}} - \beta 1_{\text{cav}} \right) \cdot (v_{on} - v_{fb})^2$$

Full Enhancement, $v_{gs} - v_{fb} \quad v_{de} > 0$

$$I_{ds} = \beta 1 \cdot \left\{ q \cdot NI \cdot v_{de} - \frac{2}{3} \beta_{cav} \beta \gamma [(v_{de} + v_{sb} + \Phi_d)^{3/2} - (v_{sb} + \Phi_d)^{3/2}] \right\}$$

$$\beta \cdot \left[(v_{on} - v_{fb}) \cdot v_{de} - \frac{v_{de}^2}{2} \right] \cdot e^{\frac{v_{gs} - v_{on}}{fast}}$$

Example

This example is based on demonstration netlist m15iv.sp, which is available in directory \$<installdir>/demo/hspice/mos:

```
FILE ML5IV.SP HSPICE LEVEL 5 MODEL EXAMPLES
*OUTPUT CHARACTERISTICS FOR ENHANCEMENT & DEPLETION MODE
.OPT ACCT LIST CO=132 POST=2
.OP
VDS 3 0 .1
VGS 2 0
M1 1 2 0 0 MODEN L=20U W=20U
.MODEL MODEN NMOS LEVEL=5
+ VT=.7 TOX=292 FRC=2.739E-2 DNB=2.423E16 UB=642.8
+ OXETCH=-.98 XJ=.29 LATD=.34 ECV=4 VST=5.595E7
+ FSB=7.095E-5 SCM=.4 FSS=2.2E11 NWM=.93 PHI=.61
+ TCV=1.45E-3 PTC=9E-5 BEX=1.8
*
VIDS 3 1
.DC VGS 0 5 0.2
.PRINT DC I(VIDS) V(2)
.PRINT DC I(VIDS)
$$$$$
.ALTER
$$$$$
M1 1 2 0 0 MODDP L=20U W=20U
.MODEL MODDP NMOS LEVEL=5 ZENH=0.
+ VT=-4.0 FRC=.03 TOX=800 DNB=6E14 XJ=0.8 LATD=0.7
+ DEL=0.4 CJ=0.1E-3 PHI=0.6 EXA=0.5 EXP=0.5 FSB=3E-5
+ ECV=5 VST=4E7 UB=850 SCM=0.5 NI=5.5E11 DP=0.7 UH=1200
*
.END
```

LEVEL 6/LEVEL 7 IDS: MOSFET Model

These models represent ASPEC, MSINC, and ISPICE MOSFET model equations. The only difference between LEVEL 6 and LEVEL 7 equations is the handling of the parasitic elements and the method of temperature compensation. See [Table 10 on page 61](#) and [Channel Length Modulation on page 73](#) for those model parameters.

LEVEL 6 and LEVEL 7 Model Parameters

MOSFET Levels 6 and 7 use the generic MOSFET model parameters described in [Chapter 2, Common MOSFET Model Parameters](#). These levels also use the parameters described in this section, which apply only to MOSFET Levels 6 and 7.

Table 12 Alternate Saturation Model Parameters

Name (Alias)	Units	Default	Description
KA		1.0	Alternate saturation model: coefficient for the short-channel vds scaling factor.
KU		0.0	Lateral field mobility parameter.
MAL		0.5	Alternate saturation model: exponent of the short-channel vds scaling factor.
MBL		1.0	Exponent for mobility reduction due to the source-drain electric field.
NU		1.0	Mobility reduction due to the source-drain electric field.

UPDATE Parameter for LEVEL 6 and LEVEL 7

The general form of the I_{ds} equation for LEVEL 6 is the same as the LEVEL 2 MOS model. However, the small size effects, mobility reduction, and channel length modulation are included differently. Also, you can use the multi-level GAMMA capability to model MOS transistors with ion-implanted channels.

The LEVEL 6 model can represent the ASPEC, MSINC, or ISPICE MOSFET model. Use the `UPDATE` model parameter to invoke different versions of the LEVEL 6 model.

UPDATE=0

This is the original Synopsys Level 6 MOSFET device model, which is not quite compatible with the ASPEC model. It has some discontinuities in the weak inversion, mobility equations (`MOB=3`), and multi-level `GAMMA` equations.

UPDATE=1

This enhanced version of the LEVEL 6 model contains improved multi-level `GAMMA` equations. The saturation voltage, drain-source current, and conductances are continuous.

UPDATE=2

This version of the LEVEL 6 model is compatible with the ASPEC model. The multi-level `GAMMA` model is not continuous as it is in the ASPEC program. See [ASPEC Compatibility on page 123](#).

- Set `UPDATE` to 1.0 to use changes to the device equations.
- Set `UPDATE` to 1.0 or 2 to use the default `RS` and `RD` handling.

These values and changes provide a more accurate ASPEC model.

UPDATE=1 or 2:

`TOX=690`

`UO (UB)=750 cm2/(V · s) (N-ch)`

`UTRA (F3)=0.0`

UPDATE=0:

`TOX=1000`

`UO (UB)=750 cm2/(V · s) (N-ch)`

`UTRA (F3)=0.0`

If you do not specify `LDIF`, then the `RD` and `RS` values change in the MOSFET:

UPDATE=1 or 2 and LDIF=0:

$$RD = \frac{(RD + NRD \cdot RL)}{M}$$

$$RS = \frac{(RS + NRS \cdot RL)}{M}$$

Note: The ASPEC program does not use the M multiplier.

LDIF \neq 0:

$$RD = \frac{LATD_{scaled} + LDIF_{scaled}}{W_{eff}} \cdot RD + NRD \cdot \frac{RL}{M}$$

$$RS = \frac{LATD_{scaled} + LDIF_{scaled}}{W_{eff}} \cdot RS + NRS \cdot \frac{RL}{M}$$

The vde value in the mobility equations change for the alternate saturation model:

$$vde = \min\left(\frac{vds}{vfa}, v_{sat}\right), \text{UPDATE}=1 \text{ or } 2$$

$$vde = \min(vds, vfa \cdot v_{sat}), \text{UPDATE}=0$$

The impact ionization equation calculates the saturation voltage:

$$vdsat = vfa \cdot v_{sat}, \text{UPDATE}=1 \text{ or } 2$$

$$vdsat = v_{sat}, \text{UPDATE}=0$$

The MOB=3 mobility equation changes:

UPDATE=1 or 2 and $(vgs - vth)^{F2} > VF1$:

$$u_{eff} = \frac{UB}{F4 + (F1 - F3) \cdot VF1 + F3 \cdot (vgs - vth)^{F2}}$$

UPDATE=0 and $(vgs - vth)^{F2} > VF1$:

$$u_{eff} = \frac{UB}{F4 + F3 \cdot (vgs - vth)^{F2}}$$

LEVEL 6 Model Equations, UPDATE=0,2

IDS Equations

$$ids = \beta \cdot \left\{ \left(vgs - vbi - \frac{\eta \cdot vde}{2} \right) \cdot vde - \frac{2}{3} \right\} \Rightarrow \left[(PHI + vde + vsb)^{3/2} - (PHI + vsb)^{3/2} \right]$$

The following equations calculate values used in the preceding equation:

$$v_{de} = \min(v_{ds}, v_{dsat})$$

$$\eta = 1 + \frac{NWE_{scaled}}{w_{eff}}$$

$$\beta = u_{eff} \cdot COX \cdot \frac{w_{eff}}{L_{eff}}$$

- The η v_{bi} , and γ values define the narrow-width effect.
- The NWE or NWM model parameters also specify the narrow-width effect.
- The v_{bi} and γ parameters specify the short-channel effect.

Effective Channel Length and Width

The following equations calculate the effective channel length and width from the drawn length and width:

$$l_{eff} = L_{scaled} \cdot LMLT + XL_{scaled} - 2 \Rightarrow (LD_{scaled} + DEL_{scaled})$$

$$w_{eff} = M \cdot (W_{scaled} \cdot WMLT + XW_{scaled} - 2 \Rightarrow WD_{scaled})$$

$$LREF_{eff} = LREF_{scaled} \cdot LMLT + XL_{scaled} - 2 \Rightarrow (LD_{scaled} + DEL_{scaled})$$

$$WREF_{eff} = M \cdot (WREF_{scaled} \cdot WMLT + XW_{scaled} - 2 \Rightarrow WD_{scaled})$$

Threshold Voltage, v_{th}

The following equation determines the effective threshold voltage:

$$v_{th} = v_{bi} + \gamma \cdot (PHI + v_{sb})^{1/2}$$

The v_{bi} and γ built-in voltage value depends on the specified model parameters.

Single-Gamma, $V_{BO}=0$

If you set the V_{BO} model parameter to zero, simulation uses the single-gamma model, which treats the $LGAMMA$ parameter as a junction depth. To modify the $GAMMA$ parameter for the short-channel effect, this model then uses the scf factor, which the Poon and Yau formulation computes. In this case, simulation multiplies $LGAMMA$ by the $SCALM$ option.

$$scf = 1 - \frac{LGAMMA}{l_{eff}} \Rightarrow \left[1 + \frac{2 \cdot LAMBDA}{LGAMMA} \cdot (PHI + v_{sb})^{1/2} \right]^{1/2} - 1$$

The XJ model parameter modifies the $GAMMA$ model parameter by the short-channel factor (gl):

$$gl = 1 - \frac{XJ_{scaled}}{leff} \Rightarrow \left[1 + \frac{2 \cdot LAMBDA}{XJ_{scaled}} \cdot (PHI + v_{sb} + SCM \cdot v_{ds})^{1/2} \right]^{1/2} - 1$$

The gl factor generally replaces the scf factor for the multi-level $GAMMA$ model.

The gw factor modifies $GAMMA$ to compute the narrow-width effect:

$$gw = \frac{1 + NWM \cdot xd}{weff}$$

The following equation calculates the xd value used in the preceding equation:

$$xd = \left(\frac{2 \cdot \epsilon_{si}}{q \cdot DNB} \right)^{1/2}$$

Finally, the effective γ , including short-channel and narrow-width effects, is

$$\gamma = GAMMA \cdot gw \cdot gl \cdot scf$$

Effective Built-in Voltage, v_{bi}

The Level 6 model includes the narrow-width effect. This effect is the increase in threshold voltage due to the extra bulk charge at the edge of the channel. To use this effect with the NWE model parameter, modify v_{bi} .

Modify v_{bi} to use the short-channel effect, which decreases threshold voltage due to the induced potential barrier-lowering effect. To include this effect, you must specify either the FDS parameter, or the $UFDS$ and $VFDS$ model parameters.

The following equations calculate v_{bi} , which sums up the preceding features.

$v_{ds} < VFDS$, or $VFDS = 0$

$$v_{bi} = VTO - \gamma \Rightarrow PHI^{1/2} + (\eta - 1) \cdot (PHI + v_{sb}) - \frac{LD_{scaled}}{Leff} \\ \Rightarrow V_{SH} - \frac{\epsilon_{si}}{COX \cdot Leff} \Rightarrow FDS \Rightarrow v_{ds}$$

$v_{ds} > VFDS$

$$v_{bi} = VTO - \gamma \Rightarrow PHI^{1/2} + (\eta - 1) \cdot (PHI + v_{sb}) - \frac{LD_{scaled}}{leff} \Rightarrow V_{SH} - \frac{\epsilon_{si}}{COX \cdot Leff}$$

$$[(FDS - UFDS) \cdot VFDS + UFDS \cdot vds]$$

The preceding equations describe piecewise linear variations of v_{bi} as a function of v_{ds} . If you do not specify $VFDS$, this model uses the first equation for v_{bi} .

Note: The Level 6 MOSFET device model calculates model parameters such as V_{TO} , Φ_I , and Γ , if you did not specify them (see [Common Threshold Voltage Parameters on page 742](#)).

Multi-Level Gamma, $V_{BO} > 0$

Use Multi-Level Gamma to model MOS transistors with Ion-Implanted channels. The doping concentration under the gate is approximated as step functions.

- Γ represents the corresponding body effects coefficient for the implant layer.
- Γ_b represents the corresponding body effects coefficient for the substrate.

[Figure 2](#) shows the variation of v_{th} as a function of v_{sb} for Multi-Level Gamma.

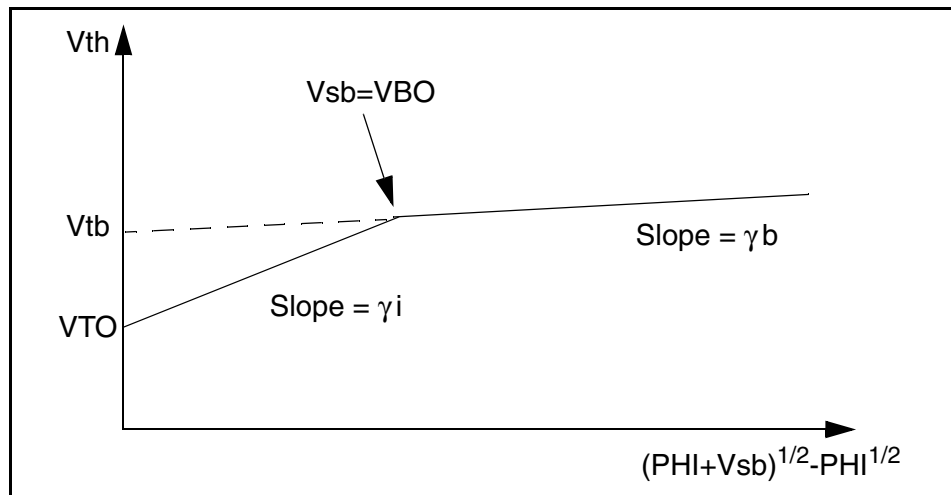


Figure 2 Threshold Voltage Variation

The following equations calculate the threshold voltage for different regions:
Channel Depletion Region is in the Implant Layer, $v_{sb} < V_{BO}$

$$\gamma = \gamma_i$$

$$v_{th} = v_{bi} + \gamma_i \cdot (v_{sb} + PHI)^{1/2}$$

$$v_{bi} = VTO - \gamma_i \cdot (PHI)^{1/2}$$

Channel Depletion Region Expands into the Bulk, $v_{sb} > VBO$

$$\gamma = \gamma_b$$

$$v_{th} = v_{bi} + \gamma_b \cdot (v_{sb} + PHI)^{1/2}$$

$$v_{bi} = v_{tb} - \gamma_b \cdot (PHI)^{1/2}$$

For the threshold voltage to be continuous at $v_{sb}=VBO$, v_{tb} must be:

$$v_{tb} = VTO + (\gamma_i - \gamma_b) \cdot [(VBO + PHI)^{1/2} - (PHI)^{1/2}]$$

- γ_i is the effective value of GAMMA.
- γ_b is the effective value of LGAMMA.

The model computes them as γ in single-gamma models, except the scf factor is 1.0.

$$\gamma_i = GAMMA \cdot g_w \cdot g_l$$

$$\gamma_b = LGAMMA \cdot g_w \cdot g_l$$

Effective Built-in Voltage, v_{bi} for $VBO > 0$

For $v_{ds} < VFDS$

if $v_{sb} \leq VBO$:

$$v_{bi} = VTO - \gamma_i \cdot (PHI)^{1/2} + (\eta - 1) \cdot (PHI + v_{sb}) - \frac{LD_{scaled}}{Leff}$$

$$\Rightarrow V_{SH} - \frac{\epsilon_{si}}{COX \cdot Leff} \Rightarrow V_{DS} \Rightarrow v_{ds}$$

if $v_{sb} > VBO$:

$$v_{bi} = VTO - \gamma_b \cdot (PHI)^{1/2} + (\gamma_i - \gamma_b) \cdot [(VBO + PHI)^{1/2} - (PHI)^{1/2}] + (\eta - 1) \cdot (PHI + v_{sb}) - \frac{LD_{scaled}}{Leff}$$

$$\Rightarrow V_{SH} - \frac{\epsilon_{si}}{COX \cdot Leff} \Rightarrow V_{DS} \Rightarrow v_{ds}$$

For $v_{ds} > VFDS$

if $v_{sb} \leq VBO$:

$$v_{bi} = V_{TO} - \gamma_i \Rightarrow (PHI)^{1/2} + (\eta - 1) \cdot (PHI + v_{sb})$$

$$- \frac{LD_{scaled}}{Leff} \Rightarrow V_{SH} - \frac{\epsilon_{si}}{COX \cdot Leff}$$

$$[(FDS - UFDS) \cdot VFDS + UFDS \cdot v_{ds}]$$

if $v_{sb} > V_{BO}$:

$$v_{bi} = V_{TO} - \gamma_b \Rightarrow (PHI)^{1/2} + (\gamma_i - \gamma_b) \cdot [(V_{BO} + PHI)^{1/2} - (PHI)^{1/2}] + (\eta - 1)$$

$$PHI + v_{sb} - \frac{LD_{scaled}}{Leff} \Rightarrow V_{SH} - \frac{\epsilon_{si}}{COX \cdot Leff}$$

$$\Rightarrow [(FDS - UFDS) \cdot VFDS + UFDS \cdot v_{ds}]$$

Saturation Voltage, v_{dsat} (UPDATE=0,2)

The following formula determines the saturation voltage due to channel pinch-off at the drain side:

$$v_{sat} = \frac{v_{gs} - v_{bi}}{\eta} + \frac{1}{2} \left(\frac{\gamma}{\eta} \right)^2 \cdot \left\{ 1 - \left[1 + \left(\frac{2 \cdot \eta}{\gamma} \right)^2 \cdot \left(\frac{v_{gs} - v_{bi}}{\eta} + PHI + v_{sb} \right) \right]^{1/2} \right\}$$

The following equation calculates the reduction of the saturation voltage due to the carrier velocity saturation effect:

$$v_{dsat} = v_{sat} + v_c - (v_{sat}^2 + v_c^2)^{1/2}$$

In the preceding equation, determines v_c if the `ECRIT` model parameter >0 , or $V_{MAX} >0$, and $KU \leq 1$. If you specify both `ECRIT` and V_{MAX} , then simulation uses only the V_{MAX} equation. However, this model does not use the V_{MAX} equation if $MOB=4$ or $MOB=5$, because these mobility equations already contain a velocity saturation term.

$$v_c = ECRIT \cdot Leff \text{ or } v_c = \frac{V_{MAX} \cdot Leff}{u_{eff}}$$

Because $v_{sb} > V_{BO}$, γ switches from γ_1 to γ_β , and the i_{ds} , v_{sat} , and conductance values are not continuous as in the following example. To correct this discontinuity problem, specify the `UPDATE=1` model parameter. The next section discusses this improvement.

Example

This example is based on demonstration netlist tgam2.sp, which is available in directory \$<installdir>/demo/hspice/mos:

```
$ tgam2.sp---multi-level gamma model
* this data is for the comparison of multi-level gamma
* update=0 or 2 and the improved multi-level gamma update=1.
*
.options post aspect nomod vntol=.1u reli=.001 relv=.0001
*
.model nch nmos bulk=99 update=2
+ fds=0.9 ku=1.6 mal=0.5 mob=1 clm=1
+ latd=0.2 phi=0.3 vt=0.9 gamma=0.72 lgamma=0.14
+ vb0=1.2 fl=0.08 esat=8.6e+4 kl=0.05
+ lambda=3.2u ub=638 f3=0.22
+ ka=0.97 mbl=0.76 nfs=1.0e+12 wic=0
+ ldel=0.084 wdel=0.037 tox=365 vsh=0.7
*
vd 1 0 5
vb 0 99 0
vg 2 0 1
ma 1 2 0 99 nch 26.0 1.4
.dc vb 1.0 1.3 .01
.probe ids=par('i(ma)') vth=par('lv9(ma)') vdsat=par('lv10(ma)')
.probe gm=par('lx7(ma)') ds=par('lx8(ma)') gmbs=par('lx9(ma)')
.end
```

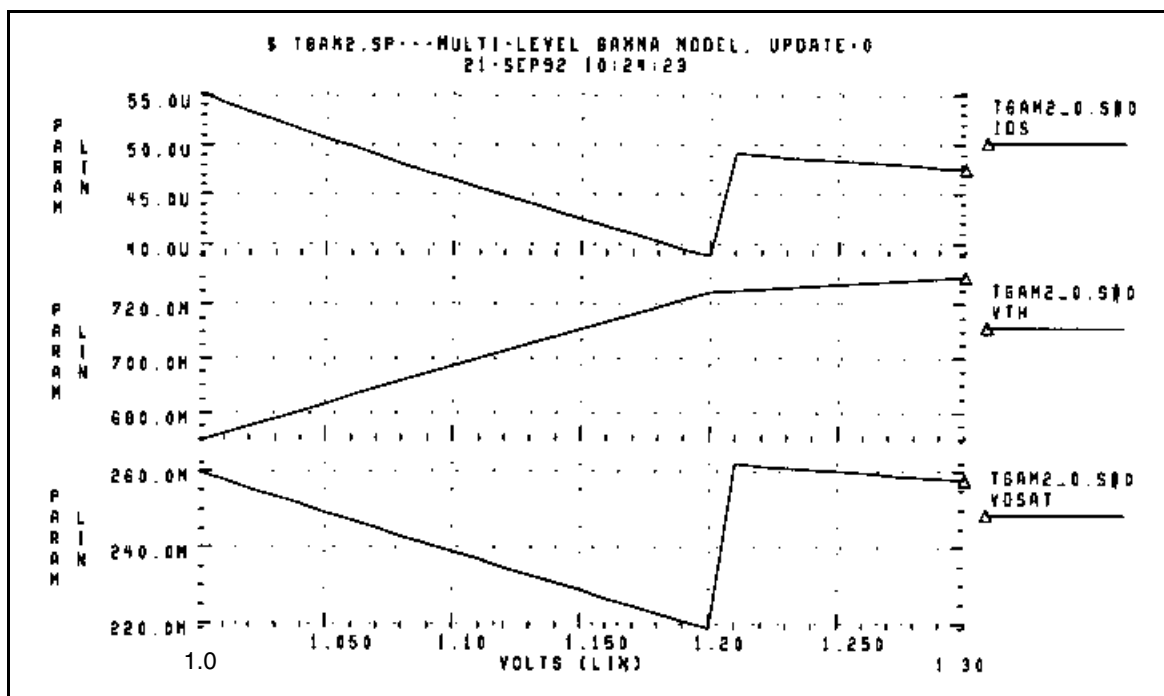



Figure 3 Variation of IDS, VTH and VDSAT for UPDATE=0

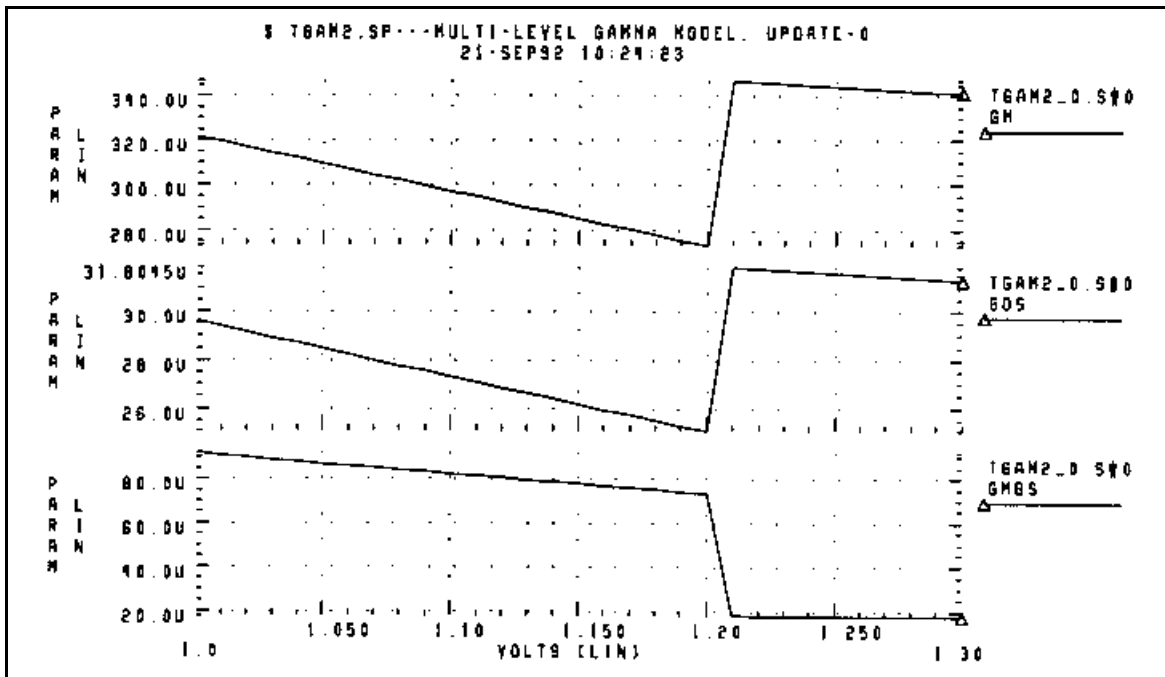


Figure 4 Variation of GM, GDS and GMBS for UPDATE=0

Each plot compares IDS, VTH, VDSAT, GM, GDS and GMBS as a function of vsb for UPDATE=0.

Improved Multi-Level Gamma, UPDATE=1

As demonstrated in previous sections, the regular Multi-Level Gamma displays some discontinuities in saturation voltage and drain current. This occurs because when v_{sb} is less than VBO, simulation sets γ to γ_i and uses it to calculate i_{ds} and v_{sat} . This is not correct; if $(v_{ds} + v_{sb})$ exceeds VBO, then the depletion regions at the drain side expands into the substrate region, and the v_{sat} computation must use γ_b instead of γ_i . Because $v_{sat} = v_{gs} - v_{th}(\text{drain})$, this model uses γ_i to compute the threshold voltage at the drain for $v_{sb} < VBO$. As a result, the existing model overestimates the threshold voltage ($\gamma_i > \gamma_b$), and underestimates the saturation voltage and the drain current in the saturation region.

This causes a discontinuous increase in the saturation drain current, crossing from the $v_{sb} < VBO$ region to the $v_{sb} > VBO$ region.

The improved Multi-Level model upgrades the saturation voltage and drain current equations, compared to the regular Multi-Level model. To use the improved model, set the model parameter to UPDATE=1.

Example

You can see an example of a multi-level gamma model with UPDATE=2 using a netlist from a previous example. Change UPDATE=0 to UPDATE=2 in the netlist located in directory \$installdir/demo/hspice/mos/tgam2.sp:

```
$ tgam2.sp---multi-level gamma model
* this data is for the comparison of multi-level gamma
* update=0 or 2 and the improved multi-level gamma update=1.
*
.options post aspect nomod vntol=.1u reli=.001 relv=.0001
*
.model nch nmos bulk=99 update=2
+ fds=0.9 ku=1.6 mal=0.5 mob=1 clm=1
+ latd=0.2 phi=0.3 vt=0.9 gamma=0.72 lgamma=0.14
+ vb0=1.2 fl=0.08 esat=8.6e+4 kl=0.05
+ lambda=3.2u ub=638 f3=0.22
+ ka=0.97 mbl=0.76 nfs=1.0e+12 wic=0
+ ldel=0.084 wdel=0.037 tox=365 vsh=0.7
*
vd 1 0 5
vb 0 99 0
vg 2 0 1
ma 1 2 0 99 nch 26.0 1.4
.dc vb 1.0 1.3 .01
.probe ids=par('i(ma)') vth=par('lv9(ma)') vdsat=par('lv10(ma)')
.probe gm=par('lx7(ma)') ds=par('lx8(ma)') gmbs=par('lx9(ma)')
.end
```

Chapter 3: MOSFET Models: LEVELs 1 through 40
LEVEL 6/LEVEL 7 IDS: MOSFET Model

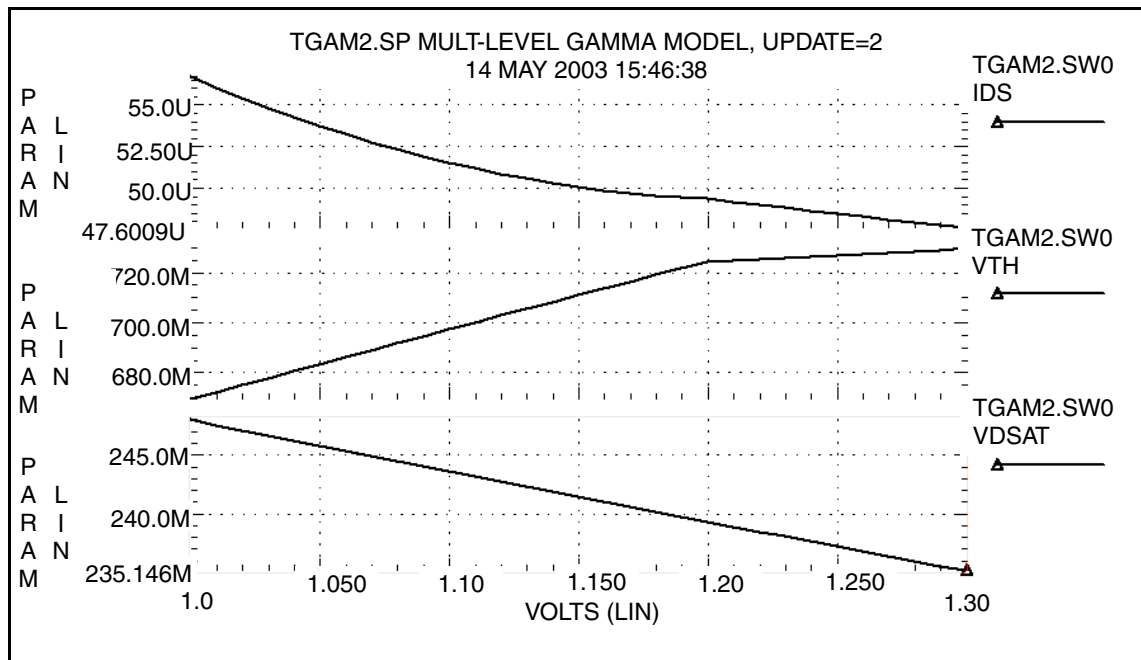


Figure 5 Variation of IDS, VTH and VDSAT for UPDATE=2

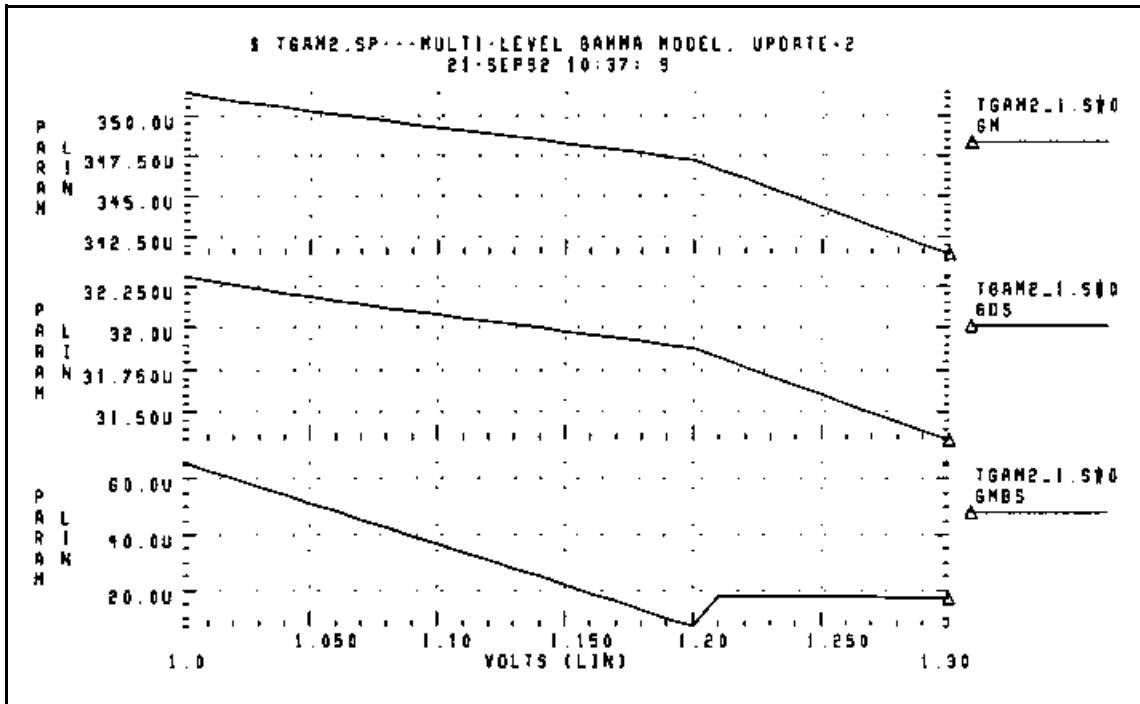


Figure 6 Variation of GM, GDS and GMBS for UPDATE=2

Each plot compares IDS, VTH, VDSAT, GM, GDS, and GMBS as a function of vsb for UPDATE=1.

Saturation Voltage, vsat

To obtain the right value for vsat, the following equations calculate two trial values of vsat corresponding to γ_i and γ_b :

$$v_{sat1} = \frac{v_{gs} - v_{bi1}}{\eta} + \frac{1}{2} \left(\frac{\gamma_i}{\eta} \right)^2 \cdot \left\{ 1 - \left[1 + \left(\frac{2 \cdot \eta}{\gamma_i} \right)^2 \cdot \left(\frac{v_{gs} - v_{bi1}}{\eta} + PHI + v_{sb} \right) \right]^{1/2} \right\}$$

$$v_{sat2} = \frac{v_{gs} - v_{bi2}}{\eta} + \frac{1}{2} \left(\frac{\gamma_b}{\eta} \right)^2 \cdot \left\{ 1 - \left[1 + \left(\frac{2 \cdot \eta}{\gamma_b} \right)^2 \cdot \left(\frac{v_{gs} - v_{bi2}}{\eta} + PHI + v_{sb} \right) \right]^{1/2} \right\}$$

- vbi1 is the built-in potential corresponding to γ_i .
- vbi2 is the built-in potential corresponding to γ_b .

- If $(v_{dsat1} + v_{sb}) \leq V_{BO}$, then $v_{dsat} = v_{dsat1}$
- If $(v_{dsat2} + v_{sb}) > V_{BO}$, then $v_{dsat} = v_{dsat2}$

To obtain v_{dsat} , v_c modifies v_{sat} for the carrier velocity saturation.

LEVEL 6 IDS Equations, UPDATE=1

You can use one of three equations for i_{ds} , depending on the region of operation. To derive these equations, this model integrates the bulk charge ($v_{gs} - v_{th}$ (v) - v) from the source to the drain.

For $v_{sb} < V_{BO} - v_{de}$, the model forms an entire gate depletion region in the implant layer.

$$i_{ds} = \beta \cdot \left\{ \left(v_{gs} - v_{bi1} - \frac{\eta \cdot v_{de}}{2} \right) \cdot v_{de}^{-\frac{2}{3}} \cdot \gamma_i \cdot [(PHI + v_{de} + v_{sb})^{3/2} - (PHI + v_{sb})^{3/2}] \right\}$$

In the preceding equation, v_{bi1} is the same as v_{bi} for $v_{sb} \leq V_{BO}$.

For $v_{sb} \geq V_{BO}$, the entire gate depletion region expands into the bulk area.

$$i_{ds} = \beta \cdot \left\{ \left(v_{gs} - v_{bi2} - \frac{\eta \cdot v_{de}}{2} \right) \cdot v_{de}^{-\frac{2}{3}} \cdot \gamma_b \cdot [(PHI + v_{de} + v_{sb})^{3/2} - (PHI + v_{sb})^{3/2}] \right\}$$

In the preceding equation, v_{bi2} is the same as v_{bi} for $v_{sb} > V_{BO}$.

$$i_{ds} = \beta \cdot \left\{ \left(v_{gs} - v_{bi2} - \frac{\eta \cdot v_{de}}{2} \right) \cdot v_{de}^{-\frac{2}{3}} \cdot \gamma_i \cdot [(V_{BO} + PHI)^{3/2} - (v_{sb} + PHI)^{3/2}] \right. \\ \left. (\gamma_i - \gamma_b) \cdot (V_{BO} + PHI)^{1/2} \cdot (V_{BO} - v_{sb}) \right\}$$

For $V_{BO} - v_{de} < v_{sb} < V_{BO}$, the source side gate depletion region is in the implant layer, but the drain side gate depletion region expands into the bulk area.

Alternate DC Model (ISPIICE model)

To invoke this model, set the $KU > 1$ model parameter. Then, the model computes vfu and vfa scale factors to scale both the vds voltage and the ids current. These scale factors are functions of $ECRIT$ and the vgs voltage. The following equations compute the vfa and vfu factors:

$$vfu = 1 - \frac{KU}{(\alpha^2 + KU^2)^{1/2} + \alpha(KU - 1)}$$

$$vfa = KA \cdot vfu^{(2 \cdot MAL)}$$

The following equation calculates the α value used in the preceding equations:

$$\alpha = \frac{ECRIT \cdot Leff}{vgs - vth}$$

Note: The vfu factor is always less than one.

The following equation modifies the ids current:

$$NU=1$$

$$ids = vfu^{(2 \cdot MBL)} \cdot ids$$

For $NU=0$, the

$$vfu^{(2 \cdot MBL)}$$

factor is set to one.

The ids current is a function of the effective drain to source voltage (vde):

$$vde = \min(vds/vfa, vsat)$$

$$vdsat = vfa \cdot vsat$$

This alternate model is generally coupled with the mobility normal field equations ($MOB=3$) and the channel length modulation drain field equation ($CLM=3$).

The mobility equations use the following vde and vds values:

$$vde = \min(vds, vfa \cdot vsat), \text{UPDATE}=0$$

$$vds = \min(vds/vfa, vsat), \text{UPDATE}=1, 2$$

Subthreshold Current, *ids*

is the choice of two different equations, selected through The **WIC** (Weak Inversion Choice) model parameter characterizes this region of operation.

Parameter	Description
WIC=0	No weak inversion (default)
WIC=1	ASPEC-style weak inversion
WIC=2	Enhanced HSPICE-style weak inversion

In addition to **WIC**, set the **NFS** parameter. **NFS** represents the number of fast states per centimeter squared. Reasonable values for **NFS** range from 1e10 to 1e12.

WIC=0

No weak inversion.

WIC=1

The *vth* threshold voltage increases by the fast term.

$$v_{on} = v_{th} + fast$$

The following equation calculates the fast value used in the preceding equation:

$$fast = v_t \cdot \left[1 + \frac{q \cdot NFS}{COX} + \frac{\gamma}{2 \cdot (v_{sb} + PHI)^{1/2}} \right]$$

In the preceding equations, *vt* is the thermal voltage. The following equation specifies the *ids* current for *vgs*<*von*:

$$ids = ids(v_{on}, v_{de}, v_{sb}) \cdot e^{\frac{v_{gs} - v_{on}}{fast}}$$

if *vgs*<*von*, then

$$ids = ids(v_{ge}, v_{de}, v_{sb})$$

Note: Strong inversion conditions do not use the modified threshold voltage (*von*).

WIC=2

The subthreshold region is limited between the cutoff region and the strong inversion region. If the gate voltage is less than v_{th-PHI} , this model cannot include any weak inversion conduction. However, this model can still include diffusion conduction from the drain-to-bulk rather than from the drain-to-source.

$$v_{on} = v_{th} + fast$$

The following equation calculates the fast value used in the preceding equation:

$$fast = v_t \cdot \left[1 + \frac{q \cdot NFS}{COX} + \frac{\gamma}{2 \cdot (v_{sb} + PHI)^{1/2}} \right]$$

Cutoff Region, $v_{gs} \leq v_{th} - PHI$

$$i_{ds} = 0$$

Weak Inversion, $v_{th} - PHI < v_{gs} \leq v_{on}$

$$i_{ds} = i_{ds}(v_{on}, v_{de}, v_{sb}) \cdot \left(1 - \frac{v_{on} - v_{gs}}{fast + PHI} \right)^{WEX}$$

Strong Inversion, $v_{gs} > v_{on}$

$$i_{ds} = i_{ds}(v_{gs}, v_{de}, v_{sb})$$

Note: Strong inversion conditions do not use the modified threshold voltage (v_{on}).

WIC=3

If $WIC=3$, simulation calculates the subthreshold current differently. In this case, the i_{ds} current is:

$$i_{ds} = i_{ds}(v_{gs}, v_{de}, v_{sb}) + i_{sub}(N0eff, NDeff, v_{gs}, v_{ds})$$

$N0eff$ and $NDeff$ are functions of the effective device width and length.

Effective Mobility, u_{eff}

All mobility equations have the following general form:

$$u_{eff} = UO \cdot factor$$

Parameter	Description
UEFF	Effective mobility at the specified a specified analysis temperature.

Chapter 3: MOSFET Models: LEVELs 1 through 40

LEVEL 6/LEVEL 7 IDS: MOSFET Model

Parameter	Description
FACTOR	Mobility degradation factor. Default=1.0

Use the MOB model parameter to select the mobility modulation equation used in the Level 6 MOSFET model.

Parameter	Description
MOB=0	No mobility reduction (default)
MOB=1	Gm equation
MOB=2	Frohman-Bentchkowski equation
MOB=3	Normal field equation
MOB=4	Universal field mobility reduction
MOB=5	Universal field mobility reduction with an independent drain field
MOB=6	Modified MOB=3 equations (lateral field effect included)
MOB=7	Modified MOB=3 equations (lateral field effect not included)

The following sections describe these equations.

MOB=0 Default, No Mobility

FACTOR=1.0 No mobility reduction

MOB=1

Table 13 MOB=1 Gm Equation

Name (Alias)	Units	Default	Description
F1	1/V	0.0	Gate field mobility reduction
UTRA (F3)	factor	0.0	Source-drain mobility reduction factor

Use the MOB=1 equation for transistors with constant source-to-bulk voltage, because the factor does not contain a vsb term. This equation sometimes over-

estimates mobility for small gate voltages and large back-bias, such as depletion pull-ups.

$$factor = \frac{1}{1 + F1 \cdot (vgs - vbi - F3 \Rightarrow vde)}$$

$$vde = \min(vds, vdsat)$$

Note: In the alternate saturation model, vde is different if UPDATE=0 than if UPDATE=1. See [Alternate DC Model \(SPICE model\) on page 111](#). Also, if VMAX>0, then vde=min (vds, vsat). If you do not specify VMAX, then vde=min (vds, vdsat).

MOB=2

Table 14 MOB=2 Frohman-Bentchkowski Equation

Name (Alias)	Units	Default	Description
F1	V/cm	0.0	Critical gate-bulk electric field at which mobility reduction becomes significant.
UEXP (F2)		0.0	Mobility exponent. Use a factor of 0.36 for n-channel and 0.15 for p-channel.
UTRA (F3)	factor	0.0	Source-drain mobility reduction factor.
VMAX (VMX)	cm/s	0.0	Maximum drift velocity of carriers. The VMAX setting determines which calculation scheme vdsat uses. Zero indicates an infinite value.

The mobility reduction equation (MOB=2)[\[3\]](#) produces good results for high gate voltages and drain fields with constant back-bias. Typically, you can use this equation for p-channel pull-ups and n-channel pull-downs. The VMAX value selects the proper vdsat calculation scheme. MOB=2 (SPICE default) corresponds to MSINC UN=2.

$$factor = \left[\frac{F1 \cdot \epsilon_{si}}{COX \cdot (vgs - vbi - F3 \Rightarrow vde)} \right]^{F2}$$

vde is the same in this equation as in the MOB=1 equation.

MOB=3

Table 15 MOB=3 Normal Field Equation

Name (Alias)	Units	Default	Description
F1	1/V	0.0	Low-field mobility multiplier
F4		1.0	Mobility summing constant
UEXP (F2)		0.0	Mobility exponent
UTRA (F3)	1/V	0.0	High-field mobility multiplier
VF1	V	0.0	Low to high field mobility (voltage switch)

This equation is the same as MSINC UN=1:

$$(vgs - vth)^{F2}$$

≤VF1:

$$factor = \frac{1}{F4 + F1 \cdot (vgs - vth)^{F2}}$$

If UPDATE=0, and $(vgs - vth)^{F2} > VF1$:

$$factor = \frac{1}{F4 + F3 \cdot (vgs - vth)^{F2}}$$

If UPDATE=1, 2 and $(vgs - vth)^{F2} > VF1$:

$$factor = \frac{1}{F4 + (F1 - F3) \cdot VF1 + F3 \cdot (vgs - vth)^{F2}}$$

MOB=4

Table 16 MOB=4 and MOB=5 Universal Field Mobility Reduction

Name (Alias)	Units	Default	Description
ECRIT	V/cm	0.0	Critical electric drain field for mobility reduction. Zero indicates an infinite value.
F1	V/cm	0.0	Source-drain mobility reduction field (typical values are 1e4 to 5e8).
MOB		0.0	Selects a mobility equation: <ul style="list-style-type: none"> Set MOB=4 for the critical field equation. Set MOB=5 for the critical field equation with an independent drain field.
UEXP (F2)	$1/V^{1/2}$	0.0	Bulk mobility reduction factor (typical values are 0 to 0.5).
UTRA (F3)	V/cm	0.0	Critical electric drain field for mobility reduction.

The MOB=4 equation is the same as the MSINC UN=3 equation.

MOB=5

The MOB=5 equation is the same as MOB=4, except that F3 substitutes for ECRIT in the v_c expression.

The MOB=5 equation provides a better fit for CMOS devices in the saturation region. Do not specify a VMAX value, because the mobility equation calculates the velocity saturation.

$$factor = \frac{1}{1 + \frac{COX}{F1 \cdot \epsilon_{ox}} \cdot (v_{gs} - c_{th}) + \frac{v_{de}}{v_c} + F2 \cdot (v_{sb} + PHI)^{1/2}}$$

- If MOB=4, then

$$v_c = ECRIT \cdot Leff$$

- If MOB=5, then

$$v_c = F3 \cdot Leff$$

Note: If you use the alternate saturation model, vde is different for UPDATE=0 than it is for UPDATE=1, 2.

MOB=6, 7 Modified MOB=3:

This mobility equation is the same as MOB=3, except that the equation uses VTO instead of vth. If you specify MOB=6, the following equation modifies the ids current:

$$ids = \frac{ids}{1 + F1 \cdot \left(vgs - vth - \frac{vde}{2} \right) + \frac{UTRA}{Leff} \cdot vde}$$

Channel Length Modulation

The basic MOSFET current equation for ids describes a parabola, where the peak corresponds to the drain-to-source saturation voltage (vdsat). Long-channel MOSFETs generally demonstrate ideal behavior. For vds voltages greater than vdsat, ids current does not increase. As channel length decreases, current in the saturation region continues to increase.

The simulator models this increase in current as a decrease in the effective channel length. Except for CLM=5 and 6, this model calculates the channel length modulation equations only when the device is in the saturation region.

The Level 6 MOSFET model provides several channel length modulation equations; all (except CLM=5) modify the ids equation:

$$ids = \frac{ids}{1 - \frac{\Delta L}{Leff}}$$

ΔL is the change in channel length due to MOSFET electric fields.

The CLM model parameter designates the channel length modulation equation for the Level 6 MOSFET device model:

Parameter	Description
CLM=0	No channel length modulation (default)
CLM=1	One-sided step depletion layer drain field equation
CLM=2	Frohman's electrostatic fringing field equation

Parameter	Description
CLM=3	One-sided step depletion layer drain field equation with carrier velocity saturation
CLM=4	Wang's equation: linearly graded depletion layer
CLM=5	Synopsys channel length modulation
CLM=6	Synopsys ΔL equations

The following sections describe these equations and the associated model parameters.

CLM=0 No Channel Modulation—Default

$$\Delta L = 0$$

This is the default channel length equation, representing no channel length modulation; it corresponds to MSINC GDS=0 . 0.

CLM=1

Table 17 CLM=1 Step Depletion Equation for MOSFET Level 6

Name (Alias)	Units	Default	Description
KL		0.0	Empirical constant (saturation voltage)
LAMBDA (LAM, LA)	cm/V ^{1/2}	1.137e-4	Channel length modulation. If you do not specify s, simulation calculates it from NSUB. The default LAMBDA corresponds to the default NSUB value.

$$\Delta L = LAMBDA \cdot (vds - vdsat)^{1/2} \cdot \left(\frac{vdsat}{vdsat} \right)^{KL}$$

If you do not specify LAMBDA, simulation calculates it as:

$$LAMBDA = \left(\frac{2 \cdot \epsilon_{si}}{q \cdot DNB} \right)^{1/2}$$

This is a one-sided step depletion region formulation by Grove: ΔL varies with the depletion layer width, which is a function of the difference between the effective saturation voltage (v_{dsat}) and the drain-to-source channel voltage (v_{ds}). Typically, you can use this equation for long channels and high dopant concentrations. This corresponds to $GDS=1$ in MSINC.

CLM=2

Table 18 CLM=2 Electrostatic Fringing Field

Name (Alias)	Units	Default	Description
A1		0.2	First fringing field factor, gate-drain
A2		0.6	Second fringing field factor, gate- v_{dsat}

$$\Delta L = \frac{\epsilon si}{COX} \cdot \frac{v_{ds} - v_{dsat}}{A1 \cdot (v_{ds} - v_{gs} + v_{bi}) + A2 \cdot (v_{gs} - v_{bi} - v_{dsat})}$$

You can use the fringing field equation or electrostatic channel length reduction (developed by Frohman-Bentchkowski) to model short-channel enhancement transistors. In MSINC, the equivalent equation is $GDS=2$.

CLM=3

Table 19 CLM=3 Carrier Velocity Saturation for MOSFET Level 6

Name (Alias)	Units	Default	Description
KA		1.0	vds scaling factor for velocity saturation.
KCL		1.0	Exponent for vsb scaling factor.
KU		0.0	Velocity saturation switch. If KU ≤1, simulation uses the standard velocity saturation equation.
LAMBDA (LAM, LA)	cm/V ^{1/2}	1.137e-4	Channel length modulation. If you do not specify LAMBDA, simulation calculates it from NSUB. The default LAMBDA corresponds to the default NSUB value.
MAL		0.5	vds exponent for velocity saturation.
MCL		1.0	Short channel exponent.

$$\Delta L = vfu^{(2 \cdot MCL)} \cdot LAMBDA$$

$$[(vds - vfa) \Rightarrow vsat + KCL \cdot vsb + PHI]^{1/2} - (KCL \cdot vsb + PHI)^{1/2}]$$

This equation is an extension of the first depletion layer equation, CLM=1. It includes effects of carrier velocity saturation, and source-to-bulk voltage (vsb) depletion layer width. It represents the basic ISPICE equation. See [Alternate DC Model \(ISPICE model\) on page 111](#) for definitions of vfa and vfu.

CLM=4

Table 20 CLM=4, Wang's Equation for MOSFET Level 6

Name (Alias)	Units	Default	Description
A1	m	0.2	Junction depth: A1scaled=A1 · SCALM
DND	cm ⁻³	1e20	Drain diffusion concentration

Linearly Graded Depletion Layer:

$$\Delta L = \left[\frac{2.73e5 \cdot A1scaled}{DNB \cdot \ln\left(\frac{DND}{DNB}\right)} \right]^{1/3} \cdot [(vds - vdsat + PHI)^{1/3} - PHI^{1/3}]$$

Wang's equation can include junction characteristics to calculate the channel length modulation. The equation assumes that the junction approximates a linearly-graded junction, and provides a value of 0.33 for the exponent. This equation is similar to MSINC_{GDS=3}.

CLM=5

Table 21 CLM=5, Channel Length Modulation for MOSFET Level 6

Name (Alias)	Units	Default	Description
LAMBDA	amp/V ²	0	Constant coefficient
VGLAM	1/V	0	Constant coefficient

If CLM=5, the ids current increases by idssat:

$$idssat = \frac{weff}{Leff} \cdot LAMBDA \cdot vds \cdot (vgs - vth) \cdot [1 + VGLAM \cdot (vgs - vth)]$$

$$ids = ids + idssat$$

Note: The equation adds the idssat term to ids in all regions of operation. Also, LAMBDA is a function of the temperature.

CLM=6

Table 22 CLM=6, ΔL Equation for MOSFET Level 6

Name (Alias)	Units	Default	Description
LAMBDA	$1/V^{KL}$	0	vds coefficient
LAM1	1/m	0	Channel length coefficient
KL		0	vds exponent
VGLAM	1/V	0	Gate drive coefficient

Unlike the other CLM values, this equation calculates the channel length modulation (ΔL) in all regions of operations, and uses it to modify the ids current.

$$\Delta L = \frac{Leff \cdot LAMBDA \cdot vds^{KL} \cdot [1 + VGLAM \cdot (vgs - vth)]}{1 + LAM1 \cdot Leff}$$

$$ids = \frac{ids}{1 - \frac{\Delta L}{Leff}}$$

Note: LAMBDA is a function of the temperature.

ASPEC Compatibility

To make MOSFET models compatible with ASPEC, specify ASPEC=1 in the .OPTION statement and LEVEL=6 in the associated MOSFET model statement.

If you assign the element parameters without keynames, specify the parameters in the same sequence as in the general format. The Level 6 MOSFET model assigns parameters in the order that you list them in the element statement. If parameter names are also element keynames, simulation reports errors.

If you use the ASPEC option, several program variations occur. The LEVEL model parameter is set to 6.

Note: Setting `LEVEL=6` in the model does not invoke ASPEC.

MOSFET control option `WL=1`

General control options `SCALE=1e-6`

`SCALM=1e-6`

ASPEC sets the `SCALE` and `SCALM` options so it effectively changes the default units in parameters that these options affect. Parameter values must be consistent with these scaling factors.

`LEVEL` = 6

`ACM` = 1

`CJ` = 0.0

`IS` = 0.0

`NSUB` = 1e15

`PHI` = 1 · Φ_f (the Fermi potential)

`TLEV` = 1

`TLEVC` = 1

Note: Do not calculate `NSUB` from `GAMMA`, if `UPDATE=1` or 2.

`TLEV` (`TLEVC`) selects the ASPEC method of updating temperatures for the `CJ`, `CJSW`, `PB`, `PHP`, `VTO`, and `PHI` parameters.

Note: If you explicitly enter `PHI`, this model does not update it for temperature. `SCALM` does not affect how simulation scales parameters for the ASPEC mode. If you specify `SCALM` when you use ASPEC, the Level 7 MOSFET model generates an error stating that it ignores `SCALM`.

LEVEL 7 IDS Model

The LEVEL 7 model is the same as the LEVEL 6 model except for the Φ_s value.

If you specify Φ_s , then:

For LEVEL=6

$$\Phi_s = \frac{\Phi_s}{2}, \text{ where } \Phi_s$$

is the surface potential.

For LEVEL=7

$$\Phi_s = \Phi_s$$

To transform a LEVEL 7 equation to LEVEL 6, make the following substitution:

$$\Phi_s \rightarrow 2 \cdot \Phi_s$$

To transform a LEVEL 6 model into a LEVEL 7 model, make the following substitution:

$$\Phi_s(\text{Level } 7) = \Phi_s(\text{Level } 6) / 2$$

LEVEL 8 IDS Model

The LEVEL 8 MOSFET model, derived from research at Intersil and General Electric, is an enhanced version of the LEVEL 2 ids equation. LEVEL 2 differs from LEVEL 8 in the following areas:

- effective substrate doping
- threshold voltage
- effective mobility
- channel length modulation
- subthreshold current.

LEVEL 8 Model Parameters

MOSFET Level 8 uses the generic MOSFET model parameters described in [Chapter 2, Common MOSFET Model Parameters](#). This level also uses the parameters described in this section, which apply only to MOSFET Level 8.

Table 23 Channel Length Modulation Parameters, MOSFET Level 8

Name (Alias)	Units	Default	Description
A1		0.2	Channel length modulation exponent (CLM=8)
CLM		7	Channel length modulation equation selector
LAM1	1/m	0.0	Channel length modulation length correction
LAMBDA (LAM, LA)		0.0	Channel length modulation coefficient

LEVEL 8 Model Equations

This section lists the LEVEL 8 model equations.

IDS Equations

LEVEL 8 ids equations are the same as in the LEVEL 2 model (see [LEVEL 2 Model Equations on page 70](#)).

Effective Channel Length and Width

The Level 8 model calculates the effective channel length and width from the drawn length and width (see [LEVEL 2 Model Equations on page 70](#)).

Effective Substrate Doping, n_{sub}

The $SNVB$ model parameter varies the substrate doping concentration linearly as a function of v_{sb} :

$$n_{sub} = NSUB + SNVB \cdot v_{sb}$$

The preceding equation computes γ , ϕ , and x_d parameters for n_{sub} :

$$\gamma = \frac{\sqrt{2 \cdot \epsilon_{si} \cdot q \cdot n_{sub}}}{COX}$$

$$\Phi = 2 \cdot v_t \cdot \ln\left(\frac{n_{sub}}{n_i}\right)$$

$$x_d = \sqrt{\frac{2 \cdot \epsilon_{si}}{q \cdot n_{sub}}}$$

If SNVB is zero, then $\gamma = \text{GAMMA}$. You can adjust the γ value for the short-channel effect the same way as in the LEVEL 2 model. NSUB calculates the ϕ value.

Threshold Voltage, vth

ETA specifies the threshold voltage reduction due to the potential barrier lowering effect.

$$v_{bi} = VTO - g \Rightarrow \sqrt{\Phi} - \frac{8.14e-22 \cdot ETA}{COX \cdot L_{eff}^3} p_{vds} + (\eta - 1) \cdot (v_{sb} + \Phi)$$

$$v_{th} = v_{bi} + g \cdot \sqrt{v_{sb} + \Phi}$$

Modify γ for the short-channel effect, the same as in the LEVEL 2 model to obtain the effective γ .

Saturation Voltage vdsat

Level 8 computes the vsat saturation voltage the same way as in the LEVEL 2 model. This model includes the carrier velocity effect only if ECRIT is greater than zero.

ECRIT > 0:

$$v_{dsat} = v_{sat} + v_c - \sqrt{v_{sat}^2 + v_c^2}$$

The following equation calculates the v_c value used in the preceding equation:

$$v_c = ECRIT \cdot L_{eff}$$

ECRIT ≤ 0 or MOB=7:

$$v_{dsat} = v_{sat}$$

This model computes vsat as in the LEVEL=2 model (see [Saturation Voltage, v_{dsat} on page 71](#)).

Effective Mobility, u_{eff}

The MOB mobility equation selector controls the mobility reduction equations. In the LEVEL 8 model, set MOB to 2, 3, 6, or 7. Default=6.

MOB=2 Mobility Reduction

$$u_{eff} = UO \cdot \left[\frac{\epsilon_{se} \cdot UCRIT}{COX \cdot (vgs - vth - UTRA \Rightarrow de)} \right]^{UEXP}$$

MOB=3 Mobility Reduction

$$u_{eff} = \frac{UO}{1 + \frac{2.1e-8 \cdot (vgs + vth + egfet - \Phi)}{6 \cdot TOX}}$$

In the preceding equation, egfet is the silicon energy gap at the analysis temperature:

$$egfet = 1.16 - \frac{7.02e-4 \cdot t^2}{t + 1108}$$

In the preceding equation, t is the temperature in degrees Kelvin.

If VMAX>1:

$$u_{eff} = \frac{u_{eff}}{1 + \frac{u_{eff}}{VMAX \cdot L_{eff}} \cdot vde}$$

MOB=6 Mobility Reduction

For UEXP>0:

$$\text{If } (vgs - vth) > \frac{\epsilon_{si} \cdot UCRIT}{COX}, \text{ then } u_{eff} = \frac{UO \cdot \left[\frac{\epsilon_{si} \cdot UCRIT}{COX \cdot (vgs - vth)} \right]^{UEXP}}{1 + \frac{UTRA}{L_{eff}} \cdot vde}$$

$$\text{Otherwise, } u_{eff} = \frac{UO}{1 + \frac{UTRA}{L_{eff}} \cdot vde}$$

For UEXP=0:

$$u_{eff} = \frac{UO}{[1 + UCRIT \cdot (vgs - vth)] \cdot \left(1 + \frac{UTRA}{L_{eff}} \cdot vde\right)}$$

UCRIT for UEXP=0 has a dimension of (1/V).

MOB=7 Mobility Reduction

$$u_{eff} = \frac{UO}{1 + UTRA \cdot \left(vgs - vbi - \eta \Rightarrow \frac{vde}{2} + \frac{body}{vde}\right)}$$

The following equation calculates the body value used in the preceding equation:

$$body = \frac{2}{3} \cdot \gamma \cdot [(vde + vsb + \Phi)^{3/2} - (vsb + \Phi)^{3/2}]$$

Channel Length Modulation

The CLM equation selector controls the channel length modulation equations. In the LEVEL 8 model, set CLM to 6, 7, or 8. Default=7.

CLM=6 SPICE Channel Length Modulation

If LAMBDA=0:

$$\lambda = \frac{xd}{leff \cdot vds} \cdot \sqrt{\frac{vds - vdsat}{4}} + \sqrt{1 + \left(\frac{vds - vdsat}{4}\right)^2}$$

Otherwise, $\lambda = LAMBDA$. Then: $\Delta L = \frac{\lambda \cdot L_{eff} \cdot vds}{1 + LAM1 \cdot L_{eff}}$

Note: The LEVEL 2 model has no LAM1 term.

This model modifies the current for the channel length modulation effect in the entire regions:

$$ids = \frac{ids}{1 - \frac{\Delta L}{L_{eff}}}$$

CLM=7 Intersil Channel Length Modulation

If CLM=7, this model computes ΔL only for the saturation region.

$$vds > vdsat$$

$$\Delta L = \frac{LAMBDA \cdot L_{eff}}{1 + LAM1 \cdot L_{eff}} \cdot (vds - vdsat)$$

$$ids = \frac{ids}{L - \frac{\Delta L}{L_{eff}}}$$

CLM=8

If CLM=8, this model computes ΔL only for the saturation region.

$$vds > vdsat$$

$$\Delta L = \frac{L_{eff}}{1 + \frac{(1 + LAM1 \cdot L_{eff}) \cdot (1 + vde)^{A1}}{LAMBDA \cdot (vds - vde)}}$$

$$ids = \frac{ids}{1 - \frac{\Delta L}{L_{eff}}}$$

Subthreshold Current Ids

The LEVEL 8 model has different subthreshold current equations, depending on the value of the CAV model parameter.

Define:

$$fast = vt \cdot \left[\eta + \frac{q \cdot NFS}{COX} + \frac{\gamma}{2 \cdot (vsb + \Phi)^{1/2}} + \frac{\epsilon_{si} \cdot q \cdot SNVB \cdot \sqrt{vsb + \Phi}}{\gamma \cdot COX^2} \right]$$

For CAV $\neq 0$

$$von = vth + CAV \cdot fast$$

Subthreshold Region, $vgs < von$

If $vgs > vth$:

$$ids = ids(von, vde, vsb) \cdot e^{\left(-1 - \frac{CAV}{2}\right)} \cdot e^{\left\{ \left[\frac{1}{fast} - \frac{(CAV-2) \cdot (vgs - vth)}{2 \cdot CAV^2 \cdot fast^2} \right] (vgs - vth) \right\}}$$

If $vgs \leq vth$

$$ids = ids(von, vde, vsb) \cdot e^{\left(-1 - \frac{CAV}{2}\right)} \cdot e^{\left(\frac{vgs - vth}{fast}\right)}$$

For CAV=0

If CLM=8: $von = vth + 3 \cdot fast$

Otherwise, $von = vth + 2 \cdot fast$

Subthreshold Region, $vgs < von$

$$ids = ids(von, vde, vsb) \cdot e^{\left(\frac{vgs - von}{fast}\right)}$$

If WIC=3, the next equation calculates the ids subthreshold current:

$$ids = ids(vgs, vde, vsb) + isub(N0eff, NDeff, vgs, vds)$$

N0eff and NDeff are functions of effective device width and length.

LEVEL 27 SOSFET Model

MOSFET Level 27 is a three-terminal silicon-on-sapphire (SOS) FET transistor model.[4] This SOSFET model is based on a sapphire insulator that isolates the substrate and models the behavior of SOS devices more accurately than standard MOSFET models with physically unreal parameter values. The SOSFET model also includes a charge conservation model (based on the Ward and Dutton model).

Because the defaults of the SOSFET model parameters depend on the channel length, you must specify the `SOSLEV` model parameter to select either the 5 μm or 3 μm processing model.

`SOSLEV=1` selects the 5 μm model; otherwise, this model automatically uses the 3 μm value, including the second-order effects (default=3 μm).

Note: This model does not include bulk nodes. If you specify bulk nodes, simulation ignores them.

This model does not use the `ACM` model parameter, because it does not include any junction diodes. Also, the only value that the `CAPOP` model parameter accepts is 7. Seven is its own charge conservation model, which you cannot use in other MOSFET models.

Temperature compensation equations for the `VTO` and `UO` SOSFET model parameters are the same as those in the MOSFET model.

Note: This model includes a special option for bulk nodes for silicon on sapphire. In the model definition, if you specify -1 for the bulk node, this model generates a special node for each element. This bulk node is named in the form, `B#<element_name>`, where the element name is the name of the defined element. Use this name in any statement, such as a `.PRINT` statement to refer to the bulk node in the element.

Syntax

```
.MODEL mname PMOS <LEVEL=27> <SOSLEV=val> <pname1=val1>
.MODEL mname NMOS <LEVEL=27> <SOSLEV=val> <pname=val1>
```

You can use this `.MODEL` syntax to include a MOSFET Level 27 model in your HSPICE netlist. For a general description of the [.MODEL](#) statement, see the *HSPICE Reference Manual: Commands and Control Options*.

Parameter	Description
<code>mname</code>	Model name.
<code>PMOS</code>	Identifies a p-channel MOSFET model.
<code>NMOS</code>	Identifies an n-channel MOSFET model.
<code>LEVEL</code>	Model level selector.
<code>SOSLEV</code>	Selects the processing model. If you set <code>SOSLEV=1</code> , the default=5 μ m. The automatic default=3 μ m.
<code>pname</code>	Parameter model.

LEVEL 27 Model Parameters

Table 24 5- μm Model Parameters

Name (Alias)	Units	Default	Description
CGDO	F/m		Gate-drain overlap capacitance per unit channel width. Default=3.1e-10 (n-type), 2.2e-10 (p-type).
CGSO	F/m		Gate-source overlap capacitance per unit channel width. Default=3.1e-10 (n-type), 2.2e-10 (p-type).
LD	m		Lateral diffusion. The default=0.6 μ (n-type), 0.3 μ (p-type).
RSH	ohm/sq		Drain and source diffusion sheet resistance. The default=25 (n-type), 100 (p-type).
SOSLEV		1	Model index.
TOX	m	7.0e-8	Oxide thickness.
UO	cm ² /(V·s)		Surface mobility. Default=350 (n-type), 220 (p-type).
VTO	V		Threshold voltage. Default=1.25 (n-type), -1.25 (p-type).

Table 25 3- μm Model Parameters

Name (Alias)	Units	Default	Description
A	m/V	0.1 μm	Channel length shortening coefficient (2nd effect)
ALPHA	V/m		Threshold voltage length dependence. Default=0.15 μ (n-type), 0.18 μ (p-type).
CAPOP		7	Capacitance model selector.

Table 25 3- μ m Model Parameters

Name (Alias)	Units	Default	Description
CGDO	F/m		Gate-drain overlap capacitance per unit channel width. Default=4.6e-10 (n-type), 3.6e-10 (p-type).
CGSO	F/m		Gate-source overlap capacitance per unit channel width. The default=4.6e-10 (n-type), 3.6e-10 (p-type).
EC	V/m		Critical electric field for velocity saturation (2nd effect). The default=3.0e6 (n-type), 7.5e6 (p-type).
FB			Body effect coefficient (2nd effect). Default=0.15 (n-type), 0 (p-type).
LD	m		Lateral diffusion. Default=0.3 μ (n-type), 0.2 μ (p-type).
LEVEL		27	Model level selector.
RSH	ohm/sq		Drain and source diffusion sheet resistance. Default=25 (n-type), 80 (p-type).
SOSLEV		2	Model index.
THETA	1/V		Mobility degradation coefficient (2nd effect). Default=0.055 (n-type), 0.075 (p-type).
TOX	m	3.4e-8	Oxide thickness.
UO	cm ² /(V·s)		Surface mobility. Default=370 (n-type), 215 (p-type).
VTO	V		Threshold voltage. Default=0.83 (n-type), -0.74 (p-type).

Example

This example is based on demonstration netlist m127iv.sp, which is available in directory \$<installdir>/demo/hspice/mos:

```

*file: ml27iv.sp ids and vgs curves for nmos and pmos sossfets.
*mosfet level=27 p and n

.options acct list nopage nomod post
.op
.dc vddn 0 5.0 .1

* n-channel ids curves (vd=0-&lt;&lt;5, vg=1,2,3,4,5)
.print dc i(vn1) i(vn2) i(vn3) i(vn4) i(vn5)
.probe dc i(vn1) i(vn2) i(vn3) i(vn4) i(vn5)

* p-channel ids curves (vd=0-&lt;&lt;-5,vg=-1,-2,-3,-4,-5)
.print dc i(vp1) i(vp2) i(vp3) i(vp4) i(vp5)
.probe dc i(vp1) i(vp2) i(vp3) i(vp4) i(vp5)

* v g s curves
.print dc i(vn6) i(vp6)
.probe dc i(vn6) i(vp6)

* n-channel lx7=gm(vd=5, vg=0-&lt;&lt;5, vs=0)
* n-channel lx8=gd (vd=0-&lt;&lt;5, vg=5, vs=0)
* n-channel lx9=gb (vd=5, vg=5, vs=0)
.print dc lx7 (m21) lx8(m5) lx9(m31)

* p-channel lx7=gm (vd=0, vg=0-&lt;&lt;-5, vs=-5)
* p-channel lx8=gd (vd=0-&lt;&lt;-5, vg=-5, vs=-5)
* p-channel lx9=gb (vd=0, vg=0, vs=-5)
.print dc lx7(m22) lx8(m15) lx9(m32)
*
vddn 99 0 5.0
epd 98 0 99 0 -1

v1 1 0 1
v2 2 0 2
v3 3 0 3
v4 4 0 4
v5 5 0 5
v11 11 0 -1
v12 12 0 -2
v13 13 0 -3
v14 14 0 -4
v15 15 0 -5
*
vn1 99 31 0
vn2 99 32 0
vn3 99 33 0
vn4 99 34 0
vn5 99 35 0

```

Chapter 3: MOSFET Models: LEVELs 1 through 40

LEVEL 27 SOSFET Model

```
m1 31 1 0 n1 8u 8u
m2 32 2 0 n1 8u 8u
m3 33 3 0 n1 8u 8u
m4 34 4 0 n1 8u 8u
m5 35 5 0 n1 8u 8u
*
vp1 98 41 0
vp2 98 42 0
vp3 98 43 0
vp4 98 44 0
vp5 98 45 0

m11 41 11 0 p1 8u 8u
m12 42 12 0 p1 8u 8u
m13 43 13 0 p1 8u 8u
m14 44 14 0 p1 8u 8u
m15 45 15 0 p1 8u 8u
*
* g m test
vn6 5 36 0
vp6 0 46 0
m21 36 99 0 n1 8u 8u
m22 46 98 15 p1 8u 8u
*
* g m b test
vn7 5 37 0
vp7 0 47 0
m31 37 5 0 98 n1 8u 8u
m32 47 0 15 99 p1 8u 8u
*
.model n1 nmos level=27 soslev=2
+vto=0.814 tox=0.34e-7 theta=0.55e-1
+fb=0.15 ec=0.3e7 a=0.1e-6
+uo=370 cgso=0.46e-9 cgdo=0.46e-9
+rsh=25 ld=0.3e-6
*
.model p1 pmos level=27 soslev=2
+vto=-0.7212 tox=0.34e-7 theta=0.75e-1
+fb=0.0 ec=0.75e7 a=0.1e-6
+uo=215 cgso=0.36e-9 cgdo=0.36e-9
+rsh=80 ld=0.2e-6
*
.end
```

Non-Fully Depleted SOI Model

Several MOSFET models are currently available for SOS/SOI applications. The 3-terminal SOS model (`LEVEL=27`) is stable for circuit design usage, but has some limitations. This model does not provide for depleted bulk. Use it only with applications that are not fully depleted and that do not consider kink effects.

The following circuit example is a 4-terminal SOI model for incompletely depleted bulk with the kink effect. Its sub-circuit allows a parasitic capacitance to the substrate. In this example, the bulk is the region under the channel. This model assumes that the substrate is the conductive layer under the insulator.

- For SOI, the insulator is usually silicon dioxide and the substrate is silicon.
- For SOS, the insulator is sapphire and the substrate is the metal that contacts the back of the integrated circuit die.

Model Components

This model consists of the following subcomponents:

- Core IDS model: any level works because the impact ionization and weak inversion models are common to all DC levels. The example uses a `LEVEL=3` DC MOS model.
- Subthreshold model: the `WIC=3` model parameter allows the older models to use the more advanced models found in the BSIM (`LEVEL=13`, `LEVEL=28`) models. The `N0` model parameter should have a typical value around 1.0.
- Impact ionization model: set `ALPHA` and `VCR` parameters to enable the impact ionization model, which is available to all MOS DC equations. Typical values are `ALPHA=0.1` and `VCR=18`.
- Charge conservation gate cap model (`CAPOP=9`, `XQC=.4`) prevents the floating bulk node from obtaining extreme values.
- The automatic periphery diode area calculation method (`ACM`) is set to 3 to automatically calculate the source and drain resistances and diode junction leakage, and the capacitance. (`ACM=3` `CJ=0` `CJSW=0` `CJGATE=4e-10` `JS=0` `JSW=1e-9` `LD=.1u` `HDIF=1.5u` `RS=40` `RD=40` `N=1`).

Note: These models assume that the source/drain diffusions extend to the buried oxide. The area part of the diode has no capacitance to bulk. However, the subcircuit includes linear capacitors to the substrate.

Obtaining Model Parameters

Use the optimizing capabilities in the Level 27 MOSFET model to obtain the core IDS model parameters.

Use the optimizer to obtain the core model, subthreshold, and impact ionization parameters. The subthreshold model selected is an improved BSIM type of model that was altered for the older models. The charge conservation model is more charge conserving than the original Ward-Dutton model in SPICE 2G6.

Calculating the automatic diode area and the resistance estimates the junction capacitance, saturation current, and resistance as a function of the transistor width. Use the `VNDS` and `NDS` parameters for a piecewise linear approximation to reverse the junction current characteristics.

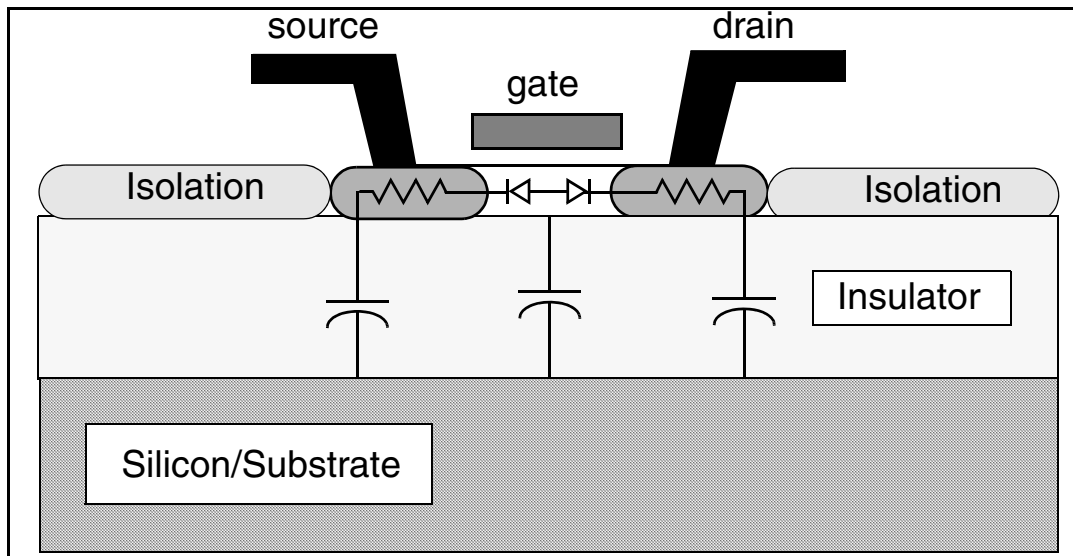


Figure 7 Non Fully Depleted SOI Model

Example

This example is based on demonstration netlist `ssoi.sp`, which is available in directory `$<installdir>/demo/hspice/mos`:

```
ssoi.sp LEVEL=3 floating bulk model
** non-fully depleted
* test 1st order soi model with floating substrate
.option nomod post
* substrate capacitance 3.45e-11 is for SiO2
.param t_sub_ox=.5u subcap='3.45e-11/t_sub_ox' hdif=1.5u
.global substrate
.dc vd 0 5 0.1 sweep vg 1.5 3.5 0.5
.print id=i(xm1.m) vds=v(d) vgs=v(g)
.param vds=0 vgs=0 vbs=0
vd d gnd vds
vg g gnd vgs
vs s gnd 0
vsub substrate gnd vbs
xm1 d g s nch w=50u L=5u
.macro nch d g s w=10u l=2u
* macro definition for fet+ parasitic cap to substrate
* assumes existence of undepleted bulk
m d g s b nch w=w L=L
cx1 d substrate c='w*2*hdif*subcap'
cx2 s substrate c='w*2*hdif*subcap'
cx3 b substrate c='w*L*subcap'
.eom
.model nch nmos LEVEL=3
+ lmin=.5u lmax=100u wmin=.5u wmax=500u $model selector
+ ld=0.1u wd=.15u xl=0 xw=0
$diffusion+photobias
+ acm=3 hdif=hdif rsh=30 rs=10k rd=10k $resistors
+ ldif=0.1u
$junction cap (ACM=3 (h9007 only) allows diode on gate edge
+ cj=0 cjsw=0 cgate=0.4e-9 mjsw=0.33 php=0.6
+ js=0 jsw=1e-9 n=1 vnds=.5 nds=1 $junction leakage
+ bex=-1.5 tcv=2m $temperature
+ tox=200 capop=9 xqc=.4 meto=0.08u $gate cap
+ alpha=0.1 vcr=18 $impact ionization
+ vto=0.7 phi=1 gamma=1 $threshold
+ eta=10 xj=0.1u $threshold
+ wic=3 n0=0.9 nd=0 $subthreshold
+ uo=400 theta=1m $dc mobility
+ vmax=100k kappa=0 $dc saturation
.end
```

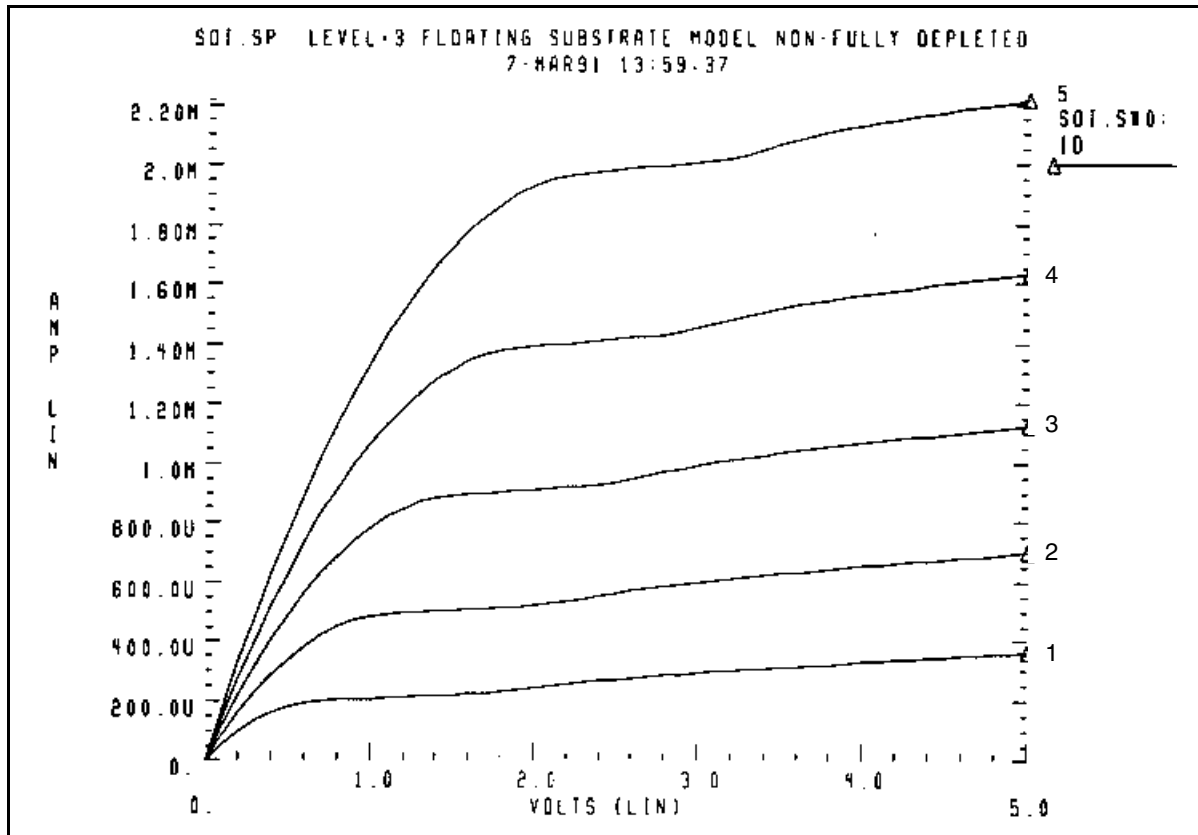


Figure 8 LEVEL 3 Floating Bulk Model

Fully Depleted SOI Model Considerations

Fully depleted transistors require additional modeling equations. The first-order effects are:

- Threshold sensitivity to the substrate.
- No kink current.
- Silicon thickness limits the minimum depletion capacitance.

Lack of these effects does not seriously affect an inverter, because the source-to-substrate voltage does not move. Digital circuits with good gate drive are not seriously affected, because a large gate voltage renders a small V_{th} shift to a small change in the I_{DS} current.

The substrate threshold sensitivity can affect circuits such as analog amplifiers that include transistors at back-bias and low gate voltages.

LEVEL 38 IDS: Cypress Depletion Model

The LEVEL 38 Cypress Depletion MOSFET model (Cypress Semiconductor Corporation) is a further development of the Synopsys Level 5 MOSFET device model. Level 38 features:

- BSIM-style length and width sensitivities
- Degraded body effect at high substrate bias (second GAMMA)
- Empirical fitting parameters for I_{ds} current calculations in the depletion mode of operations
- A comprehensive surface mobility equation
- Drain-induced barrier lowering

At the default parameter settings, the LEVEL 38 model is basically backwards-compatible with LEVEL 5 /ZENH=0.0 with the exception of the surface mobility degradation equation (see the discussion on the next page). Refer to the documentation for LEVEL 5 for the underlying physics that forms the foundation for the Huang-Taylor construct.

In LEVEL 38, the temperature compensation for threshold is ASPEC-style, concurring with the default in LEVEL 5. This section describes the model parameters that are unique to this depletion model. It also describes additional temperature compensation parameters.

LEVEL 38 lets you use all Synopsys device model capacitance options (CAPOP). CAPOP=2 is the default setting for LEVEL 38. If you set CAPOP=6 (AMI capacitance model), LEVEL 38 capacitance calculations become identical to those of LEVEL 5.

The ACM default parameter (ACM=0 in LEVEL 38) invokes SPICE-style parasitics. You can set ACM to 1 (ASPEC), or to 2 (Synopsys device model). All MOSFET models follow this convention.

You can use .OPTION SCALE with the LEVEL 5 MOSFET device model. However, you cannot use the SCALM option, due to the difference in units. You also cannot use the DERIV option.

You must specify the following parameters for MOS LEVEL 38: VTO (VT), TOX, UO (UB), FRC, ECV, and NSUB (DNB).

As with LEVEL 5, this model calculates the I_{ds} current according to three gate voltage regions:

- *Depletion Region, $v_{gs} - v_{fb} < 0$*

The low gate voltage region, which the bulk channel dominates.

- *Enhancement Region, $v_{gs} - v_{fb} > 0$, $v_{ds} < v_{gs} - v_{fb}$*

The region defined by high gate voltage and low drain voltage. In the enhancement region, both channels are fully turned on.

- *Partial enhancement region, $v_{gs} - v_{fb} > 0$, $v_{ds} > v_{gs} - v_{fb}$*

This region has high gate and drain voltages so the surface region is partially turned on, and the bulk region is fully turned on.

To better model depletion region operations, empirical fitting constants have been added to the original Huang-Taylor mechanism to account for the effects caused by nonuniform channel implants and also to make up for an oversight in the average capacitance construct[5]. The enhancement region uses a significantly more elaborate surface mobility model.

Body effect in LEVEL 38 is calculated in two regions[6].

- *Bulk body effect, $v_{sb} - v_{sbc} > 0$*

With sufficiently high (and negative) substrate bias (exceeding v_{sbc}), the depletion region at the implanted channel-substrate junction reaches the Si-oxide interface. Under such circumstances, the free carriers can accumulate only at the interface (as in an enhancement device) and the bulk doping level determines the body effect.

- *Implant-dominated body effect, $v_{sb} - v_{sbc} < 0$*

Before reaching v_{sbc} , and as long as the implant dose overwhelms the substrate doping level, the deeply-buried transistor (due to the implant) dominates the body effect of the depletion mode device. The γ body effect coefficient is proportional to both the substrate doping and to the first-order implant depth. In Level 38, the `BetaGam` empirical parameter amplifies the body effect due to deep implant.

Model parameters that start with L or W represent geometric sensitivities. In the model equations, three model parameters determine the zX quantity (X is the variable name):

- Large-and-wide channel case value (X).
- Length sensitivity (LX).
- Width sensitivity (WX).

The model calculates these parameters according to $zX=X+LX/Leff+WX/Weff$. For example, the following equation calculates the zero field surface mobility:

$$zUO = UO + \frac{LUO}{leff} + \frac{WUO}{weff}$$

Note: This model uses mostly micrometer units rather than meter units. Units and defaults are often unique in LEVEL 38. The finite difference method calculates the I_{ds} derivatives that define the gm, gds, and gmbs small signal gains. This model does not use the SCALM and DERIV options.

LEVEL 38 Model Parameters

MOSFET Level 38 uses the generic MOSFET model parameters described in [Chapter 2, Common MOSFET Model Parameters](#). This level also uses the parameters described in this section, which apply only to MOSFET Level 38.

Table 26 Capacitance Parameters

Name (Alias)	Units	Default	Description
AFC		1.0	Area factor for MOSFET capacitance
CAPOP		6	Gate capacitance selector
METO	μm	0.0	Metal overlap on gate

LEVEL 38 Model Equations

IDS Equations

Depletion, $vgs-vfb < 0$

$$ids = \beta 1 \cdot \left\{ q \cdot zKIO \cdot NI \cdot vde + cav \cdot \left[(vgs - vfb) \cdot vde - \frac{vde^2}{2} \right] \right\}$$

$$-\frac{2}{3} \cdot cav \cdot \bar{\gamma} \cdot [(vde + vsb + Phid)^{3/2} - (vsb + Phid)^{3/2}] + Icrit \left\{ \right.$$

Enhancement, vgs-vfb vde >0

$$ids = \beta 1 \cdot \left\{ q \cdot zKI0 \cdot NI \cdot vde - \frac{2}{3} cav \cdot \bar{\gamma} \cdot [(vde + vsb + Phid)^{3/2} - (vsb + Phid)^{3/2}] + Icrit \right\} + \beta \cdot \left[(vgs - vfb) \cdot vde - \frac{vde^2}{2} \right]$$

Partial Enhancement, vgs-vfb < vde

$$ids = \beta 1 \cdot \left\{ q \cdot zKI0 \cdot NI \cdot vde + cav \cdot \left[(vgs - vfb) \cdot vde - \frac{vde^2}{2} \right] - \frac{2}{3} \cdot cav \cdot \bar{\gamma} \cdot [(vde + vsb + Phid)^{3/2} - (vsb + Phid)^{3/2}] + Icrit \right\}$$

$$\left(\frac{1}{2} \beta - \frac{1}{2} \beta 1 cav \right) \cdot (vgs - vfb)^2$$

The following equations calculate values used in the preceding equations:

$$\beta 1 = \frac{zKBeta1}{1 + UHSAT \cdot \frac{vde}{Leff}} \cdot UH \cdot \frac{Weff}{Leff}$$

$$\beta = UBeff \cdot cox \cdot \frac{Weff}{Leff}, cav = \frac{cox \cdot cs}{cox + cs}$$

$$cs = \frac{KCS \cdot \epsilon Si}{DP \cdot 1e-4}, Phid = vt \cdot \ln\left(\frac{DNB \cdot nd}{ni^2}\right)$$

$$nd = \frac{NI \cdot 1e4}{DP}, vde = \min(vds, vdsat)$$

The temperature dependence of the mobility terms assume the ordinary exponential form:

$$UH(t) = UH(tnom) \cdot \left(\frac{t}{tnom} \right)^{TUH}$$

$$zUO(t) = zUO(tnom) \cdot \left(\frac{t}{tnom} \right)^{TUH}$$

The following equation calculates the continuity term at the body effect transition point:

$$I_{crit} = -\frac{2}{3} \cdot cav \cdot [(vde + vsbc + Phid)^{3/2} - (vsbc + Phid)^{3/2}] \cdot \gamma \cdot \left(\frac{1}{zBetaGam} - 1 \right)$$

This model uses the preceding equation if vsb>vsbc. Otherwise,

$$I_{crit} = 0$$

The following sections describe saturation voltage, threshold voltage, body effect transition voltage, and the γ body effect coefficient.

Threshold Voltage, vth

The V_{TO} model parameter, often called the “pinch-off,” is a zero-bias threshold voltage extrapolated from a large device operating in the depletion mode. The following equation calculates the effective pinch-off threshold voltage, including the device size effects and the terminal voltages:

$$vth = vfb - \beta d = vch - \bar{\gamma} = Phid + vsb)^{1/2} + vcrit]$$

The following equations calculate values used in the preceding equation:

$$vfb = zVTO - zETA \Rightarrow ds + \beta d \cdot (vch - \gamma_0 \Rightarrow Phid^{1/2})$$

$$vcrit = \left(\gamma - \frac{\gamma}{zBetaGam} \right) \Rightarrow Phid + vsbc)^{1/2}$$

for vsb > vsbc; 0 otherwise.

$$\beta d = \frac{UH \cdot cav}{zUO \cdot cox}, vch = \frac{q \cdot NI}{cav}$$

$$\gamma_0 = \frac{(2 \cdot \epsilon si \cdot q \cdot na1)^{1/2}}{cav}$$

$$na1 = \frac{nd \cdot DNB}{nd + DNB}, nd = \frac{NI}{DP \cdot 1e-4}$$

The following equation computes the effective γ , including small device size

effects: $\bar{\gamma} = \frac{\gamma}{zBetaGam}$ for $v_{sb} > v_{sbc}$, and $=\gamma$; otherwise,

$$\gamma = \gamma_0 \cdot (1 - scf) \cdot (1 + ncf)$$

The following equations calculate values used in the preceding equations:

If $SCM \neq 0$, then $scf = 0$; otherwise,

$$scf = \frac{XJ}{Leff} \cdot \left\{ \left[1 + \frac{2xd}{XJ} \cdot (SCM \cdot v_{ds} + v_{sb} + Phid)^{1/2} \right]^{1/2} - 1 \right\}$$

If $NWM \neq 0$, then $ncf = 0$; otherwise,

$$ncf = \frac{NWM \cdot xd \cdot (Phid)^{1/2}}{Weff}$$

This equation calculates the xd value used in the preceding equation:

$$xd = \left(\frac{2 \cdot \epsilon_{si}}{q \cdot DNB} \right)^{1/2}$$

The following equation calculates the body effect transition point:

$$V_{sbc} = \frac{qDP^2}{2\epsilon_{si}} \left(\frac{NI}{DP \cdot 1e-4} - DNB \right) + zDVSBC + TDVSBC - (t - t_{nom}) - Phid$$

If $v_{gs} \leq v_{th}$, this model inverts the surface and includes a residual DC current. If v_{sb} is large enough to make $v_{th} > v_{inth}$, then v_{th} is the inversion threshold voltage.

To determine the residual current, simulation inserts v_{inth} into the i_{ds} , v_{sat} , and mobility equation in place of v_{gs} (except for v_{gs} in the exponential term of the subthreshold current). The following equation computes the inversion threshold voltage (v_{inth}) at a specified v_{sb} :

$$v_{inth} = v_{fb} - \frac{q \cdot NI}{c_{ox}} - v_{sb} + DVIN - zETA \Rightarrow v_{ds}$$

Saturation Voltage, v_{dsat}

This equation determines the v_{sat} saturation voltage:

$$v_{sat} = v_{gs} - v_{fb} + v_{ch} + \frac{\gamma^2}{2} \cdot \left\{ 1 - \left[1 + \frac{4}{\gamma^2} \cdot (v_{gs} - v_{fb} + v_{ch} + v_{sb} + Phid) \right]^{1/2} \right\}$$

$$v_{dsat} = v_{sat}$$

Simulation modifies v_{sat} to include the carrier velocity saturation:

$$v_{dsat} = v_{sat} + v_c - (v_{sat}^2 + v_c^2)^{1/2}$$

The following equation calculates the v_c value used in the preceding equation:

$$v_c = ECV \cdot Le_{ff}$$

Mobility Reduction, UB_{eff}

The UB surface mobility depends on the terminal voltages:

$$UB_{eff} = \frac{1}{\frac{1}{z_{UO}} + \frac{(z_{FRC} + z_{VFRC} \cdot v_{de} + z_{BFRC} \cdot v_{sb}) \cdot (v_{gs} - v_{fb})}{TOX} + \frac{v_{de}}{VST \cdot Le} + z_{FSB} \cdot v_{sb}^{1/2}}$$

The following equations calculate Le for the preceding equation:

$$Le = Le_{ff}$$

Linear region

$$Le = Le_{ff} - \Delta L$$

Saturation region

At elevated temperatures, the following equation calculates the z_{FRC} value used in the preceding equation:

$$z_{FRC}(t) = z_{FRC}(t_{nom}) \cdot \left(\frac{t}{t_{nom}} \right)^{FRCEX}$$

ΔL is the channel length modulation effect, defined in the next section. v_{fb} assumes the role of v_{th} in the LEVEL 5 mobility equation. The degradation parameters are semi-empirical, and are grouped according to their (linearized) mathematical dependencies instead of their physical origin to better provide parameter extraction.[\[7\]](#)

Channel Length Modulation

To include the channel length modulation, modify the i_{ds} current:

$$i_{ds} = \frac{i_{ds}}{1 - \frac{\Delta L}{L_{eff}}}$$

The following equation calculates ΔL for the preceding equation:

$$\Delta L = 1e4 \cdot \left[\frac{2.73e3 \cdot XJ}{na1 \cdot \ln\left(\frac{1e20}{na1}\right)} \right]^{1/3} \cdot [(v_{ds} - v_{dsat} + PHI)^{1/3} - PHI^{1/3}]$$

ΔL is in microns, if XJ is in microns and $na1$ is in cm^{-3} .

Subthreshold Current, i_{ds}

If device leakage currents become important for operation near or below the normal threshold voltage, the model considers the subthreshold characteristics. In the presence of surface states, this equation determines the effective threshold voltage (v_{on}):

$$v_{on} = \max(v_{th}, v_{inth}) + fast$$

The following equation calculates the fast value used in the preceding equation:

$$fast = v_t \cdot \left[1 + \frac{q \cdot FSS}{c_{ox}} + \frac{\gamma}{2 \cdot (Phid + v_{sb})^{1/2}} \right]$$

If $v_{gs} < v_{on}$, then:

Partial Enhancement, $0 < v_{gs} - v_{fb} < v_{de}$

$$i_{ds} = \beta_1 \cdot \left\{ q \cdot z_{KIO} \cdot NI \cdot v_{de} + c_{av} \cdot \left[(v_{on} - v_{fb}) \cdot v_{de} - \frac{v_{de}^2}{2} \right] \right. \\ \left. - \frac{2}{3} \cdot c_{av} \cdot \bar{\gamma} \cdot [(v_{de} + v_{sb} + Phid)^{3/2} - (v_{sb} + Phid)^{3/2}] + I_{crit} \right\} \\ + \frac{1}{2} \cdot \left(\beta \cdot e^{\frac{v_{gs} - v_{on}}{fast}} - \beta_1 \Rightarrow c_{av} \right) \cdot (v_{on} - v_{fb})^2$$

Full Enhancement, $v_{gs}-v_{fb}-v_{de} > 0$

$$ids = \beta_1 \cdot \left\{ q \cdot z_{KIO} \cdot NI \cdot v_{de} - \frac{2}{3} \cdot cav \cdot \bar{\gamma} \cdot [(v_{de} + v_{sb} + Phid)^{3/2} - (v_{sb} + Phid)^{3/2}] + I_{crit} \right\} \cdot e^{\frac{v_{gs} - v_{on}}{fast}}$$

$$\beta \cdot \left[(v_{on} - v_{fb}) \cdot v_{de} - \frac{v_{de}^2}{2} \right] \cdot e^{\frac{v_{gs} - v_{on}}{fast}}$$

Depletion, $v_{gs}-v_{fb} < 0$

$$ids = \beta_1 \cdot \left\{ q \cdot z_{KIO} \cdot NI \cdot v_{de} + cav \cdot \left[(v_{gs} - v_{fb}) \cdot v_{de} - \frac{v_{de}^2}{2} \right] \right.$$

$$\left. - \frac{2}{3} \cdot cav \cdot \bar{\gamma} \cdot [(v_{de} + v_{sb} + Phid)^{3/2} - (v_{sb} + Phid)^{3/2}] + I_{crit} \right\} \cdot e^{\frac{v_{gs} - v_{on}}{fast}}$$

Example Model File

```
$ file Depstor.mod
.MODEL DEPSTOR NMOS LEVEL=38
* PARASITIC ELEMENTS
+ ACM=1
+ LD=0.15u WD=0.2u $ for LEFF AND WEFF
+ CJ=0.3E-16 MJ=0.4 PB=0.8 JS=2.0E-17 $ INTRINSIC DIODE
+ CJSW=0 MJSW=0.3
+ BULK=98 $ DEFAULT NODE FOR SUBSTRATE
* THRESHOLD
+ VTO=-2.5 LVT=-0.25 WVT=0
+ leta=0.02 eta=0.0 weta=0.0
+ TCV=0.003 $ TEMPERATURE COEFFICIENT
* MISC
+ DVIN=0.5 PHI=0.75
+ NFS=2e10 DNB=3.0E16
```

Mobility Model

```
+ UH=1300
+ UO=495 FRC=0.020 FSB=5e-5 VFRC=-1e-4 BFRC=-0
+ LUO=-100 LFRC=.03 LFSB=-1e-5 LVFRC=-.002 LBFR=-
1e-3
```

Chapter 3: MOSFET Models: LEVELs 1 through 40

LEVEL 40 HP a-Si TFT Model

```
+ WUO=-30 WFRC=-0.01 WFSB=5e-5 WVFRC=-0.00 + WBFRC=-
0.4e-3
+ KIO=.9 KBETA1=.5 LKIO=0.16 LKBETA1=-0.15
+ WKIO=0.0 WKBETA1=-0.0
+ BEX=-1.3 TUH=-1.0 Frcex=1.0
```

Body Effect

```
+ NWM=0.5 SCM=.1
+ DVSB=0.1 LDVSB=0 WDVSB=0
+ TDVSB=.002
+ BetaGam=0.9 LBetaGam=-.2 WBetaGam=.1
```

Saturation

```
+ ECV= 2.9 VST=8000 UHSAT=0
* CHANNEL LENGTH MODULATION
+ XJ=0.1
* OXIDE THICKNESS AND CAPACITANCE
+ TOX=165 CGSO=0 CAPOP=2
* CHANNEL IMPLANT
+ NI=1.5e12 KCS=3 DP=0.25
* .END
```

LEVEL 40 HP a-Si TFT Model

The Synopsys Level 40 MOSFET device model represents a Hewlett-Packard amorphous silicon thin-film transistor model.

MOSFET Level 40 uses only the generic MOSFET model parameters described in [Chapter 2, Common MOSFET Model Parameters](#).

Using the HP a-Si TFT Model

To use the HP a-Si TFT model:

1. Set `LEVEL=40` to identify the model as the HP a-Si TFT model.
2. Default value for `L` is 10 μ m, and the default value for `W` is 40 μ m.
3. Use the “M” designation for MOSFET rather than the “A” designation for a-Si TFT in the netlist.

4. Use the “NMOS” or “PMOS” designation for device type rather than the “NAT” or “PAT” designation.

Note: Because of the unavailability of p-channel TFTs, PMOS model testing has been limited.

5. LEVEL 40 is a three-terminal model. It lacks bulk nodes so simulation does not append any parasitic drain-bulk or source-bulk diodes to this model. You can specify a fourth node, but it does not affect the simulation results (except for GMIN terms).
6. Parasitic resistances and overlap capacitances are constant. They are not scaled with width, length, and temperature.
7. Capacitance expressions in this model do not conserve charge.
8. The `TREF` parameter is an exponent in an expression for mobility temperature dependence.
9. Other models use the `BEX` parameter for similar mobility temperature dependence expressions. The HP a-Si TFT `TREF` model parameter is not the same as the `TREF` reference temperature in other models. The reference temperature for the HP a-Si TFT model is 312 K (or 38.85 °C); you cannot modify it. Experimental results from TFT manufacturers indicate that amorphous silicon materials are most stable at this temperature.
10. The default room temperature is 25° C in Synopsys circuit simulators, but is 27° C in most other simulators. When comparing to other simulators, set the nominal simulation temperature to 27° C by using either `.TEMP 27` or `.OPTION TNOM=27` in the netlist. Although the reference temperature of the HP a-Si TFT model is fixed at 312° K (or 38.85°C), the behavior of the model adjusts to other simulation temperatures that you specify, or that are defaults in Synopsys circuit simulators. In the Level 40 MOSFET model, temperature dependency is enabled.
11. The default `CAPOP` value is 40, which is the HP a-Si TFT non-charge-conserving capacitance model. `CAPOP` values of 0, 1, 2, 3, 4, 5, 9, 12, or 13 have not been thoroughly tested.
12. The `DERIV` default is zero, which selects the analytical method. Set `DERIV` to 1 to select the finite difference method.

Effect of SCALE and SCALM

.OPTION SCALE has the same effect for LEVEL 40 as for other Synopsys device models, such as MOSFET Level 3 or Level 28. If you specify the L and W values in microns rather than meters (for example, L=1 rather than L=1m or 1e-6), set .OPTION SCALE=1e-6.

The SCALM option is disabled in the LEVEL 40 model. For standard MOSFET models (such as LEVEL 3), SCALM affects the scale of model parameters such as XL, XW, LD, WD, CJ, and CJSW.

Because the LEVEL 40 model ignores the SCALM option, you can mix LEVEL 40 models in a simulation with other models that use SCALM.

In general, netlists for Synopsys simulators should be as standard as possible. Also, you should convert L and W to meters scale instead of microns scale so that you can use the netlist without .OPTION SCALE=1E-6. If you follow these recommendations, a system-level simulation can use I/O sub-circuits from different vendors.

Noise Model

The LEVEL 40 model uses the standard NLEV=0 noise model inherited from other Synopsys MOSFET models.

DELVTO Element

You can use DELVTO and DTEMP on the element line with LEVEL 40.

Device Model and Element Statement Example

```
.MODEL nch nmos LEVEL=40 UO=0.4229 VTO=1.645 PHI=1.25 NSS=0
+ NFS=2.248E+21 VMAX=1231
+ THETA=-0.01771 ETA=0.0002703 T1=2.6E-07 T2=0 E1=3.9
E2=0
+ GO=9.206E-15 NU=0 K2=2 CHI=0.5
+ PSI=1E-20 VTIME=0.01 TREF=1.5 CGSO=5.203E-14
CGDO=4.43E-14
+ CSC=0.0001447 RD=5097
+ RS=5097 FREQ=1E+06 DEFF=2.15 TAU=1.64E-07 FEFF=0.5
MCKT 1 2 3 nch L=1e-05 W=4e-05
```


LEVEL 40 Model Equations

The following equations show model parameters in all capital letters; working variables are in lower case. Model parameters and the vgs and vds bias voltages are inputs. Ids, gm, and gds are the DC outputs. The Cgs gate-to-source capacitance and the Cgd gate-to-drain capacitance are the AC outputs. The electron charge is q, the Boltzmann's constant is k, and the permittivity of a vacuum is ϵ_0 .

This model applies the *SCALE* value before evaluating the equations, and scales by *M* after evaluation.

gm_{tft} and gds_{tft} variables are intermediate, not final, quantities.

For a complete description of TFT technology and the device physics underlying these equations, see the Hewlett-Packard HP IC-CAP manual.

Initially, $Cgdi = 0$, $Cgsi = 0$, $\phi_i = PHI$, $vto = VTO$, and $uo = UO$.

If $uo = 0$, then $uo = 1$.

The following equation computes the *Cfm* dielectric capacitance per unit area:

$$\text{If } T1 \neq 0 \text{ and } T2 \neq 0, \text{ then } Cfm = \frac{(\epsilon_0 \cdot E1 \cdot E2)}{((T2 \cdot E1) + (T1 \cdot E2))}$$

$$\text{If } T1 = 0 \text{ and } T2 \neq 0, \text{ then } Cfm = \frac{(\epsilon_0 \cdot E2)}{T2}$$

$$\text{If } T2 = 0 \text{ and } T1 \neq 0, \text{ then } Cfm = \frac{(\epsilon_0 \cdot E1)}{T1}$$

$$kp = uo \cdot Cfm \cdot 10^{-4}$$

TEMP is the Synopsys device simulation temperature, specified in °C, but converted to °K internally to evaluate these equations.

$$vt = \frac{(k \cdot TEMP)}{q}$$

$$eg = (2 \cdot 10^4 \cdot (TEMP - 312)) + 1.4$$

$$vto = vto + (DELVTOModel \cdot type) + (DELVTOelement \cdot type)$$

$$vbi = vto, \text{ ratio} = \frac{TEMP}{312}$$

$$\text{If } VTIME \leq 1, \text{ then } uo = uo \cdot (ratio^{TREF}) \text{ and } kp = kp \cdot (ratio^{TREF})$$

Note: T_{REF} is an exponent in adjusting the temperature. It is not the reference temperature of this device model.

$$vfb = vto - (0.5 \cdot PHI) + (0.5 \cdot (1.4 - eg))$$

$$vbi = vfb + (0.5 + PHI \cdot ratio)$$

$$vto = vbi \text{ (printback definition)}$$

$$phi = phi \cdot ratio \text{ (printback definition)}$$

$$vfb = vbi - phi \text{ (printback definition)}$$

$$vdsat = 0$$

$$beta = kp \cdot W \cdot L$$

$$vth = vbi + (ETA \cdot vds)$$

If $NU \neq 0$ $K2 \neq 0$ $PSI \neq 0$ and $VTIME > 1$, then:

$$vth = vth + f(vgs, vds, NU, K2, PSI, CHI, VTIME, TEMP)$$

$$von = vth$$

If $NFS \neq 0$, then:

$$xn = 1 + \left(\frac{(q \cdot NFS \cdot 10^4 \cdot W \cdot L)}{Cfm} \right)$$

$$von = f(vth, (vt \cdot xn))$$

Cutoff Region ($NFS=0$, $vgs \leq von$)

If $NFS = 0$ and $vgs \leq von$, then:

$$Cgdi = 0$$

$$Cgsi = 0$$

$$Ids = GO \cdot f(vgs, (DEFF \cdot vds))$$

$$gm = GO \cdot gds = GO \cdot DEFF$$

Noncutoff Region ($NFS \neq 0$)

- If $vgs > von$, then $vgsx = vgs$.
- If $vgs \leq von$, then $vgsx = von$.

Mobility modulation by vgs:

$$u_{eff} = f(u_o, \eta, v_{gs}, THETA)$$

If $v_{MAX} > 0$, then:

$$v_{dsc} = \frac{L \cdot V_{MAX}}{u_{eff}}$$

$$v_{dsat} = (v_{gsx} - v_{th}) + v_{dsc} - \sqrt{((v_{gsx} - v_{th})^2 + v_{dsc}^2)}$$

$$C_{fmlw} = \frac{(C_{fm} \cdot CSC)}{(C_{fm} + CSC)} \cdot L \cdot W$$

C_{fmlw} is the series combination of the dielectric and space charge capacitance for the MIS structure.

If $v_{ds} < v_{dsat}$, then:

$$v_{dsx} = v_{ds}$$

$$\epsilon_{psfm} = C_{fm} \cdot \frac{(T2 + T1)}{\epsilon_0}$$

ϵ_{psfm} is the effective equivalent dielectric constant of the insulator layers.

$$f_{val} = 0.8 + \left(\frac{\epsilon_{psfm} - 0.8}{1 + (2 \cdot \pi \cdot FREQ \cdot TAU)^2} \right)$$

$$C_{gdi} = f(C_{fmlw} \cdot f(efm, 0.8) \cdot (\exp(f_{val}, FEFF, v_{gs} - v_{th} - v_{ds})))$$

$$C_{gsi} = f(C_{fmlw} \cdot f(efm, 0.8) \cdot (\exp(f_{val}, FEFF, (v_{gs} - v_{th}), v_{ds})))$$

Otherwise, $v_{ds} \geq v_{dsat}$:

$$v_{dsx} = v_{dsat}$$

$$C_{gdi} = C_{fmlw}$$

$$C_{gsi} = \frac{C_{fmlw}}{2}$$

If $v_{dsx} \neq 0$, then

$$c_{dnorm} = v_{dsx} \cdot \left(v_{gsx} - v_{th} - \frac{v_{dsx}}{2} \right)$$

Normalized drain current:

$$gm_{tft} = vdsx$$

$$gds_{tft} = vgsx - vth - vdsx$$

$$cd1 = beta \cdot cdnorm$$

Drain current without velocity saturation effect:

$$beta = beta \cdot fgate, idrain = beta \cdot cdnorm$$

$$gm_{tft} = (beta \cdot gm_{tft}) + (dfgdvg \cdot cd1)$$

Velocity saturation factor—if $v_{MAX} \neq 0$, then:

$$fdrain = \frac{1}{\left(1 + \left(\frac{vdsx}{vds c}\right)\right)}$$

$$dfddvg = -dfgdvg \cdot \frac{((fdrain)^2) \cdot vdsx}{(vds c \cdot fgate)}$$

$$dfddvd = \frac{-(fdrain)^2}{vds c}$$

Strong inversion current:

$$gm_{tft} = (fdrain \cdot gm_{tft}) + (dfddvg \cdot idrain)$$

$$gds_{tft} = (fdrain \cdot gds_{tft}) + (dfddvd \cdot idrain)$$

$$idrain = fdrain \cdot idrain, beta = beta \cdot fdrain$$

$$Ids = idrain \cdot f(GO, vgs, DEFF, vds)$$

$$gm = f(gm_{tft}, GO)$$

$$gds = f(gds_{tft}, GO, DEFF)$$

Weak inversion current—if $vgs < von$, then:

$$idrain = idrain \cdot \exp\left(\frac{(vgs - von)}{(vt \cdot xn)}\right)$$

$$Ids = idrain + f(GO, vgs, DEFF, vds)$$

$$gm_{tft} = \frac{idrain}{(vt \cdot xn)}, gm = f(gm_{tft}, GO)$$

$$gds_{tft} = gds_{tft} \cdot \exp\left(\frac{(vgs - von)}{(vt \cdot xn)}\right)$$

$$gds = gds_{tft} + f(GO, DEFF)$$

$$vdsx = 0:$$

$$Ids = f(GO \cdot vgs, DEFF, vds)$$

$$gm = GO$$

$$gds_{tft} = beta \cdot (vgsx - vth)$$

If $NFS \neq 0$ and $vgs < von$, then:

$$gds_{tft} = gds_{tft} \cdot \exp\left(\frac{(vgs - von)}{(vt \cdot xn)}\right), gds = f(gds_{tft}, GO, DEFF)$$

Cgd, Cgs

$$Cgd = Cgdi + CGDO, Cgs = Cgsi + CGSO$$

LEVEL 40 Model Topology

Figure 9 shows the topology of the LEVEL 40 model.

Chapter 3: MOSFET Models: LEVELs 1 through 40
LEVEL 40 HP a-Si TFT Model

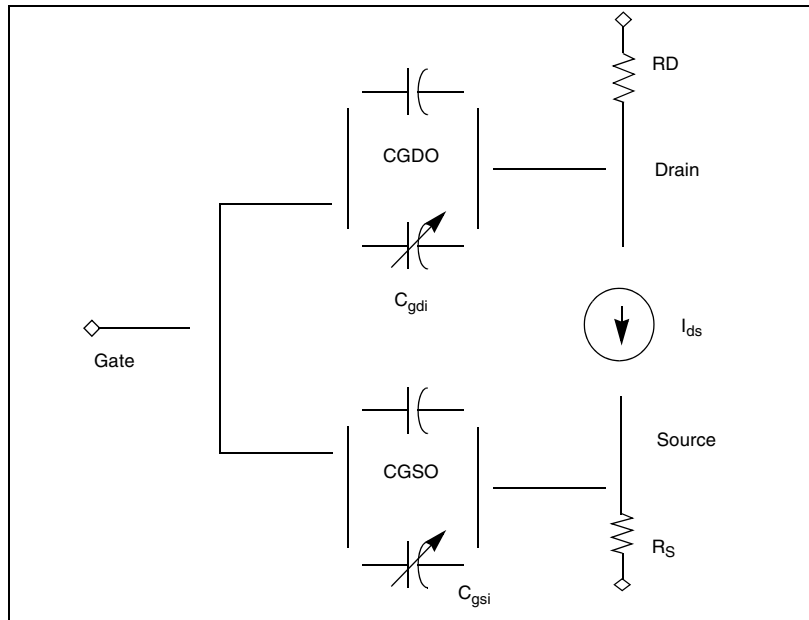


Figure 9 LEVEL 40 HP a-Si TFT Topology

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- [9] Duster, J.S., Jeng,M.C., Ko, P. K. and Hu, C. *User's Guide for the BSIM2 Parameter Extraction Program and the SPICE3 with BSIM Implementation*. Industrial Liaison Program, Software Distribution Office, University of California, Berkeley, May 1990.

Chapter 3: MOSFET Models: LEVELs 1 through 40

References

MOSFET Models: LEVELs 50 through 74

Lists and describes standard MOSFET models (Levels 50 to 69).

HSPICE ships hundreds of examples for your use; see [Listing of Demonstration Input Files](#) for paths to demo files.

The MOSFET models described in this chapter are the most currently developed and widely used of the standard MOSFET models. Synopsys MOSFET device models have introduced Levels that are compatible with models developed by the University of Florida, Rensselaer Polytechnic Institute, and others.

This chapter describes the following standard MOSFET models (Levels 50 to 64):

- [Level 50 Philips MOS9 Model](#)
- [Level 55 EPFL-EKV MOSFET Model](#)
- [Level 58 University of Florida SOI](#)
- [Level 61 RPI a-Si TFT Model](#)
- [Level 62 RPI Poli-Si TFT Model](#)
- [Level 63 Philips MOS11 Model](#)
- [Level 64 STARC HiSIM Model](#)
- [Level 68 STARC HiSIM2 Model](#)
- [Level 69 PSP100 DFM Support Series Model](#)
- [Level 73 HSPICE HiSIM-LDMOS/HiSIM-HV Model](#)
- [Level 74 MOS Model 20 Model](#)

For information about standard MOSFET Models Levels 1 to 40, see [Chapter 3, MOSFET Models: LEVELs 1 through 40](#). For information on BSIM MOSFET models (based on models developed by the University of California at

Berkeley), see [Chapter 5, MOSFET Models \(BSIM\): Levels 13 through 39](#) and [Chapter 6, MOSFET Models \(BSIM\): Levels 47 through 72](#).

Level 50 Philips MOS9 Model

The Philips MOS Model 9 LEVEL 50 defaults to version 903. If you set the model parameter VERSION, you can control it to either version 902 or 903. The 903 version includes parameters NFMOD, NFAR, NFBR, NFBR, SL3VT0. If you set `version=902`, it will select the 902 model. The Philips MOS Model 9 is available as Level 50 in the Synopsys models (based on the “Unclassified Report NL-UR 003/94” by R.M.D.A. Velghe, D.B.M. Klaassen, and F.M. Klaassen).

MOSFET Level 50 incorporates all features of Philips MOS 9, except for the gate noise current. You can select either of two MOSFET Level 50 diode models:

- ACM Parasitic Diode Model by using the JS, JSW, N, CJ, CJSW, CJGATE, MJ, MJSW, PB, PHP, ACM, and HDIF parameters. This version does not use the older IS parameter. To use this model, select the JUNCAP=0 (default) parameter.
- Philips JUNCAP Parasitic Diode Model. To use this model, select the JUNCAP=1 model parameter.

For additional information regarding the MOS Model-9, see:

http://www-us.semiconductors.com/Philips_Models

Table 27 MOSFET Level 50 Model Parameters

Name	Unit	Default (N)	Default (P)	Description
LER	m	1.1e-6	1.25e-6	Reference Leff
WER	m	20.0e-6	20.0e-6	Reference Weff
LVAR	m	-220.0e-9	-460.0e-9	Variation in gate length
LAP	m	100.0e-9	25.0e-9	Lateral diffusion per side
WVAR	m	-25.0e-9	-130.0e-9	Variation in active width
WOT	m	0.0	0.0	Channel-stop diffusion per side

Table 27 MOSFET Level 50 Model Parameters

Name	Unit	Default (N)	Default (P)	Description
TR	°C	21.0	21.0	Reference temperature for model
VTOR	V	730.0e-3	1.1	Threshold voltage at zero bias
STVTO	V/K	-1.2e-3	-1.7e-3	Temperature dependence of VTO
SLVTO	Vm	-135.0e-9	35.0e-9	Length dependence of VTO
SL2VTO	Vm ²	0.0	0.0	Second length dependence of VTO
SWVTO	Vm	130.0e-9	50.0e-9	Width dependence of VTO
KOR	V ^{-1/2}	650.0e-3	470.0e-3	Low-back-bias body factor
SLKO	V ^{-1/2} m	-130.0e-9	-200.0e-9	Length dependence of k ₀
SWKO	V ^{-1/2} m	2.0e-9	115.0e-9	Width dependence of k ₀
KR	V ^{-1/2}	110.0e-3	470.0e-3	High-back-bias body factor
SLK	V ^{-1/2} m	-280.0e-9	-200.0e-9	Length dependence of K
SWK	V ^{-1/2} m	275.0e-9	115.0e-9	Width dependence of K
PHIBR	V	650.0e-3	650.0e-3	Strong inversion surface potential
VSBR	V	660.0e-3	0.0	Transition voltage for dual-k-factor model
SLVSBX	Vm	0.0	0.0	Length dependence of VSBX
SWVSBX	Vm	-675.0e-9	0.0	Width dependence of VSBX
BETSQ	AV ⁻²	83.0e-6	26.1e-6	Gain factor of infinite square transistor
ETABET	-	1.6	1.6	Exponent of temperature dependence of gain factor
THE1R	V ⁻¹	190.0e-3	190.0e-3	Gate-induced mobility reduction coefficient

Table 27 MOSFET Level 50 Model Parameters

Name	Unit	Default (N)	Default (P)	Description
STTHE1R	V^{-1}/K	0.0	0.0	Temperature dependence coefficient THE1R
SLTHE1R	$V^{-1}m$	140.0e-9	70.0e-9	Length dependence coefficient of THE1R
STLTHE1	$V^{-1}m/K$	0.0	0.0	Temperature dependence of the length dependence for THE1R
SWTHE1	$V^{-1}m$	-58.0e-9	-80.0e-9	Width dependence coefficient of THE1R
THE2R	$V^{-1/2}$	12.0e-3	165.0e-3	Back-bias induced mobility reduction coefficient
STTHE2R	$V^{-1}m/K$	0.0	0.0	Temperature dependence coefficient THE2R
SLTHE2R	$V^{-1/2}m$	-33.0e-9	-75.0e-9	Length dependence coefficient of THE2R
STLTHE2	$V^{-1/2}m/K$	0.0	0.0	Temperature dependence of the length dependence for THE2R
SWTHE2	$V^{-1/2}m$	30.0e-9	20.0e-9	Width dependence coefficient of THE2R
THE3R	V^{-1}	145.0e-3	27.0e-3	Lateral field induced mobility reduction coefficient
STTHE3R	V^{-1}/K	-660.0e-6	0.0	Temperature dependence coefficient of THE3R
SLTHE3R	$V^{-1}m$	185.0e-9	27.0e-9	Length dependence coefficient of THE3R
STLTHE3	$V^{-1}m/K$	-620.0e-12	0.0	Temperature dependence of the length dependence for THE3R
SWTHE3	$V^{-1}m$	20.0e-9	11.0e-9	Width dependence coefficient of THE3R
GAM1R	-	145.0e-3	77.0e-3	Drain-induced threshold shift coefficient for high gate drive
SLGAM1	-	160.0e-9	105.0e-9	Length dependence of GAM1R

Table 27 MOSFET Level 50 Model Parameters

Name	Unit	Default (N)	Default (P)	Description
SWGAM1	-	-10.0e-9	-11.0e-9	Width dependence of GAM1R
ETADSR	-	600.0e-3	600.0e-3	Exponent of drain dependence of GAM1R
ALPR	-	3.0e-3	44.0e-3	Channel length modulation factor
ETAALP	-	150.0e-3	170.0e-3	Exponent of length dependence of ALPR
SLALP	-	-5.65e-3	9.0e-3	Coefficient of length dependence of ALPR
SWALP	m	1.67e-9	180.0e-12	Coefficient of width dependence of ALPR
VPR	V	340.0e-3	235.0e-3	Characteristic voltage for channel length modulation
GAMOOD	-	18.0e-3	7.0e-3	Drain-induced threshold shift coefficient, at zero gate drive, and zero back-bias
SLGAMOD	m ²	20.0e-15	11.0e-15	Length dependence of GAMOOD
ETAGAMR	-	2.0	1.0	Exponent of back-bias dependence of zero gate-drive, drain-induced threshold shift
MOR	-	500.0e-3	375.0e-3	Subthreshold slope factor
STMO	K ⁻¹	0.0	0.0	Temperature dependence coefficient MOR
SLMO	m ^{1/2}	280.0e-6	47.0e-6	Length dependence coefficient of MOR
ETAMR	-	2.0	1.0	Exponent of back-bias dependence of the subthreshold slope
ZET1R	-	420.0e-3	1.3	Weak-inversion correction factor
ETAZET	-	170.0e-3	30.0e-3	Exponent of length dependence of ZET1R

Table 27 MOSFET Level 50 Model Parameters

Name	Unit	Default (N)	Default (P)	Description
SLZET1	-	-390.0e-3	-2.8	Length dependence coefficient of ZET1R
VSBT	V	2.1	100.0	Limiting voltage for back-bias dependence
SLVSBT	Vm	-4.4e-6	0.0	Length dependence of VSBTR
A1R	-	6.0	10.0	Weak-avalanche current factor
STA1	K ⁻¹	0.0	0.0	Temperature coefficient of A1R
SLA1	m	1.3e-6	-15.0e-6	Length dependence of A1R
SWA1	m	3.0e-6	30.0e-6	Width dependence of A1R
A2R	V	38.0	59.0	Exponent of weak-avalanche current
SLA2	Vm	1.0e-6	-8.0e-6	Length dependence of A2R
SWA2	Vm	2.0e-6	15.0e-6	Width dependence of A2R
A3R	-	650.0e-3	520.0e-3	Factor of minimum drain bias, above which avalanche sets in
SLA3	m	-550.0e-9	-450.0e-9	Length dependence of A3R
SWA3	m	0.0	-140.0e-9	Width dependence of A3R
TOX	m	25.0e-9	25.0e-9	Oxide thickness
COL	F/m	320.0e-12	320.0e-12	Gate overlap capacitance per unit width
WDOG	m	0	0	Characteristic drawn gate width, below which dogboning appears
FTHE1	-	0	0	Coefficient describing the width dependence of THE1 for W < WDOG
NFMOD		0		Flicker noise selector. 0 selects the old flicker noise model added in release 98.4

Table 27 MOSFET Level 50 Model Parameters

Name	Unit	Default (N)	Default (P)	Description
NTR	J	24.4e-21	21.1e-21	Thermal noise coefficient
NFR	V^2	70.0e-12	21.4e-12	Flicker noise coefficient
NFAR	$V^{-1}m^{-2}$	7.15e+22	1.53xe+22	1st flicker noise coefficient added in release 98.4
NFBR	$V^{-1}m^{-2}$	2.16e+06	4.06e+06	2nd flicker noise coefficient added in release 98.4
NFCR	V^{-1}	0.0	2.92e-10	3rd flicker noise coefficient added in release 98.4
SL3VTO	V	0	0	Third coefficient of the length dependence of VTO
SL2KO	$V^{1/2}m^2$	0	0	Second coefficient of the length dependence of K_0
SL2K	$V^{1/2}m^2$	0	0	Second coefficient of the length dependence of K
LP1	M	1E-6	1E-6	Characteristic length of the first profile
FBET1	-	0	0	Relative mobility decrease due to the first profile
LP2	M	1E-8	1E-8	Characteristic length of the second profile
FBET2	-	0	0	Relative mobility decrease due to the second profile
GTHE1	-	0	0	Parameter that selects either the old (=0) or the new (=1) scaling rule of θ_1
SL2GAMOO	-	0	0	Second coefficient of the γ_{00} length dependence

JUNCAP Model Parameters

The following are JUNCAP model parameters specifically for the Philips MOS 9 (Level 50) model.

Table 28 JUNCAP Model Parameters, MOSFET Level 50

Name	Unit	Default	Description
JUNCAP	-	0	JUNCAP flag: 0-off, 1-on.
DTA	°C	0.0	Temperature offset of JUNCAP element relative to T_A .
VR	V	0.0	Voltage at which simulation determines the parameters.
JSGBR	$A \cdot m^{-2}$	1.00e-3	Bottom saturation-current density due to electron-hole generation at $V=V_R$.
JSDBR	$A \cdot m^{-2}$	1.00e-3	Bottom saturation-current density due to diffusion from back contact.
JSGSR	$A \cdot m^{-1}$	1.00e-3	Sidewall saturation-current density due to electron-hole generation at $V=V_R$.
JSDSR	$A \cdot m^{-1}$	1.00e-3	Sidewall saturation-current density due to diffusion from back contact.
JSGGR	$A \cdot m^{-1}$	1.00e-3	Gate edge saturation-current density due to electron-hole generation at $V=V_R$.
JSDGR	$A \cdot m^{-1}$	1.00e-3	Gate edge saturation-current density due to diffusion from back contact.
NB	-	1.00	Emission coefficient of the bottom forward current.
NS	-	1.00	Emission coefficient of the sidewall forward current.
NG	-	1.00	Emission coefficient of the gate edge forward current.
CJBR	$F \cdot m^{-2}$	1.00e-12	Bottom junction capacitance at $V=V_R$.

Table 28 JUNCAP Model Parameters, MOSFET Level 50

Name	Unit	Default	Description
CJSR	$F \cdot m^{-1}$	1.00e-12	Sidewall junction capacitance at $V=V_R$.
CJGR	$F \cdot m^{-1}$	1.00e-12	Gate edge junction capacitance at $V=V_R$.
VDBR	v	1.00	Diffusion voltage of the bottom junction at $T=T_R$.
VDSR	v	1.00	Diffusion voltage of the sidewall junction at $T=T_R$.
VDGR	v	1.00	Diffusion voltage of the gate edge junction at $T=T_R$.
PB	-	0.40	Bottom-junction grading coefficient.
PS	-	0.40	Sidewall-junction grading coefficient.
PG	-	0.40	Gate edge-junction grading coefficient.
TH3MOD	-	1	Switch that activates THE3-clipping: <ul style="list-style-type: none"> ▪ If TH3MOD ==1 (default), effective THE3 can be slightly negative, and clipping does not occur. ▪ If TH3MOD ==0, this model clips the effective THE3 to more than zero.

Using the Philips MOS9 Model

To use the Philips MOS9 model:

1. Set LEVEL=50 to identify the model as the Philips MOS Model 9.
2. The default room temperature is 25°C in Synopsys circuit simulators, but is 27°C in most other simulators. When comparing to other simulators, set the simulation temperature to 27 use `.TEMP 27` or `.OPTION TNOM=27`.
3. The model parameter set must include the TR model reference temperature, which corresponds to TREF in other model levels. The default for TR is 21.0°C to match the Philips simulator.

4. This model has its own charge-based capacitance model. Level 50 ignores the `CAPOP` parameter, which selects different capacitance models.
5. This model uses analytical derivatives for the conductances. This model ignores the `DERIV` parameter, which selects the finite difference method.
6. `DTEMP` increases the temperature of individual elements relative to the circuit temperature. Set `DTEMP` on the element line.
7. Defaults are nonzero so use the `.MODEL` statement to set every model parameter listed in the Level 50 Model Parameters table.
8. Use the `JUNCAP` model parameter to select one of two available parasitic junction diode models, `ACM` or `JUNCAP`. `JUNCAP=1` selects the Philips `JUNCAP` model, `JUNCAP=0` (default) selects the `ACM` model.
9. Philips added a switch named `TH3MOD` to MOS Model 9. You can use this switch to re-activate effective `THE3` clipping, which was removed in an earlier version of this model.
 - If `TH3MOD==1` (default), effective `THE3` can be slightly negative, and clipping does not occur.
 - If `TH3MOD==0`, this model clips the effective `THE3` to more than zero.

Model Statement Example

```
.model nch nmos Level=50
+ ler =1e-6 wer=10e-6
+ lvar =0.0 lap=0.05e-6
+ wvar =0.0 wot=0.0
+ tr  = 27.00 vtor=0.8
+ stvto =0 slvto=0
+ sl2vto =0 swvto=0
+ kor =0.7 slko=0
+ swko =0 kr=0.3
+ slk =0 swk=0
+ phibr =0.65 vsbxb=0.5
+ slvsbx =0 swvsbx=0
+ betsq =120e-6 etabet=1.5
+ the1r =0.3 stthe1r=0
+ slthe1r =0 stlthe1=0
+ swthe1 =0 the2r=0.06
+ stthe2r =0 slthe2r=0
+ stlthe2 =0 swthe2=0
+ the3r =0.1 stthe3r=0
```

```
+ slthe3r =0 stlthe3=0
+ swthe3 =0 gam1r=0.02
+ slgam1 =0 swgam1=0
+ etadsr =0.60 alpr=0.01
+ etaalp =0 slalp=0
+ swalp =0 vpr=0.4
+ gamoor =0.006 slgamoo=0
+ etagamr =2.0 mor=0.5
+ stmo =0 slmo=0
+ etamr =2.0 zet1r=1.0
+ etazet =0.5 slzet1=0
+ vsbtr =2.5 slvsbt=0
+ alr =10 stal=0
+ sla1 =0 swa1=0
+ a2r =30 sla2=0
+ swa2 =0 a3r=0.8
+ sla3 =0 swa3=0
+ tox =15.00e-9 col=0.3e-9
+ ntr =2.0e-20 nfr=5.0e-11
+ acm =2 hdif=1u
+ js =1e-3 cj=1e-3
+ mj =0.5 pb=0.8
+ cjsw =1e-9 cjgate=1e-9
+ mjsw =0.3 php=0.8
```

Level 55 EPFL-EKV MOSFET Model

The EPFL-EKV MOSFET model is a scalable and compact simulation model built on fundamental physical properties of the MOS structure. This model is dedicated to the design and simulation of low-voltage, low-current analog, and mixed analog-digital circuits using submicron CMOS technologies.

- The intrinsic part of the MOSFET includes the equations and parameters used to simulate the EPFL-EKV MOSFET model.
- The extrinsic part of the MOSFET model includes series resistances of the source and drain diffusions, junction currents, and capacitances.

Single Equation Model

The EPFL-EKV MOSFET model is a *single expression*, which preserves continuity of first-order and higher-order derivatives with respect to any terminal voltage in the entire range of validity of the model. This section describes the analytical expressions of first-order derivatives as transconductances and transcapacitances, you can use them in simulation.

Effects Modeled

The EPFL-EKV MOSFET model version 2.6 models the following physical effects:

- Basic geometrical and process-related aspects, such as oxide thickness, junction depth, and effective channel length and width.
- Effects of the doping profile.
- Substrate effect.
- Modeling of weak, moderate, and strong inversion behavior.
- Modeling of mobility effects due to vertical and lateral fields, and velocity saturation.
- Short-channel effects, such as channel-length modulation (CLM), source and drain charge-sharing (including for narrow channel widths), and the reverse short channel effect (RSCE).
- Modeling of the substrate current due to impact ionization.
- Quasi-static charge-based dynamic model.
- Thermal and flicker noise modeling.
- Short-distance geometry-dependent and bias-dependent device matching.

Coherence of Static and Dynamic Models

Simulation derives all aspects of the static, the quasi-static, and the non-quasi-static (NQS) dynamic and noise models, from the normalized transconductance-to-current ratio. These expressions use symmetric normalized forward and reverse currents.

- For quasi-static dynamic operations, you can use a charge-based model for the node charges and trans-capacitances or a simpler capacitances model.
- The dynamic model, including the time constant for the NQS model, is described in symmetrical terms of the forward and reverse normalized currents.

The charge formulation also expresses the effective mobility dependence of a local field.

Bulk Reference and Symmetry

Voltages are all referred to the local substrate:

$$V_G = V_{GB} \quad \text{Intrinsic gate-to-bulk voltage}$$

$$V_S = V_{SB} \quad \text{Intrinsic source-to-bulk voltage}$$

$$V_D = V_{DB} \quad \text{Intrinsic drain-to-bulk voltage}$$

V_S and V_D are the intrinsic source and drain voltages so the voltage drop over the extrinsic resistive elements must already be accounted for externally.

V_D is the electrical drain voltage, where $V_D > V_S$. Bulk reference handles the model symmetrically with respect to source and drain. This symmetry is inherent in common MOS technologies (excluding non-symmetric source-drain layouts).

Note: Intrinsic model equations are presented for an N-channel MOSFET. P-channel MOSFETs are dealt with as pseudo-N-channel. That is, simulation reverses the polarity of the voltages (V_G , V_S , V_D , V_{FB} , V_{TO} , and TCV) before computing the P-channel current, which has a negative sign. No other distinctions are made between N-channel and P-channel, except the η factor for calculating the effective mobility.

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Level 55 EPFL-EKV MOSFET Model

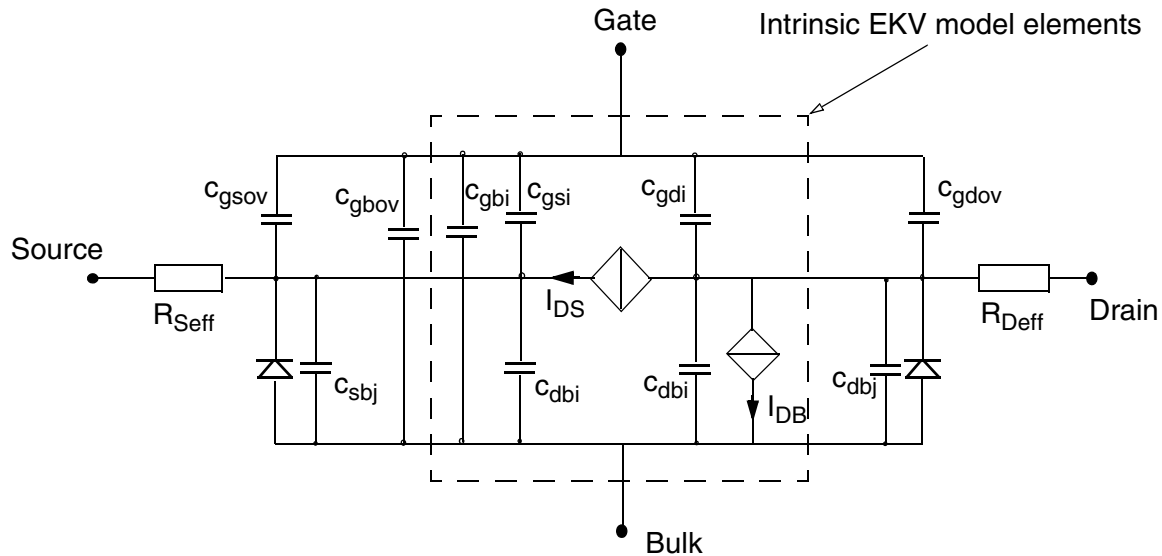


Figure 10 Level 55 Equivalent Circuit

Figure 10 represents the intrinsic and extrinsic elements of the MOS transistor. For quasi-static dynamic operation, this figure shows only the intrinsic capacitances from the simpler capacitances model. However, you can also use a charge-based transcapacitances model in simulation.

Table 29 Device Input Variables

Name	Unit	Default	Description
L	m	-	Channel length
W	m	-	Channel width
M or NP	-	1.0	Parallel multiple device number
N or NS	-	1.0	Series multiple device number

EKV Intrinsic Model Parameters

Name	Unit	Default	Range	Description
COX ¹	F/m ²	0.7e-3	-	Gate oxide capacitance per unit area
XJ	m	0.1e-6	1.0e-9	Junction depth
DW ²	m	0	-	Channel width correction
DL	m	0	-	Channel length correction

1. This model can calculate the default value of COX as a function of TOX.
2. DL and DW parameters are usually negative; see the effective length and width calculation.

Name	Unit	Default ¹	Range	Description
VTO ²	V	0.5	-	Long-channel threshold voltage
GAMMA	\sqrt{V}	1.0	≥ 0	Body effect parameter
PHI	V	0.7	≥ 0.1	Bulk Fermi potential (*2)
KP	A/V ²	50.0e-6	-	Transconductance parameter
E0 (EO)	V/m	1.0e12	$\geq 1E5$	Mobility reduction coefficient
UCRIT	V/m	2.0e6	$\geq 1E5$	Longitudinal critical field

1. This model can calculate the default values of VTO, GAMMA, PHI, and KP as a function of TOX, NSUB, UO, and VFB for statistical circuit simulation.
2. As VG, VTO also references the bulk.

Name	Unit ¹	Default	Range	Description
TOX ²	m	-	≥ 0	Oxide thickness
NSUB ³	cm ⁻³	-	≥ 0	Channel doping
VFB ⁴	V	-	-	Flat-band voltage

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Level 55 EPFL-EKV MOSFET Model

Name	Unit ¹	Default	Range	Description
UO ⁵	cm ² /(Vs)	-	≥ 0	Low-field mobility
VMAX ⁶	m/s	-	≥ 0	Saturation velocity
THETA ⁷	1/V	0	≥ 0	Mobility reduction coefficient

1. In this example, cm is the basic unit for NSUB and UO. TOX and VMAX are in m.

2. Optional parameter for calculating COX.

3. Optional parameter for the dependence of GAMMA on COX, and for calculating PHI.

4. Optional parameter for calculating VTO as a function of COX, GAMMA, or PHI.

5. Optional parameter for the dependence of KP on COX.

6. Optional parameter for calculating UCRIT.

7. Optional parameter for mobility reduction due to the vertical field.

The preceding parameters accommodate the scaling behavior of the process and basic intrinsic model parameters, and statistical circuit simulation. Simulation uses the TOX, NSUB, VFB, UO, and VMAX parameters only if you did not specify COX, GAMMA, PHI, VTO, KP, or UCRIT. You can also use a simpler mobility reduction model, due to the vertical field. Simulation uses the THETA mobility reduction coefficient only if you did not specify E0.

Name	Unit	Default	Range	Description
LAMBDA	-	0.5	≥ 0	Depletion length coefficient (channel length modulation)
WETA	-	0.25	-	Narrow-channel effect coefficient
LETA	-	0.1	-	Short-channel effect coefficient

Name	Unit	Default	Range	Description
Q0 (QO)	A · s/ m ²	0	-	Reverse short channel effect peak charge density
LK	m	0.29e-6	≥ 1.0e-8	Reverse short channel effect characteristic length

Name	Unit	Default	Range	Description
IBA	1/m	0	-	First impact ionization coefficient
IBB	V/m	3.0e8	$\geq 1.0\text{e}8$	Second impact ionization coefficient
IBN	-	1.0	≥ 0.1	Saturation voltage factor for impact ionization

Name	Unit	Default	Description
TCV	V/K	1.0e-3	Threshold voltage temperature coefficient
BEX	-	-1.5	Mobility temperature exponent
UCEX	-	0.8	Longitudinal critical field temperature exponent
IBBT	1/K	9.0e-4	Temperature coefficient for IBB

Name	Unit	Default	Description
AVTO	Vm	0 ¹	Area related threshold voltage mismatch parameter
AKP	m	0	Area related gain mismatch parameter
AGAMMA	$\sqrt{\text{Vm}}$	0	Area related body effect mismatch parameter

1. Only DEV values apply to the statistical matching parameters (AVTO, AGAMMA, AKP) for Monte-Carlo type simulations. Default is 1E-6 for all three parameters in some implementations to allow sensitivity analysis of the matching parameters. Do not specify LOT for AVTO, AGAMMA, or AKP.

Name	Unit	Default	Description
KF	₁	0	Flicker noise coefficient
AF	-	1	Flicker noise exponent

1. The unit for KF might depend on the flicker noise model that you select, if these options are available.

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Name	Unit	Default	Description
NQS ¹	-	0	Non-Quasi-Static (NQS) operation switch
SATLIM ²	-	exp(4)	Ratio defining the i_f/i_r saturation limit.
XQC ³	-	0.4	Charge/capacitance model selector

1. NQS=1 switches Non-Quasi-Static operation on, default is off (the NQS model option might not be available in all implementations).

2. Only used for operating point information. (the SATLIM option might not be available in all implementations).

3. Selects either the charges/transcapacitances (default) or the capacitances-only model. XQC=0.4: charges/transcapacitances model; XQC=1: capacitances only model. (the XQC model option might not be available in all implementations).

Static Intrinsic Model Equations

Basic Definitions

$$\epsilon_{si} = SCALE \cdot 1.045 \times 10^{-12} [F/m] \quad \text{Permittivity of silicon}$$

$$\epsilon_{ox} = SCALE \cdot 34.5 \times 10^{-12} [F/m] \quad \text{Permittivity of silicon dioxide}$$

$$q = 1.602 \times 10^{-19} [C] \quad \text{Magnitude of electron charge}$$

$$k = 1.3807 \times 10^{-23} [JK^{-1}] \quad \text{Boltzmann constant}$$

$$T_{ref} = 300.15 [K] \quad \text{Reference temperature}$$

$$T_{nom} [K] \quad \text{Nominal temperature of model parameters}$$

$$T [K] \quad \text{Model simulation temperature}$$

$$V_t(T) = \frac{k \cdot T}{q} \quad \text{Thermal voltage}$$

$$E_g(T) = \left(1.16 - 0.000702 \cdot \frac{T^2}{T + 1108} \right) [eV] \quad \text{Energy gap}$$

$$n_i(T) = 1.45 \times 10^{16} \cdot \left(\frac{T}{T_{ref}} \right) \cdot \exp \left(\frac{E_g(T_{ref})}{2 \cdot V_t(T_{ref})} - \frac{E_g(T)}{2 \cdot V_t(T)} \right) [m^{-3}] \quad \text{Intrinsic carrier concentration}$$

Parameter Preprocessing

Handling of Model Parameters for P-Channel MOSFETs

For P-channel devices, simulation reverses the sign of V_{FB} , V_{TO} , and TCV before processing. Therefore, V_{TO} and TCV are usually positive and V_{FB} is usually negative for N-channel, and vice versa for P-channel MOSFETs.

Initializing Intrinsic Parameters

The basic intrinsic model parameters are related to the fundamental process parameters as in early SPICE models:

$COX \rightarrow \epsilon_{ox} / TOX$
 $GAMMA$ and $PHI \rightarrow NSUB$
 $V_{TO} \rightarrow -V_{FB}$
 $KP \rightarrow \mu_0$
 $UCRIT \rightarrow V_{MAX}$

For statistical circuit simulation, you should introduce parameter variations on the level of the latter parameters. You can also use these dependencies to analyze device scaling and to obtain parameter sets from other MOSFET models. Therefore, you can use the following relations:

If you do not specify COX , simulation initializes it as:

$$COX = \begin{cases} \epsilon_{ox} / TOX & \text{for: } TOX > 0 \\ default & \text{otherwise} \end{cases}$$

If you do not specify $GAMMA$, simulation initializes it as:

$$GAMMA = \begin{cases} \frac{\sqrt{2q\epsilon_{si} \cdot (NSUB \cdot 10^6)}}{COX} & \text{for: } NSUB > 0 \\ default & \text{otherwise} \end{cases}$$

If you do not specify PHI , simulation initializes it as:

$$PHI = \begin{cases} 2V_t(T_{nom}) \cdot \ln\left(\frac{NSUB \cdot 10^6}{n_i(T_{nom})}\right) & \text{for: } NSUB > 0 \\ default & \text{otherwise} \end{cases}$$

If you do not specify V_{TO} , simulation initializes it as:

$$V_{TO} = \begin{cases} V_{FB} + PHI + GAMMA \cdot \sqrt{PHI} & \text{if you specify } V_{FB} \\ \text{default} & \text{otherwise} \end{cases}$$

If you do not specify DP , simulation initializes it as:

$$KP = \begin{cases} (UO \cdot 10^{-4}) \cdot COX & \text{for: } UO > 0 \\ \text{default} & \text{otherwise} \end{cases}$$

If you do not specify $UCRIT$, simulation initializes it as:

$$UCRIT = \begin{cases} V_{MAX} / (UO \cdot 10^{-4}) & \text{for: } V_{MAX} > 0, UO > 0 \\ \text{default} & \text{otherwise} \end{cases}$$

If you do not specify $E0$, simulation uses a simplified mobility model with the $THETA$ parameter:

$$E0 = \begin{cases} 0 & \text{if you specify } THETA \\ \text{default} & \text{otherwise} \end{cases}$$

Note: The $E0$ value is zero, indicating to use the simplified mobility model is used in conjunction with $THETA$, instead of the standard mobility model.

Optional parameters might not be available in all implementations.

Default Values and Parameter Ranges

If you do not define a specific model parameters, simulation either initializes it according to the above relations, or sets it to its default value. Certain parameters restrict their numerical range to avoid numerical problems, such as divisions by zero. If you specify a parameter value outside the specified range (see the range column in the parameter tables), then simulation sets its value to the closest acceptable value.

Intrinsic Parameters Temperature Dependence

$$V_{TO}(T) = V_{TO} - TCV \cdot (T - T_{nom})$$

$$KP(T) = KP \cdot \left(\frac{T}{T_{nom}} \right)^{BEX}$$

$$UCRIT(T) = UCRIT \cdot \left(\frac{T}{T_{nom}} \right)^{UCEX}$$

$$PHI(T) = PHI \cdot \frac{T}{T_{nom}} - 3 \cdot V_t \cdot \ln\left(\frac{T}{T_{nom}}\right) - E_g(T_{nom}) \cdot \frac{T}{T_{nom}} + E_g(T)$$

$$IBB(T) = IBB \cdot [1.0 + IBBT \cdot (T - T_{nom})]$$

Bulk Referenced Intrinsic Voltages

Simulation refers all voltages to the local substrate (see [Bulk Reference and Symmetry on page 173](#)):

$$V_G = V_{GB} = V_{GS} - V_{BS} \quad \text{Intrinsic gate-to-bulk voltage}$$

$$V_S = V_{SB} = -V_{BS} \quad \text{Intrinsic source-to-bulk voltage}$$

$$V_D = V_{DB} = V_{DS} - V_{BS} \quad \text{Intrinsic drain-to-bulk voltage}$$

For P-channel devices, simulation inverts all signs before processing.

Effective Channel Length and Width

$$W_{eff} = W + DW$$

$$L_{eff} = L + DL$$

Note: Unlike the convention in other MOSFET models, DL and DW usually permit a negative value due to the above definition.

Short Distance Matching

The inverse of the square root of the transistor area usually suitably describes a random mismatch between two transistors with an identical layout and close to each other. The following relationships have been adopted:

$$VTO_a = VTO + \frac{AVTO}{\sqrt{NP \cdot W_{eff} \cdot NS \cdot L_{eff}}}$$

$$KP_a = KP \cdot \left(1 + \frac{AKP}{\sqrt{NP \cdot W_{eff} \cdot NS \cdot L_{eff}}} \right)$$

$$GAMMA_a = GAMMA + \frac{AGAMMA}{\sqrt{NP \cdot W_{eff} \cdot NS \cdot L_{eff}}}$$

These model equations apply only in Monte-Carlo and sensitivity simulations. Because negative values for both KP_a and $GAMMA_a$ are not physically meaningful, simulation clips them at zero.

Reverse Short-channel Effect (RSCE)

$$C_\epsilon = 4 \cdot (22 \times 10^{-3})^2 \quad C_A = 0.028$$

$$\xi = C_A \cdot \left(10 \cdot \frac{L_{eff}}{LK} - 1 \right)$$

$$\Delta V_{RSCE} = \frac{2 \cdot Q0}{COX} \cdot \frac{1}{\left[1 + \frac{1}{2} \cdot (\xi + \sqrt{\xi^2 + C_\epsilon}) \right]^2}$$

Effective Gate Voltage Including RSCE

$$V'_G = V_G - VTO_a - \Delta V_{RSCE} + PHI + GAMMA_a \sqrt{PHI}$$

Effective substrate factor including charge-sharing for short and narrow channels

Pinch-off voltage for narrow-channel effect:

$$V_{P0} = \begin{cases} V'_G - PHI - GAMMA_a \left(\sqrt{V'_G + \left(\frac{GAMMA_a}{2} \right)^2} - \frac{GAMMA_a}{2} \right) & \text{for: } V'_G > 0 \\ -PHI & \text{for: } V'_G \leq 0 \end{cases}$$

Effective substrate factor accounting for charge-sharing:

$$V'_{S(D)} = \frac{1}{2} \cdot [V_{S(D)} + PHI + \sqrt{(V_{S(D)} + PHI)^2 + (4V_t)^2}]$$

Note: This equation prevents a negative value in the square roots argument in the subsequent code.

$$\gamma^{\circ} = GAMMA_a - \frac{\epsilon_{si}}{COX} \cdot \left[\frac{LETA}{L_{eff}} \cdot (\sqrt{V'_S} + \sqrt{V'_D}) - \frac{3 \cdot WETA}{W_{eff}} \cdot \sqrt{V_{P0} + PHI} \right]$$

$$\gamma' = \frac{1}{2} \cdot (\gamma^{\circ} + \sqrt{\gamma^{\circ 2} + 0.1 \cdot V_t})$$

Note: This equation prevents the effective substrate factor from becoming negative.

Pinch-off Voltage Including Short-Channel and Narrow-Channel Effects

$$V_P = \begin{cases} V'_G - PHI - \gamma' \cdot \left(\sqrt{V'_G + \left(\frac{\gamma'}{2}\right)^2} - \frac{\gamma'}{2} \right) & \text{for: } V'_G > 0 \\ -PHI & \text{for: } V'_G \leq 0 \end{cases}$$

Note: The pinch-off voltage accounts for channel doping effects, such as the threshold voltage and the substrate effect.

For long-channel devices, V_p is a function of gate voltage; for short-channel devices, it also becomes a function of the source and drain voltage due to the charge-sharing effect.

Slope Factor

$$n = 1 + \frac{GAMMA_a}{2 \cdot \sqrt{V_P + PHI + 4V_t}}$$

Note: The slope factor (or body effect factor) is primarily a function of the gate voltage, and links to the weak inversion slope.

Large Signal Interpolation Function

$F(v)$ is the large-signal interpolation function, relating normalized currents to normalized voltages. A simple and accurate expression for the transconductance-to-current ratio consistently formulates:

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Level 55 EPFL-EKV MOSFET Model

- The static large-signal interpolation function.
- The dynamic model for the intrinsic charges (and capacitances).
- The intrinsic time constant and the thermal noise model for the whole range of current, from weak to strong inversion.

$$\frac{g_{ms} \cdot V_t}{I_{DS}} = \frac{1}{\sqrt{0.25 + i} + 0.5}$$

Large-signal interpolation function:

$$y = \sqrt{0.25 + i} - 0.5$$

$$v = 2y + \ln(y)$$

You cannot analytically invert this equation. However, you can use a Newton-Raphson iterative scheme to invert this equation. Currently, this model uses a simplified algorithm that avoids iteration, leading to a continuous expression for the large signal interpolation function.

The (inverted) large signal interpolation function has the following asymptotes in strong and weak inversion:

$$F(v) = \begin{cases} (v/2)^2 & \text{for: } v \gg 0 \\ \exp(v) & \text{for: } v \ll 0 \end{cases}$$

Forward Normalized Current

$$i_f = F\left[\frac{V_P - V_S}{V_t}\right]$$

Velocity Saturation Voltage

$$V_C = UCRIT \cdot NS \cdot L_{eff}$$

Note: This equation accounts for the NS multiple series device number:

$$V_{DSS} = V_C \cdot \left[\sqrt{\frac{1}{4} + \frac{V_t}{V_C}} \cdot \sqrt{i_f} - \frac{1}{2} \right]$$

Note: The V_{DSS} variable is half the value of the actual saturation voltage.

Drain-to-source Saturation Voltage for Reverse Normalized Current

$$V_{DSS}' = V_C \cdot \left[\sqrt{\frac{1}{4} + \frac{V_t}{V_C} \cdot \left(\sqrt{i_f} - \frac{3}{4} \cdot \ln(i_f) \right) - \frac{1}{2}} \right] + V_t \cdot \left[\ln\left(\frac{V_C}{2V_t}\right) - 0.6 \right]$$

Channel-length Modulation

$$\Delta V = 4 \cdot V_t \cdot \sqrt{LAMBDA \cdot \left(\sqrt{i_f} - \frac{V_{DSS}}{V_t} \right) + \frac{1}{64}}$$

$$V_{ds} = \frac{V_D - V_S}{2}$$

$$V_{ip} = \sqrt{V_{DSS}^2 + \Delta V^2} - \sqrt{(V_{ds} - V_{DSS})^2 + \Delta V^2}$$

$$L_C = \sqrt{\frac{\epsilon_{si}}{COX}} \cdot XJ$$

$$\Delta L = LAMBDA \cdot L_C \cdot \ln\left(1 + \frac{V_{ds} - V_{ip}}{L_C \cdot UCRIT}\right)$$

Equivalent Channel Length Including Channel-length Modulation and Velocity Saturation

$$L' = NS \cdot L_{eff} - \Delta L + \frac{V_{ds} + V_{ip}}{UCRIT}$$

$$L_{min} = NS \cdot L_{eff} / 10$$

Note: These equations also account for the NS multiple series device number.

$$L_{eq} = \frac{1}{2} \cdot (L' + \sqrt{L'^2 + L_{min}^2})$$

Note: This equation prevents the equivalent channel length from becoming zero or negative.

Reverse Normalized Current

Reverse normalized current:

$$i_r' = F \left[\frac{V_P - V_{ds} - V_S - \sqrt{V_{DSS}'^2 + \Delta V^2} + \sqrt{(V_{ds} - V_{DSS}')^2 + \Delta V^2}}{V_t} \right]$$

Reverse normalized current for the mobility model, intrinsic charges/ capacitances, the thermal noise model, and the NQS time-constant:

$$i_r = F \left[\frac{V_P - V_D}{V_t} \right]$$

Transconductance Factor and Mobility Reduction Due to Vertical Field

$$\beta_0 = KP_a \cdot \frac{NP \cdot W_{eff}}{L_{eq}}$$

Note: The NP (or M) device parameter returns accurate results for simulating parallel devices. Using NS (or N) for series devices is only approximate.

L_{eq} accounts for multiple NS series device numbers.

$$\eta = \begin{cases} 1/2 & \text{for NMOS} \\ 1/3 & \text{for PMOS} \end{cases}$$

$$q_{B0} = GAMMA_a \cdot \sqrt{PHI}$$

$$\beta_0' = \beta_0 \cdot \left(1 + \frac{COX}{E0 \cdot \epsilon_{si}} \cdot q_{B0} \right)$$

$$\beta = \frac{\beta_0'}{1 + \frac{COX}{E0 \cdot \epsilon_{si}} \cdot V_t \cdot |q_B + \eta \cdot q_I|}$$

For the definition of the q_B normalized depletion and the q_I inversion charges refer to the [Normalized Intrinsic Node Charges on page 189](#). Use β_0' to ensure that

$$\beta \approx \beta_0$$

when

$$q_I \ll q_B$$

. The formulation of β arises from the integration of the local effective field as a function of depletion and inversion charge densities along the channel. You do not need to specify the substrate bias dependency, because the model includes the depletion charge.

Note: The resulting mobility expression also depends on V_{DS} .

Simple Mobility Reduction Model

For compatibility with the former EKV model versions (before v2.6), you can choose the simpler mobility reduction model, which uses the `THETA` parameter.

If you do *not* specify the `E0` model parameter (see [Parameter Preprocessing on page 179](#)), simulation uses the simpler mobility model:

$$V_P' = \frac{1}{2} \cdot (V_P + \sqrt{V_P^2 + 2V_t^2})$$

$$\beta = \frac{\beta_0}{1 + THETA \cdot V_P'}$$

Specific Current

$$I_S = 2 \cdot n \cdot \beta \cdot V_t^2$$

Drain-to-source Current

$$I_{DS} = I_S \cdot (i_f - i_r')$$

For P-channel devices, I_{DS} has a negative sign.

This drain current expression is a single equation, valid in all operating regions:

- weak, moderate and strong inversion
- non-saturation
- saturation

This current is therefore not only continuous among all of these regions, but also continuously derivable.

Transconductances

Simulation derives the transconductances from the drain current:

$$g_{mg} \equiv \frac{\partial I_{DS}}{\partial V_G} \quad g_{ms} \equiv -\frac{\partial I_{DS}}{\partial V_S} \quad g_{md} \equiv \frac{\partial I_{DS}}{\partial V_{DS}}$$

In the following relationships, the source for the derivatives is a reference:

$$g_m \equiv \frac{\partial I_{DS}}{\partial V_{GS}} = g_{mg} \quad g_{mbs} \equiv \frac{\partial I_{DS}}{\partial V_{BS}} = g_{ms} - g_{mg} - g_{md} \quad g_{ds} \equiv \frac{\partial I_{DS}}{\partial V_{DS}} = g_{md}$$

This model includes the analytic derivatives.

Impact Ionization Current

$$V_{ib} = V_D - V_S - IBN \cdot 2 \cdot V_{DSS}$$

$$I_{DB} = \begin{cases} I_{DS} \cdot \frac{IBA}{IBB} \cdot V_{ib} \cdot \exp\left(\frac{-IBB \cdot L_C}{V_{ib}}\right) & \text{for: } V_{ib} > 0 \\ 0 & \text{for: } V_{ib} \leq 0 \end{cases}$$

Note: The factor 2 in the v_{ib} expression accounts for the fact that the numerical value of V_{DSS} is half of the actual saturation voltage. The substrate current is a component of the total extrinsic drain current, flowing from the drain to the bulk. This model therefore expresses the total drain current as

$$I_D = I_{DS} + I_{DB}$$

Note: The substrate current therefore also affects the total extrinsic conductances, especially the drain conductance.

Quasi-static Model Equations

MOSFET Level 55 includes both a charge-based model for transcapacitances, allowing charge-conservation during transient analysis, you can select a simpler capacitances-based model instead.

Note: The charges model is symmetrical in terms of the forward and reverse normalized currents—that is, the model is symmetrical for both the drain and source sides.

The pinch-off voltage in the dynamic model provides the short-channel effects (such as charge-sharing and reverse short-channel effects).

Dynamic Model for the Intrinsic Node Charges

$$n_q = 1 + \frac{GAMMA_a}{2 \cdot \sqrt{V_P + PHI + 10^{-6}}}$$

Normalized Intrinsic Node Charges

$$x_f = \sqrt{\frac{1}{4} + i_f}$$

$$x_r = \sqrt{\frac{1}{4} + i_r}$$

$$q_D = -n_q \cdot \left(\frac{4}{15} \cdot \frac{3x_r^3 + 6x_r^2x_f + 4x_rx_f^2 + 2x_f^3}{(x_f + x_r)^2} - \frac{1}{2} \right)$$

$$q_S = -n_q \cdot \left(\frac{4}{15} \cdot \frac{3x_f^3 + 6x_f^2x_r + 4x_fx_r^2 + 2x_r^3}{(x_f + x_r)^2} - \frac{1}{2} \right)$$

$$q_I = q_S + q_D = -n_q \cdot \left(\frac{4}{3} \cdot \frac{x_f^2 + x_fx_r + x_r^2}{x_f + x_r} - 1 \right)$$

$$q_B = \begin{cases} (-GAMMA_a \cdot \sqrt{V_P + PHI + 10^{-6}}) \cdot \frac{1}{V_t} - \left(\frac{n_q - 1}{n_q} \right) \cdot q_I & \text{for: } V'_G > 0 \\ -V'_G \cdot \frac{1}{V_t} & \text{for: } V'_G \leq 0 \end{cases}$$

$$q_G = -q_I - q_{OX} - q_B$$

q_{OX} is a fixed oxide charge, which simulation assumes is zero. The preceding equations express the charge conservation among the four nodes of the transistor.

Total Charges

$$C_{ox} = COX \cdot NP \cdot W_{eff} \cdot NS \cdot L_{eff}$$

$$Q_{(I, B, D, S, G)} = C_{ox} \cdot V_t \cdot q_{(I, B, D, S, G)}$$

Intrinsic Capacitances

Transcapacitances

Simulation derives the intrinsic capacitances from the node charges for the terminal voltages:

$$C_{xy} = \pm \frac{\partial}{\partial V_y}(Q_x) \quad x, y = G, D, S, B$$

The preceding equation uses the positive sign if $x=y$ or the negative sign otherwise. This equation produces simple, continuous analytical expressions for all transcapacitances in terms of the x_f pinch-off voltage, the x_r slope factor, and derivatives thereof, from weak to strong inversion, and from non-saturation to saturation.

Normalized Intrinsic Capacitances

Set $XQC=1$ to select a simplified capacitive dynamic model that uses the five intrinsic capacitances corresponding to the [Level 55 Equivalent Circuit on page 174](#). This model ignores the slight bias dependence of the n slope factor. The result is the following simple set of functions:

$$c_{gs} = \frac{2}{3} \cdot \left(1 - \frac{x_r^2 + x_r + \frac{1}{2}x_f}{(x_f + x_r)^2} \right)$$

$$c_{gd} = \frac{2}{3} \cdot \left(1 - \frac{x_f^2 + x_f + \frac{1}{2}x_r}{(x_f + x_r)^2} \right)$$

$$c_{gb} = \left(\frac{n_q - 1}{n_q} \right) \cdot (1 - c_{gs} - c_{gd})$$

$$c_{sb} = (n_q - 1) \cdot c_{gs}$$

$$c_{db} = (n_q - 1) \cdot c_{gd}$$

Total Intrinsic Capacitances

$$C_{(gs, gd, gb, sb, db)} = C_{ox} \cdot c_{(gs, gd, gb, sb, db)}$$

Intrinsic Noise Model Equations

The *INDS* current source models the noise between the intrinsic source and the drain. This noise includes a thermal noise component and a flicker noise component, and has the following Power Spectral Density (PSD):

$$S_{INDS} = S_{thermal} + S_{flicker}$$

Thermal Noise

The following equation calculates the PSD thermal noise component:

$$S_{thermal} = 4kT \cdot \frac{\mu_{eff}}{(NS \cdot L_{eff})^2} \cdot |Q_I| = 4kT \cdot \beta \cdot |q_I|$$

The preceding thermal noise expression is valid in all regions of operation, including for small V_{DS} .

Flicker Noise

The following equation calculates the PSD flicker noise component:

$$S_{flicker} = \frac{KF \cdot g_{mg}^2}{NP \cdot W_{eff} \cdot NS \cdot L_{eff} \cdot COX \cdot f^{AF}}$$

In some implementations, you can select different expressions.

Operating Point Information

At operating points, the following information displays to help in circuit design.

Numerical values of model internal variables

The following are the intrinsic charges and capacitances:

V_G , V_S , V_D , I_{DS} , I_{DB} , g_{mg} , g_{ms} , g_{mbs} , g_{md} , V_P , n , β , IS , if , ir' , t , $t0$.

Transconductance efficiency factor

$$tef = g_{ms} \cdot V_t / I_{DS}$$

Early voltage

$$VM = I_{DS} / g_{md}$$

Overdrive voltage

$$n \cdot (V_P - V_S) \approx V_G - VTO_a - n \cdot V_S$$

For P-channel devices, $n \cdot (V_P - V_S)$ has a negative sign.

SPICE-like threshold voltage

$$VTH = VTO_a + \Delta V_{RSCE} + \gamma' \cdot \sqrt{V'_S} - GAMMA_a \cdot \sqrt{PHI}$$

This expression is the SPICE-like threshold voltage (the source). It also accounts for charge-sharing and reverse short-channel effects on the threshold voltage.

For P-channel devices, VTH has a negative sign.

Saturation voltage

$$VDSAT = 2V_{DSS} + 4V_t$$

For P-channel devices, $VDSAT$ has a negative sign.

Saturation / non-saturation flag:

$$'SAT' \quad \text{or} \quad '1' \quad \text{for} \quad \frac{i_f}{i_r} > SATLIM$$

$$'LIN' \quad \text{or} \quad '0' \quad \text{for} \quad \frac{i_f}{i_r} \leq SATLIM$$

Note: Some simulators implement the operating point differently (some information might not be available).

Estimation and Limits of Static Intrinsic Model Parameters

If you do not have access to a parameter extraction facility, simulation can roughly estimate the EKV intrinsic model parameters from the SPICE Level 2/3 parameters as indicated in [Table 30](#). Pay attention to the units of the parameters. This estimation method generally returns reasonable results. Nevertheless, be aware that the underlying modeling in SPICE Level 2/3 and in the EKV model is not the same, even if the names and the function of several parameters are similar. Therefore, it is preferred if parameter extraction is made directly from measurements.

Lower and upper limits indicated in the table should give an idea on the order of magnitude of the parameters but do not necessarily correspond to physically meaningful limits, nor to the range specified in the parameter tables. These limits may be helpful for obtaining physically meaningful parameter sets when using nonlinear optimization techniques to extract EKV model parameters.

Table 30 Static Intrinsic Model Limits

Name	Unit	Default	Example	Lower	Upper	Estimation ¹
COX	F/m ²	0.7E-3	3.45E-3	-	-	ϵ_{ox}/TOX
XJ	m	0.1E-6	0.15E-6	0.01E-6	1E-6	XJ
VTO	V	0.5	0.7	0	2	VTO
GAMMA	\sqrt{V}	1.0	0.7	0	2	$\sqrt{2q\epsilon_{si} \cdot NSUB} / COX$
PHI ²	V	0.7	0.5	0.3	2	$2V_t \cdot \ln(NSUB / n_i)$

Chapter 4: MOSFET Models: LEVELs 50 through 74

Level 55 EPFL-EKV MOSFET Model

Table 30 Static Intrinsic Model Limits

Name	Unit	Default	Example	Lower	Upper	Estimation ¹
KP	A/V2	50E-6	150E-6	10E-6	-	UO · COX
E0	V/m	1.0E12	200E6	0.1/ (0.4 · TOX)		0.2/ (THETA · TOX)
UCRIT	V/m	2.0E6	2.3E6	1.0E6	25E6	VMAX/UO
DL	m	0	-0.15*L _{min}	-0.5*L _{min}	0.5*L _{min}	XL – 2 · LD
DW	m	0	-0.1*W _{min}	-0.5*W _{min}	0.5*W _{mi}	XW – 2 · WD
LAMBDA	-	0.5	0.8	0	3	-
LETA	-	0.1	0.3	0	2	-
WETA	-	0.25	0.2	0	2	-
Q0	As/	0.0	230E-6	0	-	-
LK	m	0.29E-6	0.4E-6	0.05E-6	2E-6	-
IBA	1/m	0.0	2.0E8	0.0	5.0E8	ALPHA · VCR/ L _C
IBB	V/m	3.0E8	2.0E8	1.8E8	4.0E8	VCR/ L _C
IBN	-	1.0	0.6	0.4	1.0	-

1. Also compare with optional process parameters.

2. The minimum value of PHI also determines the minimum value of the pinch-off voltage. Due to the intrinsic temperature dependence of PHI, higher temperatures use a lower value, which limits the range of simulation for small currents.

$$\epsilon_{ox}=0.0345E-9 \text{ F/m} \quad q=1.609E-19 \text{ C} \quad k=1.381E-23 \text{ J/K} \quad L_c = \sqrt{\epsilon_{si} \cdot XJ / COX}$$

$$\epsilon_{si}=0.104E-9 \text{ F/m} \quad n_i=1.45E16 \text{ m}^{-3} \quad V_t=kT/q=0.0259 \text{ V (at room temperature)}$$

Note: Parameters in this table use m (meter) as the length unit. L_{min} is the minimum drawn length of transistors. W_{min} is the minimum drawn width of transistors. Example values are shown for enhancement N-channel devices.

Model Updates Description

Synopsys has made several improvements to the original EKV v2.6 MOSFET model. Wherever possible, these enhancements maintain backward compatibility with previous versions.

Revision I, September 1997

Description:

The narrow channel effect on the substrate factor was revised to improve the transcapacitances behavior. The narrow channel effect is no longer a function of the v_s source voltage, but of the v_p pinch-off voltage.

Consequence:

The $WETA$ and DW narrow channel effect parameters require different numerical values to achieve the same effect.

Revision II, July 1998

Intrinsic time constant

Description:

Simulation calculates the τ_0 intrinsic time constant as a function of the effective β factor (including vertical field dependent mobility and short-channel effects), instead of the maximum mobility using the KP parameter.

Consequence:

The NQS time constant has an additional gate voltage dependence, resulting in more conservative (lower) estimation of the NQS time constant at high V_G , and additional dependence on short-channel effects.

Thermal noise

Description:

Simulation calculates the S_{thermal} thermal noise power spectral density as a function of the effective β factor (including vertical field dependent mobility and short-channel effects), instead of the maximum mobility using the K_P parameter.

Consequence:

S_{thermal} has an additional gate voltage and short-channel effect dependence.

Optional process parameters to calculate electrical intrinsic parameters

Description:

This option calculates the electrical parameters as a function of the optional parameters:

~~COX~~→~~TOX~~
GAMMA and PHI→~~NSUB~~
~~VTO~~→~~VFB~~
~~KP~~→~~UO~~
~~UCRIT~~→~~VMAX~~

cm is the length unit for the $NSUB$ and UO parameters.

Consequence:

These parameters accommodate scaling behavior and allow meaningful statistical circuit simulation, due to decorrelation of physical effects. If you use these optional parameters, this version is compatible with former revisions, except for the default calculation of the parameters.

Optional simplified mobility model

Description:

The simple mobility model used in former model versions by using the θ parameter, was reinstated as an option.

Consequence:

This mobility model simplifies adaptation from earlier model versions to the current version.

Parameter synonyms

Description:

You can use $E0$ and $Q0$ as synonyms for the EO and QO parameters.

Consequence:

This option accommodates some simulators that use only alphabetic characters.

Operating point information

Description:

This enhancement models the analytical expression for the SPICE-like VTH threshold voltage in the operating point information to include the charge-sharing and reverse short-channel effects. This option modifies the analytical expression for the VDSAT saturation voltage in the operating point information so it has a non-zero value in weak inversion.

Consequence:

This enhancement improves design information.

Corrections from EPFL R11, March, 1999

Equation 45, Equation 53, Equation 54, and Equation 58 were corrected for multiple series device behavior by using the NS parameter.

Corrections from EPFL R12, July 30, 1999

EPFL released the following corrections.

Correction 1- 99/07/30 mb (r12) corrected dGAMMAprime_dVG (narrow channel). An error in the analytical model derivatives of the GAMMAprime variable affected the transconductances and transcapacitances.

Correction 2- 99/07/30 mb (r12) prevents PHI from being smaller than 0.2, both at init and after updating the temperature. For some CMOS technologies, PHI parameter values are as low as 400mV, required to account for particular process details. If you increase the temperature from room temperature, PHI decreases due to its built-in temperature dependence. As a result, PHI attains very low values or even becomes negative when it reaches 100degC. For the model to function at these temperatures, PHI has a lower limit of 200mV. The usual range for this parameter is well above this value (600mV to 1V).

Correction 3- 99/06/28 mb (r12) fixed COX/KP initialization (rg).

Correction 4- 99/05/04 mb (r12) completed parameter initialization for XQC, DL, and DW, and removed IBC and ibc (cd).

Level 58 University of Florida SOI

UFSOI includes non-fully depleted (NFD) and fully depleted (FD) SOI models (a dynamic mode must not operate between NFD and FD) that separately describe two main types of SOI devices. The UFSOI version 4.5F model is Level 58 in the Synopsys MOSFET models. This model is described in the *UFSOI Model User's Manual* at:

<http://www.soi.tec.ufl.edu/>

Some processes use an external contact to the body of the device. The Synopsys MOSFET model supports only a 4-terminal device, which includes drain, front gate, source, and back gate (or substrate). The additional body contact is currently not supported so it floats.

The effects of parasitic diodes in SOI are different from those in the bulk MOSFET. The SOI model does not include the MOSFET *junction* model (ACM), developed for bulk MOSFETs.

The general syntax for MOSFET Level 58 in a netlist is:

```
Mxxx nd ngf ns [ngb] mname [L=val] [W=val] [M=val]
+ [AD=val] [AS=val] [PD=val] [PS=val] [NRD=val]
+ [NRS=val] [NRB=val] [RTH=val] [CTH=val] [off]
+ [IC=Vds,Vgfs,VGbs]
```

In the preceding syntax, angle brackets denote optional parameters. The arguments are identical to those for the BSIM3-SOI model, but the thermal resistance and capacitance have different names.

Table 31 Thermal Resistance and Capacitance Names

Name	Description
RTH	Thermal resistance, unit in $K \cdot W^{-1}$, default is 0.0.
CTH	Thermal capacitance, unit in $W \cdot s \cdot K^{-1}$, default is 0.0.

Notes:

- The default value for channel length (L) and width (W) is 1.0e-6.
- The present version supports only 4 nodes (only floating-body devices). AB is typically zero; specify it accordingly.

- If you activate the self-heating option (on the model line), RTH and CTH define the thermal impedance of the device. Typical values are 5e3 (for RTH) and 1e-12 (for CTH), but these can vary widely from one device to another.
- For $M > 1$, you must specify W, AD, AS, NRD, NRS, NRB, PDJ, PSJ, RTH, and CTH per gate finger.
- The initial condition (IC) is in the following order: Vds drain voltage, Vgfs front gate voltage, and Vbgs back gate voltage.

Level 58 FD/SOI MOSFET Model Parameters

The following tables describe Level 58 model parameters for the fully depleted (FD) SOI, including parameter names, descriptions, units, defaults, and typical notes.

Table 32 MOSFET Level 58 Flag Parameters

Parameter	Unit	Default	Typical Value	Description
Level	-	-	-	Level 57 for UFSOI
NFDMOD	-	0	0	Model selector (0: FD)
BJT	-	1	1	Parasitic bipolar flag (0: off; 1: on)
SELFT	-	0	0	Self-heating flag: <ul style="list-style-type: none"> ▪ 0: no self-heating ▪ 1: approximate model ▪ 2: full self-heating
TPG	-	1	-	Type of gate polysilicon: <ul style="list-style-type: none"> ▪ +1: opposite to body ▪ -1: same as body
TPS	-	-1	-	Type of substrate: <ul style="list-style-type: none"> ▪ +1: opposite to body ▪ -1: same as body

Table 33 MOSFET Level 58 Structural Parameters

Parameter	Unit	Default	Typical Value	Description
TOXF	m	1.0e-8	(3-8)x10-9	Front-gate oxide thickness
TOXB	m	0.5e-6	(80-400)x10-9	Back-gate oxide thickness
NSUB	cm-3	1.0e15	1015 -1017	Substrate doping density
NGATE	cm-3	0.0	1019 -1020	Poly-gate doping density (0 for no poly-gate depletion)
NDS	cm-3	5.0e19	1019 -1020	Source/drain doping density
TB	m	0.1e-6	(30-100)x10-9	Film (body) thickness
NBODY	cm-3	5.0e16	1017 -1018	Film (body) doping density
LLDD	m	0.0	(0.05-0.2)x10-6	LDD/LDS region length (0 for no LDD)
NLDD	cm-3	5.0e19	1x1019	LDD/LDS doping density (>1e19: LDD/LDS treated as D/S extensions)
DL	m	0.0	(0.05-0.15)x10-6	Channel-length reduction
DW	m	0.0	(0.1-0.5)x10-6	Channel-width reduction

Table 34 MOSFET Level 58 Electrical Parameters

Parameter	Unit	Default	Typical Value	Description
NQFF	cm^{-2}	0.0	$\sim 10^{10}$	Front oxide fixed charge (normalized)
NQFB	cm^{-2}	0.0	$\sim 10^{11}$	Back oxide fixed charge (normalized)
NQFSW	cm^{-2}	0.0	$\sim \pm 10^{12}$	Effective sidewall fixed charge (0 for no narrow-width effect)
NSF	$\text{cm}^{-2} \cdot \text{eV}^{-1}$	0.0	$\sim 10^{10}$	Front surface state density
NSB	$\text{cm}^{-2} \cdot \text{eV}^{-1}$	0.0	$\sim 10^{11}$	Back surface state density
QM	-	0.0 -0.5		Energy quantization parameter (0 for no quantization)
UO	$\text{cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$	7.0e2	200-700 (nMOS) 70-400 (pMOS)	Low-field mobility
THETA	$\text{cm} \cdot \text{V}^{-1}$	7.0e2	$(0.1-3) \times 10^{-6}$	Mobility degradation coefficient
VSAT	$\text{cm} \cdot \text{s}^{-1}$	1.0e-6	$(0.5-1) \times 10$	Carrier saturated drift velocity
ALPHA	cm^{-1}	0.0	2.45×10^6	Impact-ionization coefficient (0 for no impact ionization)
BETA	$\text{V} \cdot \text{cm}^{-1}$	0.0	1.92×10^6	Impact-ionization exponential factor (0 for no impact ionization)

Table 34 MOSFET Level 58 Electrical Parameters

Parameter	Unit	Default	Typical Value	Description
BGIDL	V· cm-1	0.0	(4-8)x10 ⁹	Exponential factor for gate-induced drain leakage (0 for no GIDL)
GAMMA	-	0.3	0.3-1.0	BOX fringing field weighting factor
KAPPA	-	0.5	0.5-1.0	BOX fringing field weighting factor
JRO	A· m-1	1.0e-10	10-11 -10-9	Body-source/drain junction recombination current coefficient
M	-	2.0	1.0-2.0	Body-source/drain junction recombination ideality factor
LDIFF	m	1.0e-7	(0.1-0.5)x10 ⁻⁶	Effective diffusion length in source/drain
SEFF	cm· s-1	1.0e5	(0.5-5)x10 ⁵	Effective recombination velocity in source/drain
CGFDO	F· m-1	0.0	1x10 ⁻¹⁰	Gate-drain overlap capacitance
CGFSO	F· m-1	0.0	1x10 ⁻¹⁰	Gate-source overlap capacitance
CGFBO	F· m-1	0.0	0.0	Gate-body overlap capacitance
RD	ohm· m	0.0	200-1000	Specific drain parasitic resistance

Table 34 MOSFET Level 58 Electrical Parameters

Parameter	Unit	Default	Typical Value	Description
RS	ohm·m	0.0	200-1000	Specific source parasitic resistance
RHOB	ohm/sq.	0.0	30x103	Body sheet resistance
FNK	F·A	0.0	0-10-2	Flicker noise coefficient
FNA	-	1.0	0.5-2	Flicker noise exponent

Table 35 MOSFET Level 58 Optional Parameters

Parameter	Unit	Default	Typical Value	Description
VFBF	V	calc.	-1 (nMOS) 1 (pMOS)	Front-gate flatband voltage
VFBB	V	calc.	-	Back-gate flatband voltage
WKF	V	calc.	~ VFBF	Front-gate work function difference
WKB	V	calc.	-	Back-gate work function difference
TAUO	s	calc.	10-7 -10-5	Carrier lifetime in lightly doped regions
BFACT	-	0.3	0.1-0.5	V _{DS} averaging factor for mobility degradation
FVBJT	-	0.0	0-1	BJT current directional partitioning factor (0 for lateral 1D flow)
RHOSD	ohm/sq.	0.0	50	Source/drain sheet resistance

Level 58 NFD/SOI MOSFET Model Parameters

The following tables describe the Level 58 model parameters for non fully depleted (NFD) SOI, including parameter names, descriptions, units, defaults, and typical notes.

Table 36 MOSFET Level 58 Flag Parameters

Parameter	Unit	Default	Typical Value	Description
Level	-	-	-	Level 57 for UFSOI
NFDMOD	-	0	-	Model selector (1: NFD)
BJT	-	1	1	Parasitic bipolar flag: <ul style="list-style-type: none"> ▪ 0: off ▪ 1: on
SELFT	-	0	0	Self-heating flag: <ul style="list-style-type: none"> ▪ 0: no self-heating ▪ 1: approximate model ▪ 2: full self-heating
TPG	-	1	1	Type of gate polysilicon <ul style="list-style-type: none"> ▪ +1: opposite to body ▪ -1: same as body
TPS	-	-1	-1	Type of substrate <ul style="list-style-type: none"> ▪ +1: opposite to body ▪ -1: same as body)

Table 37 MOSFET Level 58 Structural Parameters

Parameter	Unit	Default	Typical Value	Description
TOXF	m	1.0e-8	(3-8)x10-9	Front-gate oxide thickness
TOXB	m	0.5e-6	(80-400)x10-9	Back-gate oxide thickness
NSUB	cm-3	1.0e15	1015 -1017	Substrate doping density

Table 37 MOSFET Level 58 Structural Parameters

Parameter	Unit	Default	Typical Value	Description
NGATE	cm-3	0.0	1019 -1020	Poly-gate doping density (0 for no poly-gate depletion)
NDS	cm-3	5.0e19	1019 -1020	Source/drain doping density
TF	m	0.2e-6	(3-8)x10-9	Silicon film thickness
TB	m	0.1e-6	(30-100)x10-9	Film (body) thickness
THALO	m	0.0	-	Halo thickness (0 for no halo)
NBL	cm-3	5.0e16	1017 -1018	Low body doping density
NBH	cm-3	5.0e17	1019 -1020	Halo doping density
NHALO	cm-3	-	~1018	Halo doping density
LRSCE	m	0.0	~0.1x10-6	Characteristic length for reverse short-channel effect (0 for no RSCE)
LLDD	m	0.0	(0.05-0.2)x10-6	LDD/LDS region length (0 for no LDD)
NLDD	cm-3	5.0e19	1x1019	LDD/LDS doping density (>1e19: LDD/LDS treated as D/S extensions)
DL	m	0.0	(0.05-0.15)x10-6	Channel-length reduction
DW	m	0.0	(0.1-0.5)x10-6	Channel-width reduction

Table 38 MOSFET Level 58 Electrical Parameters

Parameter	Unit	Default	Typical Value	Description
NQFF	cm ⁻²	0.0	~ 1010	Front oxide fixed charge (normalized)
NQFB	cm ⁻²	0.0	~ 1011	Back oxide fixed charge (normalized)
NQFSW	cm ⁻²	0.0	~ ± 1012	Effective sidewall fixed charge (0 for no narrow-width effect)
QM	-	0.0 -0.5		Energy quantization parameter (0 for no quantization)
UO	cm ² · V ⁻¹ · s ⁻¹	7.0e2	200-700 (nMOS) 70-400 (pMOS)	Low-field mobility
THETA	cm· V ⁻¹	7.0e2	(0.1-3)x10 ⁻⁶	Mobility degradation coefficient
VSAT	cm· s ⁻¹	1.0e-6	(0.5-1)x10	Carrier saturated drift velocity
ALPHA	cm ⁻¹	0.0	2.45x10 ⁶	Impact-ionization coefficient (0 for no impact ionization)
BETA	V· cm ⁻¹	0.0	1.92x10 ⁶	Impact-ionization exponential factor (0 for no impact ionization)
BGIDL	V· cm ⁻¹	0.0	(4-8)x10 ⁹	Exponential factor for gate-induced drain leakage (0 for no GIDL)

Table 38 MOSFET Level 58 Electrical Parameters

Parameter	Unit	Default	Typical Value	Description
NTR	cm ⁻³	0.0	10 ¹⁴ -10 ¹⁵	Effective trap density for trap-assisted junction tunneling (0 for no tunneling)
JRO	A·m ⁻¹	1.0e-10	10 ⁻¹¹ -10 ⁻⁹	Body-source/drain junction recombination current coefficient
M	-	2.0	1.0-2.0	Body-source/drain junction recombination ideality factor
LDIFF	m	1.0e-7	(0.1-0.5)x10 ⁻⁶	Effective diffusion length in source/drain
SEFF	cm·s ⁻¹	1.0e5	(0.5-5)x10 ⁵	Effective recombination velocity in source/drain
CGFDO	F·m ⁻¹	0.0	1x10 ⁻¹⁰	Gate-drain overlap capacitance
CGFSO	F·m ⁻¹	0.0	1x10 ⁻¹⁰	Gate-source overlap capacitance
CGFBO	F·m ⁻¹	0.0	0.0	Gate-body overlap capacitance
RD	ohm·m	0.0	200-1000	Specific drain parasitic resistance
RS	ohm·m	0.0	200-1000	Specific source parasitic resistance
RHOB	ohm/sq.	0.0	30x10 ³	Body sheet resistance

Table 38 MOSFET Level 58 Electrical Parameters

Parameter	Unit	Default	Typical Value	Description
FNK	F· A	0.0	0-10-2	Flicker noise coefficient
FNA	-	1.0	0.5-2	Flicker noise exponent

Table 39 Optional MOSFET Level 58 Parameters

Parameter	Unit	Default	Typical Value	Description
VFBB	V	calc.	-1 (nMOS) 1 (pMOS)	Front-gate flatband voltage
VFBB	V	calc.	-	Back-gate flatband voltage
WKF	V	calc.	~ VFBB	Front-gate work function difference
WKB	V	calc.	-	Back-gate work function difference
TAUO	s	calc.	10-7 -10-5	Carrier lifetime in lightly doped regions
BFACT	-	0.3	0.1-0.5	V_{DS} -averaging factor for mobility degradation
FVBJT	-	0.0	0-1	BJT current directional partitioning factor (0 for lateral 1D flow)
RHOSD	ohm/sq.	0.0	50	Source/drain sheet resistance

Notes:

- The model line must include LEVEL=58 and NFDMOD=0 for FD, or NFDMOD=1 for NFD devices.
- Specifying VFBF turns off the narrow-width effect defined by NQFSW (which can be positive or negative) and the reverse short-channel effect defined by LRSCE (and NBH or NHALO if specified); the latter effect is also turned off if you specify WKF.
- For floating-body devices, CGFBO is small; you should set it to 0.
- JRO and SEFF influence the gain of the BJT, but LDIFF affects only bipolar charge storage in the source/drain. If you specify THALO, then NBH and NHALO also influence the BJT gain.
- Loosely correlate the TAUO value with JRO in accord with basic pn-junction recombination/generation properties. Its default value is based on JRO, which is appropriate for short L; for long L, body generation predominates over that in the junctions so specify TAUO.
- The non-local impact-ionization model is physical so do not arbitrarily vary its parameters.
- The LDD option intensifies the model so set LLDD to 0 for large-scale circuit simulation, and add the unbiased LDD resistance to RD; this simplification stops if you specify NLDD > 1e19.

Level 58 Template Output

For a list of output template parameters in the MOSFET models, and which parameters this model supports, see [Table 4 on page 21](#).

Level 61 RPI a-Si TFT Model

Level 61 in the Synopsys MOSFET models is an AIM-SPICE MOS15 amorphous silicon (a-Si) thin-film transistor (TFT) model, developed by Rensselaer Polytechnic Institute.

Model Features

Features of the AIM-SPICE MOS15 a-Si TFT model include:

- Modified charge control model; induced charge trapped in localized states
- Above threshold includes:
 - Field effect mobility becoming a function of gate bias
 - Band mobility dominated by lattice scattering
- Below threshold includes:
 - Fermi level located in deep localized states
 - Relate position of Fermi level, including the deep DOS, back to the gate bias
- Empirical expression for current at large negative gate biases for hole-induced leakage current
- Applies interpolation techniques to equations to unify the model

Using Level 61 with Synopsys Simulators

To simulate using the AIM-SPICE MOS15 a-Si TFT model:

1. Set Level=61 to identify the model as the AIM-SPICE MOS15 a-Si TFT model.
2. The default value for L is 100 μm , and the default value for W is 100 μm .
3. Level 61 is a 3-terminal model. This model does not include a bulk node; therefore simulation does not append parasitic drain-bulk or source-build diodes are appended to the model. You can specify a fourth node, but it does not affect simulation results.
4. The default room temperature is 25°C in Synopsys circuit simulators, but is 27°C in most other simulators. When comparing to other simulators, use `.TEMP 27` or `.OPTION TNOM=27` to set the simulation temperature to 27 in the netlist.

Example

The following is an example of how Level 61 modifies the Synopsys MOSFET model and element statement.

```

mckt drain gate source nch L=10e-6 W=10e-6
.MODEL nch nmos Level=61
+ alphasat=0.6 cgdo=0.0 cgso=0.0 def0=0.6
+ delta=5.0 el=0.35 emu=0.06 eps=11
+ epsi=7.4 gamma=0.4 gmin=1e23 iol=3e-14
+ kasat=0.006 kvt=-0.036 lambda=0.0008 m=2.5
+ muband=0.001 rd=0.0 rs=0.0 sima0=1e-14
+ tnom=27 tox=1.0e-7 v0=0.12 vaa=7.5e3
+ vdsl=7 vfb=-3 vgs1=7 vmin=0.3 vto=0.0

```

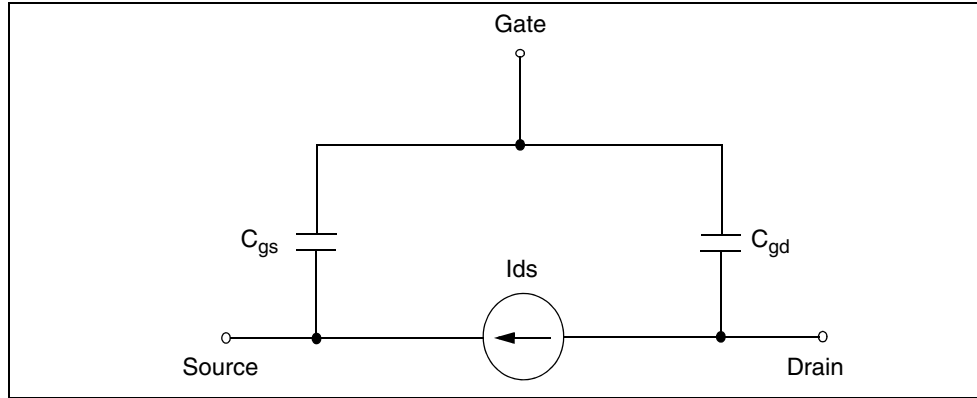
Name	Unit	Default	Description
ALPHASAT	-	0.6	Saturation modulation parameter
CGDO	F/m	0.0	Gate-drain overlap capacitance per meter channel width
CGSO	F/m	0.0	Gate-source overlap capacitance per meter channel width
DEF0	eV	0.6	Dark Fermi level position
DELTA	-	5	Transition width parameter
EL	eV	0.35	Activation energy of the hole leakage current
EMU	eV	0.06	Field effect mobility activation energy
EPS	-	11	Relative dielectric constant of the substrate
EPSI	-	7.4	Relative dielectric constant of the gate insulator
GAMMA	-	0.4	Power law mobility parameter
GMIN	m ⁻³ eV ⁻¹	1E23	Minimum density of deep states
IOL	A	3E-14	Zero-bias leakage current parameter
KASAT	1/° X	0.006	Temperature coefficient of ALPHASAT
KVT	V/° X	-0.036	Threshold voltage temperature coefficient

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Level 61 RPI a-Si TFT Model

Name	Unit	Default	Description
LAMBDA	1/V	0.0008	Output conductance parameter
M	-	2.5	Knee shape parameter
MUBAND	m^2/Vs	0.001	Conduction band mobility
RD	m	0.0	Drain resistance
RS	m	0.0	Source resistance
SIGMA0	A	1E-14	Minimum leakage current parameter
TNOM	oC	25	Parameter measurement temperature
TOX	m	1E-7	Thin-oxide thickness
V0	V	0.12	Characteristic voltage for deep states
VAA	V	7.5E3	Characteristic voltage for field effect mobility
VDSL	V	7	Hole leakage current drain voltage parameter
VFB	V	-3	Flat band voltage
VGSL	V	7	Hole leakage current gate voltage parameter
VMIN	V	0.3	Convergence parameter
VTO	V	0.0	Zero-bias threshold voltage

Equivalent Circuit



Model Equations

Drain Current

$$I_{ds} = I_{leakage} + I_{ab}, I_{ab} = g_{ch} V_{dse} (1 + LAMBDA \cdot V_{ds})$$

$$V_{dse} = \frac{V_{ds}}{[1 + (V_{ds} / V_{sate})^M]^{1/M}}$$

$$V_{sate} = \alpha_{sat} V_{gte}$$

$$g_{ch} = \frac{g_{chi}}{1 + g_{chi}(RS + RD)}, g_{chi} = q n_s W \cdot MUBAND / L$$

$$n_s = \frac{n_{sa} n_{sb}}{n_{sa} + n_{sb}}$$

$$n_{sa} = \frac{EPSI \cdot V_{gte}}{(q \cdot TOX)} \cdot \left(\frac{V_{gte}}{V_{aat}} \right)^{GAMMA}$$

$$n_{sb} = n_{so} \left(\frac{t_m}{TOX} \frac{V_{gfbe} EPSI}{V0 EPS} \right)^{\frac{2 \cdot V0}{V_e}}$$

Chapter 4: MOSFET Models: LEVELs 50 through 74

Level 61 RPI a-Si TFT Model

$$n_{so} = N_c t_m \frac{V_e}{V_0} \exp\left(-\frac{DEF0}{V_{th}}\right), N_c = 3.0 \cdot 10^{25} m^{-3}$$

$$V_e = \frac{2 \cdot V_0 \cdot V_{tho}}{2 \cdot V_0 - V_{th}}, t_m = \sqrt{\frac{EPS}{2q \cdot GMIN}}$$

$$V_{gte} = \frac{VMIN}{2} \left[1 + \frac{V_{gt}}{VMIN} + \sqrt{DELTA^2 + \left(\frac{V_{gt}}{VMIN} - 1 \right)^2} \right]$$

$$V_{gt} = V_{gs} - V_T$$

$$V_{gfbe} = \frac{VMIN}{2} \left[1 + \frac{V_{gfb}}{VMIN} + \sqrt{DELTA^2 + \left(\frac{V_{gfb}}{VMIN} - 1 \right)^2} \right]$$

$$V_{gfb} = V_{gs} - VFB, I_{leakage} = I_{hl} + I_{min}$$

$$I_{hl} = IOL \left[\exp\left(\frac{V_{ds}}{VDSL}\right) - 1 \right] \exp\left(-\frac{V_{gs}}{VGSL}\right) \exp\left[\frac{EL}{q} \left(\frac{1}{V_{tho}} - \frac{1}{V_{th}} \right) \right]$$

$$I_{min} = SIGMA0 \cdot V_{ds}$$

Temperature Dependence

$$V_{tho} = k_B \cdot TNOM / q, V_{th} = k_B \cdot (TEMP) / q$$

$$V_{aat} = VAA \exp\left[\frac{EMU}{q \cdot GAMMA} \left(\frac{1}{V_{th}} - \frac{1}{V_{tho}} \right) \right]$$

$$V_T = VTO + KVT(TEMP - TNOM)$$

$$\alpha_{sat} = ALPHASAT + KASAT(TEMP - TNOM)$$

Capacitance

$$C_{gs} = C_f + \frac{2}{3} C_{gc} \left[1 - \left(\frac{V_{sate} - V_{dse}}{2V_{sate} - V_{dse}} \right)^2 \right]$$

$$C_{gd} = C_f + \frac{2}{3} C_{gc} \left[1 - \left(\frac{V_{sate}}{2V_{sate} - V_{dse}} \right)^2 \right]$$

$$C_f = 0.5 \cdot EPS \cdot W, \left(C_{gs} = q \frac{dn_{sc}}{dV_{gs}} \right)$$

$$n_{sc} = \frac{n_{sac} n_{sbc}}{n_{sac} + n_{sbc}}, \left(n_{sa} = \frac{EPSI \cdot V_{gte}}{(q \cdot TOX)} \cdot \left(\frac{V_{gte}}{V_{aat}} \right)^{GAMMA} \right)$$

$$n_{sbc} = n_{sb}$$

Level 62 RPI Poli-Si TFT Model

Level 62 is an AIM-SPICE MOS16 poly-silicon (Poli-Si) thin-film transistor (TFT) model, developed by Rensselaer Polytechnic Institute.

The following topics are discussed in the next sections.

- [Model Features](#)
- [Using Level 62 with Synopsys Simulators](#)
- [Equivalent Circuit](#)
- [Model Equations](#)
- [Version 2 Model Equations](#)

Model Features

Features of the AIM-SPICE MOS16 Poli-Si TFT model include:

- A design based on the crystalline MOSFET model
- Field effect mobility that becomes a function of the gate bias
- Effective mobility that accounts for trap states:
 - For low V_{gs} , it is the power law
 - For high V_{gs} , it is the constant
- Reverse bias drain current function of the electric field near the drain and the temperature
- A design independent of the channel length

- A unified DC model that includes all four regimes for channel lengths down to 4 μm :
 - Leakage (thermionic emission)
 - Subthreshold (diffusion-like model)
 - Above threshold (c-Si-like with mFet)
 - Kink (impact ionization with feedback)
- An AC model accurately reproduces the C_{gc} frequency dispersion
- Automatic scaling of model parameters that accurately model a wide range of device geometries

Using Level 62 with Synopsys Simulators

To simulate using the AIM-SPICE MOS16 Poli-Si TFT model:

1. Set `LEVEL=62` to identify the model as the AIM-SPICE MOS16 Poli-Si TFT model.
2. The default value for `L` is 100 μm , and the default value for `w` is 100 μm .
3. Level 62 is a 3-terminal model. This model does not include a bulk node; therefore, simulation does not append a parasitic drain-bulk or source-bulk diode to the model. You can specify a fourth node, but it does not affect the simulation results.
4. The default room temperature is 25°C in Synopsys circuit simulators, but is 27°C in most other simulators. When comparing to other simulators, use `.TEMP 27` or `.OPTION TNOM=27` to set the simulation temperature to 27°C in the netlist.

The following is an example of how Level 62 modifies a MOSFET device model and element statement:


```
mckt drain gate source nch L=10e-6 W=10e-6
.MODEL nch nmos Level=62
+ asat=1 at=3e-8 blk=0.001 bt=0.0 cgdo=0.0
+ cgso=0.0 dasat=0.0 dd=1.4e-7 delta=4.0
+ dg=2.0e-7 dmul=0.0 dvt=0.0 dvto=0.0 eb=0.68
+ eta=7 etac0=7 etac00=0 i0=6.0 i00=150
+ lasat=0lkink=19e-6 mc=3.0 mk=1.3 mmu=3.0
+ mu0=100 mul=0.0022 mus=1.0 rd=0.0 rdx=0.0
+ rs=0.0 rsx=0.0 tnom=27 tox=1.0e7 vfb=-0.1
+ vkink=9.1 von=0.0 vto=0.0
```

Table 40 MOSFET Level 62 Model Parameters

Name	Unit	Default	Description
ASAT	-	1	Proportionality constant of Vsat
AT	m/V	3E-8	DIBL parameter 1
BLK	-	0.001	Leakage barrier lowering constant
BT	m · V	1.9E-6	DIBL parameter 2
CAPMOD	-	0	Model capacitance selector (zero recommended)
CGDO	F/m	0	Gate-drain overlap capacitance per meter channel width
CGSO	F/m	0	Gate-source overlap capacitance per meter channel width
DASAT	1/° C	0	Temperature coefficient of ASAT
DD	m	1400 Å	Vds field constant
DELTA	-	4.0	Transition width parameter
DG	m	2000 Å	Vgs field constant
DMU1	$\chi\mu^2/\zeta \propto C$	0	Temperature coefficient of MU1
DVT	V	0	The difference between VON and the threshold voltage
DVTO	V/° C	0	Temperature coefficient of VTO

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Level 62 RPI Poli-Si TFT Model

Table 40 MOSFET Level 62 Model Parameters

Name	Unit	Default	Description
EB	EV	0.68	Barrier height of the diode
ETA	-	7	Subthreshold ideality factor
ETAC0	-	ETA	Capacitance subthreshold ideality factor at zero-drain bias
ETAC00	1/V	0	Capacitance subthreshold coefficient of the drain bias
I0	A/m	6.0	Leakage scaling constant
I00	A/m	150	Reverse diode saturation current
KSS	-	0	Small signal parameter (zero is recommended)
LASAT	M	0	Coefficient for length dependence of ASAT
LKINK	M	19E-6	Kink effect constant
MC	-	3.0	Capacitance knee shape parameter
MK	-	1.3	Kink effect exponent
MMU	-	3.0	Low field mobility exponent
MU0	cm ² /Vs	100	High field mobility
MU1	cm ² /Vs	0.0022	Low field mobility parameter
MUS	cm ² /Vs	1.0	Subthreshold mobility
RD	μ	0	Drain resistance
RDX	Ω	0	Resistance in series with C _{gd}
RS	μ	0	Source resistance
RSX	Ω	0	Resistance in series with C _{gs}

Table 40 MOSFET Level 62 Model Parameters

Name	Unit	Default	Description
TNOM	°C	25	Parameter measurement temperature
TOX	m	1e-7	Thin-oxide thickness
V0	V	0.12	Characteristic voltage for deep states
VFB	V	-0.1	Flat band voltage
VKINK	V	9.1	Kink effect voltage
VON	V	0	On-voltage
VSI	V	2.0	vgs dependence parameter
VST	V	2.0	vgs dependence parameter
VTO	V	0	Zero-bias threshold voltage
ZERO	-	0	Flag for capacitance calculations in capmod=1 <ul style="list-style-type: none"> capmod=1: set the 0 capacitance value capmod=0: calculation capacitance
XL	m	0	Length bias accounts for the masking and etching effects
XW	m	0	Width bias accounts for the masking and etching effects
LMLT	-	1	Length shrink factor
WMLT	-	1	Width shrink factor
COMPATIBLE=0 1	-	0	<ul style="list-style-type: none"> COMPATIBLE=0: HSPICE implementation of AIM-SPICE MOS 16 RPI TFT model. COMPATIBLE=1: Enables compatibility to a commonly-used TFT model by the industry.

Table 41 Model Parameters Specific to Version 2

Name	Unit	Default	Description
VERSION	-	1	1=Version 1 2=Version 2
ME (MS)	-	2.5	Long channel saturation transition parameter
META	-	1	ETA floating-body parameter
MSS	-	1.5	Vdse transition parameter
VMAX	m/s	4.00E+004	Saturation velocity
THETA	M/V	0	Mobility degradation parameter
ISUBMOD	-	0	Channel length modulation selector: 0 – uses LAMBDA 1 – uses LS and VP
LAMBDA	1/V		Channel length modulation parameter
LS	-	3.50E-008	Channel length modulation parameter
VP	V	0.2	Channel length modulation parameter
INTDSNOD	-	1 if VERSION=1 0 if VERSION=2	Extrinsic series resistance mode selector: 0 - uses internal approximation for drain and source resistances 1 – uses drain and source resistances as extrinsic elements
VSIGMAT	V	VST, if specified 1.7, otherwise	VGS dependence parameter
VSIGMA	V	VSI, if specified 0.2, otherwise	VGS dependence parameter

Table 41 Model Parameters Specific to Version 2

Name	Unit	Default	Description
DIBLMOD	-	1	DIBL model selector
VSIGMAT	V	VST, if specified, 1.7 otherwise	VGS dependence parameter
VSIGMA	V	VSI, if specified, 0.2 otherwise	VGS dependence parameter
LMU0	m	0	MU0 length dependence parameter
LMU1	m	0	MU1 length dependence parameter
LME	m	0	ME length dependence parameter

Table 42 Self-Heating Parameters

Name	Unit	Default	Description
SHMOD	-	0	Self-heating flag
RTH0	m°C/W	0	Thermal resistance per unit width
CTH0	Ws/m°C	1.00E-005	Thermal capacitance per unit width
WTH0	m	0	Width offset for thermal resistance and capacitance scaling

Table 43 ACM Parameters for Drain and Source Resistance Calculus Specific to HSPICE

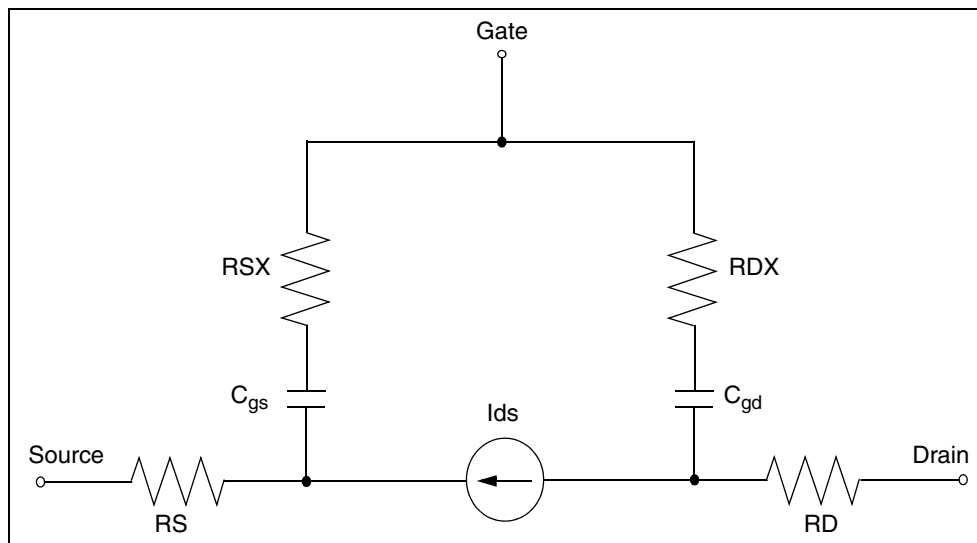
Name	Unit	Default	Description
ACM	-	-	Area calculation method
LD	m	0	Lateral diffusion into channel from source and drain diffusion
WD	m	0	Lateral diffusion into channel from bulk along width

Table 43 ACM Parameters for Drain and Source Resistance Calculus Specific to HSPICE

Name	Unit	Default	Description
HDIF	m	0	Length of heavily doped diffusion
LDIF	m	0	Length of heavily doped region adjacent to gate
RDC	ohm	0	Additional drain resistance due to contact
RSC	ohm	0	Additional source resistance due to contact
RSH	ohm/sq	0	Drain and source diffusion sheet resistance

Note: Source and drain resistances are calculated similarly to other HSPICE MOSFET models, which are based on the value of ACM .

Equivalent Circuit



Model Equations

The following sections discuss these equations:

- Drain Current
- Threshold Voltage
- Temperature Dependence
- Capacitance
- Geometry Effect
- Self Heating

Drain Current

Total Current

$$I_{ds} = \frac{I_a \cdot I_{sub}}{I_a + I_{sub}} \cdot (1 + I_{kink}) + I_{leak}$$

Subthreshold Current

The following is the expression for the subthreshold current:

$$I_{sub} = MUS \cdot C_{ox} \frac{W}{L} V_{sth}^2 \exp\left(\frac{V_{GT}}{V_{sth}}\right) \left[1 - \exp\left(-\frac{V_{DS}}{V_{sth}}\right)\right]$$

$$I_{sub} = MUS \cdot C_{ox} \cdot \frac{W_{eff}}{L_{eff}} \cdot V_{sth}^2 \cdot \exp\left(\frac{V_{GT}}{V_{sth}}\right) \cdot \left(1 - \exp\left(-\frac{V_{DS}}{V_{sth}}\right)\right)$$

$$C_{OX} = \frac{\epsilon_i}{T_{OX}}, V_{sth} = ETA \cdot V_{th}, V_{th} = \frac{k_B \cdot TEMP}{q}$$

$$V_{GT} = V_{GS} - V_{Teff}$$

$$V_{Teff} = V_{TX} - \frac{AT \cdot V_{DS}^2 + BT}{L_{eff} \cdot \left(1 + \exp\left(\frac{V_{GS} - V_{ST} - V_{TX}}{V_{SI}}\right)\right)}$$

In the preceding equations, $\epsilon\tau$ is the dielectric constant of the oxide, and k_B is the Boltzmanns constant.

Above the $V_{GT} > 0$ threshold, the following equation calculates the conduction current:

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Level 62 RPI Poli-Si TFT Model

$$I_a = \frac{\mu_{FET} \cdot C_{OX} \cdot W_{eff}}{L_{eff}} \left(V_{GTE} \cdot V_{DS} - \frac{V_{DS}^2}{2 \cdot \alpha_{sat}} \right) \text{ for } V_{DS} \leq \alpha_{sat} V_{GTE}$$

$$\frac{\mu_{FET} \cdot C_{OX} \cdot W_{eff} \cdot V_{GTE}^2 \cdot \alpha_{sat}}{2 \cdot L_{eff}} \quad \text{for } V_{DS} > \alpha_{sat} V_{GTE}$$

$$\frac{1}{\mu_{FET}} = \frac{1}{MUO} + \frac{1}{\mu l \cdot \left(\frac{2 \cdot V_{GTE}}{V_{sth}} \right)^{MMU}}$$

$$V_{GTE} = V_{sth} \cdot \left[1 + \frac{V_{GT}}{2 \cdot V_{sth}} + \sqrt{DELTA^2 + \left(\frac{V_{GT}}{2 \cdot V_{sth}} - 1 \right)^2} \right]$$

Subthreshold Leakage Current

Subthreshold leakage current is the result of the thermionic field emission of carriers through the grain boundary trap states as described in the following equations.

$$I_{leak} = IO \cdot W_{eff} \cdot \left[\exp \left(\frac{q \cdot BLK \cdot V_{DS}}{k \cdot T} \right) - 1 \right] \cdot (X_{TFE} + X_{TE}) + I_{diode}$$

$$X_{TFE} = \frac{X_{TFE, lo} \cdot X_{TFE, hi}}{X_{TFE, lo} + X_{TFE, hi}}$$

The following equations calculate values for the preceding equations:

$$X_{TE} = \exp(-W_C)$$

$$W_C = \frac{E_C - E_t}{k \cdot T} = \frac{0.55 eV}{k \cdot T}$$

$$X_{TFE, lo} = \frac{4\sqrt{\pi}}{3} \cdot f \cdot \exp \left(\frac{4}{27} \cdot f^2 - W_c \right) \text{ for } f \leq f_{lo}$$

$$X_{TFE, lo}(f_{lo}) \cdot \exp \left[\left(\frac{1}{f_{lo}} + \frac{8}{27} \cdot f_{lo} \right) \cdot (f - f_{lo}) \right] \text{ for } f > f_{lo}$$

$$X_{TFE,hi} = \frac{2W_c}{3} \cdot \exp\left(1 - \frac{2W_c}{3}\right) \quad \text{for } f > f_{hi}$$

$$\left(1 - \frac{3\sqrt{W_c}}{2 \cdot f}\right)^{-1} \exp\left[\frac{-W_c^{3/2}}{f}\right] \quad \text{for } f \geq f_{hi}$$

$$f_{hi} = 3 \cdot \left(\frac{W_c^{3/2}}{2W_c - 3}\right)$$

$$f = \frac{F_{min}}{2} \left[1 + \frac{\frac{F_f}{F_{fo}}}{\frac{F_{fo}}{F_{min}}} + \sqrt{DELTA^2 + \left(\frac{\frac{F_f}{F_{fo}}}{\frac{F_{fo}}{F_{min}}} - 1\right)^2} \right]$$

$$F_{min} = 1e^{-4}$$

$$X_{TFE,lo}(f_{lo}) = \frac{2\sqrt{4\pi}}{3} \cdot f_{lo} \cdot \exp\left(\frac{4}{27}f_{lo}^2 - W_c\right)$$

$$F_f = \left(\frac{V_{DS}}{DD} - \frac{V_{GS} - V_{FB}}{DG}\right)$$

$$F_{fo} = (k \cdot T)^{3/2} \cdot \left(\frac{4}{3} \cdot \frac{2\pi\sqrt{2m^*}}{q \cdot h}\right)$$

$$m^* = 0.27 \cdot m_0$$

$$f_{lo} = \frac{3}{2} \cdot (\sqrt{W_c + 1} - 1)$$

$$I_{diode} = IOO \cdot W_{eff} \cdot \exp\left(-\frac{EB}{k \cdot T}\right) \left[1 - \exp\left(-\frac{q \cdot V_{DS}}{k \cdot T}\right)\right]$$

Impact Ionization Effect

$V_{GT} > 0$ ery large drain biases include the kink effect. Level 62 models this effect as impact ionization in a narrow region near the drain, and adds the I_{kink} impact ionization current to the drain current. The expression is:

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Level 62 RPI Poli-Si TFT Model

$$I_{kink} = A_{kinkt} \cdot (V_{DS} - V_{DSE}) \cdot \exp\left(-\frac{VKINK}{V_{DS} - V_{DSE}}\right)$$

$$A_{kinkt} = \frac{1}{VKINK} \left(\frac{LKINK}{L_{eff}} \right)^{MK}$$

$$V_{DSE} = \frac{V_{DS}}{\left(1 + \left(\frac{V_{DS}}{V_{DSAT}}\right)^3\right)^{1/3}} - V_{th}$$

$$V_{DSAT} = \alpha_{sat} \cdot V_{GTE}$$

Threshold Voltage

If you do not specify V_{TO} , then $V_T = V_{ON} - DVT$. Otherwise, $V_T = V_{TO}$.

Temperature Dependence

$$V_{TX} = V_T - DVT0 \cdot (TEMP - TNOM)$$

$$\mu_1 = MU1 + DMU1 \cdot (TEMP - TNOM)$$

$$\alpha_{sat} = ASAT - \frac{LASAT}{L_{eff}} - DASAT \cdot (TEMP - TNOM)$$

Capacitance

CAPMOD=0

$$C_{gs} = C_f + \frac{2}{3} \cdot C_{gcs} \cdot \left[1 - \left(\frac{V_{DSAT} - V_{DSEX}}{2V_{DSAT} - V_{DSEX}} \right)^2 \right]$$

$$C_{gd} = C_f + \frac{2}{3} \cdot C_{gcd} \cdot \left[1 - \left(\frac{V_{DSAT}}{2V_{DSAT} - V_{DSEX}} \right)^2 \right]$$

$$C_f = 0.5 \cdot EPS \cdot W_{eff}$$

$$C_{gcd} = \frac{C_{OX}}{1 + \eta_{td} \cdot \exp\left(-\frac{V_{GTx}}{\eta_{td} \cdot V_{th}}\right)}$$

$$C_{gcs} = \frac{C_{OX}}{1 + ETAC0 \cdot \exp\left(-\frac{V_{GTX}}{ETAC0 \cdot V_{th}}\right)}$$

$$C_{OX} = \frac{W_{eff} \cdot L_{eff} \cdot \epsilon_i}{TOX}, \quad \eta_{td} = ETAC0 + ETAC00 \cdot V_{DSEX}$$

$$V_{DSEX} = \frac{V_{DS}}{\left[1 + \left(\frac{V_{DS}}{V_{DSAT}}\right)^{MC}\right]^{\frac{1}{MC}}}$$

$$V_{GTX} = V_{GS} - V_{TX}$$

CAPMOD=1

If ZERO equals 1:

$$V_{gst} = V_{GS} - V_{TX}$$

$$Phi = 0.6$$

$$V_{gst} < \frac{-phi}{2} \quad C_{gs} = C_{gd} = 0$$

$$\frac{-phi}{2} \leq V_{gst} < 0 \quad C_{gs} = \frac{4 \cdot V_{gst} \cdot C_{OX}}{3 \cdot Phi} + \frac{2 \cdot C_{OX}}{3}, \quad C_{gd} = 0$$

$$V_{gst} \geq 0 \quad \left\{ \begin{array}{l} V_{DS} \geq V_{DSAT} \quad C_{gs} = \frac{2C_{OX}}{3}, \quad C_{gd} = 0 \\ V_{DS} < V_{DSAT} \quad C_{gd} = \frac{2}{3} \cdot C_{OX} \cdot \left[1 - \left(\frac{V_{DSAT}}{2(V_{DSAT} - V_{DSEX})}\right)^2\right] \\ \quad \quad \quad C_{gs} = \frac{2}{3} \cdot C_{OX} \cdot \left[1 - \left(\frac{V_{DSAT} - V_{DSE}}{2(V_{DSAT} - V_{DSEX})}\right)^2\right] \end{array} \right.$$

$$C_{OX} = \frac{\epsilon_i \cdot W_{eff} \cdot L_{eff}}{T_{OX}}, V_{DSEX} = \frac{V_{DS}}{\left[1 + \left(\frac{V_{DS}}{V_{DSAT}}\right)^{MC}\right]^{\frac{1}{MC}}}$$

Geometry Effect

$$W_{eff} = W + XW$$

$$L_{eff} = L + XL$$

Self Heating

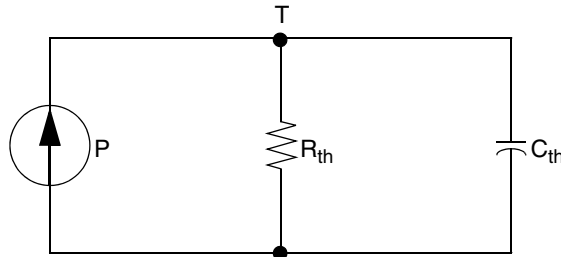
Self heating is turned on if self-heating parameters SHMOD=1 and RTH0 > 0.

SHMOD and RTH0 are also instance parameters. They override the corresponding model parameters.

The effective thermal resistance and capacitance equations and equivalent circuit are:

$$R_{th} = \frac{RTH0}{W_{eff} + WTH0_{eff}}$$

$$C_{th} = CTH0 \cdot (W_{eff} + WTH0_{eff})$$



Version 2 Model Equations

The RPI TFT poly-Si Version 2 model is available in HSPICE. Invoke the model by setting the VERSION parameter to 2.

The following sections display these equations:

- Threshold Voltage and $V_{GS} - V_T$
- Mobility
- Channel Conductance
- Saturation Voltage and Effective V_{ds}
- Drain Current
- Total Drain Current, including Kink Effect and Leakage
- Additional Geometry Scaling for Version 2
- Temperature Dependence for Version 2

Threshold Voltage and $V_{GS} - V_T$

$$V_{Teff} = V_{TX} - \Delta V_{T, DIBL}$$

$$\text{If DIBLMOD} = 0, \text{ then } \Delta V_{T, DIBL} = \frac{AT \cdot V_{DS}^2 + BT}{L_{eff}}$$

else, if DIBLMOD = 1, then

$$\Delta V_{T, DIBL} = \frac{AT \cdot V_{DS}^2 + BT}{L_{eff} \cdot \left[1 + \exp\left(\frac{V_{GS} - VSIGMAT - V_{TX}}{VSIGMA}\right) \right]}$$

otherwise

$$\Delta V_{T, DIBL} = \frac{AT \cdot V_{DS}^2}{L_{eff} \cdot \left[1 + \exp\left(\frac{V_{GS} - VSIGMAT - V_{TX}}{VSIGMA}\right) \right]} + \frac{BT}{L_{eff}}$$

$$V_{GT} = V_{GS} - V_{Teff}$$

$$V_{GTE} = ETA \cdot V_{th} \cdot \left[1 + \frac{V_{GT}}{2 \cdot ETA \cdot V_{th}} + \sqrt{DELTA^2 + \left(\frac{V_{GT}}{2 \cdot ETA \cdot V_{th}} - 1 \right)^2} \right]$$

$$V_{th} = \frac{k_B \cdot TEMP}{q}$$

Mobility

$$\Delta V_{T, DIBL} = \frac{AT \cdot V_{DS}^2}{L_{eff} \cdot \left[1 + \exp\left(\frac{V_{GS} - VSIGMAT - V_{TX}}{VSIGMA}\right) \right]} + \frac{BT}{Leff}$$

$$\mu_{eff} = MUS + \frac{\mu_{FET}}{1 + \frac{THETA}{T_{OX}} \cdot V_{GTE}}$$

$$\frac{1}{\mu_{FET}} = \frac{1}{\mu_0} + \frac{1}{\mu_1 \cdot \left(\frac{2 \cdot V_{GTE}}{\eta_f \cdot V_{th}} \right)^{MMU}}$$

$$\eta_f = \frac{ETA}{1 + META \cdot \frac{ETA - 1}{ETA} \cdot r_{i1}}$$

$$r_{i1} = \frac{i_1}{1 + i_1}$$

$$i_1 = \left(\frac{LKINK}{L_{eff}} \right)^{MKINK} \cdot \frac{W_{eff}}{L_{eff}} \cdot \frac{V_{DS} - V_{DSE}}{VKINK} \cdot \exp\left(-\frac{VKINK}{V_{DS} - V_{DSE}}\right)$$

$$V_{DSE} = \frac{V_{DS}}{\left[1 + \left(\frac{V_{DS}}{V_{GTE}} \right)^{MSS} \right]^{\frac{1}{MSS}}} - V_{th}$$

Channel Conductance

$$g_{ch} = \frac{g_{chi}}{1 + g_{chi} \cdot (R_D + R_S)}, g_{chi} = q \cdot n_s \cdot \mu_{eff} \cdot \frac{W_{eff}}{L_{eff}}$$

$$n_s = \frac{C_{OX} \cdot ETA \cdot V_{TH}}{q} \cdot \log\left[1 + \frac{1}{2} \cdot \exp\left(\frac{V_{GT}}{\eta_f \cdot V_{th}}\right) \right], C_{OX} = \frac{\epsilon_i}{T_{OX}}$$

Saturation Voltage and Effective V_{ds}

$$V_L = \frac{VMAX_L}{\mu_{eff}}$$

$$I_{sat} = \frac{g_{chi} \cdot V_{GTE}}{1 + \frac{V_{GTE}}{V_L} + g_{chi} \cdot R_S + \sqrt{1 + 2 \cdot g_{chi} \cdot R_S + \left(1 + \frac{V_{GTE}}{V_L}\right)^2}}$$

$$V_{Dsat} = \frac{I_{sat}}{g_{ch}}$$

$$I_{choo} = g_{ch} \cdot V_{DS} \cdot \frac{(1 + \lambda \cdot V_{DS})}{\left[1 + \left(\frac{V_{DS}}{V_{Dsat}}\right)^{ME_L}\right]^{\frac{1}{ME_L}}}$$

If ISUBMOD=1, then $\lambda = 0$

otherwise $\lambda = LAMBDA$

$$q_s = q \cdot \left(n_s - I_{choo} \cdot \frac{C_{OX} \cdot R_d}{q}\right)$$

$$V_{satnew} = \frac{2 \cdot VMAX_L \cdot q_s}{q_s \cdot \mu_{eff} + 2 \cdot VMAX_L \cdot \frac{C_{OX}}{\alpha_{SAT}}}$$

$$V_{DS0} = V_{DS} - I_{choo} \cdot (R_D + R_S)$$

$$V_{DSEnew} = \frac{V_{DS0}}{\left[1 + \left(\frac{V_{DS0}}{V_{satnew}}\right)^{MSS}\right]^{\frac{1}{MSS}}} - V_{th}$$

Drain Current

If ISUBMOD = 0, then $I_{dp} = I_{choo}$

otherwise

$$I_{dp} = \frac{I_{choo}}{1 - \frac{\Delta_L}{L_{eff}}}, \Delta_L = \frac{LS \cdot \log\left(1 + \frac{V_{DS0} - V_{DSEnew}}{VP}\right)}{1 + \frac{V_{DSEnew}}{VP} + C_{OX} \cdot \mu_{eff} \cdot R_s \cdot \frac{W_{eff}}{L_{eff}}},$$

Total Drain Current, including Kink Effect and Leakage

$$m = \left(\frac{LKINK}{L_{eff}}\right)^{MKINK} \cdot \frac{V_{DS} - V_{DSEnew}}{VKINK} \cdot \exp\left(-\frac{VKINK}{V_{DS} - V_{DSEnew}}\right)$$

$$I_{ds} = I_{dp} \cdot (1 + m) + I_{leak}$$

The subthreshold leakage current equation is the same as for VERSION=1.

Additional Geometry Scaling for Version 2

$$\mu_0 = MU0 \cdot \left[1 + \left(\frac{LMU0}{L_{eff}}\right)^2\right]$$

$$\mu_{1L} = MU1 \cdot \left[1 - \left(\frac{LMU1}{L_{eff}}\right)^2\right]$$

$$ME_L = ME \cdot \left[1 - \left(\frac{LME}{L_{eff}}\right)^2\right]$$

Temperature Dependence for Version 2

$$V_{TX} = VTO - DVTO \cdot (TEMP - TNOM)$$

$$\mu_1 = \mu_{1L} + DMU1 \cdot (TEMP - TNOM)$$

$$\alpha_{sat} = ASAT - \frac{LASAT}{L_{eff}} - DASAT \cdot (TEMP - TNOM)$$

Level 63 Philips MOS11 Model

The Philips MOS Model 11, Level 1101 and 1102, are available as Level 63 in the Synopsys MOSFET models.

Philips MOS Model 11, Level 1102, is an updated version of Level 1101. It uses slightly different equations than Level 1101. The surface potential is calculated iteratively using a second-order Newton-Raphson procedure, resulting in a more accurate description of the surface potential. It includes two types of geometrical scaling rules: physical rules and binning rules. You use the `BINFLAG` parameter to select these rules.

The parasitic diode model includes the Philips JUNCAP Parasitic Diode Model.

For more information about the MOS Model 11 and the Philips JUNCAP Parasitic Diode Model, see:

http://www.semiconductors.philips.com/Philips_Models

The implementation history of the Philips MOS Model 11 is as follows:

Level 1102 series implementations

- 1102 –
 - Iterative solution of surface potential.
 - More accurate, physics-based implementation of velocity saturation effects.
 - More accurate, physics-based equations for thermal noise, induced gate noise, and their correlations.
 - Self-heating implemented.
 - Temperature dependence parameter of the thermal resistance, `ATH`, added.
 - Internal variable `VDBt` was simplified, which results in a more physical description for $V_{DS} < 0$.
 - Definition of starting condition of surface potential Ψ_s and Y_{ov} rewritten to increase numerical efficiency and to avoid possible floating-point exceptions.
- 1102.1 –
 - Default of `NT` (noise parameter) changed from 1.656e-20 to 1.624e-20
 - Bug in noise equation for induced gate noise fixed.

- Maximum temperature limiting for self-heating implemented.

Level 1101 series implementations

- 1101.2 – self-heating implemented.
- 1101.4 – thermal noise density improved.
- 1101.5 – temperature dependence parameter of the thermal resistance, ATH, added.
- 1101.6 –
 - default value of NT (noise parameter) changed from 1.656e-20 to 1.624e-20
 - handling of low limit of internal variable, G_{mob} , simplified
 - maximum temperature limiting for self-heating implemented

Using the Philips MOS11 Model

To use the Philips MOS11 model:

1. Set `LEVEL=63` to identify the model as Philips MOS Model 11.
2. Set the MOS11 version:
 - Set `VERSION=1102.1` (default) to identify the model as Level 1102.1
 - Set `VERSION=1102.0` to identify the model as Level 1102.0
 - Set `VERSION=1101.6` to identify the model as Level 1101.6
 - Set `VERSION=1101.5` to identify the model as Level 1101.5
 - Set `VERSION=1101.4` to identify the model as Level 1101.4
 - Set `VERSION=1101.2` to identify the model as Level 1101.2
 - Set `VERSION=1101.1` to identify the model as Level 1101.1
 - Set `VERSION=1101.0` to identify the model as Level 1101.0
 - Set `VERSION=1100.3` to identify the model as Level 1100.3
 - Set `VERSION=1100.2` to identify the model as Level 1100.2
 - Set `VERSION=1100.1` to identify the model as Level 1100.1
 - Set `VERSION=1100.0` to identify the model as Level 1100.0
3. Set the flag for binned model:

- Set `BINFLAG=0` (default) to select the physical geometry scaling rules.
 - Set `BINFLAG=1` to select the binning geometry scaling rules.
4. The existing version is internally switched for backward compatibility as follows:
 - `VERSION=11010` switched to `VERSION=1101.1` and `BINFLAG=0`
 - `VERSION=11011` switched to `VERSION=1101.1` and `BINFLAG=1`
 5. Set the flag for self-heating:
 - Set `SHMOD=0` (default) to select no self-heating.
 - Set `SHMOD=1` to select self-heating.
 6. The default room temperature is 25°C in Synopsys circuit simulators, but is 27°C in most other simulators. When comparing to other simulators, use `.TEMP 27` or `.OPTION TNOM=27` to set the simulation temperature to 27 in the netlist.
 7. The set of model parameters should always include the `TR` model reference temperature which corresponds to `TREF` in other levels in the Synopsys MOSFET model levels. The default for `TR` is 21.0 to match the Philips simulator.
 8. This model has its own charge-based capacitance model. This model ignores the `CAPOP` parameter, which selects different capacitance models.
 9. This model uses analytical derivatives for the conductances. This model ignores the `DERIV` parameter, which selects the finite difference method.
 10. You can use `DTEMP` with this model to increase the temperature of individual elements, relative to the circuit temperature. Set `DTEMP` on the element line.
 11. Because the defaults are non-zero, you should set *every* Level 63 model parameter in the Model Parameters table in the `.MODEL` statement.
 12. The general syntax for the MOSFET element is the same as the other standard MOSFET models, other than `PS` and `PD`. In Level 63, `PS` and `PD` are the length of the sidewall of the source/drain, which is not under the gate.
 13. Philips MOS11 has its own `LMIN` parameter, which has a different definition from that of HSPICE. To avoid the conflict with `LMIN` in simulation, Synopsys changed the `LMIN` parameter in the Level 63 MOSFET model to `LLMIN`.

Description of Parameters

Table 44 Level 63 MOS11 Control, Geometry, and Self-Heating Parameters

Name (Alias)	Description	Units	NMOS	PMOS
LEVEL	Level of this model	-	63	63
VERSION	Version of this model		1102.1	1102.1
BINFLAG	Flag for binned model <ul style="list-style-type: none"> ▪ 0: physical model ▪ 1: binned model 	-	0	0
SHMOD	Flag for self-heating <ul style="list-style-type: none"> ▪ 0: no self-heating ▪ 1: self-heating 	-	0	0
LER	Effective channel length, reference transistor	m	1e-6	1e-6
WER	Effective channel width, reference transistor	m	1e-5	1e-5
LVAR	Difference between the actual and programmed poly silicon gate length	m	0	0
LAP	Effective channel length reduction per side, due to the lateral diffusion of source/drain dopant ions	m	4e-8	4e-8
WVAR	Difference between the actual and programmed field oxide opening	m	0	0
WOT	Effective reduction of the channel width per side due to the lateral diffusion of the channel stop dopant ions	m	0	0
TR	Temperature at which simulation determines the reference transistor parameters	°C	21	21

Table 44 Level 63 MOS11 Control, Geometry, and Self-Heating Parameters

Name (Alias)	Description	Units	NMOS	PMOS
DTA	Temperature offset of the device	°C	0	0
RTH	Thermal resistance	K/W	300	300
CTH	Thermal capacitance	J/W-	3e-9	3e-9
ATH	Temperature coefficient of thermal resistance	-	0	0

Table 45 Level 63 MOS11 Parameters for Physical Geometry Scaling

Name (Alias)	Description	Units	NMOS	PMOS
VFBR (VFB)	Flat-band voltage for the reference transistor at the reference temperature	V	-1.05	-1.05
STVFB	Temperature dependence coefficient of V_{FB}	V/K	5e-4	5e-4
KOR	Body-effect factor for the reference transistor	$\sqrt{V}^{1/2}$	0.5	0.5
SLKO	Coefficient of the length dependence of k_0	-	0	0
SL2KO	Second coefficient of the length dependence of k_0	-	0	0
SWKO	Coefficient of the width dependence of k_0	-	0	0
KPINV	Inverse of the body-effect factor, poly-silicon gate	$\sqrt{V}^{-1/2}$	0	0
PHIBR	Surface potential at the onset of strong inversion at the reference temperature	V	0.95	0.95
STPHIB	Temperature dependence coefficient of ϕ_B	$\sqrt{V}K^{-1}$	-8.5e-4	-8.5e-4
SLPHIB	Coefficient of the length dependence of ϕ_B	-	0	0

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Level 63 Philips MOS11 Model

Table 45 Level 63 MOS11 Parameters for Physical Geometry Scaling

Name (Alias)	Description	Units	NMOS	PMOS
SL2PHIB	Second coefficient of length dependence of ϕ_B	-	0	0
SWPHIB	Coefficient of the width dependence of ϕ_B	-	0	0
BETSQ	Gain factor for an infinite square transistor at the reference temperature	AV^{-2}	3.709e-4	1.15e-4
ETABETR (ETABET)	Exponent of the temperature dependence of the gain factor	-	1.3	0.5
SLETABET	Length dependence coefficient of $\mu\beta_R$	-	0	0
FBET1	Relative mobility decrease due to first lateral profile	-	0	0
LP1	Characteristic length of first lateral profile	m	8e-7	8e-7
FBET2	Relative mobility decrease due to second lateral profile	-	0	0
LP2	Characteristic length of second lateral profile	M	8e-7	8e-7
THESRR	Mobility reduction coefficient, due to surface roughness scattering for reference transistor at reference temperature	V^{-1}	0.4	0.73
ETASR	Exponent of temperature dependence of θ_{sr}	-	0.65	0.5
SWTHESR	Coefficient of the width dependence of θ_{sr}	-	0	0
THEPHR	Coefficient of the mobility reduction due to phonon scattering for the reference transistor at the reference temperature	V^{-1}	1.29e-2	1e-3
ETAPH	Exponent of the temperature dependence of θ_{sr} for the reference temperature	-	1.35	3.75

Table 45 Level 63 MOS11 Parameters for Physical Geometry Scaling

Name (Alias)	Description	Units	NMOS	PMOS
SWTHEPH	Coefficient of the width dependence of θ_{sr}	-	0	0
ETAMOBR	Effective field parameter, depletion/ inversion charge dependence for reference transistor	-	1.4	3
STETAMOB	Temperature dependence coefficient of η_{mob}	K^{-1}	0	0
SWETAMOB	Width dependence coefficient of η_{mob}	-	0	0
NU (NUR)	Exponent of field dependence, mobility model minus 1 (such as $v-1$) at reference temperature	-	2	2
NUEXP	Exponent of the temperature dependence of parameter v	-	5.25	3.23
THERR	Series resistance coefficient for reference transistor at reference temperature	V^{-1}	0.155	0.08
ETAR	Exponent of temperature dependence of θ_R	-	0.95	0.4
SWTHER	Coefficient of the width dependence of θ_R	-	0	0
THER1	Numerator of gate voltage dependent part of series resistance for reference transistor	V	0	0
THER2	Denominator of gate voltage dependent part of series resistance for the reference transistor	V	1	1
THESATR	Velocity saturation parameter due to optical/acoustic phonon scattering for the reference transistor at the reference temperature	V^{-1}	0.5	0.2
SLTHESAT	Length dependence coefficient of θ_{sat}	-	1	1

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Level 63 Philips MOS11 Model

Table 45 Level 63 MOS11 Parameters for Physical Geometry Scaling

Name (Alias)	Description	Units	NMOS	PMOS
THESATEXP	Exponent of length dependence of θ_{sat}	-	1	1
ETASAT	Exponent of temperature dependence of θ_{sat}	-	1.04	0.86
SWTHESAT	Width dependence coefficient of θ_{sat}	-	0	0
THETHR	Coefficient of self-heating for the reference transistor at the reference temperature	V-3	1e-3	0.5e-3
THETHEXP	Exponent of the length dependence of θ_{TH}	-	1	1
SWTHETH	Coefficient of the width dependence of θ_{TH}	-	0	0
SDIBLO	Drain-induced barrier-lowering parameter for the reference transistor	V ^{-1/2}	1e-4	1e-4
SDIBLEXP	Exponent of length dependence of α_{DIBL}	-	1.35	1.35
MOR	Parameter for short-channel subthreshold slope for the reference transistor	-	0	0
MOEXP	Exponent of the length dependence of m_0	-	1.34	1.34
SSFR	Static feedback parameter, reference transistor	V ^{-1/2}	6.25e-3	6.25e-3
SLSSF	Length dependence coefficient of α_{sf}	-	1.0	1.0
SWSSF	Coefficient of the width dependence of α_{sf}	-	0	0
ALPR	Factor of the channel length modulation for the reference transistor	-	1e-2	1e-2
SLALP	Coefficient of the length dependence of α	-	1	1
ALPEXP	Exponent of the length dependence of α	-	1	1
SWALP	Coefficient of the width dependence of α	-	0	0

Table 45 Level 63 MOS11 Parameters for Physical Geometry Scaling

Name (Alias)	Description	Units	NMOS	PMOS
VP	Characteristic voltage of the channel length modulation	V	5e-2	5e-2
LLMIN	Minimum effective channel length in technology, calculates smoothing factor m	M	1.5e-7	1.5e-7
A1R	Weak-avalanche current factor for reference transistor at reference temperature	-	6	6
STA1	Temperature dependence coefficient of a^1	K ⁻¹	0	0
SLA1	Coefficient of the length dependence of a^1	-	0	0
SWA1	Coefficient of the width dependence of a^1	-	0	0
A2R	Exponent of the weak-avalanche current for the reference transistor	V	38	38
SLA2	Coefficient of the length dependence of a^2	-	0	0
SWA2	Coefficient of the width dependence of a^2	-	0	0
A3R	Drain-source voltage factor, above which weak-avalanche occurs for reference transistor	-	1	1
SLA3	Coefficient of the length dependence of a^3	-	0	0
SWA3	Coefficient of the width dependence of a^3	-	0	0
IGINVR	Gain factor for intrinsic gate tunneling current in inversion for reference transistor	AV ⁻²	0	0
BINV	Probability factor for intrinsic gate tunneling current in inversion	V	48	87.5
IGACCR	Gain factor for intrinsic gate tunneling current in accumulation for reference transistor	AV ⁻²	0	0

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Level 63 Philips MOS11 Model

Table 45 Level 63 MOS11 Parameters for Physical Geometry Scaling

Name (Alias)	Description	Units	NMOS	PMOS
BACC	Probability factor for intrinsic gate tunneling current in accumulation	V	48	48
VFBOV	Flat-band voltage for the Source/Drain overlap extensions	V	0	0
KOV	Body-effect factor for the Source/Drain overlap extensions	$V^{1/2}$	2.5	2.5
IGOVR	Gain factor for Source/Drain overlap tunneling current for reference transistor	AV^{-2}	0	0
TOX	Thickness of the gate oxide layer	M	3.2e-9	3.2e-9
COL	Gate overlap capacitance per unit channel length	F	3.2e-16	3.2e-16
GATENOISE	In/exclusion flag of induced gate thermal noise	-	0	0
NT	Thermal noise coefficient at the actual temperature	J	1.624e-20	1.624e-20
NFAR	First coefficient of the flicker noise for the reference transistor	$V^{-1}m^{-4}$	1.573e23	3.825e24
NFBR	Second coefficient of the flicker noise for the reference transistor	$V^{-1}m^{-2}$	4.752e9	1.015e9
NFCR	Third coefficient of the flicker noise for the reference transistor	V^{-1}	0	7.3e-8
MOO	Parameter for short-channel subthreshold slop		0	0
AGIDLR	Gain factor for gate-induced drain leakage current for a channel width of 1 μm	AV^{-3}	0	0
BGIDL	Probability factor for gate-induced drain leakage current at the reference temperature	V	41.0	41.0

Table 45 Level 63 MOS11 Parameters for Physical Geometry Scaling

Name (Alias)	Description	Units	NMOS	PMOS
CGIDL	Factor for the lateral field dependence of the gate-induce drain leakage current		0	0
STBGIDL	Coefficient of the temperature dependence of B_{GIDL}	VK^{-1}	-3.638e-4	-3.638e-4

Table 46 Level 63 MOS11 Parameters for Binning Geometry Scaling

Name (Alias)	Description	Units	NMOS	PMOS
VFB	Flat-band voltage for the reference transistor at the reference temperature	V	-1.05	-1.05
POKO	Coefficient, geometry independent k_0 part	$V^{1/2}$	0.5	0.5
PLKO	Coefficient for the length dependent of k_0	$V^{1/2}$	0	0
PWKO	Coefficient for the width dependent of k_0	$V^{1/2}$	0	0
PLWKO	Coefficient, length times width k_0 dependent	$V^{1/2}$	0	0
KPINV	Inverse of body-effect factor, poly-silicon gate	$V^{-1/2}$	0	0
POPHIB	Coefficient, geometry independent Φ_B part	V	0.950	0.950
PLPHIB	Coefficient for the length dependent of Φ_B	V	0	0
PWPHIB	Coefficient for the width dependent of Φ_B	V	0	0
PLWPHIB	Coefficient, length times width Φ_B dependent	V	0	0

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Table 46 Level 63 MOS11 Parameters for Binning Geometry Scaling

Name (Alias)	Description	Units	NMOS	PMOS
POBET	Coefficient, geometry independent β part	AV^{-2}	1.922e-3	3.814e-4
PLBET	Coefficient for the length dependent of β	AV^{-2}	0	0
PWBET	Coefficient for the width dependent of β	AV^{-2}	0	0
PLWBET	Coefficient, width over length dependent of β	AV^{-2}	0	0
POTHEsr	Coefficient, geometry independent θ_{sr} part	V^{-1}	3.562e-1	7.30e-1
PLTHEsr	Coefficient for the length dependent part of θ_{sr}	V^{-1}	0	0
PWTHEsr	Coefficient for the width dependent part of θ_{sr}	V^{-1}	0	0
PLWTHEsr	Coefficient, length times width, θ_{sr} dependent	V^{-1}	0	0
POTHEph	Coefficient, geometry independent θ_{ph} part	V^{-1}	1.290e-2	1.0e-3
PLTHEph	Coefficient for the length dependent of θ_{ph}	V^{-1}	0	0
PWTHEph	Coefficient for the width dependent of θ_{ph}	V^{-1}	0	0
PLWHEph	Coefficient, length times width, θ_{ph} dependent	V^{-1}	0	0
POETAMOB	Coefficient, geometry independent η_{mob} part	-	1.40	3
PLETAMOB	Coefficient, length-dependent η_{mob} part	-	0	0

Table 46 Level 63 MOS11 Parameters for Binning Geometry Scaling

Name (Alias)	Description	Units	NMOS	PMOS
PWETAMOB	Coefficient, width-dependent η_{mob} part	-	0	0
PLWETAMOB	Coefficient, length times width dependent η_{mob} part	-	0	0
POTHER	Coefficient for the geometry-independent part of θ_R	V^{-1}	8.12e-2	7.9e-2
PLTHER	Coefficient for the length-dependent part of θ_R	V^{-1}	0	0
PWTHER	Coefficient for the width dependent part of θ_R	V^{-1}	0	0
PLWTHER	Coefficient, length times width θ_R dependent	V^{-1}	0	0
THER1	Numerator of the gate voltage dependent part of the series resistance for all transistors in bin	V	0	0
THER2	Denominator of the gate voltage dependent part of the series resistance for all transistors in the bin	V	1.0	1.0
POTHSAT	Coefficient for the geometry-independent part of θ_{sat}	V^{-1}	2.513e-1	1.728e-1
PLTHESAT	Coefficient for length-dependent part of θ_{sat}	V^{-1}	0	0
PWTHESAT	Coefficient for the width-dependent part of θ_{sat}	V^{-1}	0	0
PLWTHESAT	Coefficient, length times width θ_{sat} dependent	V^{-1}	0	0
POTHEETH	Coefficient for the geometry-independent part of θ_{TH}	V^{-3}	1.0e-5	0

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Level 63 Philips MOS11 Model

Table 46 Level 63 MOS11 Parameters for Binning Geometry Scaling

Name (Alias)	Description	Units	NMOS	PMOS
PLTHETH	Coefficient for the length-dependent part of θ_{TH}	V-3	0	0
PWTHETH	Coefficient for the width-dependent part of θ_{TH}	V-3	0	0
PLWTHETH	Coefficient for the length times width θ_{TH} dependent part	V-3	0	0
POSDIBL	Coefficient for the geometry-independent part of σ_{dibl}	$V^{-1/2}$	8.53e-4	3.551e-5
PLSDIBL	Coefficient for the length-dependent part of σ_{dibl}	$V^{-1/2}$	0	0
PWSDIBL	Coefficient for the width-dependent part of σ_{dibl}	$V^{-1/2}$	0	0
PLWSDIBL	Coefficient, length times width dependent of σ_{dibl}	$V^{-1/2}$	0	0
POMO	Coefficient for the geometry-independent part of m_0	-	0	0
PLMO	Coefficient for the length-dependent part of m_0	-	0	0
PWMO	Coefficient for the width-dependent part of m_0	-	0	0
PLWMO	Coefficient for the length times width m_0 dependent part	-	0	0
POSSF	Coefficient for the geometry-independent part of σ_{sf}	$V^{-1/2}$	1.2e-2	1.0e-2
PLSSF	Coefficient for the length-dependent part of σ_{sf}	$V^{-1/2}$	0	0

Table 46 Level 63 MOS11 Parameters for Binning Geometry Scaling

Name (Alias)	Description	Units	NMOS	PMOS
PWSSF	Coefficient for the width-dependent part of α_{sf}	$V^{-1/2}$	0	0
PLWSSF	Coefficient for the length times width α_{sf} dependent part	$V^{-1/2}$	0	0
POALP	Coefficient for the geometry-independent part of α	-	2.5e-2	2.5e-2
PLALP	Coefficient for the length-dependent part of α	-	0	0
PWALP	Coefficient for the width-dependent part of α	-	0	0
PLWALP	Coefficient for the length times width dependent part of α	-	0	0
VP	Characteristic voltage of the channel length modulation	V	5e-2	5e-2
POMEXP	Coefficient for the geometry-independent 1/m part	-	0.2	0.2
PLMEXP	Coefficient for the length-dependent part of 1/m	-	0	0
PWMEXP	Coefficient for the width dependent part of 1/m	-	0	0
PLWMEXP	Coefficient of the length times width 1/m dependent part	-	0	0
POA1	Coefficient of the geometry-independent a^1 part	-	6.022	6.858
PLA1	Coefficient for the length-dependent part of a^1	-	0	0

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Table 46 Level 63 MOS11 Parameters for Binning Geometry Scaling

Name (Alias)	Description	Units	NMOS	PMOS
PWA1	Coefficient for the width-dependent part of a^1	-	0	0
PLWA1	Coefficient for the length times width a^1 dependent part	-	0	0
POA2	Coefficient for the geometry-independent a^2 part	V	3.802e1	5.732e1
PLA2	Coefficient for the length-dependent part of a^2	V	0	0
PWA2	Coefficient for the width-dependent part of a^2	V	0	0
PLWA2	Coefficient of the length times width a^2 dependent part	V	0	0
POA3	Coefficient of the geometry-independent a^3 part	-	6.407e-1	4.254e-1
PLA3	Coefficient for the length-dependent part of a^3	-	0	0
PWA3	Coefficient for the width-dependent part of a^3	-	0	0
PLWA3	Coefficient for the length times width a^3 dependent part	-	0	0
POIGINV	Coefficient for the geometry-independent part of I_{GINV}	AV^{-2}	0	0
PLIGINV	Coefficient for the length-dependent part of I_{GINV}	AV^{-2}	0	0
PWIGINV	Coefficient for the width-dependent part of I_{GINV}	AV^{-2}	0	0

Table 46 Level 63 MOS11 Parameters for Binning Geometry Scaling

Name (Alias)	Description	Units	NMOS	PMOS
PLWIGINV	Coefficient for the length times width dependent part of I_{GINV}	AV^{-2}	0	0
POBINV	Coefficient for the geometry-independent part of I_{GINV}	V	48	87.5
PLBINV	Coefficient for the length-dependent part of I_{GINV}	V	0	0
PWBINV	Coefficient for the width-dependent part of I_{GINV}	V	0	0
PLWBINV	Coefficient for the length times width dependent part of I_{GINV}	V	0	0
POIGACC	Coefficient for the geometry-independent part of I_{GACC}	AV^{-2}	0	0
PLIGACC	Coefficient for the length-dependent part of I_{GACC}	AV^{-2}	0	0
PWIGACC	Coefficient for the width-dependent part of I_{GACC}	AV^{-2}	0	0
PLWIGACC	Coefficient for the length times width dependent part of I_{GACC}	AV^{-2}	0	0
POBACC	Coefficient for the geometry-independent part of B_{ACC}	V	48	48
PLBACC	Coefficient for the length-dependent part of B_{ACC}	V	0	0
PWBACC	Coefficient for the width-dependent part of B_{ACC}	V	0	0
PLWBACC	Coefficient for the length times width dependent part of B_{ACC}	V	0	0

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Level 63 Philips MOS11 Model

Table 46 Level 63 MOS11 Parameters for Binning Geometry Scaling

Name (Alias)	Description	Units	NMOS	PMOS
VFBOV	Flatband voltage for the source/drain overlap extensions	V	0	0
KOV	Body-effect factor for the source/drain overlap extensions	$V^{1/2}$	2.5	2.5
POIGOV	Coefficient for the geometry-independent part of I_{GOV}	AV^{-2}	0	0
PLIGOV	Coefficient for the length-dependent part of I_{GOV}	AV^{-2}	0	0
PWIGOV	Coefficient for the width-dependent part of I_{GOV}	AV^{-2}	0	0
PLWIGOV	Coefficient for the width over length dependent part of I_{GOV}	AV^{-2}	0	0
TOX	Thickness of the gate oxide layer	m	3.2e-9	3.2e-9
POCOX	Coefficient for the geometry-independent C_{OX} part	F	2.98e-14	2.717e-14
PLCOX	Coefficient for the length-dependent part of C_{OX}	F	0	0
PWCOX	Coefficient for the width-dependent part of C_{OX}	F	0	0
PLWCOX	Coefficient for the length times width dependent part of C_{OX}	F	0	0
POCGDO	Coefficient for the geometry-independent C_{GDO} part	F	6.392e-15	6.358e-15
PLCGDO	Coefficient for the length-dependent part of C_{GDO}	F	0	0
PWCGDO	Coefficient for the width dependent part of C_{GDO}	F	0	0

Table 46 Level 63 MOS11 Parameters for Binning Geometry Scaling

Name (Alias)	Description	Units	NMOS	PMOS
PLWCGDO	Coefficient for the width over length dependent part of C_{GDO}	F	0	0
POCGSO	Coefficient for the geometry-independent part of C_{GSO}	F	6.392e-15	6.358e-15
PLCGSO	Coefficient for the length-dependent part of C_{GSO}	F	0	0
PWCGSO	Coefficient for the width-dependent part of C_{GSO}	F	0	0
PLWCGSO	Coefficient for the width over length dependent part of C_{GSO}	F	0	0
GATENOISE	Inclusion/exclusion flag of the induced gate thermal noise	-	0	0
NT	Coefficient for the thermal noise at the reference temperature	J	1.656e-20	1.656e-20
PONFA	Coefficient for the geometry-independent N_{FA} part	$V^{-1}m^{-4}$	8.323e22	1.90e22
PLNFA	Coefficient for the length-dependent part of N_{FA}	$V^{-1}m^{-4}$	0	0
PWNFA	Coefficient for the width-dependent part of N_{FA}	$V^{-1}m^{-4}$	0	0
PLWNFA	Coefficient for the length times width dependent part of N_{FA}	$V^{-1}m^{-4}$	0	0
PONFB	Coefficient for the geometry-independent N_{FB} part	$V^{-1}m^{-2}$	2.514e7	5.043e6
PLNFB	Coefficient for the length-dependent part of N_{FB}	$V^{-1}m^{-2}$	0	0

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Level 63 Philips MOS11 Model

Table 46 Level 63 MOS11 Parameters for Binning Geometry Scaling

Name (Alias)	Description	Units	NMOS	PMOS
PWNFB	Coefficient for the width-dependent part of N_{FB}	$V^{-1}m^{-2}$	0	0
PLWNFB	Coefficient for the length times width dependent part of N_{FB}	$V^{-1}m^{-2}$	0	0
PONFC	Coefficient for the geometry-independent N_{FC} part	V^{-1}	0	3.627e-10
PLNFC	Coefficient for the length-dependent part of N_{FC}	V^{-1}	0	0
PWNFC	Coefficient for the width-dependent part of N_{FC}	V^{-1}	0	0
PLWNFC	Coefficient for the length times width dependent part of N_{FC}	V^{-1}	0	0
POTVFB	Coefficient for the geometry-independent part of $ST;V_{FB}$	VK^{-1}	5.0e-4	5.0e-4
PLTVFB	Coefficient for the length-dependent part of $ST;V_{FB}$	VK^{-1}	0	0
PWTVFB	Coefficient for the width-dependent part of $ST;V_{FB}$	VK^{-1}	0	0
PLWTVFB	Coefficient for the length times width dependent part of $ST;V_{FB}$	VK^{-1}	0	0
POTPHIB	Coefficient for the geometry-independent part of $ST;\phi_B$	VK^{-1}	-8.5e-4	-8.5e-4
PLTPHIB	Coefficient for the length-dependent part of $ST;\phi_B$	VK^{-1}	0	0
PWTPHIB	Coefficient for the width-dependent part of $ST;\phi_B$	VK^{-1}	0	0

Table 46 Level 63 MOS11 Parameters for Binning Geometry Scaling

Name (Alias)	Description	Units	NMOS	PMOS
PLWTPHIB	Coefficient for the length times width dependent part of $ST_0\phi_B$	VK^{-1}	0	0
POTETABET	Coefficient for the geometry-independent part of $r\beta$	-	1.30	0.5
PLTETABET	Coefficient for the length-dependent part of $r\beta$	-	0	0
PWTETABET	Coefficient for the width-dependent part of $r\beta$	-	0	0
PLWTETABET	Coefficient for the length times width dependent part	-	0	0
POTETASR	Coefficient for the geometry-independent $r\beta_r$ part	-	0.65	0.5
PLTETASR	Coefficient for the length-dependent part of $r\beta_r$	-	0	0
PWTETASR	Coefficient for the width-dependent part of $r\beta_r$	-	0	0
PLWTETASR	Coefficient for the length times width dependent part of $r\beta_r$	-	0	0
POTETAPH	Coefficient for the geometry-independent $r\beta_h$ part	-	1.35	3.75
PLTETAPH	Coefficient for the length-dependent part of $r\beta_h$	-	0	0
PWTETAPH	Coefficient for the width-dependent part of $r\beta_h$	-	0	0
PLWTETAPH	Coefficient for the length times width dependent part	-	0	0

Table 46 Level 63 MOS11 Parameters for Binning Geometry Scaling

Name (Alias)	Description	Units	NMOS	PMOS
POTETAMOB	Coefficient for the geometry-independent part of $\text{ST}:\eta_{ph}$	K^{-1}	0	0
PLTETAMOB	Coefficient for the length-dependent part of η_{ph}	K^{-1}	0	0
PWTETAMOB	Coefficient for the width-dependent part of η_{ph}	K^{-1}	0	0
PLWTETAMOB	Coefficient for the length times width dependent part of η_{ph}	K^{-1}	0	0
NU	Exponent of the field dependence of the mobility model at the reference temperature	-	2	2
POTNUEXP	Coefficient for the geometry-independent v_{exp} part	-	5.25	3.23
PLTNUEXP	Coefficient for the length-dependent part of v_{exp}	-	0	0
PWTNUEXP	Coefficient for the width-dependent part of v_{exp}	-	0	0
PLWTNUEXP	Coefficient fore the length times width dependent part of v_{exp}	-	0	0
POTETAR	Coefficient for the geometry-independent η_R part	-	0.95	0.4
PLTETAR	Coefficient for the length-dependent part of η_R	-	0	0
PWTETAR	Coefficient for the width-dependent part of η_R	-	0	0
PLWTETAR	Coefficient for the length times width dependent part of η_R	-	0	0

Table 46 Level 63 MOS11 Parameters for Binning Geometry Scaling

Name (Alias)	Description	Units	NMOS	PMOS
POTETASAT	Coefficient for the geometry-independent part of η_{sat}	-	1.04	0.86
PLTETASAT	Coefficient for the length-dependent part of η_{sat}	-	0	0
PWTETASAT	Coefficient for the width-dependent part of η_{sat}	-	0	0
PLWTETASAT	Coefficient for the length times width dependent part of η_{sat}	-	0	0
POTA1	Coefficient for the geometry-independent $S_T:a^1$ part	K^{-1}	0	0
PLTA1	Coefficient for the length-dependent part of $S_T:a^1$	K^{-1}	0	0
PWTA1	Coefficient for the width-dependent part of $S_T:a^1$	K^{-1}	0	0
PLWTA1	Coefficient for the length times width dependent part of $S_T:a^1$	K^{-1}	0	0
POAGIDL	Coefficient for the geometry-independent part of A_{GIDL}	AV^{-3}	0	0
PLAGIDL	Coefficient for the length dependence of A_{GIDL}	AV^{-3}	0	0
PWAGIDL	Coefficient for the width dependence of A_{GIDL}	AV^{-3}	0	0
PLWAGIDL	Coefficient for the width over length dependence of A_{GIDL}	AV^{-3}	0	0
POBGIDL	Coefficient for the geometry independent part of B_{GIDL}	V	41.0	41.0

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Table 46 Level 63 MOS11 Parameters for Binning Geometry Scaling

Name (Alias)	Description	Units	NMOS	PMOS
PLBGIDL	Coefficient for the length dependence of B_{GIDL}	V	0	0
PWBGIDL	Coefficient for the width dependence of B_{GIDL}	V	0	0
PLWBGIDL	Coefficient for the length times width dependence of B_{GIDL}	V	0	0
POCGIDL	Coefficient for the geometry independent part of C_{GIDL}		0	0
PLCGIDL	Coefficient for the length dependence of C_{GIDL}		0	0
PWCGIDL	Coefficient for the width dependence of C_{GIDL}		0	0
PLWCGIDL	Coefficient for the length times width dependence of C_{GIDL}		0	0
POTBGIDL	Coefficient for the geometry independent part of $S_T \cdot B_{GIDL}$	VK^{-1}	-3.638e-4	-3.638e-4
PLTBGIDL	Coefficient for the length dependence of $S_T \cdot B_{GIDL}$	VK^{-1}	0	0
PWTBGIDL	Coefficient for the width dependence of $S_T \cdot B_{GIDL}$	VK^{-1}	0	0
PLWTBGIDL	Coefficient for the length times width dependence of $S_T \cdot B_{GIDL}$	VK^{-1}	0	0

The following are JUNCAP model parameters specifically for the Philips MOS 11 (Level 63) model.

Table 47 Level 63 JUNCAP Parameters

Name	Description	Units	Default
DTA	Temperature offset of the JUNCAP element with respect to T_A	$^{\circ}\text{C}$	0
VR	Voltage at which simulation determines parameters	V	0
JSGBR	Bottom saturation-current density due to generating an electron hole at $V=V_R$	Am^{-2}	1e-03
JSDBR	Bottom saturation-current density due to diffusion from back contact	Am^{-2}	1e-03
JSGSR	Sidewall saturation-current density due to generating an electron hole at $V=V_R$	Am^{-1}	1e-03
JSDSR	Sidewall saturation-current density due to back-contact diffusion	Am^{-1}	1e-03
JSGGR	Gate edge saturation-current density due to generating an electron hole at $V=V_R$	Am^{-1}	1e-03
JSDGR	Gate edge saturation-current density due to back-contact diffusion	Am^{-1}	1e-03
NB	Emission coefficient of the bottom forward current	-	1
NS	Emission coefficient of the sidewall forward current	-	1
NG	Emission coefficient of the gate edge forward current	-	1
CJBR	Bottom junction capacitance at $V=V_R$	Fm^{-2}	1e-12
CJSR	Sidewall junction capacitance at $V=V_R$	Fm^{-1}	1e-12
CJGR	Gate edge junction capacitance at $V=V_R$	Fm^{-1}	1e-12
VDBR	Diffusion voltage of the bottom junction at $T=T_R$	V	1
VDSR	Diffusion voltage of the sidewall junction at $T=T_R$	V	1
VDGR	Diffusion voltage of the gate-edge junction at $T=T_R$	V	1

Table 47 Level 63 JUNCAP Parameters

Name	Description	Units	Default
PB	Bottom junction grading coefficient	-	0.4
PS	Sidewall junction grading coefficient	-	0.4
PG	Gate edge junction grading coefficient	-	0.4

Note: All symbols refer to “Unclassified Report NL-UR 2001/813”.

Example 1

```
.model nch nmos level=63
+ VERSION=1100
+ LER=1E-06 WER=1E-05 LAP=-1.864E-08
+ TR=21 VFBR=-1.038 SLPHIB=-1.024E-08
+ SL2PHIB=1.428E-14 KOR=5.763E-01 SLKO=2.649E-08
+ SL2KO=-1.737E-14 KPINV=2.2E-01 PHIBR=0.85
+ BETSQ=1.201E-04 ETABET=1.3 FBET1=-3.741000E-01
+ LP1=2.806E-06 LP2=1E-10 THESATEXP=2
+ THESRR=7.109E-01 THEPHR=1E-03 TOX=3.2E-09
+ ETAPH=1.75E+00 ETAMOBR=2.825 NUR=1
+ NUEXP=3.228 THERR=1.267E-01 ETAR=0.4
+ THER2=1 THESATR=6.931E-02 SLTHESAT=1
+ ETASAT=8.753E-01 SSFR=2.304E-03 VP=5E-02
+ SLSSF=1.002E-06 ALPR=1.062E-02 SLALP=9.957E-01
+ ALPEXP=1.039 THETHR=2.413E-03 THETHEXP=1
+ SDIBLO=1.06E-06 SDIBLEXP=6.756 LLMIN=2E-07
+ MOR=1.05E-03 MOEXP=3.146
+ A1R=9.938E+04 STA1=9.3E-02 SLA1=-2.805E-03
+ A2R=4.047E+01 SLA2=1E-15
+ A3R=7.54E-01 SLA3=-8.705E-08
+ COL=3.2E-10
+ NTR=1.6237E-20 NFAR=1 NFBR=0
+ NFCR=0 GATENOISE=0
+ CJBR=1.347E-3 CJSR=0.183E-9 CJGR=0.374E-9
+ JSDBR=0.027E-6 JSDSR=0.040E-12 JSDGR=0.100E-12
+ VR=0.000
+ JSGBR=1.900E-6 JSGSR=78.000E-12 JSGGR=54.000E-12
+ VB=20.000
+ VDBR=0.828 VDSR=0.593 VDGR=0.500
+ PB=0.394 PS=0.171 PG=0.193
+ NB=1.000 NS=1.000 NG=1.000
```

Example 2

```
.model nch nmos level=63
+ VERSION=11010
+ LVAR=0.000000E+00
+ LAP=-1.864000E-08 WVAR=0.000000E+00 WOT=0.000000E+00
+ TR=2.100000E+01 VFB=-1.038000E+00 STVFB=0.000000E+00
+ SLPHIB=-1.024000E-08 SL2PHIB=1.428000E-14 SWPHIB=0.000000E+00
+ KOR=5.763000E-01 SLKO=2.649000E-08 SL2KO=-1.737000E-14
+ SWKO=0.000000E+00 KPINV=2.200000E-01 PHIBR=8.500000E-01
+ BETSQ=1.201000E-04 ETABETR=1.300000E+00 FBET1=-3.741000E-01
+ LP1=2.806000E-06 FBET2=0.000000E+00 LP2=1.000000E-10
+ THESRR=7.109000E-01 SWTHESR=0.000000E+00 THEPHR=1.000000E-03
+ ETAPH=1.750000E+00 SWTHEPH=0.000000E+00 ETAMOB=2.825000E+00
+ STETAMOB=0.000000E+00 SWETAMOB=0.000000E+00 NU=1.000000E+00
+ NUEXP=3.228000E+00 THERR=1.267000E-01 ETAR=4.000000E-01
+ SWTHER=0.000000E+00 THER1=0.000000E+00 THER2=1.000000E+00
+ THESATR=6.931000E-02 SLTHESAT=1.000000E+00
THESATEXP=2.000000E+00
+ ETASAT=8.753000E-01 SWTHESAT=0.000000E+00 SSFR=2.304000E-03
+ SLSSF=1.002000E-06 SWSSF=0.000000E+00 ALPR=1.062000E-02
+ SLALP=9.957000E-01 ALPEXP=1.039000E+00 SWALP=0.000000E+00
+ VP=5.000000E-02 THETHR=2.413000E-03 THETHEXP=1.000000E+00
+ SWTHETH=0.000000E+00 SDIBLO=1.060000E-06 SDIBLEXP=6.756000E+00
+ MOR=1.050000E-03 MOEXP=3.146000E+00 LLMIN=2.000000E-07
+ A1R=9.938000E+04 STA1=9.300000E-02 SLA1=-2.805000E-03
+ SWA1=0.000000E+00 A2R=4.047000E+01 SLA2=1.000000E-15
+ SWA2=0.000000E+00 A3R=7.540000E-01 SLA3=-8.705000E-08
+ SWA3=0.000000E+00 TOX=3.200000E-09 COL=3.200000E-10
+ NT=1.623700E-20 NFAR=1.000000E-00 NFBR=0.000000E+00
+ NFCR=0.000000E+00 GATENOISE =0.00000E-00 DTA=0.000000E-00
```

Example 3

```
.model nch nmos level=63
+ LEVEL =63
+ VERSION=11011
+ LVAR=0 LAP=4.0E-08 WVAR=0.0 WOT=0.0 TR=21 VFB=-0.105E+01
+ POKO=0.5 PLKO=0.0 PWKO=0.0 PLWKO=0.0 KPINV=0.0
+ POPHIB=0.95 PLPHIB=0.0 PWP HIB=0.0 POBET=1.922E-03
+ POTHE SR=3.562E-01 POTHE PH=1.29E-02 POETAMOB=1.4 POTHER=8.120E-
02
+ THER1=0.0 THER2=0.1E+01 POTHE SAT=0.2513 POTHE TH =1.0E-5
+ POSDIBL=8.530E-4 POSSF=1.2E-2 POALP=2.5E-2 VP=5.0E-2
+ POMEXP=0.2 POA1=6.022 POA2=38.02 POA3=0.6407
+ POBINV=48 POBACC=48 KOV=2.5 TOX=3.2E-09
+ POCOX=2.980E-14 POCGDO=6.392E-15 POCGSO=6.392E-15
+ NT=1.656E-20 PONFA=8.323E+22 PONFB=2.514E+7
+ POTVFB=5.0E-4 POTPHIB=-8.5E-4
+ POTETABET=1.30 POTETASR=0.65 POTETAPH=1.350 NU=2.0
+ POTNUEXP=5.25 POTETAR=0.95 POTETASAT=1.040
```

Level 64 STARC HiSIM Model

Note: See [Level 68 STARC HiSIM2 Model](#) for the latest version of this model.

HiSIM (Hiroshima-university STARC IGFET Model) is a publicly-available MOSFET model for circuit simulation. It uses drift-diffusion approximation, and a channel-surface-potential description. You can model all MOSFET characteristics closely, based on their physical origins by using fewer model parameters (about 90 model parameters); each parameter set is sufficient for all gate lengths. These model parameters are directly related to the MOSFET physics that a simulator can easily extract according to its physical meanings.

The STARC HiSIM model is Level 64 in the Synopsys MOSFET models. To use this model, specify:

```
M1 drain gate source bulk NCH w=4u l=1u
.MODEL NCH NMOS LEVEL=64
```

HSPICE HiSIM model code is based on the Spice3f5 version that Hiroshima University/STARC released at the following web site:

<http://www.starc.jp/index-j.html>

Chapter 4: MOSFET Models: LEVELs 50 through 74

Level 64 STARC HiSIM Model

Since the STARC HiSIM1.1.0 release, the Synopsys version of the HiSIM model has included a `VERSION` number parameter to facilitate backward compatibility. Starting in the 2003.03 release, Synopsys uses the STARC version control mechanism so you must enter an integer for the `VERSION` model parameter. For example, to specify HiSIM version 1.0.0, set the `VERSION` model parameter to 100. If you do not set the `VERSION` parameter, simulation issues a warning and automatically sets this parameter to 100.

You can set the `VERSION` value to:

- 100, 101, 102 (HiSIM1.0.* series)
- 110, 111, 112 (HiSIM1.1.* series)
- 120 (HiSIM1.2.*)

Table 48 Level 64 Model Selectors

Parameter	Default	Description
LEVEL	64	Model selector
VERSION	100	Model version number
CORSRD	0(no)	Flag. Indicates whether to include the Rs and Rd contact resistors, and whether to solve equations iteratively. CORSRD=1(yes)
COOVLP	0	Overlap capacitance model selector. <ul style="list-style-type: none">▪ COOVLP=-1, constant value▪ COOVLP=0, approximating the field linear reduction▪ COOVLP=1, considering the lateral impurity profile.
COISUB	0	Substrate current model selector. <ul style="list-style-type: none">▪ for VERSION < 110, COISUB=0 (yes),▪ otherwise, COISUB=1 (no)
COIIGS	0	Selects the gate tunneling current model. <ul style="list-style-type: none">▪ COIIGS=0 (yes),▪ COIIGS=1 (no)

VERSION < 111 does not support this model.

Table 48 Level 64 Model Selectors

Parameter	Default	Description
COGIDL	0	<p>Selects the gate induced drain leakage (GIDL) current model.</p> <ul style="list-style-type: none"> COGIDL=0 (yes) COGIDL=1 (no) <p>VERSION < 111 does not support this model.</p>
CONOIS	0	<p>1/f noise model selector.</p> <ul style="list-style-type: none"> CONOIS=0 (no) CONOIS=1 (yes)
COISTI	0	<p>Selects the shallow-trench-isolation (STI) leakage current.</p> <ul style="list-style-type: none"> COISTI=0 (no) COISTI=1 (yes), only if VERSION ≥ 110.
NOISE	5	<p>Channel thermal and flicker noises combination selector.</p> <ul style="list-style-type: none"> NOISE=1 Channel thermal noise=SPICE2 model Flicker noise=SPICE2 model NOISE=2 Channel thermal noise=HiSIM1 model for the BSIM3 model Flicker noise=HiSIM1 model NOISE=3 Channel thermal noise=SPICE2 model Flicker noise=HiSIM1 model NOISE=4 Channel thermal noise=HiSIM1 model for the BSIM3 model Flicker noise=SPICE2 model NOISE=5 Channel thermal noise=NONE Flicker noise=HiSIM1 model

Chapter 4: MOSFET Models: LEVELs 50 through 74

Level 64 STARC HiSIM Model

Table 49 Level 64 Technological Parameters

Parameter	Default	Description
TOX	3.6e-9m	Oxide thickness
XLD	0.0m	Gate-overlap length
XWD	0.0m	Gate-overlap width
XPOLYD	0.0m	Difference between the gate-poly and the design lengths
TPOLY	0.0m	Height of the gate poly-Si
RS	0.0ohm*m	Source-contact resistance
RD	0.0ohm*m	Drain-contact resistance
NSUBC	5.94e+17cm-3	Substrate-impurity concentration
NSUBP	5.94e+17cm-3	Maxim pocket concentration
VFBC	-0.722729V	Flat-band voltage
LP	0.0m	Pocket penetration length
XJ	0.0m	Junction depth (if VERSION < 110)
XQY	0.0m	Distance from the drain junction to the maximum electric field point (if VERSION ≥ 110)

Table 50 Level 64 Temperature Dependence Parameters

Parameter	Default	Description
BGTMP1	9.03e-5eVK ⁻¹	Bandgap narrowing
BGTMP2	3.05e-7eVK ⁻²	Bandgap narrowing

Table 51 Level 64 Quantum Effect Parameters

Parameter	Default	Description
QME1	0.0mV	Coefficient for the quantum mechanical effect
QME2	0.0V	Coefficient for the quantum mechanical effect
QME3	0.0m	Coefficient for the quantum mechanical effect

Table 52 Level 64 Poly Depletion Parameters

Parameter	Default	Description
PGD1	0.0V	Strength of the poly depletion
PGD2	0.0V	Threshold voltage of the poly depletion
PGD3	0.0	V_{ds} dependence of the poly depletion

Table 53 Level 64 Short Channel Parameters

Parameter	Default	Description
PARL1	1.0	Strength of the lateral-electric-field gradient
PARL2	2.2e-8m	Depletion width of the channel/contact junction
SC1	13.5V ⁻¹	Short-channel coefficient 1
SC2	1.8V ⁻²	Short-channel coefficient 2
SC3	0.0V ⁻² m	Short-channel coefficient 3
SCP1	0.0V ⁻¹	Short-channel coefficient 1 for the pocket
SCP2	0.0V ⁻²	Short-channel coefficient 2 for the pocket
SCP3	0.0V ⁻² m	Short-channel coefficient 3 for the pocket

Table 54 Level 64 Narrow Channel Parameters

Parameter	Default	Description
WFC	0.0m*F/cm ²	Voltage reduction
MUEPH2	0.0	Mobility reduction
W0	0.0log(cm)	Minimum gate width
WVTHSC	0.0	Short-channel effect at the shallow-trench-isolation (STI) edge, if VERSION ≥ 110
NSTI	0.0cm-3	Substrate-impurity concentration at the shallow-trench-isolation (STI) edge, if VERSION ≥ 110
WSTI	0.0m	Width of the high-field region at the shallow-trench-isolation (STI), if VERSION ≥ 110

Table 55 Level 64 Mobility Parameters

Parameter	Default	Description
VDS0	0.05V	Drain voltage for extracting low-field mobility
MUECB0	300.0cm ² /Vs	Coulomb scattering
MUECB1	30.0cm ² /Vs	Coulomb scattering
MUEPH0	0.295	Phonon scattering
MUEPH1	1.0e7	Phonon scattering
MUETMP	0.0	Temperature dependence of phonon scattering
MUESR0	1.0	Surface-roughness scattering
MUESR1	7.0e8	Surface-roughness scattering
NDEP	1.0	Coefficient of the effective-electric field
NINV	0.5	Coefficient of the effective-electric field
NINVD	0.0V ⁻¹	Modification of NINV

Table 55 Level 64 Mobility Parameters

Parameter	Default	Description
BB	2.0(NMOS) 1.0(PMOS)	High-field-mobility degradation
VMAX	1.0e7cm/s	Maximum saturation velocity
VOVER	0.0	Velocity overshoot effect
VOVERP	0.0	L_{gate} dependence of the velocity overshoot
RPOCK1	$0.0V^{2*}m^{1/2}/A$	Resistance coefficient caused by the potential barrier
RPOCK2	0.0V	Resistance coefficient caused by the potential barrier
RPOCP1	0.0	Resistance coefficient caused by the potential barrier, if VERSION \geq 110
RPOCP2	0.0	Resistance coefficient caused by the potential barrier, if VERSION \geq 110

Table 56 Level 64 Channel Length Modulation Parameters

Parameter	Default	Description
CLM1	0.3	Hardness coefficient of the channel/contact junction
CLM2	0.0	Coefficient for the Q_B contribution
CLM3	0.0	Coefficient for the Q_I contribution

Table 57 Level 64 Substrate Current Parameters

Parameter	Default	Description
SUB1	$0.0V^{-1}$	Substrate current coefficient 1
SUB2	-70.0	Substrate current coefficient 2
SUB3	1.0	Substrate current coefficient 3

Table 58 Level 64 Gate Current Parameters

Parameter	Default	Description
GLEAK1	$0.0A \cdot V^{-3/2}/C$	Gate current coefficient 1
GLEAK2	0.0	Gate current coefficient 2
GLEAK3	0.0	Gate current coefficient 3

Table 59 Level 64 GIDL Current Parameters

Parameter	Default	Description
GIDL1	$0.0A \cdot m \cdot V^{-3/2}/C$	GIDL current coefficient 1
GIDL2	$0.0V^{-1/2}/cm$	GIDL current coefficient 2
GIDL3	0.0	GIDL current coefficient 3

Table 60 Level 64 1/f Noise Parameters

Parameter	Default	Description
NFALP	$2.0e-15$	Contribution of the mobility fluctuation
NFTRP	$1.0e11$	Ratio of trap density to the attenuation coefficient
CIT	$0.0F/cm^2$	Capacitance caused by the interface trapped carriers
AF	1.0	SPICE2 flicker noise exponent
KF	0.0	SPICE2 flicker noise coefficient
EF	0.0	SPICE2 flicker noise frequency exponent

Table 61 Conserving Symmetry at $V_{ds}=0$ for Short-Channel MOSFETS

Parameter	Default	Description
VZADD0	$1.0e-2V$	Symmetry conservation coefficient

Table 61 Conserving Symmetry at $V_{ds}=0$ for Short-Channel MOSFETS

Parameter	Default	Description
PZADD0	1.0e-3V	Symmetry conservation coefficient

Table 62 MOS DIODE

Parameter	Default	Description
JSO	1.0e-4Am ⁻²	Saturation current density
JSOSW	0.0Am ⁻¹	Sidewall saturation current density
NJ	1.0	Emission coefficient
NJSW	1.0	Sidewall emission coefficient
XTI	3.0	Junction current temperature exponent coefficient
CJ	8.397247e-04Fm ⁻²	Bottom junction capacitance per unit area at zero bias
CJSW	5.0e-10Fm ⁻¹	Source/drain sidewall junction capacitance per unit area at zero bias
CJSWG	5.0e-10Fm ⁻¹	Source/drain gate sidewall junction capacitance per unit area at zero bias
MJ	0.5	Bottom junction capacitance grading coefficient
MJSW	0.33	Source/drain sidewall junction capacitance grading coefficient
MJSWG	0.33	Source/drain gate sidewall junction capacitance grading coefficient
PB	1.0V	Bottom junction build-in potential
PBSW	1.0V	Source/drain sidewall junction build-in potential
PBSWG	1.0V	Source/drain gate sidewall junction build-in potential

Table 62 MOS DIODE

Parameter	Default	Description
VDIFFJ	0.5V	Diode threshold voltage between source/drain and substrate

Table 63 Subthreshold Swing

Parameter	Default	Description
PTHROU	0.0	Correction for steep subthreshold swing

Note: Model parameter defaults in the above tables are valid only for versions 100 and 110. For other versions, please refer to the following table:

Table 64 Model Parameter Version Defaults

Parameter	Version=100, 110	Others
VMAX	1.00e+7	7.00e+6
BGTMP1	9.03e-5	90.25e-6
BGTMP2	3.05e-7	100.0e-9
TOX	3.60e-9	5.0e-9
RS	0.0	80.0e-6
RD	0.0	80.0e-6
VFBC	-0.722729	-1.0
NSUBC	5.94e+17	1.0e+17
PARL2	2.20e-8	1.0e+17
LP	0.0	15.0e-9
NSUBP	5.94e+17	1.0e+17
SC1	13.5	0.0

Table 64 Model Parameter Version Defaults

Parameter	Version=100, 110	Others
SC2	1.8	0.0
PGD1	0.0	0.01
PGD2	0.0	1.0
PGD3	0.0	0.8
NINVD	0.0	1.0e-9
MUEPH1	1.00e+7	25.0e+3
MUEPH0	0.295	0.300
MUESR1	7.00e+8	2.0e+15
MUESR0	1.0	2.0
MUETMP	0.0	1.5
SUB1	0.0	10.0
SUB2	-70.0	20.0
SUB3	1.0	0.8
CJ	8.397247e-04	5.0e-04
CLM1	0.3	0.7
CLM2	0.0	2.0
CLM3	0.0	1.0
RPOCK1	0.0	0.01
RPOCK2	0.0	0.1
RPOCP1	0.0	1.0
VOVER	0.0	0.01

Table 64 Model Parameter Version Defaults

Parameter	Version=100, 110	Others
VOVERP	0.0	0.1
QME1	0.0	40.0e-12
QME2	0.0	300.0e-12
GIDL1	0.0	5.0e-3 for HiSIM101, 5.0e-6 for others
GIDL2	0.0	1.0e+6
GIDL3	0.0	0.3
GLEAK1	0.0	0.01e+6 for HiSIM101, 10.0e+3 for others
GLEAK2	0.0	20.0e+6
GLEAK3	0.0	0.3
PZADD0	1.0e-3	5.0e-3
NFTRP	100.0e+9	10.0e+9
NFALP	2.00e-15	1.0e-16

To turn off the model effects, use the following settings:

- Short-Channel Effect $SC1=SC2=SC3=0$
- Reverse-Short-Channel Effect $LP=0$
- Quantum-Mechanical Effect $QME1=QME2=QME3=0$
- Poly-Depletion Effect $PGD1=PGD2=PGD3=0$
- Channel-Length Modulation $CLM1=CLM2=CLM3=0$
- Narrow-Channel Effect $WFC=MUEPH2=0$

Level 68 STARC HiSIM2 Model

HiSIM (Hiroshima University/STARC IGFET Model) is the first complete surface-potential-based MOSFET model for circuit simulation. The most important advantage of the surface-potential-based modeling is the unified description of device characteristics for all bias conditions. The physical reliability of the drift-diffusion approximation has been proved by 2-D device simulations with channel lengths below 0.1 μm .

Note: HiSIM2 source code, and all copyrights, trade secrets or other intellectual property rights in and to the source code in its entirety, is owned by Hiroshima University and STARC.

The following sections discuss these topics:

- [HiSIM Version 2.3.1](#)
- [Level 68 HiSIM Model v2.4.1, 2.4.2, 2.4.3, and 2.5.0](#)
- [Updates Based on HiSIM 2.4.1](#)
- [Updates Based on HiSIM 2.4.2](#)
- [Updates Based on HiSIM 2.4.3](#)
- [Updates Based on HiSIM 2.5.0](#)

HiSIM Version 2.3.1

The STARC HiSIM2 is Level 68 in the Synopsys MOSFET models. HiSIM2.3.1 is an improved version that resolved many issues of previous releases.

HiSIM version 2.3.1 provides:

- Improved Linear Region Modeling
- Improved Small Size Model
- Improved Isub Model
- Inclusion of Induced Gate Noise
- Support for DFM (Interface to Instance Parameters)

Level 68 HiSIM Model v2.4.1, 2.4.2, 2.4.3, and 2.5.0

To obtain analytical solutions for describing device performances, the charge sheet approximation of the inversion layer with zero thickness has been introduced. Together with the gradual-channel approximation all device characteristics are then described analytically by the channel-surface potentials at the source side and at the drain side. These surface potentials are functions of applied voltages on the four MOSFET terminals; the gate voltage V_g , the drain voltage V_d , the bulk voltage V_b and the reference potential of the source V_s . This is the long-channel basis of the HiSIM model, and extensions of the model approximations are done for advanced technologies. All newly appearing phenomena such as short-channel and reverse-short-channel effects are included in the surface potential calculations causing modifications resulting from the features of these advanced technologies. See also: [Updates Based on HiSIM 240SC2](#), [Updates Based on HiSIM 2.4.1](#), [Updates Based on HiSIM 2.4.2](#), [Updates Based on HiSIM 2.4.3](#), and [Updates Based on HiSIM 2.5.0](#).

For details and usage, contact the Synopsys support team.

The following sections describe these topics:

- [General Syntax for the HiSIM241 Model](#)
- [Listing of Instance Parameters for HiSIM 2.4.1](#)
- [Updates Based on HiSIM 240SC2](#)

General Syntax for the HiSIM241 Model

The following lists and describes the HiSIM Level 68 general parameters.

```
Mxxx nd ng ns [nb] mname [L=val] [W=val] [M=val]
+ [AD=val] [AS=val] [PD=val] [PS=val]
+ [NRS=val] [NRD=val] [XGW=val] [XGL=val]
+ [NF=val] [NGCON=val] [RBPB=val] [RBPD=val]
+ [RBPS=val] [RBDB=val] [RBSB=val] [SA=val]
+ [SB=val] [SD=val] [TEMP=val] [DTEMP=val]
+ [NSUBCDFM=val]

.MODEL MNAME N(P)MOS LEVEL=68 VERSION=240.0
+ [CORSRD=val] [COOVLP=val] [COISUB=val]
+ [COIIGS=val] [COGIDL=val] [COISTI=val]
+ [COADOV=val] [CONQS=val] [CORG=val] [CORBNET=val]
+ [COFLICK=val] [COTHRML=val] [COIGN=val] [COIPRV=val]
```

+ [COPPRV=*val*] [CODFM=*val*]
+

The following tables list parameters that have been updated to the HiSIM 240 SC2 release.

Table 65 HiSIM Level 68 General Parameters

Parameter	Description
CORSRD= <i>val</i>	The following flags are prepared to select required model options. <ul style="list-style-type: none"> 0: no (default) 1 & $RS/RD \neq 0$: yes, as internal resistances of HiSIM 2 & $RD \neq 0$: yes, analytical description 3 & $RD \neq 0$: yes, both internal and analytical descriptions -1 $RS/RD \neq 0$: yes, as external resistances of HiSIM
COOVLP= <i>val</i>	Overlap capacitance model is selected as: <ul style="list-style-type: none"> 0: constant overlap capacitance 1: (yes, default)
COISUB = <i>val</i>	Substrate current I_{sub} is calculated: <ul style="list-style-type: none"> 0: no (default) 1: yes
COIIGS = <i>val</i>	Gate current I_{gate} is calculated: <ul style="list-style-type: none"> 0: no (default) 1: yes
COGIDL = <i>val</i>	GIDL current I_{GIDL} is calculated: <ul style="list-style-type: none"> 0: no (default) 1: yes
COISTI = <i>val</i>	STI leakage current $I_{ds, STI}$ is calculated: <ul style="list-style-type: none"> 0: no (default) 1: yes
COADOV = <i>val</i>	Lateral field induced and overlap charges/capacitances are added to intrinsic ones: <ul style="list-style-type: none"> 0: no 1: yes (default)

Table 65 HiSIM Level 68 General Parameters

Parameter	Description
CONQS = <i>val</i>	Non-quasi-static mode is invoked: <ul style="list-style-type: none"> ▪ 0: no (default) ▪ 1: yes
CORG = <i>val</i>	Gate-contact resistance is included (This flag can also be given as an instance parameter): <ul style="list-style-type: none"> ▪ 0: no (default) ▪ 1: yes
CORBNET = <i>val</i>	Substrate resistance network is invoked (This flag can also be given as a instance parameter): <ul style="list-style-type: none"> ▪ 0: no (default) ▪ 1: yes
COFLICK = <i>val</i>	1/f noise is calculated: <ul style="list-style-type: none"> ▪ 0: no (default) ▪ 1: yes
COTHRML = <i>val</i>	Thermal noise is calculated: <ul style="list-style-type: none"> ▪ 0: no (default) ▪ 1: yes
COIGN = <i>val</i>	Induced gate and cross correlation noise are calculated: <ul style="list-style-type: none"> ▪ 0 COTHRML = 0: no (default) ▪ 1 & COTHRML = 1: yes
COIPRV = <i>val</i>	Previous I_{ds} is used for calculating source/drain resistance effect (R_s and/or $R_d \neq 0$): <ul style="list-style-type: none"> ▪ 0: no ▪ 1: yes (default)
COPPRV = <i>val</i>	Previous ϕ_s is used for the iteration: <ul style="list-style-type: none"> ▪ 0: no ▪ 1: yes (default)
CODFM = <i>val</i>	Parameter variations for the DFM support is considered: <ul style="list-style-type: none"> ▪ 0: no (default) ▪ 1: yes

Table 65 HiSIM Level 68 General Parameters

Parameter	Description
COSELFHEAT = <i>val</i>	<ul style="list-style-type: none"> ▪ 0: no (default) ▪ 1: yes

Listing of Basic Device Parameters

Table 66 Basic Device Parameters

Parameter	Description
TOX	Physical oxide thickness
XL	Difference between real and drawn gate length
XW	Difference between real and drawn gate width
XLD	Gate-overlap in length
XWD	Gate-overlap in width
TPOLY	Height of the gate poly-Si for fringing capacitance
LL	Coefficient of gate length modification
LLD	Coefficient of gate length modification
LLN	Coefficient of gate length modification
WL	Coefficient of gate width modification
WLD	Coefficient of gate width modification
WLN	Coefficient of gate width modification
NSUBC	Substrate-impurity concentration
NSUBP	Maximum pocket concentration
LP	Pocket penetration length
*NPEXT	Maximum concentration of pocket tail

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Level 68 STARC HiSIM2 Model

Table 66 Basic Device Parameters

Parameter	Description
*LPEXT	Extension length of pocket tail
VFBC	Flat-band voltage
VBI	Built-in potential
KAPPA	Dielectric constant for gate dielectric
EG0	Bandgap
BGTMP1	Temperature dependence of bandgap
BGTMP2	Temperature dependence of bandgap
TNOM	Temperature selected as nominal temperature value

Table 67 Velocity

Parameter	Description
VMAX	Saturation velocity
VOVER	Velocity overshoot effect
VOVERP	L_{eff} dependence of velocity overshoot
*VTMP	Temperature dependence of the saturation velocity

Table 68 Quantum-Mechanical Effects

Parameter	Description
QME1	V_{gs} dependence
QME2	V_{gs} dependence
QME3	Minimum T_{ox} modification

Table 69 Poly-Silicon Depletion Effects

Parameter	Description
PGD1	Strength of poly depletion
PGD2	Threshold voltage of poly depletion
PGD3	V_{ds} dependence of poly depletion
*PGD4	L_{gate} dependence of poly depletion

Table 70 Short Channel Effect

Parameter	Description
PARL2	Depletion width of channel/contact junction
SC1	Magnitude of short-channel effect
SC2	V_{ds} dependence of short-channel effect
*SC3	V_{bs} dependence of short-channel effect
SCP1	Magnitude of short-channel effect due to pocket
SCP2	V_{ds} dependence of short-channel due to pocket
*SCP3	V_{bs} dependence of short-channel effect due to pocket
*SCP21	Short-channel-effect modification for small V_{ds}
*SCP22	Short-channel-effect modification for small V_{ds}
*BS1	Body-coefficient modification due to impurity profile
*BS2	Body-coefficient modification due to impurity profile

HSPICE prints mobility parameters for Level 68.

Table 71 Mobility Model

Parameter	Description
MUECB0	Coulomb scattering

Table 71 Mobility Model (Continued)

Parameter	Description
MUECB1	Coulomb scattering
MUEPH0	Phonon scattering
MUEPH1	Phonon scattering
*MUEPHL	Length dependence of phonon mobility reduction
*MUEPHP	Length dependence of phonon mobility reduction
MUESR0	Surface roughness scattering
MUESR1	Surface roughness scattering
*MUESRL	Length dependence of surface roughness mobility reduction
*MUESLP	Length dependence of surface roughness mobility reduction
NDEP	Depletion charge contribution on effective-electric field
*NDEPL	Modification of depletion charge contribution for short-channel case
*NDEPLP	Modification of depletion charge contribution for short-channel case
NINV	Inversion charge of depletion charge contribution for short-channel case
BB	High-field-mobility degradation
VOVERP	L_{eff} dependence of velocity overshoot

Table 72 Channel-Length Modulation

Parameter	Description
CLM1	Hardness coefficient of channel/contact junction
CLM2	Coefficient for Q_B contribution
CLM3	Coefficient for Q_I contribution
CLM4	No longer used

Table 72 Channel-Length Modulation (Continued)

Parameter	Description
*CLM5	Effect of pocket implantation
*CLM6	Effect of pocket implantation

Table 73 Narrow Channel Effects

Parameter	Description
WFC	Threshold voltage change due to capacitance change
*WVTH0	Threshold voltage drift
*NSUBP0	Modification of pocket concentration for narrow width
*NSUBWP	Modification of pocket concentration for narrow width
*MUEPHW	Phonon-related mobility reduction
*MUEPHP	Phonon-related mobility reduction
*MUESRW	Change of surface roughness related mobility
*MUESRW	Change of surface roughness related mobility
*VTHSTI	Threshold voltage shift due to STI
*VDSTI	V_{ds} dependence of threshold voltage shift due to STI
*SCSTI1	The same effect as SC1 but at STI edge
*SCSTI2	The same effect as SC2 but at STI edge
SCSTI3	No longer use
NSTI	Substrate impurity concentration at STI edge
WSTI	Width of the high-field region at STI edge
*WSTIL	Channel-width dependence of WSTI
*WSTILP	Channel-width dependence of WSTI

Chapter 4: MOSFET Models: LEVELs 50 through 74

Level 68 STARC HiSIM2 Model

Table 73 Narrow Channel Effects (Continued)

Parameter	Description
*WSTILW	Channel-width dependence of WSTI
*WSTIWP	Channel-width dependence of WSTI
WL1	Threshold voltage shift of STI leakage due to small size effect
WL1P	Threshold voltage shift of STI leakage due to small size effect
NSUBPSTI1	Pocket concentration change due to diffusion-region length between gate and STI
NSUBPSTI2	Pocket concentration change due to diffusion-region length between gate and STI
NSUBPSTI3	Pocket concentration change due to diffusion-region length between gate and STI
MUESTI1	Mobility change due to diffusion-region length between gate and STI
MUESTI2	Mobility change due to diffusion-region length between gate and STI
MUESTI3	Mobility change due to diffusion-region length between gate and STI
SAREF	Length of diffusion between gate and STI
SBREF	Length of diffusion between gate and STI

Table 74 Small Size Effect

Parameter	Description
WL2	Threshold voltage shift due to small size effect
WL2P	Threshold voltage shift due to small size effect
*MUEPHS	Mobility modification due to small size
*MUEPSP	Mobility modification due to small size
*VOVERS	Modification of maximum velocity due to small size
*VOVERSP	Modification of maximum velocity due to small size

Table 75 Substrate Currents

Parameter	Description
SUB1	Substrate current coefficient of magnitude
SUB1L	L_{gate} dependence SUB1
SUB1LP	L_{gate} dependence SUB1
SUB2	Substrate current coefficient of exponential term
SUB2L	L_{gate} dependence SUB2
SVDS	Substrate current dependence on V_{ds}
SLG	Substrate current dependence on L_{gate}
SLGL	Substrate current dependence on L_{gate}
SLGLP	Substrate current dependence on L_{gate}
SVBS	Substrate current dependence on V_{bs}
SVBSL	L_{gate} dependence of SVBS
SVBSLP	L_{gate} dependence of SVBS
SVGS	Substrate current dependence of SVGS
SVGSL	L_{gate} dependence of SVGS
SVGSLP	L_{gate} dependence of SVGS
SVGSLW	W_{gate} dependence of SVGS
SVGSLWP	W_{gate} dependence of SVGS

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Table 76 Subthreshold Swing

Parameter	Description
*PTHOU	Correction for subthreshold swing

Table 77 Impact- Ionization Induced Bulk Potential Change

Parameter	Description
IBPC1	Impact-ionization induced bulk potential change
IBPC2	Impact-ionization induced bulk potential change

Table 78 Gate Leakage Current

Parameter	Description
GLEAK1	Gate to channel current coefficient
GLEAK2	Gate to channel current coefficient
GLEAK3	Gate to channel current coefficient
GLEAK4	Gate to channel current coefficient
*GLEAK5	Gate to channel current coefficient (short channel correction)
*GLEAK6	Gate to channel current coefficient (V_{ds} dependence correction)
*GLEAK7	Gate to channel current coefficient (gate length and width dependence correction)
*EGIG	Bandgap of gate leakage
*IGTEMP2	Temperature dependence of gate leakage
*IGTEMP3	Temperature dependence of gate leakage
GLKB1	Gate to bulk current coefficient
GLKB2	Gate to bulk current coefficient
GLKB3	Flat-band shift for gate to bulk current

Table 78 Gate Leakage Current (Continued)

Parameter	Description
GLKBD1	Gate to source/drain current coefficient
GLKBD2	Gate to source/drain current coefficient
GLKBD3	Gate to source/drain current coefficient
GLPART1	Partitioning ratio of gate leakage current
FN1	Coefficient of Fowler-Nordheim-current contribution
FN2	Coefficient of Fowler-Nordheim-current contribution
FN3	Coefficient of Fowler-Nordheim-current contribution
FVBS	V_{bs} dependence of Fowler-Nordheim current

Table 79 GIDL Current

Parameter	Description
GIDL1	Magnitude of the GIDL
GIDL2	Field dependence of the GIDL
GIDL3	V_{ds} of the GIDL
*GIDL4	Threshold of V_{ds} dependence
*GIDL5	Correction of high-field contribution

Table 80 Parasitic Resistances

Parameter	Description
RS	Source-contact resistance of LDD region
RD	Drain-contact resistance of LDD region
RSH	Source/drain sheet resistance of diffusion region
RSHG	Gate sheet resistance

Table 80 Parasitic Resistances (Continued)

Parameter	Description
GBMIN	Substrate resistance network
RBPB	Substrate resistance network
RBPD	Substrate resistance network
RBPS	Substrate resistance network
RBDB	Substrate resistance network
RBSB	Substrate resistance network

Table 81 Binning Model

Parameter	Description
LBINN	Power of L_{drawn} dependence
WBINN	Power of W_{drawn} dependence
LMAX	Maximum length of L_{drawn} valid
LMIN	Minimum length of L_{drawn} valid
WMAX	Maximum length of W_{drawn} valid
WMIN	Minimum length of W_{drawn} valid

Table 82 Capacitances

Parameter	Description
XQY	Distance from drain junction to maximum electric field point
*XQY1	V_{bs} dependence of Q_y
*XQY2	L_{gate} dependence of Q_y
LOVER	Overlap length

Table 82 Capacitances (Continued)

Parameter	Description
NOVER	Impurity concentration in overlap region
VFBOVER	Flat-band voltage in overlap region
OVSLP	Coefficient for overlap capacitance
OVMAG	Coefficient for overlap capacitance
CGSO	Gate-to-source overlap capacitance
CGDO	Gate-to-drain overlap capacitance
CGBO	Gate-to-bulk overlap capacitance

Table 83 Conservation of Symmetry at $V_{ds} = 0$ for Short-Channel MOSFETs

Parameter	Description
VZADD0	Symmetry conservation coefficient
PZADD0	Symmetry conservation coefficient

Table 84 Smoothing Coefficient Between Linear and Saturation Region

Parameter	Description
*DDLTMAX	Smoothing coefficient for V_{ds}
*DDLTSKP	L_{gate} dependence of smoothing coefficient
*DDLTICT	L_{gate} dependence of smoothing coefficient

Table 85 Source/Bulk and Drain/Bulk Diodes

Parameter	Description
JS0	Saturation current density
JS0SW	Sidewall saturation current density
NJ	Emission coefficient

Table 85 Source/Bulk and Drain/Bulk Diodes (Continued)

Parameter	Description
NJSW	Sidewall emission coefficient
XTI	Temperature coefficient for forward-current densities
XTI2	Temperature coefficient for reverse-current densities
DIVX	Reverse current coefficient
CISB	Reverse biased saturation current
CVB	Bias dependence coefficient of CISB
CTEMP	Temperature coefficient of reverse currents
CISBK	Reverse biased saturation current (at low temperature)
CVBK	Bias dependence coefficient of CISB (at low temperature)
CJ	Bottom junction capacitance grading coefficient
CJSW	Source/drain sidewall junction capacitance grading coefficient per unit length at zero bias
CJSWG	Source/drain sidewall junction capacitance per unit length at zero bias
MJ	Bottom junction capacitance grading coefficient
MJSW	Source/drain sidewall junction capacitance grading coefficient
MJSWG	Source/drain gate sidewall junction capacitance grading coefficient
PB	Bottom junction built-in potential
PBSW	Source/drain sidewall junction built-in potential
PBSWG	Source/drain gate sidewall junction built-in potential
VDIFFJ	Diode threshold voltage between source/drain and substrate

Table 86 *1/f Noise*

Parameter	Description
NFALP	Contribution of the mobility fluctuation
NFTRP	Ratio of trap density to attenuation coefficient
*CIT	Capacitance caused by the interface trapped carriers

Table 87 *DFM Support*

Parameter	Description
MPHDFM	Mobility dependence on NSUBC due to μ_{phonon}

Table 88 *Non-Quasi-Static (NQS) Model*

Parameter	Description
DLY1	Coefficient for delay due to diffusion of carriers
DLY2	Coefficient for delay due to conduction of carriers
DLY3	Coefficient for RC delay of bulk carriers

Listing of Instance Parameters for HiSIM 2.4.1

The following table lists the general instance parameters, following by instance parameters for: Source/Drain Resistance, Gate Resistance, Substrate Network, Length of Diffusion, Temperature and DFM.

Table 89 *Instance Parameters*

Parameter	Description
L	Gate length (L_{gate})
W	Gate width (W_{gate})
Diode	
AD	Junction area of the drain contact

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Table 89 Instance Parameters

Parameter	Description
PD	Junction periphery of the drain contact
AS	Junction area of the source contact
PS	Junction periphery of the source contact
Source/Drain Resistance	
NRS	Number of source squares
NRD	Number of drain squares
Gate Resistance	
XGW	Distance from the gate contact to the channel edge
XGL	Offset of the gate length
NF	Number of gate fingers
NGCON	Number of gate contacts
Substrate Network	
RBPB	Substrate resistance network
RBPD	Substrate resistance network
RBPS	Substrate resistance network
RBDB	Substrate resistance network
RBSB	Substrate resistance network
Length of Diffusion	
SA	Length of diffusion between gate and STI
SB	Length of diffusion between gate and STI
SD	Length of diffusion between gate and gate

Table 89 Instance Parameters

Parameter	Description
Temperature	
TEMP	Device temperature (T)
DTEMP	Device temperature change
Design for Manufacturability	
NSUBCDFM	Substrate impurity concentration

Updates Based on HiSIM 240SC2

The following changes and fixed issues are implemented in the SC2 release:

- Multiplication factor #M is introduced.
- Bugs in the derivatives of Ps0 in the accumulation zone.
- Bugs in the derivatives of T10 in Igate model.
- Bug in Vdsat output for users (caused by Qover model).
- ISBS2-related bugs in the junction-diode-current model.
- Default values for NSTI and EGIG were wrong. NSTI = 0.0 changed to NSTI = 5.0e17, EGIG = 1.1 changed to EGIG = 0.0
- Coding bug in the DFM model.

Changed Parameters

The following parameters have been changed or modified:

- Removed Parameter: SCSTI3
- Replaced Parameters: CLM4 (replaced for DDLTMAX, DDLTICT and DDLTSLP), #LOD (replaced for #SA, #SB, #SD, SAREF and SBREF)
- Renamed Parameter: IGTEMP1 changed to EGIG

In the following table: “//” indicates values not changed from HiSIM2.3.1-SC9.
The # mark indicates instance parameters.

Table 90 Changed/Added Default Parameters/Ranges from HiSIM2.3.1-SC9

Parameter	Unit	Min	Default	Max	Description
Unit/default value modified parameters					
RS	$\Omega \cdot m$	//	//	//	Source-contact resistance in LDD region
RD	$\Omega \cdot m$	//	//	//	Drain-contact resistance in LDD region
LOVER	//	//	30e-9	//	Overlap length.
VBI	//	//	1.1	1.2	Built-in potential.
PGD1	//	//	0.0	//	Strength of poly-Si gate depletion.
GIDL4	V	//	0.0	//	Threshold of Vds dependence.
NSTI	cm-3	//	5.0e17	//	Substrate-impurity concentration at STI edge.
Added model flag					
CODFM	None	0	0	1	Flag for DFM support.
Added parameters					
DDLTMAX	None	0.0	10.0	20.0	Smoothing coefficient for Vds
DDLTICT	None	-3.0	10.0	20.0	Lgate dependence of smoothing coeff.
DDLTSLP	1/ (μm)	0.0	0.0	20.0	Lgate dependence of smoothing coeff.
VFBOVER	V		-0.5		Flat-band voltage in overlap region
NOVER	cm-3		0.0		Impurity concentration in overlap region
XL	m		0.0		Gate length offset due to mask/etch effect
XW	m		0.0		Gate width offset due to mask/etch effect

Table 90 Changed/Added Default Parameters/Ranges from HiSIM2.3.1-SC9

Parameter	Unit	Min	Default	Max	Description
SAREF	m		1e-6		Reference distance from STI edge to Gate edge
SBREF	m		1e-6		Reference distance from STI edge to Gate edge
#SA	m		0		Distance from STI edge to Gate edge
#SB	m		0		Distance from STI edge to Gate edge
#SD	m		0		Distance from Gate edge to Gate edge
XQY1	$F \cdot \mu m^{Q_{XY2}-1}$		0.0		Vbs dependence of Qy
XQY2	None		2.0		Lgate dependence of Qy
NDEPL	None		0.0		Modification of Qb contribution for short-channel case
NDEPLP	None		1.0		Modification of Qb contribution for short-channel case
WSTIW	μm^{WSTIWP}		0.0		Channel-width dependence of WSTI
WSTIWP	None		1.0		Channel-width dependence of WSTI
VDSTI	None		0.0		Vds dependence of STI subthreshold
GLKB3	V		0.0		Flat-band shift for gate to bulk current
MPHDFM	None	-3.0	-0.3	3.0	NSUBC dependence of μ_{phonon} for DFM support
#NSUBCDFM	None	1.0e16	None	1.0e19	NSUBC as an instance parameter for DFM support
#M	None		1.0		Multiplication factor

6 + 74 × 3 = 228 binning parameters are added in addition to the above parameters.

Updates Based on HiSIM 2.4.1

The following is a summary of updates and changes from HiSIM 240-SC2 to HiSIM 2.4.1:

1. Induced Gate Noise model: bug fix to avoid division by zero and use of uninitialized values.
2. Impact-ionization-induced Bulk Potential Change model: bug fix of derivatives when **CORSRD = 1**.
3. Bug fix of numerical calculation for surface potentials.
4. The W and/or L dependence of the gate resistance model was discontinuous.
5. Bug fix to avoid division by zero if **DLY1 = 0** and **DLY2 = 0** in **NQS** model.
6. Improved capacitance reciprocity in **AC** analysis.
7. Fixed the inconsistency result of **AC** analysis and **TR** analysis in **NQS** model.
8. Bug fix of sign of the parasitic capacitances for the small-signal **NQS** model.
9. Bug fix of handling the multiplication factor **M**.
10. Bug fix of handling the number of gate fingers **NF**.
11. The thermal noise and flicker noise were incorrect in some cases.
12. The temperature specification with an instance parameter **TEMP** was invalid.
13. The **M * NF** was multiplied twice for output values like **gigds** and **gigss**.
14. Bug fix of extrapolation when Vbse less than 10.5 V.
15. Changed the minimum and maximum values of the model parameters **CVB**, **CVBK** and **DDLMAX**.
16. The parameter **SVBSLP**, **SVGSW** and **SVGSWP** were not declared in hsm2mask.
17. Bug fix to avoid the negative **Cgb**.
18. Improvements and bug fixes of the overlap charge model.
19. Bug fix to avoid division by zero in calculation of **Vdx2**.
20. The temperature dependence of the noise value was incorrect.
21. Deleted the unnecessary 'ifdef' statements in hsm2acld.c.

22. Initialize the pyABb_i for **AC-NQS** model.
23. Fixed the gate partitioning model for **lgate**.
24. If **GLPART1 != 0.5**, the option calculating explicitly is selected.

For the full release note for the HiSIM 2.4.1, go to:

<http://www.starc.jp/other/contactus-e.html>

Updates Based on HiSIM 2.4.2

The following is a summary of bug fixes and changes over version 2.4.1 per the HiSim-STARC release note.

1. The calculation of Taub for NQS model was corrected.
2. The avoidance of zero division.
3. The deletion of the unnecessary sentence.
4. Bug fix of asymmetrical Qover model.
5. The initial setting of GLPART1 was missed.
6. The default value of model parameter 'VERSION' was corrected.
7. The calculation of the induced gate noise with M factor != 1 was corrected.
8. The calculation of lgate model was corrected.
9. Changes to the default model parameters as follows:
 - GLKSD2 1e-2
 - GLKSD3 -1e-2
 - FN1 0.0
 - FN2 0.0
 - FVBS 0.0

Updates Based on HiSIM 2.4.3

The following summarizes the bug fixes and changes from HiSIM 2.4.2 to 2.4.3 per the HiSim-STARC release note.

1. A bug in hsm2temp was fixed.
2. Bugs of the Vbsz dependence were fixed.

3. Improved capacitance characteristics.

Updates Based on HiSIM 2.5.0

The following is a summary of bug fixes and enhancements from version 2.4.3 to 2.5.0 per the HiSim-STARC release notes.

1. A new highly accurate intrinsic capacitance model is added, which is controlled by new model parameter CORECIP (default=0). In addition, if CORECIP=1 is set and an overlap capacitance is added with COADOV=1, it is recommended to give a non-zero NOVER value. For Igb calculation, model parameter values must preserve that VFBC+GLKB3 <= 0.
2. Changed some smoothing parameter values for better fitting.
3. Fixed bugs related to poly-depletion model.
4. Removed negative-capacitance clamping.
5. Fixed several bugs related to QM effects.
6. Added reverse-mode treatment for IGISL and IGIDL.
7. Fixed bugs related to derivative calculations.

For more details, please refer to the official Hiroshima University HiSIM2 release website:

<http://home.hiroshima-u.ac.jp/usdl/HiSIM2/C-Code/protect.cgi>

Level 69 PSP100 DFM Support Series Model

The PSP100 model is a compact MOSFET model intended for digital, analog, and RF designs. It has been jointly developed by the Pennsylvania State University and Philips Research. The roots of this model lie in both SP (Penn State) and MOS Model 11 (Philips).

It is a surface-potential based MOS model containing all relevant physical effects (mobility reduction, velocity saturation, DIBL, gate current, lateral doping gradient effects, STI stress, and so forth), to model present-day and upcoming deep-submicron bulk CMOS technologies. The JUNCAP2 source/drain junction model is an integrated part of PSP100.

For a full description of the PSP100 models, see <http://pspmodel.asu.edu/>.

The following sections discuss these topics:

- [General Features](#)
- [PSP100.1 Model](#)
- [PSP101.0 Model](#)
- [PSP102.0 Model](#)
- [PSP102.1 Model](#)
- [PSP102.2 Model](#)
- [PSP102.3 Model](#)
- [PSP103.0 Model](#)
- [Usage in HSPICE](#)
- [Instance Parameter Lists](#)
- [Model Parameter Lists](#)
- [Source- and Drain-Bulk Junction Model Parameters](#)
- [Output Templates: PSP Models](#)

General Features

The PSP general features of this model are:

- Physical surface-potential-based formulation in both intrinsic and extrinsic model modules
- Physical and accurate description of the accumulation region
- Inclusion of all relevant small-geometry effects
- Modeling of the halo implant effects, including the output conductance degradation in long devices
- Coulomb scattering and non-universality in the mobility model
- Non-singular velocity-field relation enabling the modeling of RF distortions, including intermodulation effects
- Complete Gummel symmetry
- Mid-point bias linearization enabling accurate modeling of the ration-based circuits (for example, R2R circuits)
- Quantum-mechanical corrections

- Correction for the polysilicon depletion effects
- Gate-induced drain leakage (GIDL) and gate-induced source leakage current (GISL) model
- Surface-potential-based noise model including channel thermal noise, flicker noise, and channel-induced gate noise
- Advanced junction model, including trap-assisted tunneling, band-to-band tunneling, and avalanche breakdown
- Spline-collocation-based non-quasi-static (NQS) model, including all terminal currents
- Stress model (based on BSIM4 version)

PSP100.1 Model

The PSP100.1 model is compatible with the PSP100 model. It improves performance by about a factor of 2, and adds a thermal noise coefficient (FNT) parameter. This parameter is used to add in thermal noise. Set $FNT=1$ (default) to turn on thermal noise. Set $FNT=0$ to turn off thermal noise.

PSP101.0 Model

The PSP101.0 model is *not* backward compatible with PSP100.1.

The most important changes include:

- A complete set of binning scaling rules was added as a phenomenological alternative to the physics-based geometrical scaling rules
- BSIM-like instance parameters AS, AD, PS and PD were added for the junction model
- To avoid confusion between zeros and “O”s, zeros no longer occur in parameter names. They have all been replaced by “O”s
- Some global parameter names have an additional “O” in their names in order to avoid duplicate names in the global and local model

PSP102.0 Model

The PSP102.0 model is backward-compatible with PSP101.0 in all practical cases.

The most important changes include:

- The value for LG when SWJUNCAP=2 was corrected
- The clipping/limiting behavior of NP has been made more transparent
- A minor numerical issue was resolved
- The scaling rule for DPHIB is now correctly implemented

PSP102.1 Model

The PSP102.1 model is backward-compatible with PSP102.0.

The main changes include:

- Added clipping boundaries for SWNQS
- Made several minor changes and improvements in model implementation
- Solved bug in stress model
- Solved bug in JUNCAP2

PSP102.2 Model

The PSP102.2 model is backward-compatible with PSP102.1.

The main changes are:

- Added well proximity effect (WPE) model according to CMC's specification
- Added parameters EPSROX (local), EPSROXO (global), POEPSROX (binning) representing relative dielectric constant of gate oxide
- Added instance parameters DELVTO and FACTUO to local, global, and binning model
- Added NF support to global and binning model
- Extended stress model to support NF
- Added substrate resistance network and external gate resistance to PSP model besides NQS mode

- Added geometry scaling for gate resistance in global and binning models, resulting in additional model parameters RSHG, RINT, DLSIL, and RVPOLY and instance parameters NGCON and XGW
- Added JUNCAP2 Express as an optional alternative to the full JUNCAP2 model. Added related model parameters SWJUNEXP, VJUNREF, and FJUNQ, using model parameter SWJUNEXP=1 to enable JUNCAP2 Express model
- Added “dummy” parameters LMIN, LMAX, WMIN, WMAX to binning model, which can be used as labels for the binning parameter sets
- Some minor bug fixes and minor implementation changes

PSP102.3 Model

PSP 102.3 is backward compatible with PSP 102.2. The main changes are:

- Added asymmetric junction model for the drain-bulk junction. The new junction parameters have a suffix “D” added to their names. When SWJUNASYM = 1 the original parameters are used for the sourcebulk junction and the new parameters are used for drain-bulk junction. When SWJUNASYM = 0 the original junction parameters are used for both source-bulk and drain-bulk junctions as in symmetric case, and the new junction parameters are neglected.
- Added asymmetric models for the overlap region of the drain side. These include:
 - Added related model parameters TOXOVDO, LOVD and NOVDO to global, TOXOVD and NOVD to local and POTOXOVD, PONOVD, PLNOVD, PWNOVD and PLWNOVD to binning models.
 - Asymmetric GIDL/GISL model. Added related parameters AGIDLDO, BGIDLDO, STBGIDLDO and CGIDLDO to global, AGIDL, BGIDL, STBGIDL and CGIDL to local and POAGIDL, PLAGIDL, PWAGIDL, PLWAGIDL, POBGIDL, POSTBGIDL and POCGIDL to binning models.
 - Asymmetric overlap gate current model. Added related parameters IGOVDW to global, IGOVD to local and POIGOVD, PLIGOVD, PWIGOVD and PLWIGOVD to binning models.
 - Asymmetric overlap capacitance model. Added related parameters CGOVD to local, POCGOVD, PLCGOVD, PWCGOVD and PLWCGOVD to binning models.

- Asymmetric outer fringe capacitance model. Added related parameters CFRDW to global, CFRD to local and POCFRD, PLCFRD, PWCFRD and PLWCFRD to binning models.
- When SWJUNASYM = 1 the original parameters for the models listed above are used for the source side and the newly added parameters are used for the drain side. When SWJUNASYM = 0 the original parameters are used for both source and drain sides and the new parameters are ignored.
- Added EF(local), EFO(global) and POEF(binning) as flicker noise frequency exponent parameters.
- Added noise parameters LINTNOI and ALPNOI to global model to increase the flexibility of the length scaling of the flicker noise.
- Some minor bug-fixes and implementation changes.

PSP103.0 Model

The PSP103 model is NOT completely backward-compatible with PSP102.3.

The main changes are:

- Global, local and binning models are unified. When SWGEO = 1 (default) the global model is used. When SWGEO = 0 the local model is selected. The binning model is invoked if SWGEO is set to 2.
- Added non-uniform doping (NUD) model. The model can be invoked on by setting SWNUD = 1 or 2. When SWNUD = 1, a separate surface potential calculation is carried out and the NUD model does not affect the CV results. This avoids non-reciprocal capacitances. When SWNUD = 2, the extra surface potential calculation is skipped and this may result in non-reciprocal capacitances.
- Added related model parameters GFACNUDO, GFACNUDL, GFACNUDLEXP, GFACNUDW, GFACNUDLW, VSBNUDO and DVSBNUDO to global, GFACNUD, VSBNUD and DVSBNUD to local and POGFACNUD, PLGFACNUD, PWGFACNUD, PLWGFACNUD, POVSBNUD and PODVSBNUD to binning models.
- Added Vth-adjustment model for CV. It can be turned on by setting SWDELVTAC = 1. Note that this requires extra computation of surface potentials. Added related model parameters FACNEFFACO, FACNEFFACL, FACNEFFACW, FACNEFFACLW, DELVTACO, DELVTACL, DELVTACLEXP, DELVTACW and DELVTACLW to global, FACNEFFAC and DELVTAC to

local and POFACNEFFAC, PLFACNEFFAC, PWFACNEFFAC, PLWFACNEFFAC, PODELVTAC, PLDELVTAC, PWDELVTAC and PLWDELVTAC to binning model.

- Added external diffusion resistances to source and drain.
- Added instance parameters NRS and NRD; added model parameters RSH to global and binning, RSE and RDE to local model.
- Modified the geometrical scaling rules of following parameters: VFB, STVFB, DPHIB, STBET, and STTHESAT.
- Modified the binning rule of BETN.
- Removed the effect of FETA from CV.
- Some minor bug-fixes and implementation changes.

Usage in HSPICE

The PSP model is Level 69 in the Synopsys MOSFET models. To use this model, specify:

```
M1 drain gate source bulk NCH w=4u l=1u
.MODEL NCH NMOS LEVEL=69
+ SWGEO = [0|1|2]
+ VERSION=num VER_CONTROL= 0|1
```

Where,

- SWGEO=0: Local model
- SWGEO=1: Default, Global model
- SWGEO=2: Binning model
- VERSION=num: Specify version number of the PSP model
- VER_CONTROL=0: (Default) Version control is off
- VER_CONTROL=1: Version control is on; the simulation will abort for non-supported version

Instance Parameter Lists

PSP 103.0 instance parameters are listed in [Table 92](#), [Table 92](#) lists the instance parameters for the PSP1000 model and the instance parameters for the PSP100 model are listed in [Table 91 on page 303](#).

Table 91 Level 69 Instance parameters, Model PSP103.0

Parameter	Unit	Default	Min.	Description
MULID0		1.0		Scaling factor of drain current, the default is 1.0.
MULU0		1.0		Low-field mobility (U0) multiplier
NRD		1	0	Number of squares of drain diffusion
NRS		1	0	Number of squares of source diffusion

Table 92 Level 69 Instance Parameters, Model PSP1000

Parameter	Unit	Default	Min.	Description
L	m	1.00e-006	1.00e-009	Drawn channel length
W	m	1.00e-006	1.00e-009	Drawn channel width
SA	m	0	-	Distance between OD-edge and poly at source side
SB	m	0	-	Distance between OD-edge and poly at drain side
ABSOURCE(AS)	m ²	1.00e-012	0	Source junction area
LSSOURCE(PS)	m	1.00e-006	0	STI-edge part of source junction perimeter
LGSOURCE(JW)	m	1.00e-006	0	Gate-edge part of source junction perimeter
ABDRAIN(AD)	m ²	1.00e-012	0	Drain junction area
LSDRAIN(PD)	m	1.00e-006	0	STI-edge part of drain junction perimeter
LGDRAIN(JW)	m	1.00e-006	0	Gate-edge part of drain junction perimeter
MULT	-	1	0	Number of devices in parallel

Table 93 Level 69 Instance Parameters, Model PSP100

Parameter	Unit	Default	Min.	Max.	Description
ABSOURCE(AS)	m ²	1.00E-012	0	-	Source junction area
LSSOURCE(PS)	m	1.00E-006	0	-	STI-edge part of source junction perimeter
LGSOURCE	m	1.00E-006	0	-	Gate-edge part of source junction perimeter
ABDRAIN(AD)	m ²	1.00E-012	0	-	Drain junction area
LSDRAIN(PD)	m	1.00E-006	0	-	STI-edge part of drain junction perimeter
LGDRAIN	m	1.00E-006	0	-	Gate-edge part of drain junction perimeter
MULT	-	1	0	-	Number of devices in parallel

Model Parameter Lists

- [Table 94](#) lists the three new added model parameters.
- [Table 95 on page 305](#) lists the parameters for a local model.
- [Table 96 on page 305](#) lists the parameters for a global model.
- [Table 97 on page 307](#) lists the parameters for a binning model.
- [Table 98 on page 307](#) lists the model parameters for the PSP1000 model.

Model PSP103.0

Shared PSP102 model parameters and newly added:

Table 94 Level 69 Model Parameters, Model PSP103.0

Parameter	Unit	Default	Min	Max	Description
SWGEO	-	1	0	2	Flag for geometrical model (0 ↔ local, 1 ↔ global, 2 ↔ binning)
SWNUD	-	0	0	2	Flag for NUD-effect (0 ↔ off)
SWDELVTAC	-	0	0	1	Flag for separate charge calculation 0 ↔ off

SWGEO=0, Local Model

Table 95 Level 69 Model Parameters, Local Model PSP103.0

Parameter	Unit	Default	Min	Max	Description
GFACNUD	-	1	0.01	1	Bodyfactor change due to NUD-effect
VSBNUD	V	0	0	-	Lower VSB-value for NUD-effect
DVSBNUD	V	1	0.1	-	VSB-range for NUD-effect
FACNEFFAC	-	1	0	-	Pre-factor for effective substrate doping in separate charge calculation when SWDELVTAC = 1
DELVTAC	V	0	-	-	Offset of Φ_B in separate charge calculation when SWDELVTAC = 1
RSE	Ohm	0	-	-	External source resistance
RDE	Ohm	0	0	-	External drain resistance

SWGEO=1, Global Model

Table 96 Level 69 Model parameters, Global Model PSP103.0

Parameter	Unit	Default	Min	Max	Description
GFACNUDO	-	1	-	1	Geometry independent part

Chapter 4: MOSFET Models: LEVELs 50 through 74

Level 69 PSP100 DFM Support Series Model

Table 96 Level 69 Model parameters, Global Model PSP103.0

Parameter	Unit	Default	Min	Max	Description
GFACNUDL	-	0	-	-	Length dependence
GFACNUDLEXP	-	1	-	-	Exponent for length dependence
GFACNUDW	-	0	-	-	Width dependence
GFACNUDLW	-	0	-	-	Area dependence
VSBNUDO	V	0	-	-	Geometry independent part
DVSBNUDO	V	1	-	-	Geometry independent part
FACNEFFACO	-	1	0	-	Geometry independent part
FACNEFFACL	-	0	-	-	Length dependence
FACNEFFACW	-	0	-	-	Width dependence
FACNEFFACLW	-	0	-	-	Area dependence
DELVTACO	V	0	-	-	Geometry independent part
DELVTACL	V	0	-	-	Length dependence
DELVTACLEXP	-	1	-	-	Exponent for length dependence
DELVTACW	V	0	-	-	Width dependence
DELVTACLW	V	0	-	-	Area dependence

SWGEO=2, Binning Model

Table 97 Level 69 Model parameters, Binning Model PSP103.0

Parameter	Unit	Default	Min	Max	Description
POGFACNUD	-	1	-	-	Geometry independent part
PLGFACNUD	-	0	-	-	Length dependence
PWGFACNUD	-	0	-	-	Width dependence
PLWGFACNUD	-	0	-	-	Area dependence
POVSBNUD	V	0	-	-	Geometry independent part
PODVSBNUD	V	1	-	-	Geometry independent part
POFACNEFFAC	-	1	-	-	Geometry independent part
PLFACNEFFAC	-	0	-	-	Length dependence
PWFACNEFFAC	-	0	-	-	Width dependence
PLWFACNEFFAC	-	0	-	-	Area dependence
PODELVTAC	V	0	-	-	Geometry independent part
PLDELVTAC	V	0	-	-	Length dependence
PWDELVTAC	V	0	-	-	Width dependence
PLWDELVTAC	V	0	-	-	Area dependence

Model PSP1000 Parameters

Table 98 Level 69 Model Parameters, Model PSP1000(Continued)

Name	Unit	Default	Min.	Max.	Description
LEVEL	-	69	-	-	Model Selector
GEOMOD	-	1	-	-	Geometrical model or Electrical model

Table 98 Level 69 Model Parameters, Model PSP1000(Continued)

Name	Unit	Default	Min.	Max.	Description
VERSION	-	100.1 (Default)/ 100	-	-	Model Version Number
TR	°C	21	-273	-	Reference temperature
Switch Parameters					
SWIGATE	-	0	0	1	Flag for gate current (0=off)
SWIMPACT	-	0	0	1	Flag for impact ionization current (0= off)
SWGIDL	-	0	0	1	Flag for GIDL/GISL current (0=off)
SWJUNCAP	-	0	0	1	Flag for JUNCAP (0=off)
Process Parameters					
VFB	V	-1	-	-	Flat-band voltage at TR
STVFB	V/K	5.00 e-004	-	-	Temperature dependence of V_{FB}
TOX	m	2.00 e-009	1.00 e-010	-	Gate oxide thickness
NSUB	m-3	5.00 e+023	1.00 e+020	1.00 e+026	Substrate doping
VNSUB	V	0	-	-	Effective doping bias-dependence parameter
NSLP	V	0.05	1.00 e-003	-	Effective doping bias-dependence parameter
DNSUB	V ⁻¹	0	0	1	Effective doping bias-dependence parameter

Table 98 Level 69 Model Parameters, Model PSP1000(Continued)

Name	Unit	Default	Min.	Max.	Description
NP	m-3	1.00 e+026	0	-	Gate poly-silicon doping
QMC	-	1	0	-	Quantum-mechanical correction
CT	-	0	0	-	Interface states factor
TOXOV	m	2.00 e-009	1.00 e-010	-	Overlap oxide thickness
NOV	m-3	5.00 e+025	1.00 e+020	1.00 e+027	Effective doping of overlap region
Lateral Gradient Factor Parameters					
F0	-	1	1.00 e-003	1	Lateral gradient factor coefficient
AF	V ⁻¹	0	0	1	Back-bias dependence of lateral gradient factor
BF	V ⁻¹	0	0	-	Surface-potential dependence of lateral gradient factor
CF	V ⁻¹	0	0	-	Drain-bias dependence of lateral gradient factor
CFB	V ⁻¹	0	0	1	Back-bias dependence of CF
Mobility Parameters					
BETN	m ² /V/s	7.00 e-002	0	-	Product of channel aspect ratio and zero- field mobility at TR
STBET	-	1	-	-	Temperature dependence of BETN
MUE	m/V	0.5	0	-	Mobility reduction coefficient at TR

Table 98 Level 69 Model Parameters, Model PSP1000(Continued)

Name	Unit	Default	Min.	Max.	Description
STMUE	-	0	-	-	Temperature dependence of MUE
THEMU	-	1.5	0	-	Mobility reduction exponent at TR
STTHEMU	-	1.5	-	-	Temperature dependence of THEMU
CS	-	0	0	-	Coulomb scattering parameter at TR
STCS	-	0	-	-	Temperature dependence of CS
XCOR	V^{-1}	0	0	-	Non-universality parameter
STXCOR	-	0	-	-	Temperature dependence of non-universality parameter
Series Resistance Parameters					
RS	ohm	30	0	-	Source/drain series resistance at TR
STRS	-	1	-	-	Temperature dependence of series resistance RS
RSB	V^{-1}	0	0	1	Back-bias dependence of series resistance RS
RSG	V^{-1}	0	0	-	Gate-bias dependence of series resistance RS
Velocity Saturation Parameters					
THESAT	V^{-1}	1	0	-	Velocity saturation parameter at TR
STTHESAT	-	1	-	-	Temperature dependence of THESAT

Table 98 Level 69 Model Parameters, Model PSP1000(Continued)

Name	Unit	Default	Min.	Max.	Description
THESATB	V^{-1}	0	0	1	Back-bias dependence of velocity saturation
THESATG	V^{-1}	0	0	-	Gate-bias dependence of velocity saturation
Saturation Voltage Parameters					
SO	-	0.98	0	0.99	Drain saturation voltage parameter
AX	-	3	2	-	Linear/ saturation transition factor
Channel Length Modulation (CLM) Parameters					
ALP	-	0.01	0	-	CLM pre-factor
ALP1	V	0	0	-	CLM enhancement factor above threshold
ALP2	V^{-1}	0	0	-	CLM enhancement factor below threshold
VP	V	0.05	1.00 e-010	-	CLM logarithmic dependence parameter
Impact Ionization (II) Parameters					
A1	-	1	0	-	Impact-ionization pre-factor
A2	V	10	0	-	Impact-ionization exponent at TR
STA2	V	0	-	-	Temperature dependence of A2
A3	-	1	0	-	Saturation-voltage dependence of II
A4	$V^{-1/2}$	0	0	-	Back-bias dependence of II

Table 98 Level 69 Model Parameters, Model PSP1000(Continued)

Name	Unit	Default	Min.	Max.	Description
Gate Current Parameters					
GC0	-	0	-10	10	Gate tunnelling energy adjustment
IGINV	A	0	0	-	Gate channel current pre-factor
IGOV	A	0	0	-	Gate overlap current pre-factor
STIG	-	2	-	-	Temperature dependence of gate current
GC2	-	0.375	0	10	Gate current slope factor
GC3	-	0.063	-2	2	Gate current curvature factor
CHIB	V	3.1	1	-	Tunnelling barrier height
Gate-Induced Drain Leakage (GIDL) Parameters					
AGIDL	A/V^3	0	0	-	GIDL pre-factor
BGIDL	V	41	0	-	GIDL probability factor at TR
STBGIDL	V/K	0	-	-	Temperature dependence of BGIDL
CGIDL	-	0	-	-	Back-bias dependence of GIDL
Charge Model Parameters					
COX	F	1.00 e-014	0	-	Oxide capacitance for intrinsic channel
CGOV	F	1.00 e-015	0	-	Oxide capacitance for gate drain/source overlap
CGBOV	F	0	0	-	Oxide capacitance for gate bulk overlap

Table 98 Level 69 Model Parameters, Model PSP1000(Continued)

Name	Unit	Default	Min.	Max.	Description
IFK	$C/V^{1/2}$	0	0	-	Inner fringe capacitance parameter
IFC	V^{-1}	0	0	-	Inner fringe capacitance parameter
IFVBI	V	1.2	1.12	-	Built-in potential
CFR	F	0	0	-	Outer fringe capacitance
Noise Model Parameters					
NFA	V^{-1}/m^4	8.00 e+022	0	-	First coefficient of flicker noise
NFB	V^{-1}/m^2	3.00 e+007	0	-	Second coefficient of flicker noise
NFC	V^{-1}	0	0	-	Third coefficient of flicker noise
FNT	-	1	0	-	Thermal noise coefficient (Only for PSP100.1 Version)
Other Parameters					
DTA	K	0	-	-	Temperature offset w.r.t. ambient circuit temperature

Source- and Drain-Bulk Junction Model Parameters

The parameters listed in [Table 99](#) apply to both PSP100 models

Table 99 Source- and Drain-bulk Junction Model Parameters

Name	Unit	Default	Min.	Max.	Description
TRJ	°C	21	-250	-	Reference temperature
IMAX	A	1000	1.00 e-012	-	Maximum current up to which forward current behaves exponentially

Table 99 Source- and Drain-bulk Junction Model Parameters

Name	Unit	Default	Min.	Max.	Description
Capacitance Parameters					
CJORBOT	F/m ²	1.00 e-003	1.00 e-012	-	Zero-bias capacitance per unit-of-area of bottom component
CJORSTI	F/m	1.00 e-009	1.00 e-018	-	Zero-bias capacitance per unit-of-length of STI-edge component
CJORGAT	F/m	1.00 e-009	1.00 e-018	-	Zero-bias capacitance per unit-of-length of gate-edge component
VBIRBOT	V	1	0.05	-	Built-in voltage at the reference temperature of bottom component
VBIRSTI	V	1	0.05	-	Built-in voltage at the reference temperature of STI-edge component
VBIRGAT	V	1	0.05	-	Built-in voltage at the reference temperature of gate-edge component
PBOT	-	0.5	0.05	0.95	Grading coefficient of bottom component
PSTI	-	0.5	0.05	0.95	Grading coefficient of STI-edge component
PGAT	-	0.5	0.05	0.95	Grading coefficient of gate-edge component
Ideal-current Parameters					
PHIGBOT	V	1.16	-	-	Zero-temperature bandgap voltage of bottom component
PHIGSTI	V	1.16	-	-	Zero-temperature bandgap voltage of sti-edge component
PHIGGAT	V	1.16	-	-	Zero-temperature bandgap voltage of gate-edge component
IDSATRBOT	A/m ²	1.00 e-012	0	-	Saturation current density at the reference temperature of bottom component

Table 99 Source- and Drain-bulk Junction Model Parameters

Name	Unit	Default	Min.	Max.	Description
IDSATRSTI	A/m	1.00 e-018	0	-	Saturation current density at the reference temperature of sti-edge component
IDSATRGAT	A/m	1.00 e-018	0	-	Saturation current density at the reference temperature of gate-edge component
Shockley-Read-Hall Parameters					
CSRHBOT	A/m ³	1.00 e+002	0	-	Shockley-Read-Hall prefactor of bottom component
CSRHSTI	A/m ²	1.00 e-004	0	-	Shockley-Read-Hall prefactor of STI-edge component
CSRHGAT	A/m ²	1.00 e-004	0	-	Shockley-Read-Hall prefactor of gate-edge component
XJUNSTI	m	1.00 e-007	1.00 e-009	-	Junction depth of STI-edge component
XJUNGAT	m	1.00 e-007	1.00 e-009	-	Junction depth of gate-edge component
CTATBOT	A/m ³	1.00 e+002	0	-	Trap-Assisted Tunneling Prefactor Of Bottom Component
CTATSTI	A/m ²	1.00 e-004	0	-	Trap-Assisted Tunneling Prefactor Of Sti-Edge Component
CTATGAT	A/m ²	1.00 e-004	0	-	Trap-Assisted Tunneling Prefactor Of Gate-Edge Component
MEFFTATBOT	-	0.25	0.01	-	Effective Mass (In Units Of M0) For Trap-Assisted Tunneling of bottom component
MEFFTATSTI	-	0.25	0.01	-	Effective Mass (In Units Of M0) For Trap-Assisted Tunneling of STI-edge component
MEFFTATGAT	-	0.25	0.01	-	Effective Mass (In Units Of M0) For Trap-Assisted Tunneling of gate-edge component

Table 99 Source- and Drain-bulk Junction Model Parameters

Name	Unit	Default	Min.	Max.	Description
Band-to-band Tunneling Parameters					
CBBTBOT	AV^{-3}	1.00 e-012	0	-	Band-to-band tunneling prefactor of bottom component
CBBTSTI	AV^{-3}_m	1.00 e-018	0	-	Band-to-band tunneling prefactor of sti-edge component
CBBTGAT	AV^{-3}_m	1.00 e-018	0	-	Band-to-band tunneling prefactor of gate-edge component
FBBTBOT	V_m^{-1}	1.00 e+009	-	-	Normalization field at the reference temperature for band-to-band tunneling of bottom component
FBBTSTI	V_m^{-1}	1.00 e+009	-	-	Normalization field at the reference temperature for band-to-band tunneling of STI-edge component
FBBTGAT	V_m^{-1}	1.00 e+009	-	-	Normalization field at the reference temperature for band-to-band tunneling of gate-edge component
STFBTBOT	K^{-1}	-1.00 e-003	-	-	Temperature scaling parameter for band-to-band tunneling of bottom component
STFBTSTI	K^{-1}	-1.00 e-003	-	-	Temperature scaling parameter for band-to-band tunneling of sti-edge component
STFBTGAT	K^{-1}	-1.00 e-003	-	-	Temperature scaling parameter for band-to-band tunneling of gate-edge component
Avalanche and Breakdown Parameters					
VBRBOT	V	10	0.1	-	Breakdown voltage of bottom component
VBRSTI	V	10	0.1	-	Breakdown voltage of sti-edge component
VBRGAT	V	10	0.1	-	Breakdown voltage of gate-edge component

Table 99 Source- and Drain-bulk Junction Model Parameters

Name	Unit	Default	Min.	Max.	Description
PBRBOT	V	4	0.1	-	Breakdown onset tuning parameter of bottom component
PBRSTI	V	4	0.1	-	Breakdown onset tuning parameter of sti-edge component
PBRGAT	V	4	0.1	-	Breakdown onset tuning parameter of gate-edge component

Output Templates: PSP Models

The following output templates (and recommended templates) are available for use with PSP models.

Table 100 PSP Output Templates

Name	Alias
Channel current	LX44, LX4 (recommended)
Diode current	LX5, LX6
Junction capacitance	LX28, LX29
l _{ii}	LX46, LX69 (recommended)
l _{gidl}	LX47, LX70 (recommended)
W _{eff} /L _{eff}	LX62, LX63
Total capacitances	LX83, LX84
Capacitance	LX82~LX87 (recommended, since they include intrinsic, overlap, and fringe capacitances), LX18~LX23

Level 73 HSPICE HiSIM-LDMOS/HiSIM-HV Model

HiSIM (Hiroshima University STARC IGFET Model) is the first complete surface-potential-based MOSFET model for circuit simulation based on the drift-diffusion theory, which was originally developed by Pao and Sah. The model has been extended for power MOSFETs by considering the resistance effect explicitly, which is named HiSIM_HV. There are two types of structures commonly used for high voltage applications. One is the asymmetrical laterally diffused structure called LDMOS and the other is originally the symmetrical structure, which we distinguish by referring to it as HVMOS. However, the asymmetrical HVMOS structure is also possible. HiSIM_HV is valid for modeling all these structure types. The most important features of LDMOS/HVMOS devices, different from the conventional MOSFET, originate from the drift region introduced to achieve the sustainability of high voltages. By varying the length and the dopant concentration of the drift region, various devices with various operating bias conditions are realized as shown in [Figure 11](#) for the LDMOS structure.

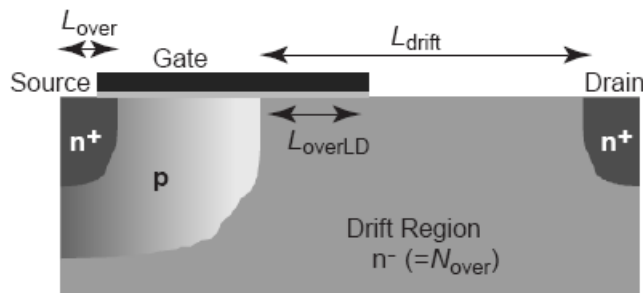


Figure 11 Schematic of a typical LDMOS structure and device parameters

A schematic of the general structures for LDMOS and HVMOS are shown in [Figure 11 on page 318](#) for the n-channel case.

Note: HSPICE currently supports Version 1.2.0 and earlier. When running this model with HSPICE Precision Parallel (HPP) the simulator automatically resets the version to the compatible one for the HPP technology and issues a warning message.

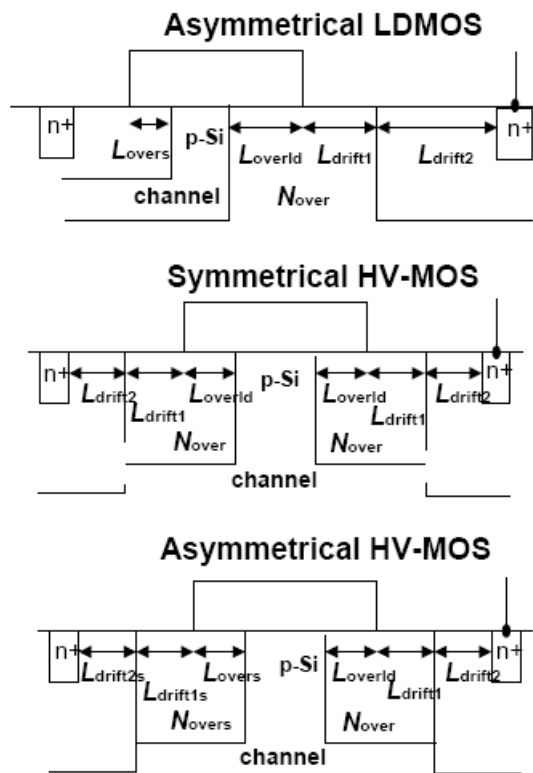


Figure 12 Device parameters in HiSIM HV

To make the structural definition easy, the flag COSYM is introduced as shown in [Figure 13 on page 320](#). COSYM=0 refers to the asymmetrical LDMOS, and all structural parameters have to be determined independently. COSYM=1 refers to symmetrical/asymmetrical HVMOS. If parameter values of the source side are given, they are activated. If they are not given, parameter values of the drain side are copied to the source side automatically.

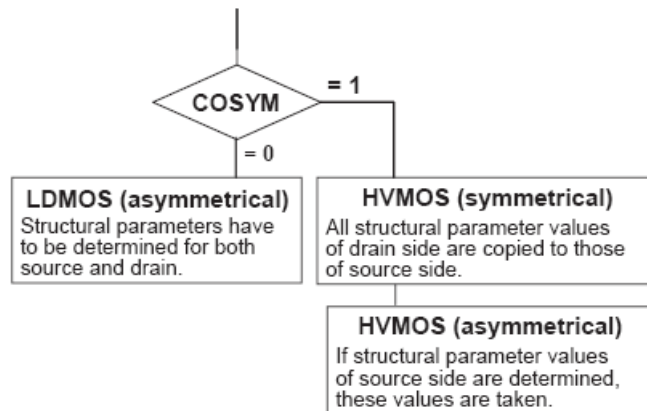


Figure 13 COSYM flag usage: =0 for LDMOS, =1 for HVMOS

[Table 101](#) summarizes the structural parameters to be determined. If the overlap length LOVER is determined instead of LOVERS, then LOVER is taken for LOVERS. Model parameters for resistances at the source side and the drain side are distinguished by RS and RD for the asymmetrical HVMOS.

Table 101 HiSIM HV 1.2.0 model parameters introduced

Flag	Structure	Source	Drain
COSYM=0	LDMOS	LOVERS RS	LOVERLD LDRIFT1S LDRIFT2S NOVERS RD
COSYM=1	Symmetrical and asymmetrical HVMOS	LOVERS LDRIFT1S LDRIFT2S NOVERS RS	LOVERLD LDRIFT1S LDRIFT2S NOVERS RD

The currently supported version, HiSIM HV 1.2.0, includes the substrate node Vsub as schematically shown in [Figure 14 on page 321](#), where model parameters DDRIFFT and NSUBSUB are newly introduced for Ddrift and Nsubsub, respectively. The node inclusion is done by selecting Flag COSUBNODE=0 as the 5th node.

For details and usage, and current parameters, contact the Synopsys support team.

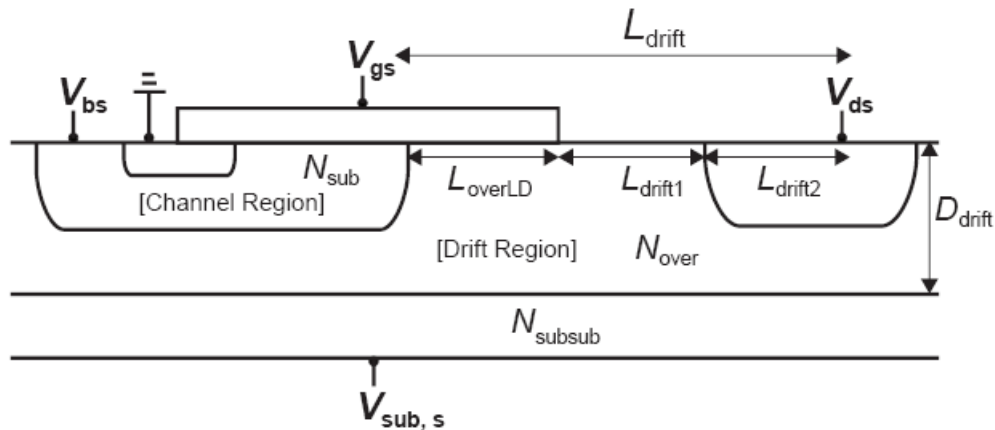


Figure 14 Schematic of a LDMOS with the substrate node $V_{sub,s}$

Note: HiSIM-LDMOS source code, and all copyrights, trade secrets or other intellectual property rights in and to the source code in its entirety, is owned by Hiroshima University and STARC.

This section discusses the following topics

- [General Syntax for the HiSIM-LDMOS-1.2.0 Level 73 Model](#)
- [Template Output for Parameters in HiSIM-HVMOS v.1.2.0 and Higher](#)
- [Previous Versions of the HiSIM LDMOS-HVMOS Model](#)

General Syntax for the HiSIM-LDMOS-1.2.0 Level 73 Model

The following lists and describes the HiSIM-LDMOS/HVMOS-1.2.0 Level 73 general parameters.

```
Mxxx nd ng ns [nb] mname [L=val] [W=val] [M=val]
+ [AD=val] [AS=val] [PD=val] [PS=val]
+ [NRS=val] [NRD=val] [XGW=val] [XGL=val]
+ [NF=val] [NGCON=val] [RBPB=val] [RBPB=val]
+ [RBPS=val] [SA=val] [SB=val] [SD=val] [DTEMP=val]
+ [NSUBCDFM=val] [SUBLD1=val] [SUBLD2=val]
+ [LDRIFT1=val] [LDRIFT2=val] [LDSRIFT1S=val] [LDRIFT2S=val]
+ [LOVER=val] [LOVERLD=val] [LOVERS=val]
+ [COSELFHEAT=val] [CONSUBNODE=val]
```

Notes for Mxxx Card

- nd, ng, ns, nb: drain, gate, source, and bulk node, respectively
- nsub: substrate node
- nth: thermal node
- The square brackets "[]" indicate optional content which may be omitted.
- If 5 nodes are specified and COSUBNODE=0, the 5th node is nth.
 - If 5 nodes are specified and COSUBNODE=1, the 5th node is nsub.
 - If 6 nodes are specified, the 5th node is nsub and the 6th node is nth.
- COSUBNODE is a new instance parameter and at the same time is recognized as a model parameter for the specification and the recognition of the node order.
- Originally COSELFHEAT was treated as a model parameter as other flags. It is additionally recognized as an instance parameter.
- See [Table 103 on page 325](#) for model options and descriptions.

General Model Parameters

Table 102 HiSIM-LDMOS/HVMOS Level 73 Instance Parameters

Parameter	Default	Description
L	2.0 μm	Gate length (L_{gate})
W	5.0 μm	Gate width (W_{gate})
Diode		
AD	0.0	Area of drain junction
AS	0.0	Area of source junction
PD	0.0	Perimeter of drain junction
PS	0.0	Perimeter of source junction
Source/Drain Resistance		
NRS	1.0	Number of source squares
NRD	1.0	Number of drain squares
Gate Resistance		
XGW	0.0	Distance from the gate contact to the channel edge
XGL	0.0	Offset of the gate length
NF	1.0	Number of gate fingers
M	1.0	Multiplication factor
NGCON	1.0	Number of gate contacts
Substrate Network		
RBPB	Model parameter value	Substrate Resistance Network
RBPD	Model parameter value	Substrate Resistance Network
RBPS	Model parameter value	Substrate Resistance Network

Table 102 HiSIM-LDMOS/HVMOS Level 73 Instance Parameters (Continued)

Parameter	Default	Description
RBDB		Obsolete
RBSB		Obsolete
Lenth of Diffusion		
SA	0.0	Length of diffusion between gate and STI
SB	0.0	Length of diffusion between gate and STI
SD	0.0	Length of diffusion between gate and gate
Temperature		
DTEMP	0.0	Device temperature change
Design for Manufacturability		
NSUBCDFM	0.0	Substrate impurity concentration
Substrate Current		
SUBLD1	Model parameter value	Substrate current induced in L_{drift}
SUBLD2	Model parameter value	Substrate current induced in L_{drift}
Resistance		
LDRIFT1	0.0	Length of lightly doped drift region
LDRIFT2	$1.0\mu m$	Length of heavily doped drift region
LDRIFT1S	0.0	Length of lightly doped drift region in source side
LDRIFT2S	$1.0\mu m$	Length of heavily doped drift region in source side

Table 102 HiSIM-LDMOS/HVMOS Level 73 Instance Parameters (Continued)

Parameter	Default	Description
Overlap		
LOVER	0.0	Length of overlap region in source side for LDMOS
LOVERLD	Model parameter value	Length of overlap region in drain side
LOVERS	Model parameter value	Length of overlap region in source side for HVMOS
COSELFHEAT	Model parameter value	Flag to switch on the self-heating effect
COSUBNODE	Model parameter value	Flag for selection of the 5th node

Control Option Flags for LDMOS-HVMOS 1.2.0 Model

The following control flags are operational for the LDMOS-HVMOS 1.2.0 model

Table 103 HiSIM LDMOS-HVMOS Level 73 Control Options

Description	Flag
1 Selects asymmetrical (LDMOS) or HVMOS structure	<ul style="list-style-type: none"> ▪ COSYM = 0: asymmetrical LDMOS (default) ▪ COSYM = 1: symmetrical and asymmetrical HVMOS
2 Include contact resistances Rs and Rd	<ul style="list-style-type: none"> ▪ CORSRD= 0: no ▪ CORSRD = 1 & $RS/RD \neq 0$: yes, as internal resistance nodes ▪ CORSD=2 & $RS/RD \neq 0$: yes, analytical description ▪ CORSD=3 & $RS/RD \neq 0$: yes, analytical description (default) ▪ CORSRD = -1 & $RS/RD \neq 0$: yes, as external resistance nodes
3 Adds overlap charges/capacitances to intrinsic ones	<ul style="list-style-type: none"> ▪ COADOV = 0: no ▪ COADOV = 1: yes (default)

Table 103 HiSIM LDMOS-HVMOS Level 73 Control Options

	Description	Flag
4	Selects bias-dependent overlap capacitance model at drain side	<ul style="list-style-type: none"> ▪ COOVLP = 0: constant overlap capacitance ▪ COOVLP = 1: yes (default) including constant values as option
5	Selects bias-dependent overlap capacitance model at source side	<ul style="list-style-type: none"> ▪ COOVLP = 0: constant overlap capacitance ▪ COOVLP = 1: yes (default) including constant values as option
6	Considers self-heating effect	<ul style="list-style-type: none"> ▪ COSELFHEAT = 0: no (default) ▪ COSELFHEAT = 1: yes
7	Calculates substrate current I_{sub}	<ul style="list-style-type: none"> ▪ COISUB = 0: no (default) ▪ COISUB = 1: yes
8	Calculates gate current I_{gate}	<ul style="list-style-type: none"> ▪ COIGS = 0: no (default) ▪ COIGS = 1: yes
9	Calculates GIDL current I_{GIDL}	<ul style="list-style-type: none"> ▪ COGIDL = 0: no (default) ▪ COGIDL = 1: yes
10	Calculates STI leakage current $I_{ds,STI}$	<ul style="list-style-type: none"> ▪ COISTI = 0: no (default) ▪ COISTI = 1: yes
11	Invokes non-quasi-static	<ul style="list-style-type: none"> ▪ CONQS = 0: no (default) ▪ CONQS = 1: yes
12	Includes gate-contact resistance	<ul style="list-style-type: none"> ▪ CORG = 0: no (default) ▪ CORG = 1: yes
13	Invokes substrate resistance network	<ul style="list-style-type: none"> ▪ CORBNET = 0: no (default) ▪ CORBNET = 1: yes
14	Calculates 1/f noise	<ul style="list-style-type: none"> ▪ COFLICK = 0: no (default) ▪ COFLICK = 1: yes
15	Calculates thermal noise	<ul style="list-style-type: none"> ▪ COTHRML = 0: no (default) ▪ COTHRML = 1: yes
16	Calculates induced-gate and cross-correlation noise	<ul style="list-style-type: none"> ▪ COIGN = 0 & COTHRML = 0: no (default) ▪ COIGN = 1 & COTHRML = 1: yes
17	Uses previous $_S$ for the iteration	<ul style="list-style-type: none"> ▪ COPPRV = 0: no ▪ COPPRV = 1: yes (default)

Table 103 HiSIM LDMOS-HVMOS Level 73 Control Options

Description	Flag
18 Considers parameter variations for DFM support	<ul style="list-style-type: none"> ▪ CODFM = 0: no (default) ▪ CODFM = 1: yes
19 Uses previous I_{ds} is used for calculating source/drain resistance effect (RS_{and} or $RD \neq 0$): This flag is deactivated.	<ul style="list-style-type: none"> ▪ COIPRV = 0: no ▪ COIPRV = 1: yes (default)
20 Selects temperature dependence of models	<div style="display: flex; justify-content: space-around; margin-bottom: 5px;"> $R_{d0,temp}$ $R_{dvd,temp}$ V_{max} N_{invd} </div> <ul style="list-style-type: none"> ▪ COTEMP=0 T T0 T0 T0 (default and backward compatible) ▪ COTEMP=1 T0 T0 T0 T0 ▪ COTEMP=2 T T T T ▪ COTEMP=3 T T T0 T0 <p>where T includes the temperature increase by the self-heating effect and T0 omits it.</p>
21 Selects the 5th node	<ul style="list-style-type: none"> ▪ COSUBNODE = 0: the 5th node is the thermal node. ▪ COSUBNODE = 1: the 5th node is the Vsub node.
22 Selects the Ldrift	<ul style="list-style-type: none"> ▪ COLDRIFT = 0: Ldrift includes LOVER (default & backward compatible) ▪ COLDRIFT = 1: without LOVER.

For full information regarding the HiSIM 1.2.0 version of this model, see *HiSIM_HV 1.1.0 User's Manual*, available through Hiroshima University and STARC.

Template Output for Parameters in HiSIM-HVMOS v.1.2.0 and Higher

HSPICE supports parameter template output beginning with HiSIM-HV1.2.0 model (version=1.20, level=73).

Table 104 Output Templates for HiSIM LDMOS/HDMOS Model -1.2.0

Name	Alias	Description
L	LX291	Channel Length (L)

Chapter 4: MOSFET Models: LEVELs 50 through 74

Level 73 HSPICE HiSIM-LDMOS/HiSIM-HV Model

Table 104 Output Templates for HiSIM LDMOD/HDMOS Model -1.2.0

Name	Alias	Description
W	LX292	Channel Width (W)
AD	LX293	Area of the drain diode (AD)
AS	LX294	Area of the source diode (AS)
ICVDS	LX295	Initial condition for the drain-source voltage (VDS)
ICVGS	LX296	Initial condition for the gate-source voltage (VGS)
ICVBS	LX297	Initial condition for the bulk-source voltage (VBS)
PD	LX298	Drain diode periphery (PD)
PS	LX299	Source diode periphery (PS)
RSS	LX301	Source resistance (squares) (RSS)
WEFF	LX302	Effective channel width
LEFF	LX303	Effective channel length
CAPFG	LX304	Fringing capacitance
VTH	LX305	Threshold voltage (bias dependent)
VDSAT	LX306	Saturation voltage (VDSAT)
GDEFF	LX307	Effective drain conductance (1/RDeff)
GSEFF	LX308	Effective source conductance (1/RSeff)
VDBEFF	LX309	Effective drain bulk voltage.
BETAEFF	LX310	BETA effective
GAMMAEFF	LX311	GAMMA effective
VFBEFF	LX312	VFB effective
COVLGS	LX313	Gate-source overlap and fringing capacitances

Table 104 Output Templates for HiSIM LDMOD/HDMOS Model -1.2.0

Name	Alias	Description
COVLGD	LX314	Gate-drain overlap and fringing capacitances
COVLGB	LX315	Gate-bulk overlap capacitances
VBD	LX316	Bulk-drain voltage
VBS	LX317	Bulk-source voltage (VBS)
VGS	LX318	Gate-source voltage (VGS)
VDS	LX319	Drain-source voltage (VDS)
CDO	LX320	Channel current (IDS)
CBSO	LX321	DC source-bulk diode current (CBSO)
CBDO	LX322	DC drain-bulk diode current (CBDO)
GMO	LX323	DC MOSFET gate transconductance (GMO)
GDSO	LX324	DC drain-source conductance (GDSO)
GMBSO	LX325	DC substrate transconductance (GMBSO)
GBDO	LX326	Conductance of the drain diode (GBDO)
GBSO	LX327	Conductance of the source diode (GBSO)
QB	LX328	Total bulk (body) charge (QB)—Meyer and Charge Conservation
CQB	LX329	Bulk (body) charge current (CQB)—Meyer and Charge Conservation
QG	LX330	Total Gate charge (QG)—Meyer and Charge Conservation
CQG	LX331	Gate charge current (CQG)—Meyer and Charge Conservation
QD	LX332	Channel charge (QD)
CQD	LX333	Channel charge current (CQD)
CGGBO	LX334	Intrinsic gate capacitance

Chapter 4: MOSFET Models: LEVELs 50 through 74

Level 73 HSPICE HiSIM-LDMOS/HiSIM-HV Model

Table 104 Output Templates for HiSIM LDMOD/HDMOS Model -1.2.0

Name	Alias	Description
CGDBO	LX335	Intrinsic gate-to-drain capacitance
CGSBO	LX336	Intrinsic gate-to-source capacitance
CBGBO	LX337	Intrinsic bulk-to-gate capacitance
CBDBO	LX338	Intrinsic bulk-to-drain capacitance
CBSBO	LX339	CBSBO = $-dQ_b/dV_s$
QBD	LX340	Drain-bulk charge (QBD)
QBS	LX341	Source-bulk charge (QBS)
CAP_BS	LX342	Bias dependent bulk-source capacitance
CAP_BD	LX343	Bias dependent bulk-drain capacitance
CDGBO	LX344	Intrinsic drain-to-gate capacitance
CDDBO	LX345	Intrinsic drain capacitance
CDSBO	LX346	CDSBO = $-dQ_d/dV_s$, Drain-to-source capacitance
SFT	LX347	Value of the temperature node
weffcv	LX348	Effective channel width for CV
leffcv	LX349	Effective channel length for CV
igso	LX350	Gate-to-Source Current
igdo	LX351	Gate-to-Drain Current
igbo	LX352	Gate-to-Substrate Current
igcso	LX353	Source Partition of I_{gc}
igcdo	LX354	Drain Partition of I_{gc}
iimi	LX355	Impact ionization current

Table 104 Output Templates for HiSIM LDMOD/HDMOS Model -1.2.0

Name	Alias	Description
igidlo	LX356	Gate-induced drain leakage current
igislo	LX357	Gate-induced source leakage current
igdt	LX358	Gate Dielectric Tunneling Current ($I_g = I_{gs} + I_{gd} + I_{gcs} + I_{gcd} + I_{gb}$)
vgse	LX359	Effective Gate-to-Source Voltage
rdv	LX360	Asymmetric and Bias-Dependent Source Resistance
rsv	LX361	Asymmetric and Bias-Dependent Drain Resistance
cap_bsz	LX362	Zero voltage bias bulk-source capacitance
cap_bdz	LX363	Zero voltage bias bulk-drain capacitance
CGGBM	LX364	Total gate capacitance (including intrinsic), and overlap and fringing components
CGDBM	LX365	Total gate-to-drain capacitance (including intrinsic), and overlap and fringing components
CGSBM	LX366	Total gate-to-source capacitance (including intrinsic), and overlap and fringing components
CDDBM	LX367	Total drain capacitance (including intrinsic), overlap and fringing components, and junction capacitance
CDSBM	LX368	Total drain-to-source capacitance
CDGBM	LX369	Total drain-to-gate capacitance (including intrinsic), and overlap and fringing components
CBGBM	LX370	Total bulk-to-gate (floating body-to-gate) capacitance, including intrinsic and overlap components
CBDBM	LX371	Total bulk-to-drain capacitance (including intrinsic) and junction capacitance
CBSBM	LX372	Total bulk-to-source capacitance (including intrinsic), and junction capacitance

Table 104 Output Templates for HiSIM LDMOD/HDMOS Model -1.2.0

Name	Alias	Description
Ueff	LX373	Effective mobility at the specified analysis temperature
VGB	LX374	Gate to bulk voltage
VDG	LX375	Drain to gate voltage
mult	LX376	Prints value of multiplier (M) for a specified MOSFET
sa	LX377	sa for STI or LOD-induced mechanical stress-effects
sb	LX378	sb for STI or LOD-induced mechanical stress-effects
sd	LX379	sd for STI or LOD-induced mechanical stress-effects
hsmhv_nf	LX380	nf for STI or LOD-induced mechanical stress-effects

Previous Versions of the HiSIM LDMOS-HVMOS Model

The following sections discuss updates to the model as they occurred:

- [HiSIM-LDMOS-100 Updates](#)
- [Extension to LDMOS and HVMOS](#)
- [HiSIM-HV Version 1.0.1 and 1.0.2](#)

HiSIM-LDMOS-100 Updates

The following changes were made in the HiSIM-LDMOS 100 model as reported in the SC1 through SC3 release notes provided by Hiroshima University/ STARC.

- SC1:
 - Self-heating effect Temperature node is handled as an internal node.
 - The model parameter RD26 was deleted, and the smoothing parameter was fixed to a constant value.
 - Qover Overlap Capacitance: The model description of Qover was changed from external bias to internal bias.

- The charge-partitioning scheme with model parameters QOVRAT1 and QOVRAT2 was deactivated.
- The new model parameter RD26 was introduced to fit transition characteristics at depletion and/or inversion.
- SC2:
 - The self-heating effect (COSELFHEAT=1) was stabilized for HSPICE. The temperature node can be treated either as an external or internal node.
 - The NF dependability in the drift resistance model was removed for to improve accuracy.
- SC3:
 - The self-heating effect became applicable for AC analysis
 - Introduction of drift-length (LDRIFT) dependence of the drift resistance.
 - Introduction of model parameters RDTEMP1 and RDTEMP2 for temperature dependent drift resistance.

Extension to LDMOS and HVMOS

To facilitate the structural definition, the COSYM flag was introduced with HiSIM-HV1.0.0. **COSYM=0** refers to the asymmetrical LDMOS, and all drain-side and source-side parameters of the drain side are copied to the source side. **COSYM=1** refers to symmetrical HVMOS, and all parameters have to be determined independently. HiSIM-LDMOS/HV considers the length of the drift region L_{drift} , the overlap length L_{over} , and the impurity concentration of the drift region N_{over} explicitly. In the HVMOS case, the parameter values for the drain side have to be determined, and are copied to the source side automatically. If parameters are not determined, default values are taken.

HiSIM-HV Version 1.0.1 and 1.0.2

HSPICE supports HiSIM-HV 1.0.1, version 1.01 and 1.0.2, version 1.02. To address the need for accurate modeling of high-voltage MOSFETs, Hiroshima University and STARC developed the HiSIM-HVMOS model as an extension to the IGFET model. The HV model focuses on symmetrical structure while the HiSIM-LDMOS model is used for asymmetrical structures. According to the *HiSIM_HV User Guide*: the most important advantage of the surface-potential-based modeling is the unified description of device characteristics for all bias conditions. The physical reliability of the drift-diffusion theory has been proved

by 2-D device simulations with channel lengths even down to below $0.1\text{ }\mu\text{m}$. To obtain analytical solutions for describing device performances, the charge sheet approximation of the inversion layer with zero thickness has been introduced. Together with the gradual-channel approximation all device characteristics are then described analytically by the channel-surface potentials at the source side ($S0$) and at the drain side (SL) (see [Figure 15 on page 334](#)).

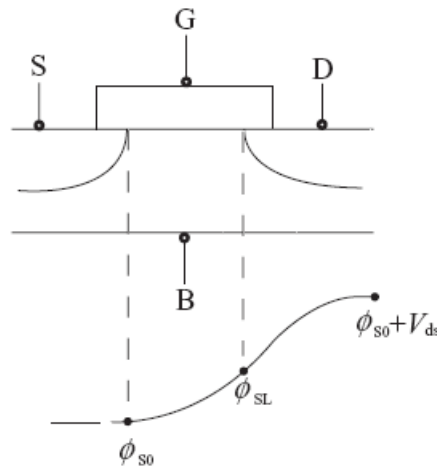


Figure 15 Schematic of the surface potential distribution in the channel

These surface potentials are functions of applied voltages on the four terminals: the gate voltage V_g , the drain voltage V_d , the bulk voltage V_b and the reference potential of the source V_s . The resistance in the contact region causing potential drops also affects the surface potential values. Since the surface potentials are implicit functions of the applied voltages, model-internal iteration procedures are introduced only for calculating ϕ_{S0} , and ϕ_{SL} is calculated in addition to the global iteration of the circuit simulator.

The potential $\phi_s(\Delta L)$ is calculated with ϕ_{S0} , ϕ_{SL} , and V_{ds} together with a fitting parameter.

The most important features of LDMOS/HVMOS devices, different from the conventional MOSFET, originate from the drift region introduced to achieve the sustainability of high voltages. By varying the length as well as the dopant concentration of the drift region, various devices with various operating bias conditions are realized. In many cases, the drift region acts as the resistance for the current flow and also induces additional charge, which causes the

especially unique features of the LDMOS capacitances. Thus, accurate modeling of the drift region is the main task of HiSIM-LDMOS/HV.

For the LDMOS/HVMOS devices the iterative solution is only one possible to model the specific features of this device accurately, because the resistance effect in the drift region is dependent on the bias condition as well as the detailed geometrical LDMOS/HVMOS structure. The basic modeling method is taken over from the HiSIM2 model for advanced MOSFETs, and additional equations for capturing the drift-region effects are included. Since the overlap length is relatively long for LDMOS/HVMOS, accurate surface potential calculation for the overlap region as a function of applied voltages is also necessary for accurate prediction of the high-voltage MOS capacitances.

Level 74 MOS Model 20 Model

MOS Model 20 (MM20) is a compact MOSFET model developed by NXP, intended for analog circuit simulation in high-voltage MOS technologies. MOS Model 20 describes the electrical behavior of the region under the thin gate oxide of a high-voltage MOS device, similar to a Lateral Double-diffused MOS (LDMOS) device or an extended-drain MOSFET. It combines the MOSFET-operation of the channel region with that of the drift region under the thin gate oxide in a high-voltage MOS device. As such, MOS Model 20 is aimed as a successor of the combination of MOS Model 9 (MM9) for the channel region in series with MOS Model 31 (MM31) for the drift region under the thin gate oxide, in macro models of various high-voltage MOS devices. MOS Model 20 has especially been developed to improve the convergence behavior during simulation, by having the voltage at the transition from the channel region to the drift region calculated inside the model itself.

Please check following URL from NXP for original MOS Model 20 release and documentation.

http://www.nxp.com/models/hv_models/model20/

The following sections discuss these topics:

- [General Syntax for MOS Model 20 Model](#)
- [MOS Model 20 Instance and Model Parameter Lists](#)
- [Addition to HSPICE MOS Model 20 Implementation](#)

General Syntax for MOS Model 20 Model

Mxxxx drain gate source bulk *mname* W=*val* Wd=*val* ...

MOS Model 20 Instance and Model Parameter Lists

Table 105 Instance Parameters for MOS Model 20

Name	Unit	Default	Description
W	m	2E-5	Drawn width of the channel region
WD	m	2E-5	Drawn width of the drift region
MULT		1	Number of devices in parallel

MM 20 Geometrical Model Parameters

Table 106 Geometrical Model Parameters

Name	Unit	Default	Description
LEVEL		74	HSPICE model level as 74 for MOS Model 20
VERSION		2002.2	VERSION 2002.2 is the default version number to define NXP model level 2002
GEOMOD		1	GEOMOD is used as a switch between geometrical model and electrical model, 0 for geometrical model and 1 for electrical model
WVAR	m	0	Width offset of the channel region
WDVAR	m	0	Width offset of the drift region
TREF	deg.C	25	Reference temperature
VFB	V	-1	Flatband voltage of the channel region, at reference temperature
STVFB	V/K	0	Temperature scaling coefficient for VFB

Table 106 Geometrical Model Parameters (Continued)

Name	Unit	Default	Description
VFBD	V	-0.1	Flatband voltage of the drift region, at reference temperature
STVFBD	V/K	0	Temperature scaling coefficient for the flatband voltage of the drift region
KOR	$V^{(1/2)}$	1.6	Body factor of the channel region of an infinitely wide transistor
SWKO		0	Width scaling coefficient for KO
KODR	$V^{(1/2)}$	1	Body factor of the drift region of an infinitely wide transistor
SWKOD		0	Width scaling coefficient for the body factor of the drift region
PHIB	V	0.86	Surface potential at the onset of strong inversion in the channel region, at reference temperature
STPHIB	V/K	-0.0012	Temperature scaling coefficient for PHIB
PHIBD	V	0.78	Surface potential at the onset of strong inversion in the drift region, at reference temperature
STPHIBD	V/K	-0.0012	Temperature scaling coefficient for PHIBD
BETW	A/V^2	7.00E-05	Gain factor of a channel region of 1 μm wide, at reference temperature
ETABET		1.6	Temperature scaling exponent for BET
BETACCW	A/V^2	7.00E-05	Gain factor of drift region of 1 μm wide, at reference temperature
ETABETACC		1.5	Temperature scaling exponent for BETACC
RDW	Ohm	4000	On-resistance of a drift region of 1 μm wide, at reference temperature
ETARD		1.5	Temperature scaling exponent for RD

Chapter 4: MOSFET Models: LEVELs 50 through 74

Level 74 MOS Model 20 Model

Table 106 Geometrical Model Parameters (Continued)

Name	Unit	Default	Description
LAMD		0.2	Quotient of the depletion layer thickness to the effective thickness of the drift region at $V_{SB} = 0$ V
THE1R	V^{-1}	0.09	Mobility reduction coefficient of infinitely wide transistor, due to vertical strong-inversion field in a channel region
SWTHE1		0	Width scaling coefficient for THE1
THE1ACC	V^{-1}	0.02	Mobility reduction coefficient in the drift region due to the vertical electrical field caused by accumulation
THE2R	$V^{(-1/2)}$	0.03	Mobility reduction coefficient for $V_{SB} > 0$ of an infinitely wide transistor, due to vertical depletion field in channel region
SWTHE2		0	Width scaling coefficient for THE2
THE3R	V^{-1}	0.4	Mobility reduction coefficient in a channel region of an infinitely wide transistor due to velocity saturation
ETATHE3		1	Temperature scaling exponent for THE3
SWTHE3		0	Width scaling coefficient for THE3
MEXP		2	Smoothing factor for transition from linear to saturation regime
THE3DR	V^{-1}	0	Mobility reduction coefficient in a channel region of an infinitely wide transistor due to velocity saturation
ETATHE3D		1	Temperature scaling exponent for THE3D
SWTHE3D		0	Width scaling coefficient for THE3D
MEXPD		2	Smoothing factor for transition from linear to quasi-saturation regime
ALP		0.002	Factor for channel length modulation
VP	V	0.05	Characteristic voltage of channel length modulation
SDIBL	$V^{(-1/2)}$	0.001	Factor for drain-induced barrier lowering

Table 106 Geometrical Model Parameters (Continued)

Name	Unit	Default	Description
MSDIBL		3	Exponent for the drain-induced barrier lowering dependence on the backgate bias
MO	V	0	Parameter for the (short-channel) sub-threshold slope
SSF	$V^{(-1/2)}$	1E-12	Factor for static feedback
A1CHR		15	Factor of channel weak avalanche current, at reference temperature
STA1CH	K^{-1}	0	Temperature scaling coefficient for A1CH
SWA1CH		0	Width scaling coefficient for A1CH
A2CH	V	73	Exponent of weak avalanche current, related to channel
A3CH		0.8	Factor of the internal drain-source voltage, above which channel weak avalanche occurs
A1DRR		15	Factor of drift weak avalanche current, at reference temperature
STA1DR	K^{-1}	0	Temperature scaling coefficient for A1DR
SWA1DR		0	Width scaling coefficient for A1DR
A2DR	V	73	Exponent of weak avalanche current, related to drift
A3DR		0.8	Factor of the internal drain-source voltage, above which drift weak avalanche occurs
COXW	F	7.5E-16	Oxide capacitance for an intrinsic channel region of 1 um wide
COXDW	F	7.5E-16	Oxide capacitance for an intrinsic drift region of 1 um wide
CGDOW	F	0	Gate-to-drain overlap capacitance for a drift region of 1 um wide
CGSOW	F	0	Gate-to-source overlap capacitance for a drift region of 1 um wide

Chapter 4: MOSFET Models: LEVELs 50 through 74

Level 74 MOS Model 20 Model

Table 106 Geometrical Model Parameters (Continued)

Name	Unit	Default	Description
NT	J	1.645E-20	Coefficient of thermal noise, at reference temperature
NFAW	$V^{-1}m^{-4}$	1.4E+25	First coefficient of flicker noise for a channel region of 1 um wide
NFBW	$V^{-1}m^{-2}$	2.00E+08	Second coefficient of flicker noise for a channel region of 1 um wide
NFCW	V^{-1}	0	Third coefficient of flicker noise for a channel region of 1 um wide
TOX	m	3.80E-08	Thickness of the oxide above the channel region
DTA	K	0	Temperature offset to the ambient temperature
SHMOD		0	SHMOD is used as a switch of self-heating effect, 0 for off and 1 for on
RTH	K/W	300	Thermal resistance
CTH	J/K	3.00E-09	Thermal capacitance
ATH		0	Temperature coefficient of the thermal resistance
JUNCAPMOD		0	JUNCAPMOD as a switch of juncap200.2 model effective, 0 for off and 1 for on

MM20 Electrical Model Parameters*Table 107 Electrical Model Parameters*

Name	Unit	Default	Description
VERSION		2002.2	VERSION 2002.2 is the default version number to define NXP model level 2002
GEOMOD		1	GEOMOD is used as a switch between geometrical model and electrical model, 0 for geometrical model and 1 for electrical model
TYPE		1	TYPE=1 NMOS;TYPE=-1 PMOS

Table 107 Electrical Model Parameters (Continued)

Name	Unit	Default	Description
TREF	deg.C	25	Reference temperature
VFB	V	-1	Flatband voltage of the channel region, at reference temperature
STVFB	V/K	0	Temperature scaling coefficient for VFB
VFBD	V	-0.1	Flatband voltage of the drift region, at reference temperature
STVFBD	V/K	0	Temperature scaling coefficient for the flatband voltage of the drift region
KO	$V^{(1/2)}$	1.6	Body factor of the channel region
KOD	$V^{(1/2)}$	1	Body factor of the drift region
PHIB	V	0.86	Surface potential at the onset of strong inversion in the channel region, at reference temperature
STPHIB	V/K	-0.0012	Temperature scaling coefficient for PHIB
PHIBD	V	0.78	Surface potential at the onset of strong inversion in the drift region, at reference temperature
STPHIBD	V/K	-0.0012	Temperature scaling coefficient for PHIBD
BET	A/V^2	7.00E-05	Gain factor of a channel region, at reference temperature
ETABET		1.6	Temperature scaling exponent for BET
BETACC	A/V^2	7.00E-05	Gain factor of drift region of 1 um wide, at reference temperature
ETABETACC		1.5	Temperature scaling exponent for BETACC
RD	Ohm	200	On-resistance of a drift region, at reference temperature
ETARD		1.5	Temperature scaling exponent for RD

Chapter 4: MOSFET Models: LEVELs 50 through 74

Level 74 MOS Model 20 Model

Table 107 Electrical Model Parameters (Continued)

Name	Unit	Default	Description
LAMD		0.2	Quotient of the depletion layer thickness to the effective thickness of the drift region at $V_{SB} = 0$ V
THE1	V^{-1}	0.09	Mobility reduction coefficient due to vertical strong-inversion field in a channel region
THE1ACC	V^{-1}	0.02	Mobility reduction coefficient in the drift region due to the vertical electrical field caused by accumulation
THE2	$V^{(-1/2)}$	0.03	Mobility reduction coefficient for $V_{SB} > 0$, due to vertical depletion field in channel region
THE3	V^{-1}	0.4	Mobility reduction coefficient in a channel region due to velocity saturation
ETATHE3		1	Temperature scaling exponent for THE3
MEXP		2	Smoothing factor for transition from linear to saturation regime
THE3D	V^{-1}	0	Mobility reduction coefficient in a channel region due to velocity saturation
ETATHE3D		1	Temperature scaling exponent for THE3D
MEXPD		2	Smoothing factor for transition from linear to quasi-saturation regime
ALP		0.002	Factor for channel length modulation
VP	V	0.05	Characteristic voltage of channel length modulation
SDIBL	$V^{(-1/2)}$	0.001	Factor for drain-induced barrier lowering
MSDIBL		3	Exponent for the drain-induced barrier lowering dependence on the backgate bias
MO	V	0	Parameter for the (short-channel) sub-threshold slope
SSF	$V^{(-1/2)}$	1E-12	Factor for static feedback

Table 107 Electrical Model Parameters (Continued)

Name	Unit	Default	Description
A1CH		15	Factor of channel weak avalanche current, at reference temperature
STA1CH	K ⁻¹	0	Temperature scaling coefficient for A1CH
A2CH	V	73	Exponent of weak avalanche current, related to channel
A3CH		0.8	Factor of the internal drain-source voltage, above which channel weak avalanche occurs
A1DR		15	Factor of drift weak avalanche current, at reference temperature
STA1DR	K ⁻¹	0	Temperature scaling coefficient for A1DR
A2DR	V	73	Exponent of weak avalanche current, related to drift
A3DR		0.8	Factor of the internal drain-source voltage, above which drift weak avalanche occurs
COX	F	15E-15	Oxide capacitance for an intrinsic channel region
COXD	F	15E-15	Oxide capacitance for an intrinsic drift region
CGDO	F	0	Gate-to-drain overlap capacitance for a drift region
CGSO	F	0	Gate-to-source overlap capacitance for a drift region
NT	J	1.645E-20	Coefficient of thermal noise, at reference temperature
NFA	V ^{-1m⁻⁴}	7.0E+23	First coefficient of flicker noise for a channel region
NFB	V ^{-1m⁻²}	1.0E+07	Second coefficient of flicker noise for a channel region
NFC	V ⁻¹	0	Third coefficient of flicker noise for a channel region
TOX	m	3.80E-08	Thickness of the oxide above the channel region
DTA	K	0	Temperature offset to the ambient temperature

Table 107 Electrical Model Parameters (Continued)

Name	Unit	Default	Description
SHMOD		0	SHMOD is used as a switch of self-heating effect, 0 for off and 1 for on
RTH	K/W	300	Thermal resistance
CTH	J/K	3.00E-09	Thermal capacitance
ATH		0	Temperature coefficient of the thermal resistance
JUNCAPMOD		0	JUNCAPMOD as a switch of juncap200.2 model effective, 0 for off and 1 for on

Addition to HSPICE MOS Model 20 Implementation

Juncap 200.2 is supported in HSPICE MOS Model 20 as an alternative to the MOSFET junction diode model. You can use model parameter, JUNCAPMOD=1, to invoke Juncap200.2.

MOSFET Models (BSIM): Levels 13 through 39

Lists and describes three of the earliest BSIM-type MOSFET models supported by HSPICE.

This chapter describes three of the earliest Berkeley Short Channel IGFET (BSIM) type MOSFET device models that HSPICE supports:

- [LEVEL 13 BSIM Model](#)
- [LEVEL 28 Modified BSIM Model](#)
- [LEVEL 39 BSIM2 Model](#)

These models are all based on models developed by the University of California at Berkeley. You can find documentation on BSIM3 and BSIM4 at this website:

<http://www.eigroup.org/cmc/cmos/default.htm>

For descriptions of the newest BSIM models that Synopsys supports, see [Chapter 6, MOSFET Models \(BSIM\): Levels 47 through 72](#).

LEVEL 13 BSIM Model

Level 13 is based on the SPICE 2G.6 BSIM model, which models the device physics of small-geometry MOS transistors. To invoke the subthreshold region, set the `N0` model parameter (low field weak inversion gate drive coefficient) to less than 200. Level 13 provides three MOSFET models:

- Wire (resistor) model, compatible with the SPICE BSIM interconnect model for polysilicon and metal layers. Simulates resistors and capacitors with interconnects.
- Capacitor model. Simulates only capacitors with interconnects.
- Diffusion model, compatible with SPICE BSIM diffusion models.

To set Level 13 model parameters, either:

- Enter model parameters as numbers (as in SPICE), or
- Assign the model parameters.

If you convert from SPICE to the Synopsys models, use the S keyletter for SPICE BSIM, or M for the Synopsys model. (see [IDS and VGS Curves for PMOS and NMOS on page 368](#)).

BSIM Model Features

- Vertical field dependence of the carrier mobility
- Carrier velocity saturation
- Drain-induced barrier lowering
- Depletion charge sharing by source and drain
- Non-uniform doping profile for ion-implanted devices
- Channel length modulation
- Subthreshold conduction
- Geometric dependence of electrical parameters

LEVEL 13 Model Parameters

MOSFET Level 13 uses the generic MOSFET model parameters described in [Chapter 2, Common MOSFET Model Parameters](#). It also uses the parameters described in this section, which apply only to MOSFET Level 13.

Note: When you read parameter names, be careful about the difference in appearance between the upper case letter O, the lower case letter o, and the number zero (0).

For reference purposes only, simulation obtains the following default values from a medium size n-channel MOSFET device.

To specify Level 13 parameters, use NMOS conventions, even for PMOS (for example, $\text{ETA0}=0.02$, not $\text{ETA0}=-0.02$).

Table 108 Transistor Parameters, MOSFET Level 13

Name (Alias)	Units	Default	Description
LEVEL		1	MOSFET model level selector. 13 is the BSIM model
CGBOM, (CGBO)	F/m	2.0e-10	Gate-to-bulk parasitic capacitance (F/m of length)
CGDOM, (CGDO)	F/m	1.5e-9	Gate-to-drain parasitic capacitance (F/m of width)
CGSOM, (CGSO)	F/m	1.5e-9	Gate-to-source parasitic capacitance (F/m of width)
DL0	μm	0.0	Difference between drawn poly and electrical
DW0	μm	0.0	Difference between drawn diffusion and electrical
DUM1		0.0	Dummy (not used)
DUM2		0.0	Dummy (not used)
ETA0		0.0	Linear vds threshold coefficient
LETA	mm	0.0	Length sensitivity
WETA	μm	0.0	Width sensitivity
K1	$\text{V}^{1/2}$	0.5	Root- v_{sb} threshold coefficient
LK1	$\text{V}^{1/2} \cdot \mu\text{m}$	0.0	Length sensitivity
WK1	$\text{V}^{1/2} \cdot \mu\text{m}$	0.0	Width sensitivity
K2		0.0	Linear v_{sb} threshold coefficient

Table 108 Transistor Parameters, MOSFET Level 13

Name (Alias)	Units	Default	Description
LK2	μm	0.0	Length sensitivity
WK2	μm	0.0	Width sensitivity
MUS	$\text{cm}^2/(\text{V} \cdot \text{s})$	600	High drain field mobility
LMS (LMUS)	$\mu\text{m} \cdot \text{cm}^2/(\text{V} \cdot \text{s})$	0.0	Length sensitivity
WMS (WMUS)	$\mu\text{m} \cdot \text{cm}^2/(\text{V} \cdot \text{s})$	0.0	Width sensitivity
MUZ	$\text{cm}^2/(\text{V} \cdot \text{s})$	600	Low drain field first order mobility
LMUZ	$\mu\text{m} \cdot \text{cm}^2/(\text{V} \cdot \text{s})$	0.0	Length sensitivity
WMUZ	$\mu\text{m} \cdot \text{cm}^2/(\text{V} \cdot \text{s})$	0.0	Width sensitivity
N0		0.5	Low field weak inversion gate drive coefficient (a value of 200 for N0 disables the weak inversion calculation)
LN0		0.0	Length sensitivity
WN0		0.0	Width sensitivity
NB0		0.0	Vsb reduction to the low field weak inversion gate drive coefficient
LNB		0.0	Length sensitivity
WNB		0.0	Width sensitivity
ND0		0.0	Vds reduction to the low field weak inversion gate drive coefficient
LND		0.0	Length sensitivity
WND		0.0	Width sensitivity

Table 108 Transistor Parameters, MOSFET Level 13

Name (Alias)	Units	Default	Description
PHI0	V	0.7	Two times the Fermi potential
LPHI	V· μm	0.0	Length sensitivity
WPHI	V· μm	0.0	Width sensitivity
TREF	°C	25.0	Reference temperature of model (local override of TNOM)
TOXM, (TOX)	μm , (m)	0.02	Gate oxide thickness (simulation interprets TOXM or TOX >1 as Angstroms)
U00	1/V	0.0	Gate field mobility reduction factor
LU0	$\mu\text{m}/\text{V}$	0.0	Length sensitivity
WU0	$\mu\text{m}/\text{V}$	0.0	Width sensitivity
U1	$\mu\text{m}/\text{V}$	0.0	Drain field mobility reduction factor
LU1	$\mu\text{m}^2/\text{V}$	0.0	Length sensitivity
WU1	$\mu\text{m}^2/\text{V}$	0.0	Width sensitivity
VDDM	V	50	Critical voltage for the high-drain field mobility reduction
VFB0 (VFB)	V	-0.3	Flatband voltage
LVFB	V· μm	0.0	Length sensitivity
WVFB	V· μm	0.0	Width sensitivity
X2E	1/V	0.0	Vsb correction to the linear vds threshold coefficient
LX2E	$\mu\text{m}/\text{V}$	0.0	Length sensitivity

Table 108 Transistor Parameters, MOSFET Level 13

Name (Alias)	Units	Default	Description
WX2E	$\mu\text{m}/\text{V}$	0.0	Width sensitivity
X2M (X2MZ)	$\text{cm}^2/(\text{V}^2 \cdot \text{s})$	0.0	Vsb correction to the low field first-order mobility
LX2M (LX2MZ)	$\mu\text{m} \cdot \text{cm}^2/(\text{V}^2 \cdot \text{s})$	0.0	Length sensitivity
WX2M (WX2MZ)	$\mu\text{m} \cdot \text{cm}^2/(\text{V}^2 \cdot \text{s})$	0.0	Width sensitivity
X2MS	$\text{cm}^2/(\text{V}^2 \cdot \text{s})$	0.0	Vbs reduction to the high-drain field mobility
LX2MS	$\mu\text{m} \cdot \text{cm}^2/(\text{V}^2 \cdot \text{s})$	0.0	Length sensitivity
WX2MS	$\mu\text{m} \cdot \text{cm}^2/(\text{V}^2 \cdot \text{s})$	0.0	Width sensitivity
X2U0	$1/\text{V}^2$	0.0	Vsb reduction to the GATE field mobility reduction factor
LX2U0	$\mu\text{m}/\text{V}^2$	0.0	Length sensitivity
WX2U0	$\mu\text{m}/\text{V}^2$	0.0	Width sensitivity
X2U1	$\mu\text{m}/\text{V}^2$	0.0	Vsb reduction to the DRAIN field mobility reduction factor
LX2U1	$\mu\text{m}^2/\text{V}^2$	0.0	Length sensitivity
WX2U1	$\mu\text{m}^2/\text{V}^2$	0.0	Width sensitivity
X3E	$1/\text{V}$	0.0	Vds correction to the linear vds threshold coefficient
LX3E	$\mu\text{m}/\text{V}$	0.0	Length sensitivity
WX3E	$\mu\text{m}/\text{V}$	0.0	Width sensitivity
X3MS	$\text{cm}^2/(\text{V}^2 \cdot \text{s})$	5.0	Vds reduction to the high-drain field mobility

Table 108 Transistor Parameters, MOSFET Level 13

Name (Alias)	Units	Default	Description
LX3MS	$\mu\text{m} \cdot \text{cm}^2/(\text{V}^2 \cdot \text{s})$	0.0	Length sensitivity
WX3MS	$\mu\text{m} \cdot \text{cm}^2/(\text{V}^2 \cdot \text{s})$	0.0	Width sensitivity
X3U1	$\mu\text{m}/\text{V}^2$	0.0	Vds reduction to the drain field mobility reduction factor
LX3U1	$\mu\text{m}^2/\text{V}^2$	0.0	Length sensitivity
WX3U1	$\mu\text{m}^2/\text{V}^2$	0.0	Width sensitivity
XPART		1.0	Selects a gate capacitance charge-sharing coefficient

Table 109 Diffusion Layer Parameters, MOSFET Level 13

Name (Alias)	Units	Default	Description
CJW, (CJSW)	F/m	0.0	Zero-bias bulk junction sidewall capacitance
CJM, (CJ)	F/m ²	4.5e-5	Zero-bias bulk junction bottom capacitance
DS	m	0.0	Average size variation due to the side etching or the mask compensation (not used)
IJS, (JS)	A/m ²	0	Bulk junction saturation current
JSW	A/m	0.0	Sidewall bulk junction saturation current
MJ0, (MJ)		0.5	Bulk junction bottom grading coefficient
MJW, (MJSW)		0.33	Bulk junction sidewall grading coefficient
PJ, (PB)	V	0.8	Bulk junction bottom potential
PJW, (PHP)	V	0.8	Bulk junction sidewall potential

Table 109 Diffusion Layer Parameters, MOSFET Level 13

Name (Alias)	Units	Default	Description
RSHM, (RSH)	ohm/sq	0.0	Sheet resistance/square
WDF	m	0.0	Default width of the layer (not used)

The wire model includes poly and metal layer process parameters.

Table 110 Temperature Parameters

Name (Alias)	Units	Default	Description
BEX		-1.5	Temperature exponent for the MUZ and MUS mobility parameters.
FEX		0.0	Temperature exponent for the U1 mobility reduction factor.
TCV	V/°K	0.0	Flat-band voltage temperature coefficient.
TREF	°C	25	Temperature at which simulation extracts parameters. This parameter defaults to the TNOM option, which defaults to 25 °C.

Sensitivity Factors of Model Parameters

To denote the L (channel length) and W (channel width) sensitivity factors of a basic electrical parameter in a transistor, add L and W characters at the start of the name. For example, V_{FB0} sensitivity factors are LV_{FB} and WV_{FB} . If $A0$ is a basic parameter, then LA and WA are the corresponding L and W sensitivity factors of this parameter. Do not use the $SCALM$ option to scale LA and WA .

The Level 13 MOSFET model uses the following equation to obtain this parameter value:

$$A = A0 + LA \cdot \left(\frac{1}{L_{eff}} - \frac{1}{LREF_{eff}} \right) + WA \cdot \left(\frac{1}{W_{eff}} - \frac{1}{WREF_{eff}} \right)$$

Specify LA and WA in units of microns times the units of $A0$.

The left side of the equation represents the effective model parameter value after you adjust the device size. All effective model parameters are in lower case and start with the *z* character, followed by the parameter name.

Example

$$VFB0 = -0.350v, LVFB = -0.1v\mu$$

$$WVFB = 0.08v \cdot \mu, Leff = 1 \cdot 10^{-6}m = 1\mu$$

$$Weff = 2 \cdot 10^{-6}m = 2\mu, LREff = 2 \cdot 10^{-6}m = 2\mu$$

$$WREff = 1 \cdot 10^{-5}m = 10\mu$$

$$zvfb = VFB0 + LVFB \cdot \left(\frac{1}{Leff} - \frac{1}{LREff} \right) + WVFB \cdot \left(\frac{1}{Weff} - \frac{1}{WREff} \right)$$

$$zvfb = -0.35v + -0.1v \cdot \mu \cdot \left(\frac{1}{1\mu} - \frac{1}{2\mu} \right) + 0.08v \cdot \mu \cdot \left(\frac{1}{2\mu} - \frac{1}{10\mu} \right)$$

$$zvfb = -0.35v - 0.05v + 0.032v, zvfb = -0.368v$$

.MODEL VERSION Changes to BSIM Models

You can use the `VERSION` parameter in the `.MODEL` statement to move Level 13 BSIM and Level 39 BSIM2 models between versions. Using the `VERSION` parameter in a Level 13 `.MODEL` statement results in the following changes to the BSIM model.

Model Version	Effect of VERSION on BSIM model
9007B	Introduced the LEVEL 13 BSIM model: no changes
9007D	Removed the K2 limit
92A	Changed the TOX parameter default from 1000 Å to 200 Å
92B	Added the K2LIM parameter, which specifies the K2 limit
93A	Introduced the gds constraints
93A.02	Introduced the VERSION parameter

Model Version	Effect of VERSION on BSIM model
95.1	Fixed the nonprinting TREF and incorrect GMBS problems
96.1	Changed the flatband voltage temperature adjustment

LEVEL 13 Equations

This section lists the Level 13 model equations.

Effective Channel Length and Width

The effective channel length and width for Level 13 depends on the specified model parameters.

If you specify $DL0$, then:

$$Leff = Lscaled \cdot LMLT - DL0 \Rightarrow 1e-6$$

$$LREFeff = LREFscaled \cdot LMLT - DL0 \Rightarrow 1e-6$$

Otherwise, if you specify XL or LD :

$$Leff = Lscaled \cdot LMLT + XLscaled - 2 \Rightarrow LDscaled$$

$$LREFeff = LREFscaled \cdot LMLT + XLscaled - 2 \Rightarrow LDscaled$$

If you specify $DW0$, then:

$$Weff = Wscaled \cdot WMLT - DW0 \Rightarrow 1e-6$$

$$WREFeff = WREFscaled \cdot WMLT - DW0 \Rightarrow 1e-6$$

Otherwise, if you specify XW or WD , then:

$$Weff = Wscaled \cdot WMLT + XWscaled - 2 \Rightarrow WDscaled$$

$$WREFeff = WREFscaled \cdot WMLT + XWscaled - 2 \Rightarrow WDscaled$$

IDS Equations

Process-oriented model parameters model the device characteristics. Simulation maps these parameters into model parameters at a specific bias voltage. The ids equations are as follows:

Cutoff Region, $v_{gs} \leq v_{th}$

$i_{ds} = 0$ (see subthreshold current)

On Region, $v_{gs} > v_{th}$

For the $v_{ds} < v_{dsat}$ triode region:

$$i_{ds} = \frac{\beta}{1 + x_{u1} \cdot v_{ds}} \cdot \left[(v_{gs} - v_{th}) \cdot v_{ds} - \frac{body}{2} v_{ds}^2 \right]$$

For the $v_{ds} > v_{dsat}$ saturation region:

$$i_{ds} = \frac{\beta}{2 \cdot body \cdot arg} \cdot (v_{gs} - v_{th})^2$$

The following equations calculate values used in the preceding equation:

$$\beta = u_{eff} \cdot COX \cdot \frac{W_{eff}}{L_{eff}}$$

$$u_{eff} = \frac{u_o}{1 + x_{u0} \cdot (v_{gs} - v_{th})}$$

$$x_{u0} = z_{u0} - z_{x2u0} \cdot v_{sb}$$

Simulation uses quadratic interpolation, through three data points to calculate the u_o carrier mobility.

$$u_o|_{v_{ds}=0} = MUZ - z_{x2mz} \cdot v_{sb}$$

$$u_o|_{v_{ds}=V_{DDM}} = z_{mus} - z_{x2ms} \cdot v_{sb}$$

Simulation also calculates the sensitivity of u_o to v_{ds} at $v_{ds}=V_{DDM}$, which is z_{x3ms} .

The following equation calculates the body factor:

$$body = 1 + \frac{g \cdot z_{k1}}{2 \cdot (z_{phi} + v_{sb})^{1/2}}$$

The following equation calculates the g value used in the preceding equation:

$$g = 1 - \frac{1}{1.744 + 0.8364 \cdot (z_{phi} + v_{sb})}$$

The following equation calculates the arg term in the saturation region:

$$arg = \frac{1}{2} \cdot [1 + v_c + (1 + 2 \cdot v_c)^{1/2}]$$

The following equations calculate values used in the preceding equation:

$$v_c = \frac{xu1 \cdot (v_{gs} - v_{th})}{body}$$

$$xu1 = zu1 - zx2u1 \Rightarrow sb + zx3u1 \cdot (v_{ds} - VDDM), \text{UPDATE}=2$$

$$xu1 = \frac{zu1 - zx2u1 \Rightarrow sb + zx3u1 \cdot (v_{ds} - VDDM)}{Leff}, \text{UPDATE}=0, 1$$

Threshold Voltage

You can express the threshold voltage as:

$$v_{th} = zvfb + zphi + gamma \cdot (zphi + vsb)^{1/2} - xeta \Rightarrow ds$$

The following equations calculate values used in the preceding equation:

$$gamma = zk1 - zk2 \Rightarrow (zphi + vsb)^{1/2}$$

$$xeta = zeta - zx2e \Rightarrow sb + zx3e \cdot (v_{ds} - VDDM), \text{UPDATE}=0, 2$$

$$xeta = zeta + zx2e \cdot (zphi + vsb) + zx3e \cdot (v_{ds} - VDDM), \text{UPDATE}=1$$

Saturation Voltage (vdsat)

The following equation calculates the saturation voltage in the BSIM Level 13 model:

$$v_{dsat} = \frac{v_{gs} - v_{th}}{body \cdot arg^{1/2}}$$

ids Subthreshold Current

Simulation calculates the isub subthreshold current if zn0 is less than 200:

$$isub = \frac{Ilim \cdot Iexp}{Ilim + Iexp}$$

The following equations calculate values used in the preceding equation:

$$Iexp = \beta_o \cdot vt^2 \cdot e^{1.8} \cdot e^{\frac{v_{gs} - v_{th}}{xn \cdot vt}} \cdot \left(1 - e^{-\frac{v_{ds}}{vt}}\right)$$

$$Ilim = 4.5 \cdot \beta_o \cdot vt^2, \beta_o = uo \cdot COX \cdot \frac{W_{eff}}{Leff}$$

$$x_n = z_{n0} - z_{nb} \cdot v_{sb} + z_{nd} \cdot v_{ds}$$

Simulation also adds the *isub* current to the *ids* current in the strong inversion.

Resistors and Capacitors Generated with Interconnects

Refer to the wire model table (resistor element) for the model parameters that you used. For an example, see [IDS and VGS Curves for PMOS and NMOS on page 368](#).

Resistances

$$r = RSH \cdot \frac{Leff}{Weff}$$

Capacitances

$$c = COX \cdot Leff \cdot Weff + 2 \cdot CAPSW \cdot (Leff + Weff)$$

Temperature Effect

$$MUZ(t) = MUZ \cdot \left(\frac{t}{tnom} \right)^{BEX}, \text{ UPDATE}=0, 1$$

$$z_{mus}(t) = z_{mus} \cdot \left(\frac{t}{tnom} \right)^{BEX}, \text{ UPDATE}=0, 1$$

$$uo(t) = uo \cdot \left(\frac{t}{tnom} \right)^{BEX}, \text{ UPDATE}=2$$

$$xu1(t) = xu1 \cdot \left(\frac{t}{tnom} \right)^{FEX}$$

$$z_{vfb}(t) = z_{vfb} - \Delta t \cdot TCV$$

The following equation calculates the Δt value used in the preceding equations:

$$\Delta t = t - tnom$$

Charge-Based Capacitance Model

The Level 13 capacitance model conserves charge and has nonreciprocal attributes. Using charge as the state variable guarantees charge conservation.

To obtain the total stored charge in each of the gate, bulk, and channel regions, integrate the distributed charge densities/area of the active region.

The `XPART` 40/60 model parameter or 0/100 in the saturation region, partitions the channel charge into drain and source components. This partitioning smoothly changes to 50/50 in the triode region.

- `XPART=0` selects 40/60 drain/source charge-partitioning in the saturation region. That is, 40% of the channel charge in the saturation region is at the drain, and 60% is at the source.
- `XPART=1` selects 0/100 for drain/source charge-partitioning in the saturation region. That is, 100% of the channel charge in the saturation region is at the source; there is no drain charge.
- `XPART=0.5` selects 50/50 partitioning. Half of the channel charge in the saturation region is at the source, and half is at the drain.

Define:

$$v_{tho} = z_{vfb} + z_{phi} + z_{k1} \cdot (z_{phi} + v_{sb})^{1/2}$$

$$cap = COX \cdot Leff \cdot Weff, v_{pof} = \frac{v_{gs} - v_{tho}}{body}$$

$$argx = \frac{body \cdot v_{ds}}{12 \cdot (v_{gs} - v_{tho} - 0.5 \cdot body \cdot v_{ds})}$$

$$\text{If } (v_{gs} - v_{tho} - 0.5 \cdot body \cdot v_{ds}) \leq 1e-8 \text{ then: } argx = \frac{1}{6}$$

$$argy = \frac{(v_{gs} - v_{tho})^2 - 0.75 \cdot body \cdot (v_{gs} - v_{tho}) \cdot v_{ds} + 0.15 \cdot body^2 \cdot v_{ds}^2}{6 \cdot (v_{gs} - v_{tho} - 0.5 \cdot body \cdot v_{ds})^3}$$

$$\text{If } (v_{gs} - v_{tho} - 0.5 \cdot body \cdot v_{ds}) \leq 1e-8 \text{ then: } argy = \frac{4}{15}$$

Regions Charge Expressions

Accumulation Region, $v_{gs} \geq v_{tho}$, $v_{gs} \geq z_{vfb} - v_{sb}$

$$Q_g = cap \cdot (v_{gs} - z_{vfb} + v_{sb})$$

$$Q_b = -q_g, Q_s = 0, Q_d = 0$$

Subthreshold Region, $v_{gs} \leq v_{tho}$, $v_{gs} > v_{fb} - v_{sb}$

$$Q_g = \frac{cap \cdot z_{k1}}{2} \cdot \left\{ [(z_{k1})^2 + 4(v_{gs} - z_{vfb} + v_{sb})]^{1/2} - z_{k1} \right\}$$

$$Q_b = -q_g, Q_s = 0$$

50/50 Channel-Charge Partitioning for Drain and Source, $XPART=0.5$; Triode Region, $v_{gs} > v_{tho}$, $v_{ds} \leq v_{pof}$

$$Q_g = cap \cdot (v_{gs} - z_{vfb} - z_{phi} - 0.5 \Rightarrow v_{ds} + v_{ds} \cdot \arg x)$$

$$Q_b = cap \cdot [-v_{tho} + z_{vfb} + z_{phi} + (1 - body) \cdot (0.5 - \arg x) \cdot v_{ds}]$$

$$Q_d = -0.5 \Rightarrow q_g + q_b, Q_s = Q_d$$

Saturation Region, $v_{gs} > v_{tho}$, $v_{ds} > v_{pof}$

$$Q_g = cap \cdot \left(v_{gs} - z_{vfb} - z_{phi} - \frac{v_{gs} - v_{tho}}{3 \cdot body} \right)$$

$$Q_b = cap \cdot \left[z_{vfb} + z_{phi} - v_{tho} + (1 - body) \cdot \frac{(v_{gs} - v_{tho})}{3 \cdot body} \right]$$

$$Q_d = -\frac{cap}{3} \Rightarrow (v_{gs} - v_{tho}), Q_s = Q_d$$

40/60 Channel-Charge Partitioning for Drain and Source, $XPART=0$; Triode Region, $v_{gs} > v_{tho}$, $v_{ds} \leq v_{pof}$

$$Q_g = cap \cdot (v_{gs} - z_{vfb} - z_{phi} - 0.5 \Rightarrow v_{ds} + \arg x \cdot v_{ds})$$

$$Q_b = cap \cdot [-v_{tho} + z_{vfb} + z_{phi} + (1 - body) \cdot (0.5 - \arg x) \cdot v_{ds}]$$

$$Q_d = -(cap \cdot [0.5 \cdot (v_{gs} - v_{tho} - body \Rightarrow v_{ds}) + body \cdot \arg x \cdot v_{ds}])$$

$$Q_s = -(Q_g + Q_b + Q_d)$$

Saturation Region, $v_{gs} > v_{tho}$, $v_{ds} > v_{pof}$

$$Q_g = cap \cdot \left(v_{gs} - z_{vfb} - z_{phi} - \frac{v_{gs} - v_{tho}}{3 \cdot body} \right)$$

$$Q_b = cap \cdot \left[z_{vfb} + z_{phi} - v_{tho} + (1 - body) \cdot \frac{(v_{gs} - v_{tho})}{3 \cdot body} \right]$$

$$Q_d = -\frac{4 \cdot cap}{15} \cdot (v_{gs} - v_{tho}), Q_s = \frac{3}{2} \cdot Q_d$$

0/100 Channel-Charge Partitioning for Drain and Source, $XPART=1$; Triode Region, $v_{gs} > v_{tho}$, $v_{ds} \leq v_{pof}$

$$Q_g = cap \cdot (v_{gs} - z_{vfb} - z_{phi} - 0.5 \cdot P_{vds} + v_{ds} \cdot \arg x)$$

$$Q_b = cap \cdot [-v_{tho} + z_{vfb} + z_{phi} + (1 - body) \cdot (0.5 - \arg x) \cdot v_{ds}]$$

$$Q_d = -(cap \cdot [0.5 \cdot (v_{gs} - v_{tho}) - body \cdot P_{vds} \cdot P(0.75 - 1.5 \cdot P_{argx})])$$

$$Q_s = -(Q_g + Q_b + Q_d)$$

Saturation Region, $v_{gs} > v_{tho}$, $v_{ds} > v_{pof}$

$$Q_g = cap \cdot \left(v_{gs} - z_{vfb} - z_{phi} - \frac{v_{gs} - v_{tho}}{3 \cdot body} \right)$$

$$Q_b = cap \cdot \left[z_{vfb} + z_{phi} - v_{tho} + (1 - body) \cdot \frac{(v_{gs} - v_{tho})}{3 \cdot body} \right]$$

$$Q_d = 0, Q_s = -Q_g - Q_b$$

Preventing Negative Output Conductance

The Level 13 model internally protects against conditions that might cause convergence problems, due to negative output conductance. The constraints imposed are:

$$ND \geq 0$$

$$MUS \geq MUZ + X3MS + VDD(M/2)$$

This model imposes these constraints after adjusting the length and width and setting the V_{BS} dependence. This feature loses some accuracy in the saturation region, particularly at high V_{gs} .

You might need to qualify BSIM1 models again, if the following occur:

- Devices exhibit self-heating during characterization, which causes declining I_{ds} at high V_{ds} . This does not occur if the device characterization measurement sweeps V_{ds} .
- Extraction produces parameters that result in negative conductance.
- This model attempts voltage simulation outside the characterized range of the device.

Calculations Using LEVEL 13 Equations

To verify the equations, start some simple simulation and analysis tests, and check the results with a hand calculator. Check the threshold, vdsat, and ids for a very simple model with many parameters set to zero:

- series resistance, RSH=0.
- Turn off diode current, JS=JSW=IS=0.
- Turn off the Level 13 subthreshold current, n0=200.
- Set the geometry parameters to zero so $L_{\text{eff}}=L=1\mu$, $W_{\text{eff}}=W=1\mu$.

This test returns the following TOX value:

$$cox = \frac{2.00000e - 3F}{m^2}$$

The test is at vbs=-0.35 so that phi-vbs=1.0. The netlist for this test is located in directory \$<installdir>/demo/hspice/mos/t1.sp.

```
$ t1
.option ingold=2 numdgt=6
vd d 0 5
vg g 0 5
vb b 0 -0.35
m1 d g 0 b nch w=10u L=1u
.dc vd 4 5 1
.print ids=lx4(m1) vth=lv9(m1) vdsat=lv10(m1)
.model nch nmos LEVEL=13
+ vfb0=-0.4 lvfb=0 wvfb=0
+ phi0=0.65 lphi=0 wphi=0
+ k1=0.5 lk1=0 wk1=0
+ k2=0 lk2=0 wk2=0
+ eta0=1e-3 leta=0 weta=0
+ muz=600 mus=700 x3ms=10
+ xl=0 ld=0 xw=0 wd=0
+ u00=0 lu0=0 wu0=0
+ u1=0 lu1=0 wu1=0
+ tox=172.657
+ acm=2 rsh=0 js=0 jsw=0 is=0 n0=200
.end
```

Simulation Results

```
ids          vth          vdsat
1.09907e-02  7.45000e-01  3.69000e+00
```

Calculations at $v_{gs}=v_{ds}=5$, $v_{bs}=-0.35$

$$\phi - v_{bs} = 1$$

$$v_{th} = -0.4 + 0.65 + (0.5 \cdot 1) - (ETA \cdot v_{ds}) = 0.75 - (0.001 \cdot v_{ds}) = 0.745$$

$$g = 1 - \frac{1}{(1.744 + 0.8364 \cdot 1)} = 0.612463$$

$$body = 1 + \frac{g \cdot 0.5}{(2 \cdot 1)} = 1 + 0.25 \cdot g = 1.153116$$

$$vc = 0 \text{ arg} = 1$$

$$v_{dsat} = \frac{(v_{gs} - v_{th})}{body \cdot \sqrt{arg}} = \frac{(5 - 0.745)}{body} = 3.69000$$

Calculations at $v_{ds}=V_{DDM}$ (default $V_{DDM}=5$), mobility= $\mu_s=700$

$$i_{ds} = c_{ox} \cdot \left(\frac{W_{eff}}{L_{eff}} \right) \cdot 700 \cdot \frac{(v_{gs} - v_{th})^2}{(2 \cdot body \cdot arg)}$$

$$i_{ds} = \left(\frac{10 \cdot 700 \cdot 4.255^2}{2 \cdot 1.15311 \cdot 1} \right) \cdot c_{ox} = 54953.36 \cdot c_{ox}$$

$$i_{ds} = 1.09907e-2$$

These calculations agree with the above simulation results.

Compatibility Notes

Model Parameter Naming

The following names are HSPICE-specific: U00, DL0, DW0, PHI0, ETA0, NB0, and ND0. A zero was added to the SPICE names to avoid conflicts with other standard parameter names. For example, you cannot use U0 because it is an alias for UB, the mobility parameter in many other levels. You cannot use DL, because it is an alias for XL, a geometry parameter available in all levels.

You can use DL0 and DW0 with this model, but you should use XL, LD, XW, and WD instead (noting the difference in units).

Watch the units of TOX. It is safest to enter a number greater than one, which simulation always interprets as Angstroms.

To avoid negative gds:

1. Set X3U1, LX3U1, and WX3U1 to zero.
2. Check that
 $zx3ms \geq 0$, where $zx3ms = X3MS$ with L , W adjustment
3. Check that
 $zmuz + VDDM \cdot zx3ms < zmus$

SPICE/Synopsys Model Parameter Differences

[Table 111](#) compares the UCB BSIM1 and the Synopsys Level 13 model parameters. Units in this table are in brackets. This comparison uses the model parameter name only if it differs from the SPICE name. The model specifies parameter units only if they differ from SPICE units. These aliases are in parentheses. Some parameter aliases match the SPICE names.

An asterisk (*) in front of a UCB SPICE name denotes an incompatibility between the parameter name in the Synopsys Level 13 MOSFET device model and the UCB SPICE name (that is, the parameter alias does not match or the units are different).

Even if the parameter name in this model is not the same as in SPICE, the corresponding L and W sensitivity parameter names might not differ. [Table 111](#) lists the L and W sensitivity parameters only for the few cases where the parameters are different.

*Table 111 Comparing Synopsys Model Parameters & UCB
SPICE 2/3*

UC Berkeley SPICE 2, 3	Synopsys Device Model
VFB [V]	VFB0 (VFB)
PHI [V]	PHI0
K1 [$V^{1/2}$]	same
K2	same
* ETA	ETA0
MUZ [$cm^2/V \cdot s$]	same

Chapter 5: MOSFET Models (BSIM): Levels 13 through 39
LEVEL 13 BSIM Model

*Table 111 Comparing Synopsys Model Parameters & UCB
SPICE 2/3*

UC Berkeley SPICE 2, 3	Synopsys Device Model
* DL [μm]	DL0
* DW [μm]	DW0
* U0 [$1/\text{V}$]	U00
* U1 [μ/V]	same
X2MZ [$\text{cm}^2/\text{V}^2 \cdot \text{s}$]	X2M (X2MZ)
LX2MZ [$\mu\text{m} \cdot \text{cm}^2/\text{V}^2 \cdot \text{s}$]	X2M (LX2MZ)
WX2MZ [$\mu\text{m} \cdot \text{cm}^2/\text{V}^2 \cdot \text{s}$]	WX2M (WX2MZ)
X2E [$1/\text{V}$]	same
X3E [$1/\text{V}$]	same
X2U0 [$1/\text{V}^2$]	same
X2U1 [$\mu\text{m}/\text{V}^2$]	same
MUS [$\text{cm}^2/\text{V} \cdot \text{s}$]	same
LMUS [$\mu\text{m} \cdot \text{cm}^2/\text{V} \cdot \text{s}$]	LMS (LMUS)
WMUS [$\mu\text{m} \cdot \text{cm}^2/\text{V} \cdot \text{s}$]	WMS (WMUS)
X2MS [$\text{cm}^2/\text{V}^2 \cdot \text{s}$]	same
X3MS [$\text{cm}^2/\text{V}^2 \cdot \text{s}$]	same
X3U1 [$\mu\text{m}/\text{V}^2$]	same
* TOX [μm]	TOXM[μ] (TOX[m])
* TEMP [$\times\text{C}$]	TREF

Table 111 Comparing Synopsys Model Parameters & UCB
SPICE 2/3

UC Berkeley SPICE 2, 3	Synopsys Device Model
* VDD [V]	VDDM
CGDO [F/m]	CGDOM (CGDO)
CGSO [F/m]	CGSOM (CGSO)
CGBO [F/m]	CGBOM (CGBO)
XPART	same
N0	same
* NB	NB0
* ND	ND0
RSH [ohm/sq]	RSHM (RSH)
JS [A/m ²]	IJS (JS)
PB [V]	PJ (PB)
MJ	MJ0 (MJ)
* PBSW [V]	PJW (PHP)
MJSW	MJW (MJSW)
CJ [F/m ²]	CJM (CJ)
CJSW [F/m]	CCJW (CJSW)
* WDF [m]	—
* DELL [m]	—

In UCB SPICE, you must specify all BSIM model parameters. The Synopsys model provides default values for the parameters.

Parasitics

ACM >0 invokes parasitic diode models. ACM=0 (default) is SPICE style.

Temperature Compensation

The default `TNOM` model reference temperature is 25°C, unless you use `.OPTION SPICE` to set the default `TNOM` value to 27°C. This option also sets some other SPICE compatibility parameters. You set `TNOM` in an `.OPTION` line in the netlist, and you can always use the `TREF` model parameter to override it locally (that is, for a model). (The model “reference temperature” means that the model parameters were extracted at and are valid at that temperature.

UCB SPICE does not use `TNOM` (default 27°C) for the BSIM models. Instead, you must specify the `TEMP` model parameter as both the model reference temperature and the analysis temperature. Analysis at `TEMP` applies only to thermally-activated exponentials in the model equations. You cannot adjust model parameter values when you use `TEMP`. Simulation assumes that you extracted the model parameters at `TEMP`, because `TEMP` is both the reference and the analysis temperature.

In contrast to UCB SPICE’s BSIM, the Synopsys Level 13 model does provide for temperature analysis. The default analysis temperature is 25°C (and 27°C in UCB SPICE for all model levels except for BSIM as explained in the previous paragraph). Use a `.TEMP` statement in the netlist to change the analysis temperature.

The Level 13 model provides two temperature coefficients: `TCV` and `BEX`. The following equation adjusts the threshold voltage:

$$v_{th}(t) = v_{th} - TCV \cdot (t - tnom)$$

This model includes two implementations of the `BEX` factor. To select a `BEX` version, use the `UPDATE` parameter, described in the next section. The mobility in BSIM is a combination of five quantities: `MUZ`, `zmus`, `z3ms`, `zx2mz`, and `zx2ms`.

BEX Usage

$$MUZ(t) = MUZ \cdot \left(\frac{t}{tnom} \right)^{BEX}$$

$$zmus(t) = zmus \cdot \left(\frac{t}{tnom} \right)^{BEX}$$

$$z_{x3ms}(t) = z_{x3ms} \cdot \left(\frac{t}{t_{nom}} \right)^{BEX}$$

$$z_{x2mz}(t) = z_{x2mz} \cdot \left(\frac{t}{t_{nom}} \right)^{BEX}$$

$$z_{x2ms}(t) = z_{x2ms} \cdot \left(\frac{t}{t_{nom}} \right)^{BEX}$$

This is equivalent to multiplying the final mobility by the factor:

$$\left(\frac{t}{t_{nom}} \right)^{BEX}$$

UPDATE Parameter

The UPDATE parameter selects between variations of the BSIM equations. UPDATE=0 (default) is consistent with UCB SPICE3. UPDATE=3 also is consistent with UCB SPICE3 and BEX usage.

Parameter	Description
UPDATE=0	UCB compatible, previous BEX usage
UPDATE=1	Special X2E equation, previous BEX usage
UPDATE=2	Remove 1/L _{eff} in U1 equation, present BEX usage
UPDATE=3	UCB compatible, present BEX usage

Explanations

The normal X2E equation is:

$$xeta = zeta - (zx2e \cdot vsb) + zx3e \cdot (vds - VDDM)$$

The special X2E equation for UPDATE=1 only, is:

$$xeta = zeta + zx2e \cdot (zphi + vsb) + zx3e \cdot (vds - VDDM)$$

The special X2E equation was developed to match a parameter extraction program. If you use a parameter extraction program, check the equations carefully.

The original U1 equation divides by L_{eff} in microns:

$$x_{u1} = \frac{(z_{u1} - (z_{x2u1} \cdot v_{sb}) + z_{x3u1} \cdot (v_{ds} - V_{DDM}))}{L_{eff}}$$

This is one of the few places where L_{eff} explicitly enters into the BSIM equations; usually, the L-adjustment model parameters (such as `LU1`) handles the L_{eff} variation.

Physically x_{u1} should decrease as $1/L_{eff}$ at long channels, but when dealing with short-channel devices, you can turn off this variation. Set `UPDATE=2` to remove the $1/L_{eff}$ factor in the x_{u1} equation.

`UPDATE=2` introduces the present `BEX` usage as the $1/L_{eff}$ removal ability.

`UPDATE=3` provides the present `BEX` using the previous x_{u1} equation.

IDS and VGS Curves for PMOS and NMOS

The netlists for the `IDS` and `VGS` curves for PMOS and NMOS are located in directory `$<installdir>/demo/hspice/mos/ml13iv.sp`. This file contains examples of the following model parameter and curve descriptions:

- Two Types of Model Parameter Formats Used
- `VGS` Curves
- GM Test
- GM B CVN7 5 37 0
- `.PROCESS PC Filename=M57R`
- N-channel Devices
- First Model Parameter Format
- PMOS Model
- Second Model Parameter Format
- N+ Diffusion Layer
- PMOS Model
- Wire Model for Poly and Metal Layers

LEVEL 28 Modified BSIM Model

This section lists the LEVEL 28 parameters and equations for the modified BSIM model.

LEVEL 28 Features

The following are the significant features of the LEVEL 28 model.

- Vertical field dependence of the carrier mobility
- Carrier velocity saturation
- Drain-induced barrier lowering
- Depletion charge sharing by the source and drain
- Nonuniform doping profile for ion-implanted devices
- Channel length modulation
- Subthreshold conduction
- Geometric dependence of the electrical parameters

LEVEL 28 Model Parameters

MOSFET Level 28 uses the generic MOSFET model parameters described in [Chapter 2, Common MOSFET Model Parameters](#). It also uses the parameters described in this section, which apply only to MOSFET Level 28.

Table 112 Transistor Process Parameters

Name (Alias)	Units	Default	Description
LEVEL		1	MOSFET model level selector. Set this parameter to 28 for this model.
B1		0.0	Lower vdsat transition point
LB1	μm	0.0	Length sensitivity

Table 112 Transistor Process Parameters

Name (Alias)	Units	Default	Description
WB1	μm	0.0	Width sensitivity
B2		1	Upper vdsat transition point
LB2	μm	0.0	Length sensitivity
WB2	μm	0.0	Width sensitivity
CGBO	F/m	2.0e-10	Gate-to-bulk parasitic capacitance (F/m of length)
CGDO	F/m	1.5e-9	Gate-to-drain parasitic capacitance (F/m of width)
CGSO	F/m	1.5e-9	Gate-to-source parasitic capacitance (F/m of width)
ETA0		0.0	Linear vds threshold coefficient
LETA	μm	0.0	Length sensitivity
WETA	μm	0.0	Width sensitivity
ETAMN		0.0	Minimum linear vds threshold coefficient
LETAMN	μm	0.0	Length sensitivity
WETAMN	μm	0.0	Width sensitivity
GAMMN	$V^{1/2}$	0.0	Minimum root-vsb threshold coefficient
LGAMN	$V^{1/2} \cdot \mu\text{m}$	0.0	Length sensitivity
WGAMN	$V^{1/2} \cdot \mu\text{m}$	0.0	Width sensitivity
K1	$V^{1/2}$	0.5	Root-vsb threshold coefficient
LK1	$V^{1/2} \cdot \mu\text{m}$	0.0	Length sensitivity

Table 112 Transistor Process Parameters

Name (Alias)	Units	Default	Description
WK1	$V^{1/2} \cdot \mu m$	0.0	Width sensitivity
K2		0.0	Linear vsb threshold coefficient
LK2	μm	0.0	Length sensitivity
WK2	μm	0.0	Width sensitivity
MUZ	$cm^2/V \cdot s$	600	Low drain field first order mobility
LMUZ	$\mu m \cdot cm^2/V \cdot s$	0.0	Length sensitivity
WMUZ	$\mu m \cdot cm^2/V \cdot s$	0.0	Width sensitivity
N0		200	Low field weak inversion gate drive coefficient (value of 200 for N0 disables the weak inversion calculation)
LN0	μm	0.0	Length sensitivity
WN0	μm	0.0	Width sensitivity
NB0		0.0	Vsb reduction to the low field weak inversion gate drive coefficient
LNB	μm	0.0	Length sensitivity
WNB	μm	0.0	Width sensitivity
ND0		0.0	Vds reduction to the low field weak inversion gate drive coefficient
LND	μm	0.0	Length sensitivity
WND	μm	0.0	Width sensitivity
PHI0	V	0.7	Two times the Fermi potential
LPHI	$V \cdot \mu m$	0.0	Length sensitivity

Table 112 Transistor Process Parameters

Name (Alias)	Units	Default	Description
WPHI	V· μm	0.0	Width sensitivity
TOXM (TOX)	μm (m)	0.02	Gate oxide thickness (if TOXM or TOX >1, uses Angstroms)
U00	1/V	0.0	Gate field mobility reduction factor
LU0	$\mu\text{m}/\text{V}$	0.0	Length sensitivity
WU0	$\mu\text{m}/\text{V}$	0.0	Width sensitivity
U1	1/V	0.0	Drain field mobility reduction factor
LU1	$\mu\text{m}/\text{V}$	0.0	Length sensitivity
WU1	$\mu\text{m}/\text{V}$	0.0	Width sensitivity
VDDM	V	5.0	Critical voltage for the high-drain field mobility reduction
VFB0 (VFB)	V	-0.3	Flatband voltage
LVFB	V· μm	0.0	Length sensitivity
WVFB	V· μm	0.0	Width sensitivity
WFAC		4	Weak inversion factor
LWFAC	μm	0.0	Length sensitivity
WWFAC	μm	0.0	Width sensitivity
WFACU		0.0	Second weak inversion factor
LWFACU	μm	0.0	Length sensitivity
WWFACU	μm	0.0	Width sensitivity
X2E	1/V	0.0	Vsb correction to the linear vds threshold coefficient
LX2E	$\mu\text{m}/\text{V}$	0.0	Length sensitivity

Table 112 Transistor Process Parameters

Name (Alias)	Units	Default	Description
WX2E	$\mu\text{m}/\text{V}$	0.0	Width sensitivity
X2M (X2MZ)	$\text{cm}^2/\text{V}^2 \cdot \text{s}$	0.0	Vsb correction to the low field first order mobility
LX2M (LX2MZ)	$\mu\text{m} \cdot \text{cm}^2/\text{V}^2 \cdot \text{s}$	0.0	Length sensitivity
WX2M (WX2MZ)	$\mu\text{m} \cdot \text{cm}^2/\text{V}^2 \cdot \text{s}$	0.0	Width sensitivity
X2U0	$1/\text{V}^2$	0.0	Vsb reduction to the GATE field mobility reduction factor
LX2U0	$\mu\text{m}/\text{V}^2$	0.0	Length sensitivity
WX2U0	$\mu\text{m}/\text{V}^2$	0.0	Width sensitivity
X2U1	$\mu\text{m}/\text{V}^2$	0.0	Vsb reduction to the DRAIN field mobility reduction factor
LX2U1	$\mu\text{m}^2/\text{V}^2$	0.0	Length sensitivity
WX2U1	$\mu\text{m}^2/\text{V}^2$	0.0	Width sensitivity
X33M	$\text{cm}^2/\text{V}^2 \cdot \text{s}$	0.0	Gate field reduction of X3MS
LX33M	$\mu\text{m} \cdot \text{cm}^2/\text{V}^2 \cdot \text{s}$	0.0	Length sensitivity
WX33M	$\mu\text{m} \cdot \text{cm}^2/\text{V}^2 \cdot \text{s}$	0.0	Width sensitivity
X3E	$1/\text{V}$	0.0	Vds correction to the linear vds threshold coefficient
LX3E	$\mu\text{m}/\text{V}$	0.0	Length sensitivity
WX3E	$\mu\text{m}/\text{V}$	0.0	Width sensitivity
X3MS	$\text{cm}^2/\text{V}^2 \cdot \text{s}$	5.0	Vds correction for the high-drain field mobility

Table 112 Transistor Process Parameters

Name (Alias)	Units	Default	Description
LX3MS	$\mu\text{m} \cdot \text{cm}^2/\text{V}^2 \cdot \text{s}$	0.0	Length sensitivity
WX3MS	$\mu\text{m} \cdot \text{cm}^2/\text{V}^2 \cdot \text{s}$	0.0	Width sensitivity
X3U1	$1/\text{V}^2$	0.0	Vds reduction to the drain field mobility reduction factor
LX3U1	$\mu\text{m}/\text{V}^2$	0.0	Length sensitivity
WX3U1	$\mu\text{m}/\text{V}^2$	0.0	Width sensitivity
XPART		1.0	Selects the coefficient for sharing the gate capacitance charge

Notes:

- When you read parameter names, be careful about the difference in appearance between the capital letter O and the number zero (0).
- Use NMOS conventions to specify all Level 28 parameters, even for PMOS—for example, $\text{ETA0}=0.02$, not $\text{ETA0}=-0.02$.
- You can use the WL -product sensitivity parameter for any parameter with an L and W sensitivity. Replace the leading “L” of the L sensitivity parameter name with a “P”.

Table 113 Temperature Parameters

Name (Alias)	Units	Default	Description
BEX		-1.5	Temperature exponent for the MUZ, X2M, X3MS, and X33M mobility parameters
FEX		0.0	Temperature exponent for the U1 mobility reduction factor
TCV	$\text{V}/^\circ\text{K}$	0.0	Flat-band voltage temperature coefficient

Sensitivity Factors of Model Parameters

For transistors, drop the 0 from the end of the parameter name, and add one of the following product sensitivity factors for a basic electrical parameter:

- L (channel length)
- W (channel width)
- WL (width and length)

For example, the V_{FB0} sensitivity factors are LV_{FB} , WV_{FB} , and PV_{FB} . If $A0$ is a basic parameter, LA , WA and PA are the corresponding sensitivity factors for this parameter (you cannot use the $SCALM$ option to scale LA , WA , and PA). Then the model uses the following general formula to obtain the parameter value.

The left side of the equation represents the effective model parameter value after you adjust the device size. All effective model parameters are in lower case and start with the z character, followed by the parameter name.

$$za = A0 + LA \cdot \left[\frac{1}{Leff} - \frac{1}{LREFeff} \right] + WA \cdot \left[\frac{1}{Weff} - \frac{1}{WREFeff} \right]$$

$$PA \cdot \left[\frac{1}{Leff} - \frac{1}{LREFeff} \right] \cdot \left[\frac{1}{Weff} - \frac{1}{WREFeff} \right]$$

Specify LA and WA in units of microns times the units of $A0$. Specify PA in units of square microns times the units of $A0$.

If you set $LREF$ or $WREF=0$, you effectively set the parameter value to infinity. This is the default.

Example

$$V_{FB0} = -0.350v$$

$$LV_{FB} = -0.1v\mu$$

$$WV_{FB} = 0.08v \cdot \mu$$

$$Leff = 1 \cdot 10^{-6}m = 1\mu$$

$$Weff = 2 \cdot 10^{-6}m = 2\mu$$

$$LREFeff = 2 \cdot 10^{-6}m = 2\mu$$

$$WREFeff = 1 \cdot 10^{-5}m = 10\mu$$

$$z_{vfb} = VFB0 + LVFB \cdot \left(\frac{1}{L_{eff}} - \frac{1}{LREF_{eff}} \right) + WVFB \cdot \left(\frac{1}{W_{eff}} - \frac{1}{WREF_{eff}} \right)$$

$$z_{vfb} = -0.35v + -0.1v \cdot \mu \cdot \left(\frac{1}{1\mu} - \frac{1}{2\mu} \right) + 0.08v \cdot \mu \cdot \left(\frac{1}{2\mu} - \frac{1}{10\mu} \right)$$

$$z_{vfb} = -0.35v - 0.05v + 0.032v$$

$$z_{vfb} = -0.368v$$

LEVEL 28 Model Equations

The LEVEL 28 model equations follow.

Effective Channel Length and Width

The effective channel length and width for Level 28 is consistent with the LEVEL 3 model. L, W, and the M multiplier are from the .MODEL statement in the netlist. SCALE and SCALM are options. If you do not specify any scaling options or multipliers, then:

$$L_{eff} = L + XL - 2 \cdot LD \quad W_{eff} = W + XW - 2 \cdot WD$$

Note: If you specify LDAC and WDAC in the .MODEL statement,

$$L_{eff} = L + XL - 2 \cdot LDAC \quad W_{eff} = W + XW - 2 \cdot WDAC$$

$$L_{scaled} = L \cdot SCALE$$

$$W_{scaled} = W \cdot SCALE$$

$$XL_{scaled} = XL \cdot SCALM$$

$$LD_{scaled} = LD \cdot SCALM$$

$$XW_{scaled} = XW \cdot SCALM$$

$$WD_{scaled} = WD \cdot SCALM$$

$$L_{eff} = L_{scaled} \cdot LMLT + XL_{scaled} - 2 \cdot LD_{scaled}$$

$$LREF_{eff} = LREF_{scaled} \cdot LMLT + XLREF_{scaled} - 2 \cdot LD_{scaled}$$

$$W_{eff} = M \cdot (W_{scaled} \cdot WMLT + XWREF_{scaled} - 2 \cdot WD_{scaled})$$

$$WREF_{eff} = MP \cdot (WREF_{scaled} \cdot WMLT + XW_{scaled} - 2 \cdot WD_{scaled})$$

Threshold Voltage

Effective model parameter values for the threshold voltage, after you adjust the device size, are $zphi$, $zvfb$, $zk1$, $zk2$, $zeta$, $zx2e$, $zx3e$, $zgammn$, and $zetamn$. Simulation calculates these values from the $PHI0$, $VFB0$, $K1$, $K2$, $ETA0$, $X2E$, $X3E$, $GAMMN$, and $ETAMN$ model parameters, and from their respective length and width sensitivity parameters.

$$xbs = (zphi - vbs)^{1/2}$$

$$xeta = zeta + zx2e \cdot vbs + zx3e \cdot vds$$

$$vth = zvfb + zphi + zk1 \cdot xbs - zk2 \cdot xbs^2 - xeta \cdot vds$$

This equation is quadratic in xbs and vds . It is joined to linear equations at $d(vth)/d(xbs) = zgammn$ and at $d(vth)/d(vds) = -zetamn$, which prevents the quadratics from going in the wrong direction.

Both $gammn$ and $etamn$ default to zero, and typically do not affect behavior in the normal operating region.

Effective Mobility

The effective model parameter values for mobility, after you adjust the device size, are $zmuz$, $zx2m$, $zx3m$, $zx33m$, $zu0$, and $zx2u0$. Simulation calculates these values from the MUZ , $X2M$, $X3m$, $X33M$, $U00$, and $X2U0$ model parameters, and from their respective length and width sensitivity parameters.

$$v_{gst} = v_{gs} - v_{th}$$

$$m_{eff} = (zmuz + zx2m \cdot v_{bs})$$

$$cx3ms = \frac{zx3ms}{(muz + zx33m \cdot v_{gst})}$$

$$(1 + cx3ms \cdot (VDDM + v_{ds} - (VDDM \cdot VDDM + v_{ds} \cdot v_{ds})^{1/2}))$$

$$xu0 = zu0 + zx2u0 \cdot v_{bs}$$

$$u_{eff} = \frac{m_{eff}}{(1 + xu0 \cdot v_{gst})}, \quad beta = u_{eff} \cdot COX \cdot \frac{W_{eff}}{L_{eff}}$$

Saturation Voltage (vdsat)

The effective model parameter values for the saturation voltage, after you adjust the device size, are zu1, zx2u1, and zx3u1. Simulation calculates these values from the U1, X2U1, and X3U1 model parameters, and from their length and width sensitivity parameters.

$$xbs = (zphi - v_{bs})^{1/2}, g = 1 - \frac{1}{(1.744 + 0.8364 \cdot xbs^2)}$$

$$body = \frac{1 + g \cdot zk1}{(2 \cdot xbs)}, xu1 = zu1 + v_{bs} \cdot zx2u1$$

$$rx = (body^2 + zu1 \cdot 2 \cdot body \cdot v_{gst} + zx3u1 \cdot 4 \cdot v_{gst}^2)^{1/2}$$

$$v_{dsat} = \frac{2 \cdot v_{gst}}{(body + rx)}$$

This vds value generates the partial derivative of:

$$f(v_{ds}, v_{gst}, v_{bs}) = (v_{gst} - body/2 \cdot v_{ds}) \cdot \frac{v_{ds}}{(1 + (xu1 + zx3u1 \cdot v_{ds}) \cdot v_{ds})}$$

In the preceding equation, vds=zero.

Transition Points

The effective model parameter values for the transition points, after you adjust the device size, are zb1 and zb2. Simulation calculates these values from the B1 and B2 model parameters, and from their respective length and width sensitivity parameters.

$$v1 = v_{dsat} - zb1 \cdot \frac{v_{dsat}}{1 + v_{dsat}}, v2 = v_{dsat} + zb2 \cdot v_{gst}$$

Strong Inversion Current

For vds < v1:

$$I_{ds} = \beta \cdot (v_{gs} - v_{th})^2 \cdot \frac{v_{ds}}{(1 + (z_{u1} + z_{x3u1} \cdot v_{ds}) \cdot v_{ds})}$$

The v_{ds} derivative varies approximately linearly between v_1 and v_2 .

For $v_{ds} > v_2$, i_{ds} is a function of β and v_{gs} only. If z_{b1} and z_{b2} are both positive, their main effect is to increase the saturation current.

Weak Inversion Current

The effective model parameter values for weak inversion current, after you adjust the device size, are z_{n0} , z_{nb} , z_{nd} , z_{wfac} , and z_{wfacu} . Simulation calculates these values from the N_0 , ND_0 , NB_0 , $WFAC$, and $WFACU$ model parameters, and from their respective length and width sensitivity parameters.

Simulation calculates the weak inversion current when z_{n0} is less than 200, and adds it to the strong inversion current:

$$I_{total} = I_{strong} + I_{weak} \cdot \left(1 - \exp\left(\frac{-v_{ds}}{v_{therm}}\right)\right)$$

In deep subthreshold:

$$x_n = z_{n0} + z_{nb} \cdot v_{bs} + z_{nd} \cdot v_{ds}$$

$$v_{therm} = \frac{KT}{Q}, \quad x_{weak} = \frac{(v_{gs} - v_t)}{(x_n \cdot v_{therm})}$$

$$I_{weak} = const \cdot \exp(x_{weak})$$

z_{wfac} and z_{wfacu} control the modification of this formula near the threshold. Just above threshold, the device is in saturation:

$$I_{strong} = const \cdot x_{weak}^2$$

I_{weak} needs an x_{weak}^2 term to cancel the kink in g_m at the threshold. Then I_{weak} goes to zero for $x_{weak} > A_0$, which is at a small voltage above the threshold. I_{weak} has four regions.

$$x_{weak} < -z_{wfac} + A_0$$

$$I_{weak} = const \cdot \exp(x_{weak})$$

$$-z_{wfac} + A_0 < x_{weak} < 0$$

$$I_{weak} = const \cdot \exp(x_{weak} - const \cdot wf)$$

In the preceding equation, wf is the integral with respect to the $xweak$ value of:

$$dwf = \frac{(xweak + zwfac - A0)^2}{[(1 + xweak + zwfac - A0)(1 + zwfacu \cdot (xweak + zwfac - A0))]}$$

$0 < xweak < A0$

$$Iweak = (\text{same formula as in region 2}) - const \cdot xweak^2$$

$A0 < xweak$

$$Iweak = 0$$

$A0$, and the constants in the preceding equations, are not model parameters. Continuity conditions, at the boundaries between regions, uniquely determine these constants.

LEVEL 39 BSIM2 Model

BSIM2 (Berkeley Short-Channel IGFET Model 2) is the LEVEL 39 MOSFET model. The Synopsys implementation of this model is based on Berkeley SPICE 3E2.

To provide input to the Level 39 device model, assign the model parameters as for other device models. You can use a tabular model entry without model parameter names in BSIM1, but *not* in BSIM2.

LEVEL 39 Model Parameters

MOSFET Level 39 uses the generic MOSFET model parameters described in [Chapter 5, MOSFET Models \(BSIM\): Levels 13 through 39](#). It also uses the parameters described in this section, which apply only to MOSFET Level 39.

This section lists the BSIM2 parameters, their units, their defaults (if any) in the Level 39 MOSFET model, and their descriptions. [Table 114](#) lists 47 BSIM2-specific parameters. The Synopsys model does not use three of the parameters (TEMP, DELL, and DFW). The width and length sensitivity parameters are associated with the remaining parameters, except the first six (TOX, VDD, VGG, VBB, DL, and DW). So the total parameter count is 120. (Unlike Berkeley SPICE, the Synopsys Level 39 MOSFET model has L and W

sensitivity for μ_{U0}). This count does not include the *generic* MOS parameters or the μ_{L} -product sensitivity parameters, which are Synopsys enhancements.

Table 114 BSIM2 Model Parameters

Name (Alias)	Units	Default	Description
TOX	m	0.02	Gate oxide thickness (assumes that TOX>1 is in Angstroms)
TEMP	C	-	Not used in Level 39 (see Compatibility Notes on page 388)
VDD	V	5	Drain supply voltage (NMOS convention)
VGG	V	5	Gate supply voltage (NMOS convention)
VBB	V	-5	Body supply voltage (NMOS convention)
DL	m	0	Channel length reduction
DW	m	0	Channel width reduction
VGHIGH	V	0	Upper bound of the weak-strong inversion transition region
VGLOW	V	0	Lower bound of the weak-strong inversion transition region
VFB	V	-0.3	Flat band voltage
PHI	V	0.8	Surface potential
K1	V-1	0.5	Body effect coefficient
K2	-	0	Second-order body effect coefficient (for nonuniform channel doping)
ETA0	-	0	Drain-induced barrier lowering coefficient
ETAB	V-1	0	Sensitivity of the drain-induced barrier lowering coefficient to V_{bs}
μ_{U0}	$\text{cm}^2/\text{V} \cdot \text{s}$	400	Low-field mobility

Table 114 BSIM2 Model Parameters

Name (Alias)	Units	Default	Description
MU0B	$\text{cm}^2/\text{V}^2 \cdot \text{s}$	0	Sensitivity of low-field mobility to V_{bs}
MUS0	$\text{cm}^2/\text{V} \cdot \text{s}$	600	High-drain field mobility
MUSB	$\text{cm}^2/\text{V}^2 \cdot \text{s}$	0	Sensitivity of the high-drain field mobility to V_{bs}
MU20	-	0	Empirical parameter for the output resistance
MU2B	V-1	0	Sensitivity of the empirical parameter to V_{bs}
MU2G	V-1	0	Sensitivity of the empirical parameter to V_{gs}
MU30	$\text{cm}^2/\text{V}^2 \cdot \text{s}$	0	Empirical parameter for the output resistance
MU3B	$\text{cm}^2/\text{V}^3 \cdot \text{s}$	0	Sensitivity of the empirical parameter to V_{bs}
MU3G	$\text{cm}^2/\text{V}^3 \cdot \text{s}$	0	Sensitivity of the empirical parameter to V_{gs}
MU40	$\text{cm}^2/\text{V}^3 \cdot \text{s}$	0	Empirical parameter for the output resistance
MU4B	$\text{cm}^2/\text{V}^4 \cdot \text{s}$	0	Sensitivity of the empirical parameter to V_{bs}
MU4G	$\text{cm}^2/\text{V}^4 \cdot \text{s}$	0	Sensitivity of the empirical parameter to V_{gs}
UA0	V-1	0	First-order vertical-field mobility reduction factor
UAB	V-2	0	Sensitivity of the first-order factor to V_{bs}
UB0	V-2	0	Second-order vertical-field mobility reduction factor
UBB	V-3	0	Sensitivity of the second-order factor to V_{bs}
U10	V-1	0	High-drain field (velocity saturation) mobility reduction factor

Table 114 BSIM2 Model Parameters

Name (Alias)	Units	Default	Description
U1B	V-2	0	Sensitivity of the mobility reduction factor to V_{bs}
U1D	V-2	0	Sensitivity of the mobility reduction factor to V_{ds}
N0	-	0.5	Subthreshold swing coefficient
NB	V1/2	0	Sensitivity of the subthreshold swing to V_{bs}
ND	V-1	0	Sensitivity of the subthreshold swing to V_{ds}
VOF0	-	0	Threshold offset (normalized to NKT/q) for the subthreshold
VOFB	V-1	0	Sensitivity of the offset to V_{bs}
VOFD	V-1	0	Sensitivity of the offset to V_{ds}
AI0	-	0	Impact ionization coefficient
AIB	V-1	0	Sensitivity of the impact ionization coefficient to V_{bs}
BI0	V	0	Impact ionization exponent
BIB	-	0	Sensitivity of the impact ionization exponent to V_{bs}
DELL	m	-	Length reduction of the source drain diffusion (not used in the Level 39 MOSFET model)
WDF	m	-	Default width (not used in the Level 39 MOSFET model); use <code>.OPTION DEFW=#</code> in the netlist instead

Specify all BSIM2 parameters according to the NMOS convention, even for a PMOS model. Examples: $V_{DD}=5$, not -5 ; $V_{BB}=-5$, not 5 ; and $\text{ETA}0=0.02$, not -0.02 . See [Compatibility Notes on page 388](#).

The Level 39 MOSFET model also includes the $J_{SW}[A/m]$ source/drain bulk diode sidewall reverse saturation current density.

Other Device Model Parameters that Affect BSIM2

You must specify the following MOSFET model parameters before you can use some Synopsys enhancements, such as

- LDD-compatible parasitics.
- Adjusts the model parameter geometry, relative to a reference device.
- Impact ionization modeling with bulk-source current partitioning.
- Element temperature adjustment of the key model parameters.

This is a partial list. For complete information, see the following:

- [Calculating Effective Length and Width for AC Gate Capacitance on page 691](#)
- [Drain and Source Resistance Model Parameters on page 697](#)
- [MOSFET Impact Ionization on page 744](#)

[.MODEL VERSION Changes to BSIM2 Models on page 390](#) describes how the `VERSION` parameter in the `.MODEL` statement changes the BSIM2 model, depending on the model version number.

LEVEL 39 Model Equations

In the following expressions, model parameters are in all upper case Roman. These expressions assume that you have already adjusted all model parameters for geometry, and that you have already adjusted parameters without a trailing 0 for the bias as appropriate. The exceptions are `U1` and `N` for which the following equations explicitly calculate the bias dependences.

Threshold voltage, V_{th}

$$V_{th} = V_{bi} + K1 \sqrt{PHI - V_{bs}} - K2(PHI - V_{bs}) - ETA \cdot V_{ds}$$

The following equation calculates the v_{bi} value used in the preceding equation:

$$V_{bi} = VFB + PHI$$

Strong inversion ($V_{gs} > V_{th} + V_{GHIGH}$)

Linear region ($V_{ds} < V_{dsat}$) drain-source current I_{DS} :

$$I_{DS} = \frac{\beta' \left(V_{gs} - V_{th} - \frac{a}{2} V_{ds} \right) V_{ds}}{1 + UA(V_{gs} - V_{th}) + UB(V_{gs} - V_{th})^2 + U1 \cdot V_{ds}}$$

The following equations calculate values used in the preceding equation:

$$V_{dsat} = \frac{V_{gs} - V_{th}}{a\sqrt{K}},$$

$$K = \frac{1 + V_c + \sqrt{1 + 2V_c}}{2},$$

$$V_c = \frac{U_{1S}(V_{gs} - V_{th})}{a[1 + UA(V_{gs} - V_{th}) + UB(V_{gs} - V_{th})^2]},$$

$$U_{1S} = U_{10} + U_{1B} \cdot V_{bs},$$

$$U1 = U_{1S} \left[1 - \Theta(V_{dsat} - V_{ds}) \frac{U1D(V_{ds} - V_{dsat})^2}{V_{dsat}^2} \right]$$

In the preceding equations, $\Theta(x)$ is the usual unit step function:

$$\beta' = \beta_0 + \beta_1 \tanh\left(MU2 \frac{V_{ds}}{V_{dsat}}\right) + \beta_3 V_{ds} - \beta_4 V_{ds}^2$$

$$\beta_0 = \frac{W_{eff}}{L_{eff}} MU \cdot C_{ox},$$

$$\beta_1 = \beta_S - (\beta_0 + \beta_3 VDD - \beta_4 VDD^2),$$

$$\beta_i = \frac{W_{eff}}{L_{eff}} MU i \cdot C_{ox}, i = S, 3, 4, a = 1 + \frac{gK1}{2\sqrt{PHI - V_{bs}}},$$

$$g = 1 - \frac{1}{1.744 + 0.8364(PHI - V_{bs})}$$

Saturation ($V_{ds} > V_{dsat}$) drain-source current, I_{DS} :

$$I_{DS} = \frac{\beta'(V_{gs} - V_{th})^2}{2aK[1 + UA(V_{gs} - V_{th}) + UB(V_{gs} - V_{th})^2]} \cdot (1 + f)$$

In the preceding equation, the f impact ionization term is:

$$f = AI \cdot e^{\frac{-BI}{V_{ds} - V_{dsat}}}$$

Weak Inversion ($V_{gs} < V_{th} + VGLOW$; [$VGLOW < 0$])

Subthreshold drain-source current, I_{ds} :

$$I_{DS} = \beta' \cdot V_{tm}^2 \cdot \exp\left(\frac{V_{gs} - V_{th}}{N \cdot V_{tm}} + VOFF\right) \cdot \left[1 - \exp\left(-\frac{V_{ds}}{V_{tm}}\right)\right] \cdot (1 + f)$$

The following equations calculate the V_{tm} and N values used in the preceding equation:

$$V_{tm} = \frac{kT}{q} \text{ and } N = N0 + \frac{NB}{\sqrt{PHI - V_{bs}}} + ND \cdot V_{ds}$$

Strong inversion-to-weak inversion transition region ($V_{th} + VGLOW \leq V_{gs} \leq V_{th} + VGHIGH$)

$$V_{geff}(V_{gst}) = \sum_{j=0}^3 C_j V_{gst}^j$$

The preceding equation replaces $V_{gst} = V_{gs} - V_{th}$ in the linear or saturation drain currents, based on $V_{dsat}(V_{geff})$.

At the lower boundary ($V_{gs} - V_{th} = VGLOW$), the saturation equation is valid for all V_{ds} (that is, $V_{dsat}(V_{geff}(VGLOW)) \approx 0$) to allow a match to the above subthreshold equation.

To internally determine the C_j coefficients of the V_{geff} cubic spline, the I_{DS} and dI_{ds}/dV_{gs} conditions must both be continuous at the $V_{gs} = V_{th} + VGLOW$ and $V_{gs} = V_{th} + VGHIGH$ boundaries.

Effective Length and Width

If DL is nonzero

$$L_{eff} = L_{scaled} \cdot LMLT - DL$$

$$LREF_{eff} = LREF_{scaled} \cdot LMLT - DL$$

Otherwise:

$$L_{eff} = L_{scaled} \cdot LMLT + XL_{scaled} - 2 \cdot LD_{scaled}$$

$$LREF_{eff} = LREF_{scaled} \cdot LMLT + XLREF_{scaled} - 2 \cdot LD_{scaled}$$

If DW is nonzero

$$W_{eff} = (W_{scaled} \cdot WMLT - DW) \cdot M$$

$$WREF_{eff} = (WREF_{scaled} \cdot WMLT - DW) \cdot M$$

Otherwise:

$$W_{eff} = (W_{scaled} \cdot WMLT + XW - 2 \cdot WD_{scaled}) \cdot M$$

$$WREF_{eff} = (WREF_{scaled} \cdot WMLT + XWREF_{scaled} - 2 \cdot WD_{scaled}) \cdot M$$

Geometry and Bias of Model Parameters

Most of the BSIM2 parameters include width and length sensitivity parameters. You can also specify Synopsys-proprietary WL-product sensitivity parameters. If P is a parameter, then its associated width, length, and WL-product sensitivity parameters are WP, LP, and PP.

The value of the P' parameter, adjusted for width, length, and WL-product, is:

$$P' = P + WP \cdot \left(\frac{1}{W_{eff}} - \frac{1}{WREF_{eff}} \right) + LP \cdot \left(\frac{1}{L_{eff}} - \frac{1}{LREF_{eff}} \right) \\ + PP \cdot \left(\frac{1}{W_{eff}} - \frac{1}{WREF_{eff}} \right) \cdot \left(\frac{1}{L_{eff}} - \frac{1}{LREF_{eff}} \right)$$

Berkeley SPICE does not use the WREF and LREF terms. They are effectively infinite, which is the default in the Level 39 MOSFET model.

The following BSIM2 parameters do not have associated geometry-sensitivity parameters:

TOX
TEMP (not used)
VDD
VGG
VBB
DL
DW

BSIM2 parameters ending in 0 are valid at zero bias, and they have associated bias sensitivities, listed in the BSIM2 parameter table.

If PB , PD , and PG are the geometry-adjusted v_{bs} -, v_{ds} -, and v_{gs} - sensitivity parameters, and if they are associated with the $P0$ geometry-adjusted zero-bias parameter, then the following equation calculates the P bias-dependent parameter:

$$P = P0 + PB \cdot V_{bs} + PD \cdot V_{ds} + PG \cdot V_{gs}$$

The exceptions are the $U1$ velocity saturation factor and the N subthreshold swing coefficient. [Modeling Guidelines, Removing Mathematical Anomalies on page 395](#) shows expressions for their bias dependences.

Compatibility Notes

SPICE3 Flag

If you specify the $SPICE3=0$ (default) model parameter, certain Synopsys corrections to the BSIM2 equations are effective. If you set the $SPICE3$ value to 1, the equations are as faithful as possible to the BSIM2 equations for $SPICE3E2$. Even in this mode, certain numerical problems have been addressed and should not normally be noticeable.

Temperature

The default model reference temperature ($TNOM$) is 25°C in the Level 39 MOSFET model, unless you set `.OPTION SPICE`, which sets the $TNOM$ default to 27° C. This option also sets some other SPICE compatibility parameters. In the Level 39 model, you set $TNOM$ in an `.OPTION` line in the netlist; to override this locally (that is, for a model), use the $TREF$ model parameter. (“Reference temperature” means that the model parameters were extracted at, and are therefore valid at, that temperature.)

UCB SPICE 3 does not use $TNOM$ (default 27° C) for the BSIM models. Instead, you must specify the $TEMP$ model parameter as both the model reference temperature and the analysis temperature. Analysis at $TEMP$ applies only to thermally-activated exponentials in the model equations. You cannot adjust the model parameter values if you use $TEMP$. Simulation assumes that you extracted the model parameters at $TEMP$, because $TEMP$ is both the reference and analysis temperature.

For model levels *other than* 4 (BSIM1) and 5 (BSIM2) in UCB SPICE3, simulation adjusts the key model parameters for the difference between `TEMP` (default 27°C) and `TNOM`. To specify `TEMP` in the netlist, use `.TEMP #` as in the Level 39 MOSFET model.

In contrast to UCB SPICE's BSIM models, the Synopsys Level 39 MOSFET model does provide for temperature analysis. The default analysis temperature is 25°C in the Level 39 model. Set `.TEMP #` in your netlist to change the analysis temperature (you cannot use `TEMP` as a model parameter). The Level 39 MOSFET model adjusts the temperature of the key model parameters as explained in [Temperature Effect on page 357](#).

Parasitics

`ACM > 0` invokes the MOS source-drain parasitics in the Level 39 MOSFET device model. `ACM=0` (default) is SPICE style. See [Synopsys Device Model Enhancements on page 392](#).

Selecting Gate Capacitance

`CAPOP=39` selects the BSIM2 charge-conserving capacitance model as shipped with Berkeley SPICE 3E2. This is the default selection if you set `SPICE3=1`.

- `XPART` (charge-sharing flag) is currently not a BSIM2 model parameter, despite its specification in the sample BSIM2 input decks shipped with Berkeley SPICE 3E. It appears that its use in SPICE 3E was as a printback debug aid.
- Saturation charge sharing appears to be fixed at 60/40 (S/D) in the BSIM2 capacitance model. For the charge equations, see [Charge-based Gate Capacitance Model \(CAPOP=39\) on page 391](#). See also [Modeling Guidelines, Removing Mathematical Anomalies on page 395](#).

You can choose other `CAPOP` values. `CAPOP=13` (recommended) selects the BSIM1-based charge-conserving capacitance model for the MOSFET LEVEL 13 (BSIM1) or LEVEL 28 (modified BSIM1) device models. This option is the default selection if `SPICE3=0`. If you use this capacitance model, you can use the `XPART` or `XQC` model parameters to adjust charge sharing. See [LEVEL 13 BSIM Model on page 345](#) for more information.

Unused Parameters

The Level 39 MOSFET model does not use the DELL (S/D diode length reduction) and WDF (default device width) SPICE model parameters. SPICE 3E does not use the DELL function. You can specify a default width in the Level 39 MOSFET model, on the .OPTION line as DEFW (which defaults to 100μ).

.MODEL VERSION Changes to BSIM2 Models

The Level 39 MOSFET model provides a VERSION parameter to the .MODEL statement, which lets you move LEVEL 13 BSIM and LEVEL 39 BSIM2 models between device model versions. Use the VERSION parameter in a LEVEL 13 .MODEL statement. [Table 115](#) lists the changes in the BSIM model.

Table 115 BSIM2 Model Features by Version Number

Model Version	Effect of VERSION on BSIM2 Model
92A	LEVEL 39 BSIM2 model introduced: no changes
92B	No changes
93A	Introduced gds constraints, fixed a defect in the WMU3B parameter, and introduced a defect in the MU4 parameter
93A.02	Introduced the VERSION parameter, and fixed an MU4 parameter defect
95.1	Fixed defects that caused PMUSB, LDAC, and WDAC parameter problems, fixed the GMBS defect if you used gds constraints
96.1	Limited $ETA + ETAB \cdot vb5 \geq 0$

Preventing Negative Output Conductance

The Level 39 MOSFET model internally protects against conditions in the LEVEL 13 model that cause convergence problems due to negative output conductance. This model imposes the following constraints:

$$MU2 \geq 0 \quad ND \geq 0 \quad AI \geq 0$$

Simulation imposes these constraints after adjusting the length and width and setting the VBS dependence. This feature loses some accuracy in the saturation region, particularly at high Vgs.

Consequently, you might need to requalify the BSIM2 models in the following situations:

- Devices exhibit self-heating during characterization, which causes declining I_{ds} at high V_{ds} . This does not occur if the device characterization measurement sweeps V_{ds} .
- The extraction technique produces parameters that result in negative conductance.
- This model simulates the voltage outside the device's characterized range.

Charge-based Gate Capacitance Model (CAPOP=39)

The BSIM2 gate capacitance model conserves charge and has non-reciprocal attributes. Using charges as state variables guarantees charge conservation. Charge partitioning is fixed at 60/40 (S/D) in saturation and is 50/50 in the linear region. $Q_s = -(Q_g + Q_d + Q_b)$ in all regions.

Accumulation region ($V_{gs} < V_{bs} + V_{FB}$)

$$Q_g = C_{ox} W_{eff} \cdot L_{eff} (V_{gs} - V_{bs} - V_{FB})$$

$$Q_b = -Q_g$$

$$Q_d = 0$$

Subthreshold region ($V_{bs} + V_{FB} < V_{gs} < V_{th} + V_{GLOW}$)

$$Q_g = C_{ox} W_{eff} \cdot L_{eff} (V_{gs} - V_{bs} - V_{FB})$$

$$\left[1 - \frac{V_{gs} - V_{bs} - V_{FB}}{V_{gs} - V_{bs} - V_{FB} - V_{gst}} + \frac{1}{3} \left\{ \frac{V_{gs} - V_{bs} - V_{FB}}{V_{gs} - V_{bs} - V_{FB} - V_{gst}} \right\}^2 \right]$$

$$Q_b = -Q_g$$

$$Q_d = 0$$

Saturation region ($V_{ds} > V_{dsat}$)

$$Q_g = \frac{2}{3} C_{ox} W_{eff} \cdot L_{eff} \cdot V_{gst} + Q_{bulk}$$

The following equations calculate values used in the preceding equation:

$$Q_{bulk} = \frac{1}{3} C_{ox} W_{eff} \cdot L_{eff} [V_{th} - V_{bs} - V_{FB}]$$

$$Q_b = -Q_{bulk}$$

$$Q_d = -\frac{4}{10} \cdot \frac{2}{3} C_{ox} W_{eff} \cdot L_{eff} \cdot V_{gst} = \left(-\frac{4}{15}\right) C_{ox} W_{eff} \cdot L_{eff} \cdot V_{gst}$$

Linear region ($V_{ds} < V_{dsat}$):

$$Q_g = \frac{2}{3} C_{ox} W_{eff} \cdot L_{eff} \cdot V_{gst} \cdot \left[\frac{3 \left(1 - \frac{V_{ds}}{V_{dsat}}\right) + \left(\frac{V_{ds}}{V_{dsat}}\right)^2}{2 - \frac{V_{ds}}{V_{dsat}}} \right] + Q_{bulk}$$

$$Q_b = -Q_{bulk}, Q_d = -\frac{1}{3} C_{ox} W_{eff} \cdot L_{eff} \cdot V_{gst}$$

$$\left[\frac{3 \left(1 - \frac{V_{ds}}{V_{dsat}}\right) + \left(\frac{V_{ds}}{V_{dsat}}\right)^2}{2 - \frac{V_{ds}}{V_{dsat}}} + \frac{\frac{V_{ds}}{V_{dsat}} \left(1 - \frac{V_{ds}}{V_{dsat}}\right) + 0.2 \left(\frac{V_{ds}}{V_{dsat}}\right)^2}{\left(2 - \frac{V_{ds}}{V_{dsat}}\right)^2} \right] + Q_{bulk}$$

Synopsys Device Model Enhancements

In the following expressions, model parameters are in all upper case Roman. Simulation assumes that you have already adjusted all model parameters without a trailing 0 for both geometry and bias as appropriate.

Temperature Effects

LEVEL=39 enforces TLEV=1. You cannot currently use any other TLEV value. The following equation adjusts the threshold voltage for Level 39 TLEV=1:

$$V_{th}(T) = V_{bi}(T) + K1 \cdot \sqrt{\phi(T) - V_{bs}} - K2 \cdot (\phi(T) - V_{bs}) - ETA \cdot V_{ds}$$

The following equations calculate values used in the preceding equation:

$$V_{bi}(T) = V_{to}(T) - K1 \cdot \sqrt{\phi(T)} + K2 \cdot \phi(T)$$

$$V_{to}(T) = V_{to} - TCV \cdot (T - T_{nom})$$

In the preceding equations, the nominal-temperature, zero-bias threshold voltage is:

$$\begin{aligned} V_{to} &= V_{bi} + K1 \cdot \sqrt{PHI} - K2 \cdot PHI \\ &= VFB + PHI + K1 \cdot \sqrt{PHI} - K2 \cdot PHI, \end{aligned}$$

Simulation calculates $\phi(T)$ according to the specified `TLEV` value.

The following equation adjusts the mobility:

$$\mu(T) = \mu(T_{nom}) \cdot \left(\frac{T}{T_{nom}} \right)^{BEX} \text{ where } \mu = \frac{\beta'}{C_{ox}(W_{eff}/L_{eff})}.$$

UIS adjusts the velocity saturation:

$$UIS(T) = UIS \cdot \left(\frac{T}{T_{nom}} \right)^{FEX}$$

This model also includes all of the usual Synopsys model adjustments to capacitances, parasitics, diodes, and resistors.

Alternate Gate Capacitance Model

Select `CAPOP=13` for the charge-conserving capacitance model, widely used with `LEVEL=13` (BSIM1) and `LEVEL=28` (improved BSIM1). See [LEVEL 13 BSIM Model on page 345](#) for more details.

Impact Ionization

To select impact ionization modeling (instead of BSIM2), keep the `AI0=0` value, and specify the `ALPHA` [`ALPHA \cdot (V_{ds} - V_{dsat})` replaces `AI` in equation for f in the BSIM2 equations section], `VCR` (replaces `BI`), and `IIRAT` (multiplies f) model parameters.

Synopsys impact ionization modeling differs from BSIM2 modeling in two ways:

- A bias term ($V_{ds} - V_{dsat}$) multiplies the exponential and `ALPHA` values.
- You can use the `IIRAT` model parameter to partition the impact ionization component of the drain current, between the source and the bulk. `IIRAT` multiplies f in the saturation I_{ds} equation. Thus, the `IIRAT` fraction of the

impact ionization current goes to the source, and the $1 - IIRAT$ fraction goes to the bulk, adding to IDB . $IIRAT$ defaults to zero (that is, 100% of impact ionization current goes to the bulk).

BSIM2's impact ionization assumes that all of the impact ionization current is part of I_{ds} . In other words, it flows to the source. This assumption can lead to inaccuracies, for example, in cascode circuits.

Parasitic Diode for Proper LDD Modeling

The Level 39 MOSFET model includes alternative MOS parasitic diodes to replace SPICE-style MOS parasitic diodes. You can use these alternatives to geometrically scale the parasitics with MOS device dimension, properly modeling the LDD parasitic resistances, shared sources and drains, and select different diode sidewall capacitances along the gate edge and field edge.

To select the MOS parasitic diode, use the `ACM` model parameter.

- `ACM=0` (default) chooses SPICE style. The alternatives likely to be of most interest to the BSIM2 user are `ACM=2` and `3`.
- `ACM=2` calculates the diode area based on `W`, `XW`, and `HDIF` (contact to gate spacing). You can override the calculation from the element line. You can specify `LDIF` (spacer dimension); `RS` and `RD` (source and drain sheet resistance under the spacer) for LDD devices, and `RSH` (sheet resistance of the heavily-doped diffusion). Thus, simulation properly calculates the total parasitic resistance of the LDD devices.
- `ACM=3` uses all features of `ACM=2`. Its calculations of diode parasitics take into account the sharing of source/drains, and different junction sidewall capacitances along the gate and field edges. Use the `GEO` parameter to specify source/drain sharing from the element line. See [Using an ACM=3 MOS Diode on page 707](#) for details.

Skewing of Model Parameters

As in any other Synopsys model, you can set up the BSIM2 model file for skewing to reflect the process variation. You can perform Worst-Case or Monte-Carlo analysis, based on fab statistics. For more information, see [Monte Carlo - Traditional Flow and Statistical Analysis](#) or [Monte Carlo Analysis Variation Block Flow](#) in the *HSPICE User Guide: Simulation and Analysis*.

HSPICE Optimizer

You can tie the BSIM2 model, like any other HSPICE model, into the optimizer in a Synopsys circuit simulator to fit to actual device data. An example fit appears at the end of this chapter.

Modeling Guidelines, Removing Mathematical Anomalies

Because of the somewhat arbitrary geometric and bias adjustments made in the original BSIM2 parameters, they can take on non-physical values or values that are not mathematically allowed in Berkeley SPICE 3. This can lead to illegal function arguments, program crashes, and unexpected model behavior (for example, negative conductance). You must satisfy the following guidelines and corrections at all geometries of interest, and at biases up to double the supply voltages (that is, to $V_{ds}=2 \cdot V_{DD}$, $V_{gs}=2 \cdot V_{GG}$, and $V_{bs}=2 \cdot V_{BB}$).

To avoid a drain current discontinuity at $V_{ds}=V_{dsat}$, be sure that $BI \neq 0$ if $AI0 \neq 0$.

To prevent negative g_{ds} , be sure that $ETA>0$, $MU3>0$, and $MU4<MU3 / (4 \cdot V_{DD})$. This should ensure a positive g_{ds} value at biases up to double the supply voltages. To simplify matters, set all $MU4$ parameters to zero. You can obtain reasonably good fits to submicron devices without using $MU4$ [1].

In the Level 39 MOSFET model, $U1S$ cannot become negative. A negative $U1S$ is physically meaningless, and causes negative arguments in a square root function in one of the BSIM2 equations. The $U1D$ value should be less than unity (between 0 and 1).

For reasonable V_{th} behavior, make sure that:

$$K1 - 2K2 \cdot \sqrt{PHI - V_{bs}} \geq 0$$

For the equations to make sense, the following must hold: $N > 0$, $V_{GLOW} \leq 0$, and $V_{GHIGH} \geq 0$.

The BSIM2 gate capacitance model in SPICE 3E tends to display negative C_{gs} in the subthreshold. This is due to $C_{gg} \rightarrow 0$ as $V_{gs} \rightarrow V_{th}$ by construction of the gate charge equation so that $C_{gs}=C_{gg} - C_{gd} - C_{gb}' - C_{gd} - C_{gb} \approx -C_{gb}$. Therefore, use $CAPOP=13$ (default) until UC Berkeley releases an improved BSIM2 gate capacitance model.

Modeling Example

The following is the result of fitting data from a submicron channel-length NMOS device to BSIM2. To fit this data, this example uses the Synopsys ATEM characterization software and the Synopsys simulation optimizer.

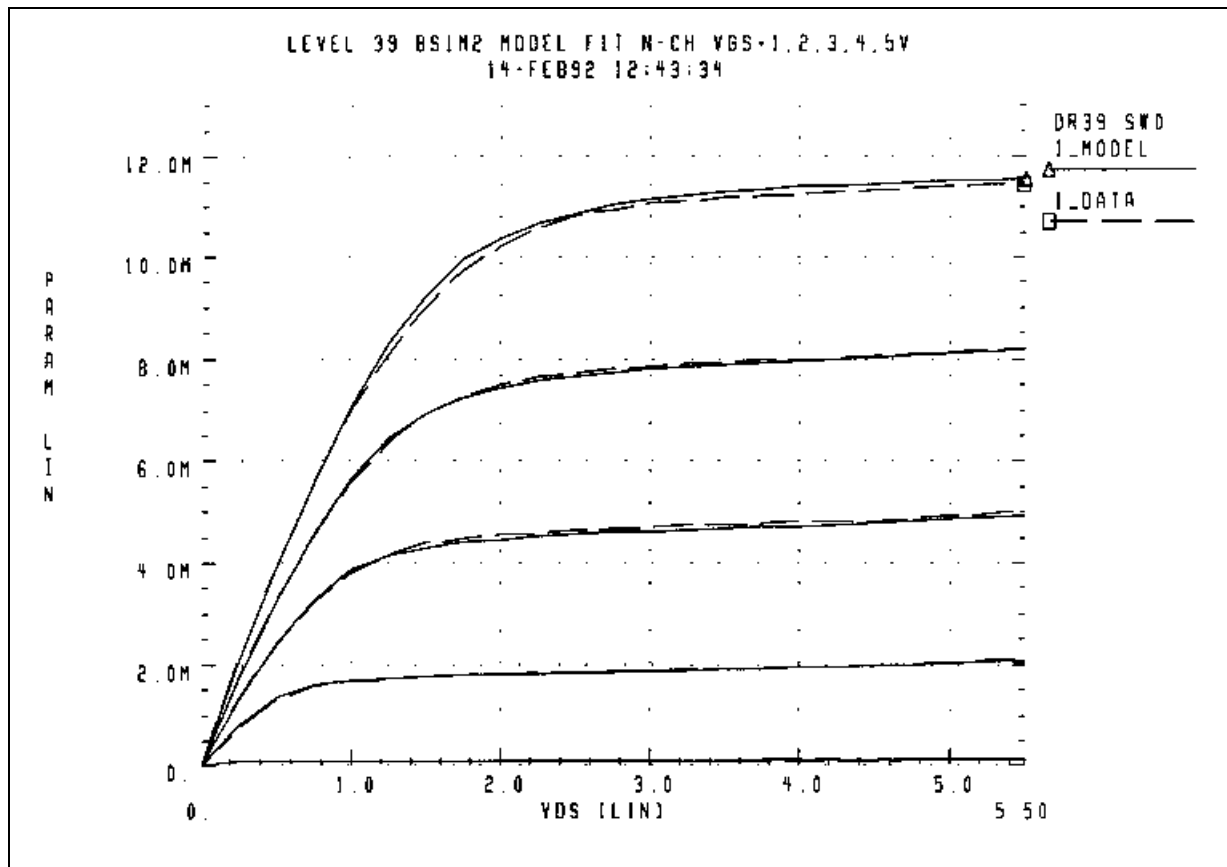


Figure 16 I_{DS} vs. V_{ds} for $V_{gs}=1, 2, 3, 4, 5V$; BSIM2 Model vs. Data

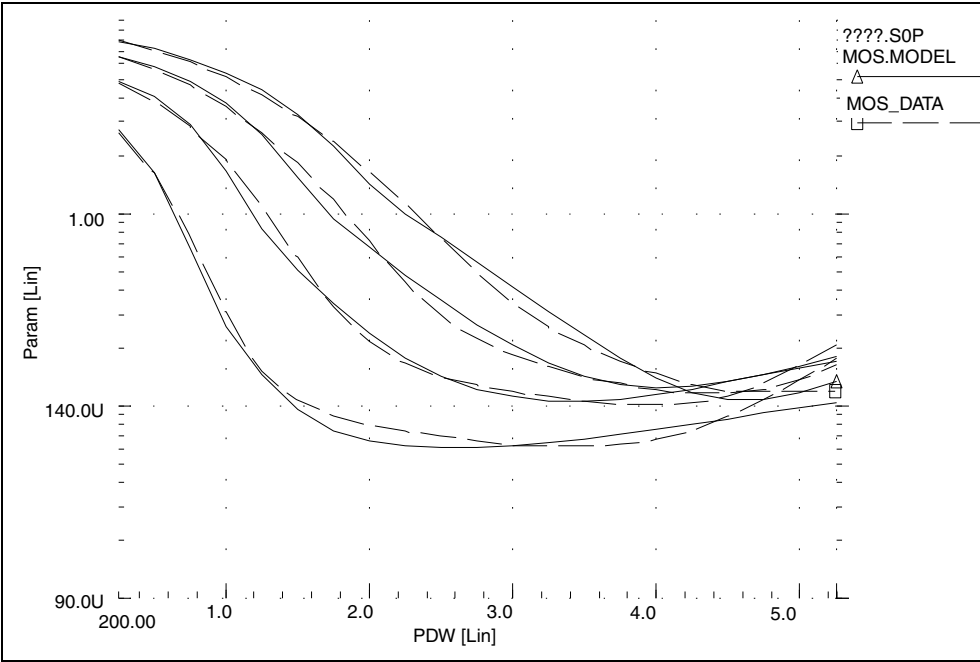


Figure 17 I_{ds} vs. V_{ds} for $V_{gs}=2, 3, 4, 5V$; BSIM2 Model vs. Data, LOG scale

Chapter 5: MOSFET Models (BSIM): Levels 13 through 39
LEVEL 39 BSIM2 Model

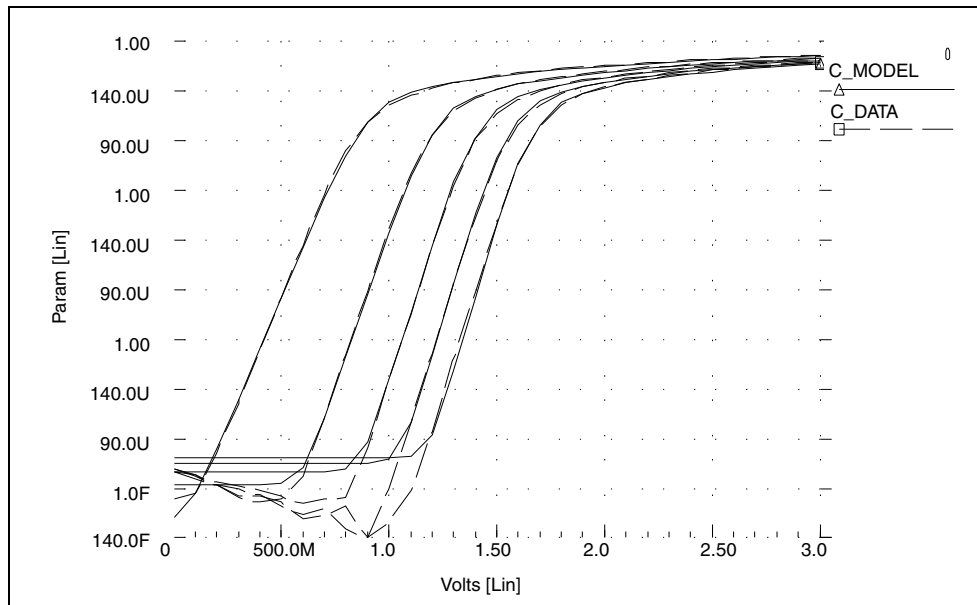


Figure 18 I_{DS} vs. V_{GS} for $V_{DS}=0.1V$, $V_{BS}=0, -1, -2, -3, -4V$, Showing Subthreshold Region; Model vs. Data

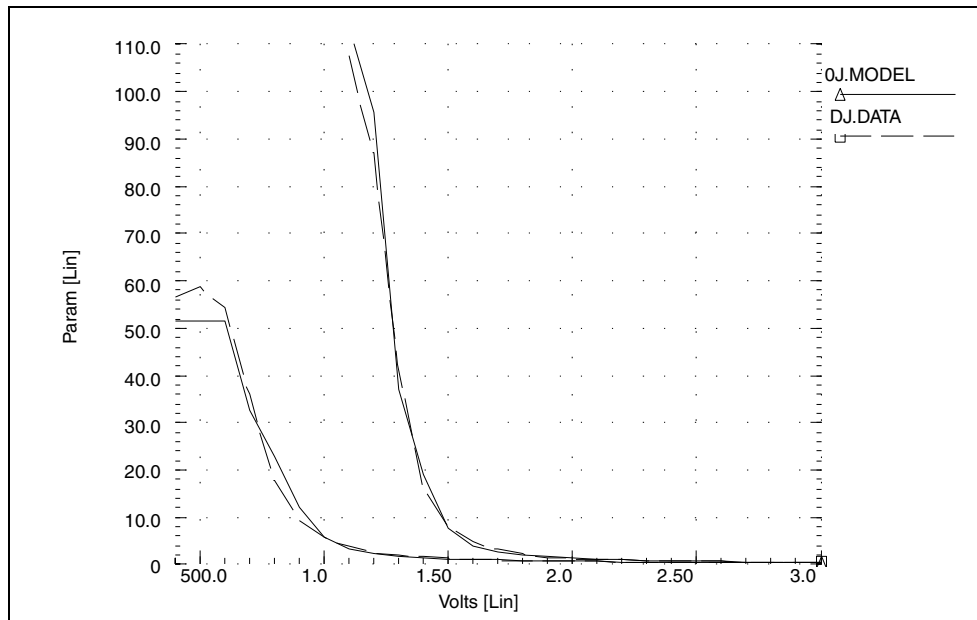


Figure 19 g_m/I_{DS} vs. V_{gs} for $V_{ds}=0.1V$, $V_{bs}=0, -2V$; BSIM2 Model vs. Data

Typical BSIM2 Model Listing

In this example, geometry sensitivities are set to zero because a fit at only one geometry has been performed. This example includes extra HSPICE parameters for LDD, temperature, and geometry.

Chapter 5: MOSFET Models (BSIM): Levels 13 through 39
LEVEL 39 BSIM2 Model

```
.MODEL NCH NMOS LEVEL=39
+ TOX=2.000000E-02 TEMP=2.500000E+01
+ VDD=5.000000E+00 VGG=5.000000E+00
+ VBB =-5.000000E+00 DL =0.000000E+00
+ DW=0.000000E+00 VGHIGH=1.270000E-01
+ LVGHIGH=0.000000E+00 WVGHIGH=0.000000E+00
+ VGLow =-7.820000E-02 LVGLow=0.000000E+00
+ WVGLOW=0.000000E+00 VFB =-5.760000E-01
+ LVFB=0.000000E+00 WVFB=0.000000E+00
+ PHI=6.500000E-01 LPHI=0.000000E+00
+ WPHI=0.000000E+00 K1=9.900000E-01
+ LK1=0.000000E+00 WK1=0.000000E+00
+ K2=1.290000E-01 LK2=0.000000E+00
+ WK2=0.000000E+00 ETA0=4.840000E-03
+ LETA0=0.000000E+00 WETA0=0.000000E+00
+ ETAB =-5.560000E-03 LETAB=0.000000E+00
+ WETAB=0.000000E+00 MU0=3.000000E+02
+ MU0B=0.000000E+00 LMU0B=0.000000E+00
+ WMU0B=0.000000E+00 MUS0=7.050000E+02
+ LMUS0=0.000000E+00 WMUS0=0.000000E+00
+ MUSB=0.000000E+00 LMUSB=0.000000E+00
+ WMUSB=0.000000E+00 MU20=1.170000E+00
+ LMU20=0.000000E+00 WMU20=0.000000E+00
+ MU2B=0.000000E+00 LMU2B=0.000000E+00
+ WMU2B=0.000000E+00 MU2G=0.000000E+00
+ LMU2G=0.000000E+00 WMU2G=0.000000E+00
+ MU30=3.000000E+01 LMU30=0.000000E+00
+ WMU30=0.000000E+00 MU3B=0.000000E+00
+ LMU3B=0.000000E+00 WMU3B=0.000000E+00
+ MU3G =-2.970000E+00 LMU3G=0.000000E+00
+ WMU3G=0.000000E+00 MU40=0.000000E+00
+ LMU40=0.000000E+00 WMU40=0.000000E+00
+ MU4B=0.000000E+00 LMU4B=0.000000E+00
+ WMU4B=0.000000E+00 MU4G=0.000000E+00
+ LMU4G=0.000000E+00 WMU4G=0.000000E+00
+ UA0=0.000000E+00 LUA0=0.000000E+00
+ WUA0=0.000000E+00 UAB=0.000000E+00
+ LUAB=0.000000E+00 WUAB=0.000000E+00
+ UB0=7.450000E-03 LUB0=0.000000E+00
+ WUB0=0.000000E+00 UBB=0.000000E+00
+ LUBB=0.000000E+00 WUBB=0.000000E+00
+ U10=0.000000E+00 LU10=7.900000E-01
+ WU10=0.000000E+00 U1B=0.000000E+00
+ LU1B=0.000000E+00 WU1B=0.000000E+00
+ U1D=0.000000E+00 LU1D=0.000000E+00
+ WU1D=0.000000E+00 N0=8.370000E-01
+ LN0=0.000000E+00 WN0=0.000000E+00
+ NB =6.660000E-01 LNB=0.000000E+00
```



```
+ WNB=0.000000E+00 ND=0.000000E+00
+ LND=0.000000E+00 WND=0.000000E+00
+ VOF0=4.770000E-01 LVOF0=0.000000E+00
+ WVOF0=0.000000E+00 VOFB =-3.400000E-02
+ LVOFB=0.000000E+00 WVOFB=0.000000E+00
+ VOFD =-6.900000E-02 LVOFD=0.000000E+00
+ WVOFD=0.000000E+00 AIO=1.840000E+00
+ LAIO=0.000000E+00 WAI0=0.000000E+00
+ AIB=0.000000E+00 LAIB=0.000000E+00
+ WAIB=0.000000E+00 BIO=2.000000E+01
+ LBI0=0.000000E+00 WBI0=0.000000E+00
+ BIB=0.000000E+00 LBIB=0.000000E+00
+ WBIB=0.000000E+00 DELL=0.000000E+00
+ WDF=0.000000E+00
```

Common SPICE Parameters

```
+ CGDO=1.000000E-09 CGSO=1.000000E-09
+ CGBO=2.500000E-11
+ RSH=3.640000E+01 JS=1.380000E-06
+ PB=8.000000E-01 PBSW=8.000000E-01
+ CJ=4.310000E-04 CJSW=3.960000E-10
+ MJ=4.560000E-01 MJSW=3.020000E-01
```

Synopsys Parameters

```
+ ACM=3 LMLT=8.500000E-01
+ WMLT=8.500000E-01
+ XL =-5.000000E-08 LD=5.000000E-08
+ XW=3.000000E-07 WD=5.000000E-07
+ CJGATE=2.000000E-10 HDIF=2.000000E-06
+ LDIF=2.000000E-07
+ RS=2.000000E+03 TRS=2.420000E-03
+ RD=2.000000E+03 TRD=2.420000E-03
+ TCV=1.420000E-03 BEX =-1.720000E+00
+ FEX =-2.820000E+00 LMU0=0.000000E+00
+ WMU0=0.000000E+00 JSW =2.400000E-12
```

References

- [1] Duster, J.S., Jeng, M.C., Ko, P. K., and Hu, C. *User's Guide for the BSIM2 Parameter Extraction Program and the SPICE3 with BSIM Implementation*. Industrial Liaison Program, Software Distribution Office, University of California, Berkeley, May 1990.

MOSFET Models (BSIM): Levels 47 through 72

Lists and describes the newest MOSFET models supported by HSPICE.

HSPICE ships hundreds of examples for your use; see [Listing of Demonstration Input Files](#) for paths to demo files.

This chapter describes seven of the newest Berkeley Short Channel IGFET (BSIM) type MOSFET models that HSPICE supports:

- [Level 47 BSIM3 Version 2 MOS Model](#)
- [Level 49 and 53 BSIM3v3 MOS Models](#)
- [Level 54 BSIM4 Model](#)
- [Level 57 UC Berkeley BSIM3-SOI Model](#)
- [Level 59 UC Berkeley BSIM3-SOI FD Model](#)
- [Level 60 UC Berkeley BSIM3-SOI DD Model](#)
- [Level 65 SSIMSOI Model](#)
- [Level 66 HSPICE HVMOS Model](#)
- [Level 70 BSIMSOI4.x Model Parameters](#)
- [Level 71 TFT Model](#)
- [Level 72 BSIM-CMG MOSFET Model](#)
- [Supported Instance Parameters, BSIM3, BSIM4, BSIM3SOI and BSIM4SOI](#)

These models are all based on models developed by the University of California at Berkeley. You can find documentation on BSIM3 and BSIM4 at this website:

<http://www.eigroup.org/cmc/cmos/default.htm>

For descriptions of older BSIM models that Synopsys supports, see [Chapter 5, MOSFET Models \(BSIM\): Levels 13 through 39](#).

Level 47 BSIM3 Version 2 MOS Model

The BSIM3 version 2.0 MOS model from UC Berkeley is available as the Synopsys Level 47 model.

Table 116 MOSFET Level 47 Model Parameters

Name	Unit	Default	Description
VTH0	V	0.7	Threshold voltage of the long channel at $V_{bs}=0$ and small V_{ds} <ul style="list-style-type: none"> ▪ 0.7 for n-channel. ▪ - 0.7 for p-channel.
K1	$V^{1/2}$	0.53	First-order body effect coefficient
K2		-0.0186	Second-order body effect coefficient
K3		80.0	Narrow width effect coefficient
K3B	1/V	0	Body width coefficient of the narrow width effect
KT1	V	-0.11	Temperature coefficient for the threshold voltage
KT2		0.022	Body bias coefficient of the threshold temperature effect
GAMMA1	$V^{1/2}$	See Level 47 Model Equations on page 411 .	Body effect coefficient, near interface
GAMMA2	$V^{1/2}$	See Level 47 Model Equations on page 411 .	Body effect coefficient in the bulk
W0	m	2.5e-6	Narrow width effect coefficient
NLX	m	1.74e-7	Lateral nonuniform doping along the channel
TOX	m	150e-10	Gate oxide thickness
XJ	m	0.15e-6	Junction depth

Table 116 MOSFET Level 47 Model Parameters

Name	Unit	Default	Description
DL	m	0.0	Channel length reduction on one side (multiplied by SCALM)
DW	m	0.0	Channel width reduction on one side (multiplied by SCALM)
NPEAK	cm ⁻³ See (8)	1.7e17	Peak doping concentration near the interface
NSUB	cm ⁻³	6.0e16	Substrate doping concentration
PHI	V	See Level 47 Model Equations on page 411.	Surface potential under strong inversion
XT	m	1.55e-7	Doping depth
VBM	V	-5.0	Maximum substrate bias
VBX	V	See Level 47 Model Equations on page 411.	V _{bs} at which the depletion width equals XT
DVT0		2.2	Short-channel effect coefficient 0
DVT1		0.53	Short-channel effect coefficient 1
DVT2	1/V	-0.032	Short-channel effect coefficient 2
U0	m ² /Vsec See (8)	0.067	Low field mobility at T=TREF <ul style="list-style-type: none"> ▪ 0.067 for n-channel ▪ 0.025 for p-channel
UA	m/V	2.25e-9	First-order mobility degradation coefficient
UA1	m/V	4.31e-9	Temperature coefficient of UA
UB	m ² /V ²	5.87e-19	Second-order mobility degradation coefficient

Chapter 6: MOSFET Models (BSIM): Levels 47 through 72

Level 47 BSIM3 Version 2 MOS Model

Table 116 MOSFET Level 47 Model Parameters

Name	Unit	Default	Description
UB1	m ² /V ²	-7.61e-18	Temperature coefficient of UB
UC	1/V	0.0465	Body bias sensitivity coefficient of mobility
UC1	1/V	-0.056	Temperature coefficient of UC
VSAT	cm/sec	8e6	Saturation velocity of the carrier at T=TREF
AT	m/sec	3.3e4	Temperature coefficient of VSAT
RDSW	ohm · μm	0.0	Source drain resistance per unit width
RDS0	ohm	0.0	Source drain contact resistance
LDD	m	0.0	Total length of the LDD region
ETA		0.3	Coefficient of the drain voltage reduction
ETA0		0.08	DIBL (Drain Induced Barrier Lowering) coefficient for the subthreshold region
ETAB	1/V	-0.07	Subthreshold region DIBL coefficient
EM	V/m	4.1e7	Electrical field in the channel above which the hot carrier effect dominates
NFACTOR		1.0	Subthreshold region swing
VOFF	V	-0.11	Offset voltage in the subthreshold region
LITL	m		Characteristic length. Default is: $LITL = \left(\frac{\epsilon_{si} T_{ox} X_j}{\epsilon_{ox}} \right)^{1/2}$
VGLOW	V	-0.12	Lower bound of the weak-strong inversion transition region
VGHIGH	V	0.12	Upper bound of the weak-strong inversion transition region

Table 116 MOSFET Level 47 Model Parameters

Name	Unit	Default	Description
CDSC	F/m ²	2.4e-4	Drain/source and channel coupling capacitance
CDSCB	F/Vm ²	0	Body coefficient for CDSC
CIT	F/m ²	0.0	Interface state capacitance
DSUB		DROUT	DIBL coefficient in the subthreshold region
PSCBE1	V/m	4.24e8	Exponent 1 for the substrate current induced body effect
PSCBE2	m/V	1.0e-5	Coefficient 2 for the substrate current induced body effect
A0		1	Bulk charge effect. Default is 4.4 for PMOS.
TNOM (TREF)	°C	25	Temperature at which simulation extracts parameters. This parameter defaults to the TNOM option, which defaults to 25° C. See 4 and 5 in Level 47 Notes on page 408 .
SUBTHMOD		2	Subthreshold model selector
SATMOD		2	Saturation model selector
KETA	1/V	-0.047	Body bias coefficient of the bulk charge effect
A1	1/V	0	First nonsaturation factor (0 for NMOS, 0.23 for PMOS)
A2		1.0	Second nonsaturation factor (1.0 for NMOS, 0.08 for PMOS)
UTE		-1.5	Mobility temperature exponent
KT1L	Vm	0	Channel length sensitivity of the temperature coefficient for the threshold voltage
UC0*	(V/m) ²		Temperature coefficient
BULKMOD		1	Bulk charge model selector

Table 116 MOSFET Level 47 Model Parameters

Name	Unit	Default	Description
XPART		1	Charge partitioning flag
VFB	V		Flat-band voltage
PVAG		0	Gate dependence of the output resistance
* UC0 has no effect on the model			

The following sections discuss these topics:

- [Using the BSIM3 Version 2 MOS Model](#)
- [Level 47 Notes](#)
- [Leff and Weff Equations for BSIM3 Version 2.0](#)
- [Level 47 Model Equations](#)

Using the BSIM3 Version 2 MOS Model

The Level 47 model uses the same model parameters for the source/drain diode current, capacitance, and resistance as used in the other supported MOS levels. The `ACM` model parameter controls the choice of source/drain equations.

The Level 47 model also uses the same noise equations as the other MOSFET model levels. The `NLEV` parameter controls the choice of noise equations.

This model, like all Synopsys simulation device models, can include parameters. You can use these parameters to model the process skew, either by worst-case corners or by Monte Carlo. For information about Worst-Case and Monte Carlo analysis, see [Worst Case Analysis](#) and [Monte Carlo Analysis](#) in the *HSPICE User Guide: Simulation and Analysis*.

Level 47 Notes

The following are usage notes regarding Level 47 MOSFETs:

1. Set `LEVEL=47` to identify the model as a BSIM3 model.

2. This model is based on BSIM3 version 2.0 from UC Berkeley. Code was received from UC Berkeley in July 1994 in the form of SPICE3e2. Changes announced in a letter from UCB September 13, 1994, have been included. DC sweeps have been checked against SPICE3e2.
3. The default setting for `CAPOP` is `CAPOP=13`, which is the BSIM1 charge-conserving capacitance model. This model does not use the BSIM3 capacitance model.
4. The Level 47 model supports the `TNOM` model parameter name as an alias for `TREF`. The conventional terminology is `TREF`, which is supported as a model parameter in all Synopsys MOS levels. Level 47 supports the `TNOM` alternative name for compatibility with SPICE3.
5. The default room temperature is 25° C in Synopsys simulators, but is 27° C in SPICE3. If you specify the BSIM3 model parameters at 27° C, add `TREF=27` to the model so that simulation correctly interprets the model parameters. To set the nominal simulation temperature to 27, add `.OPTION TNOM=27` to the netlist when you test the Synopsys model versus SPICE3.
6. The default of `DERIV` is zero, the analytical method. You can set `DERIV` to 1 for the finite difference method. Analytic derivatives in the SPICE3e2 code are not exact in some regions. Setting `DERIV=1` returns more accurate derivatives (`GM`, `GDS`, and `GMBS`), but consumes more CPU time.
7. You can select one of three ways to calculate V_{th} .
 - Using `K1` and `K2` values that you specify.
 - Using `GAMMA1`, `GAMMA2`, `VBM`, and `VBX` values that you enter in the `.MODEL` statement.
 - Using `NPEAK`, `NSUB`, `XT`, and `VBM` values that you specify.
8. You can enter the `NPEAK` and `U0` model parameters in meters or centimeters. Simulation converts `NPEAK` to cm^{-3} as follows: if `NPEAK` is greater than 1e20, simulation multiplies it by 1e-6, and converts `U0` to m^2/Vsec as follows: if `U0` is greater than 1, simulation multiplies it by 1e-4. You must enter the `NSUB` parameter in cm^{-3} units.
9. The specified value of the threshold decreases with increasing temperature for NMOS and PMOS.
10. The default value of `KT1` is -0.11. The negative sign ensures that the absolute value of the threshold decreases with increasing temperature for NMOS and PMOS.

11. You cannot set the `LITL` model parameter below a minimum value of $1.0\text{e-}9$ m to avoid a possible divide by zero error.
12. After you adjust the temperature, `VSAT` cannot go below a minimum value of $1.0\text{e}4$ m/sec to assure that it is positive after temperature compensation.
13. Seven model parameters accommodate the temperature dependencies of six temperature-dependent model variables. These parameters are `KT1` and `KT2` for `VTH`, `UTE` for `U0`, `AT` for `VSAT`, `UA1` for `UA`, `UB1` for `UB`, and `UC1` for `UC`.
14. Set up the temperature conversion between this model and SPICE3 as follows:

```
SPICE3:      .OPTION TEMP=125
             .MODEL NCH NMOS Level=8
             + TNOM=27 ...
HSPICE:      .TEMP 125
             .MODEL NCH NMOS Level=47
             + TREF=27 ...
```

15. The `SCALM` option does not affect parameters that are unique to this model, but it does affect the common MOS parameters, such as `XL`, `LD`, `XW`, `WD`, `CJ`, `CJSW`, `JS`, and `JSW`.
16. Level 47 uses the common Synopsys MOS parasitic models, which `ACM` specifies.
17. Level 47 uses the common Synopsys MOS noise models, which `NLEV` specifies.
18. You can use `DELVTO` and `DTEMP` on the element line with MOSFET Level 47.
19. The `PSCBE1` and `PSCBE2` model parameters determine the impact ionization current, which contributes to the drain-source current. Impact ionization does not contribute to the bulk current.

Leff and Weff Equations for BSIM3 Version 2.0

The standard equations for L_{eff} and W_{eff} in the Synopsys model are:

$$L_{eff} = L + XL - (2 \cdot LD)$$

$$W_{eff} = W + XW - (2 \cdot WD)$$

BSIM3 uses the following UCB SPICE3 equations:

$$L_{eff} = L - (2 \cdot DL)$$

$$W_{eff} = W - (2 \cdot DW)$$

The units for these parameters are meters with defaults of zero.

Simulation uses the standard Synopsys model equation for both cases, and accepts DL(DW) as the value for LD(WD). If you specify both LD(WD) and DL(DW) in a .MODEL statement, simulation uses the LD(WD) value.

If you specify LDAC and WDAC in the .MODEL statement, then:

$$L_{eff} = L + XL - 2 \cdot LDAC, \quad W_{eff} = W + XW - 2 \cdot WDAC$$

This model uses the LD(DL) and WD(DW) values with the RS and RD parameters for ACM>0.

Example

The following two models return the same simulation results:

```
* HSPICE style:
.MODEL n1 nmos Level=47 XL=0.1e6 LD=0.15e-6
+ SatMod=2 SubthMod=2 BulkMod=1
+ CGSO=0.3e-9 CGDO=0.3e-9 CGBO=0
* SPICE3 style:
.MODEL n2 nmos Level=47 LD=0.1e-6
+ SatMod=2 SubthMod=2 BulkMod=1
+ CGSO=0.3e-9 CGDO=0.3e-9 CGBO=0
```

Level 47 Model Equations

The following model equations are based on the BSIM3 source code:

Threshold Voltage

Model Parameters

V_{th0} , $K1$, $K2$, ϕ_s , N_{lx} , $K3$, W_0 , T_{ox} , V_{bi} , D_{vt0} , D_{vt1} ,

D_{vt2} , N_{peak} , N_{sub} , Υ_1 , Υ_2 , V_{bx} , V_{bm} , V_{bi} , X_t , $TREF$

$$V_{th} = V_{th0} + K1(\sqrt{\phi_s - V_{bs}} - \sqrt{\phi_s}) - K2V_{bs} + K1 \left(\sqrt{1 + \frac{N_{lx}}{L_{eff}} \sqrt{\frac{\phi_s}{\phi_s - V_{bs}}}} - 1 \right) \sqrt{\phi_s}$$

Chapter 6: MOSFET Models (BSIM): Levels 47 through 72

Level 47 BSIM3 Version 2 MOS Model

$$+ (K3 + K3B \cdot V_{bs}) \cdot \left(\frac{T_{ox}}{W_{eff} + W_0} \right) \phi_s - \Delta V_{th}$$

$$T_{ratio} = \frac{(TEMP + DTEMP + 273.15)}{(TREF + 273.15)}$$

$$\Delta V_{th} = \theta_{th}(L_{eff}) \cdot (V_{bi} - \phi_s)$$

$$\theta_{th}(L_{eff}) = D_{vt0} \cdot \left[\exp\left(\frac{-D_{vt1} \cdot L_{eff}}{2l_t}\right) + 2 \exp\left(\frac{-D_{vt1} \cdot L_{eff}}{l_t}\right) \right]$$

$$l_t = \sqrt{3 \cdot T_{ox} \cdot X_{dep}} \cdot (1 + D_{vt2} \cdot V_{bs})$$

$$X_{dep} = \sqrt{\frac{2 \cdot \epsilon_{si} \cdot (\phi_s - V_{bs})}{q \cdot N_{peak}}}$$

If you do not specify Phi as a model parameter, then:

$$\phi_s = 2 \cdot V_{tm} \cdot \ln\left(\frac{N_{peak}}{n_i}\right) \text{ (Npeak and } n_i \text{ in cm}^{-3}\text{)}$$

$$V_{tm} = K \cdot T / q$$

$$n_i = 1.45e10 \cdot \left(\frac{T}{300.15}\right)^{1.5} \cdot \exp(21.5565981 - Eg / (2 \cdot V_{tm}))$$

$$Eg = 1.16 - (7.02e - 4) \cdot T^2 / (T + 1108.0)$$

If you do not specify K1 and K2 as model parameters, simulation calculates them as follows:

$$K_1 = \Upsilon_2 - 2 \cdot K_2 \cdot \sqrt{\phi_s - V_{bm}}$$

$$K_2 = (\Upsilon_1 - \Upsilon_2) \cdot \frac{\sqrt{\phi_s - V_{bx}} - \sqrt{\phi_s}}{2 \cdot \sqrt{\phi_s} \cdot (\sqrt{\phi_s - V_{bm}} - \sqrt{\phi_s}) + V_{bm}}$$

$$\Upsilon_1 = \frac{\sqrt{2 \cdot q \cdot \epsilon_{si} \cdot N_{peak}}}{C_{ox}}, \Upsilon_2 = \frac{\sqrt{2 \cdot q \cdot \epsilon_{si} \cdot N_{sub}}}{C_{ox}}$$

$$V_{bx} = \phi_s - \left(\frac{q \cdot N_{peak} \cdot X_t^2}{2 \cdot \epsilon_{si}} \right)$$

If you do not specify V_{bi} as a model parameter, then:

$$V_{bi} = \frac{k \cdot T}{q} \cdot \ln \left(\frac{1.0e22 \cdot N_{peak}}{n_i^2} \right)$$

Mobility of Carrier

Model Parameters

μ_0 , U_a , U_b , U_c

$$\mu_{eff} = \frac{\mu_0}{1 + U_a \cdot \left(\frac{V_{gs} + V_{th}}{T_{ox}} \right) + U_b \cdot \left(\frac{V_{gs} + V_{th}}{T_{ox}} \right)^2 + U_c \cdot V_{bs}}$$

Drain Saturation Voltage

Model Parameters

A_0 , v_{sat} , X_j , A_1 , A_2 , R_{ds0} , R_{dsw}

R_{ds} and $Pfactor$:

$$R_{ds} = R_{ds0} + R_{dsw} / (1e6 \cdot W_{eff})$$

$$Pfactor = A_1 \cdot V_{gst} + A_2$$

If $Pfactor > 1$, simulation sets it to $Pfactor=1$.

$$V_{gst} = V_{gs} - V_{th}$$

If $R_{ds}=0$ and $Pfactor=1$, then:

$$V_{dsat} = \frac{E_{sat} \cdot L_{eff} \cdot V_{gst}}{A_{bulk} \cdot E_{sat} \cdot L_{eff} + V_{gst}}$$

For BULKMOD=1:

$$A_{bulk} = \left(1 + \frac{K1 \cdot A_0 \cdot L_{eff}}{(L_{eff} + T1) \cdot T1s \cdot 2} \right) / (1 + KETA \cdot V_{bs})$$

Chapter 6: MOSFET Models (BSIM): Levels 47 through 72

Level 47 BSIM3 Version 2 MOS Model

For BULKMOD=2:

$$A_{bulk} = \left(\frac{K1 \cdot A_0 \cdot L_{eff}}{(L_{eff} + T1) \cdot \sqrt{\phi_s} \cdot 2} \right) / (1 + KETA \cdot V_{bs})$$

$$T1 = 2 \cdot \sqrt{X_j \cdot X_{dep}}$$

For $V_{bs} \leq 0$:

$$T1s = \sqrt{\phi_s - V_{bs}}$$

For $V_{bs} \geq 0$:

$$T1s = \frac{\phi_s \cdot \sqrt{\phi_s}}{\phi_s + \frac{V_{bs}}{2}}, E_{sat} = 2 \cdot \frac{v_{sat}}{\mu_{eff}}$$

In general, V_{dsat} solves $Tmpa \cdot V_{dsat} \cdot V_{dsat} - Tmpb \cdot V_{dsat} + Tmpc = 0$:

$$V_{dsat} = (Tmpb - \sqrt{Tmpb^2 - 4 \cdot Tmpa \cdot Tmpc}) / (2 \cdot Tmpa)$$

$$Tmpa = A_{bulk} \cdot (A_{bulk} \cdot W_{eff} \cdot v_{sat} \cdot C_{ox} \cdot R_{ds} - 1 + 1/Pfactor)$$

$$Tmpb = V_{gst} \cdot (2/Pfactor - 1) + (A_{bulk} \cdot E_{sat} \cdot L_{eff}) + (3 \cdot A_{bulk} \cdot V_{gst} \cdot W_{eff} \cdot v_{sat} \cdot C_{ox} \cdot R_{ds})$$

$$Tmpc = (V_{gst} \cdot E_{sat} \cdot L_{eff}) + (V_{gst}^2 \cdot 2 \cdot W_{eff} \cdot v_{sat} \cdot C_{ox} \cdot R_{ds})$$

Linear Region

$$I_{dslin0} = \mu_{eff} \cdot C_{ox} \cdot \frac{W_{eff}}{L_{eff}} \cdot \frac{1}{1 + V_{ds} / (E_{sat} \cdot L)} \cdot \left(V_{gs} - V_{th} - A_{bulk} \cdot \frac{V_{ds}}{2} \right) \cdot V_{ds}$$

$$I_{ds} = \frac{I_{dslin0}}{1 + \frac{R_{ds} \cdot I_{dslin0}}{V_{ds}}}$$

Saturation Region

Model Parameters

$litl$, eta , L_{dd} , E_m , D_{rout} , P_{clm} , P_{dibl1} , P_{dibl2} , P_{scbe1} , P_{scbe2}

V_{asat} and F_{vag} :

$$V_{asat} = \frac{E_{sat} \cdot L_{eff} + V_{dsat} + 2R_{ds} \cdot v_{sat} \cdot C_{ox} \cdot W_{eff} \cdot \left(V_{gst} - \frac{A_{bulk} \cdot V_{dsat}}{2} \right)}{2 / Pfactor - 1 + R_{ds} \cdot v_{sat} \cdot C_{ox} \cdot W_{eff} \cdot A_{bulk}}$$

$$F_{vag} = 1 + \frac{P_{vag} \cdot V_{gst}}{E_{sat} \cdot L_{eff}}$$

Early Voltage, satMod=1

$$V_A = V_{asat} + F_{vag} \cdot \left(\frac{1 + eta \cdot \frac{L_{dd}}{litl}}{P_{clm} \cdot A_{bulk}} \right) \cdot \left(\frac{(A_{bulk} \cdot E_{sat} \cdot L_{eff} + V_{gst} - \lambda \cdot (V_{ds} - V_{dsat})) \cdot (V_{ds} - V_{dsat})}{E_{sat} \cdot litl} \right)$$

$$\lambda = \frac{A_{bulk} \cdot E_{sat} \cdot L_{eff} + (V_{gst})}{2 \cdot litl \cdot E_m}$$

Early Voltage, satMod=2

$$V_A = V_{asat} + F_{vag} \cdot U_{vds} \cdot \left(\frac{1}{V_{aclm}} + \frac{1}{V_{adibl}} \right)^{-1}$$

$$U_{vds} = 1 + eta \cdot \frac{L_{dd}}{litl}$$

$$V_{aclm} = \frac{1}{P_{clm}} \cdot \frac{A_{bulk} \cdot E_{sat} \cdot L_{eff} + V_{gst}}{A_{bulk} \cdot E_{sat} \cdot litl} \cdot (V_{ds} - V_{dsat})$$

$$V_{adibl} = \frac{1}{\theta_{rout}} \cdot \left[(V_{gs} - V_{th}) - \left(\frac{1}{A_{bulk} \cdot V_{dsat}} + \frac{1}{V_{gst}} \right)^{-1} \right]$$

$$\theta_{rout} = P_{dibl1} \cdot \left[\exp\left(\frac{-D_{rout} \cdot L_{eff}}{2 \cdot l_t}\right) + 2 \exp\left(\frac{-D_{rout} \cdot L_{eff}}{l_t}\right) \right] + P_{dibl2}$$

Chapter 6: MOSFET Models (BSIM): Levels 47 through 72

Level 47 BSIM3 Version 2 MOS Model

$$V_{ahce} = \left[\frac{P_{scbe2}}{L_{eff}} \cdot \exp\left(\frac{-P_{scbe1} \cdot litl}{V_{ds} - V_{dsat}}\right) \right]^{-1}$$

Drain Current

$$I_{dsat} = W_{eff} \cdot v_{sat} \cdot C_{ox} \cdot (V_{gs} - V_{th} - A_{bulk} \cdot V_{dsat}) \cdot Pfactor$$

$$Pfactor = A_1 \cdot V_{gst} + A_2$$

$$I_{ds} = I_{dsat} \cdot \left(1 + \frac{V_{ds} - V_{dsat}}{V_A}\right) \cdot \left(1 + \frac{V_{ds} - V_{dsat}}{V_{ahce}}\right)$$

Subthreshold Region

Model Parameters

$$Nfactor, C_{dsc}, C_{dscb}, V_{off}, C_{it}, D_{sub}, eta_0, eta_b$$

n and DIBL:

$$n = 1 + \frac{Nfactor \cdot 1.034e-10}{X_{dep} \cdot C_{ox}} + \frac{(C_{dsc} + C_{dscb} \cdot V_{bs}) \cdot \left[\exp\left(\frac{-L_{eff}}{2 \cdot l_t}\right) + 2 \exp\left(\frac{-L_{eff}}{l_t}\right) \right] + C_{it}}{C_{ox}}$$

$$DIBL = (eta_0 + eta_b \cdot V_{bs}) \cdot \left[\exp\left(\frac{-D_{sub} \cdot L_{eff}}{2 \cdot l_{t0}}\right) + 2 \exp\left(\frac{-D_{sub} \cdot L_{eff}}{l_{t0}}\right) \right]$$

$$l_{t0} = \sqrt{3 \cdot T_{ox} \cdot X_{dep0}}, X_{dep0} = \sqrt{\frac{2 \cdot \epsilon_{si} \cdot \phi_s}{q \cdot N_{peak}}}$$

subthMod=0

$$I_{ds} = g_m = g_{ds} = g_{mb} = 0$$

subthMod=1

$$I_{ds} = \frac{I_{limit} \cdot I_{exp}}{I_{limit} + I_{exp}} \cdot \left[1 - \exp\left(\frac{-V_{ds}}{V_{tm}}\right) \right],$$

$$I_{limit} = \frac{9}{2} \cdot u0 \cdot \sqrt{\frac{q \epsilon_{si} \cdot N_{peak}}{2 \cdot \phi_s}} \cdot \frac{W_{eff}}{L_{eff}} \cdot V_{tm}^2$$

$$I_{exp} = u0 \cdot \sqrt{\frac{q \cdot \epsilon_{si} \cdot N_{peak}}{2 \cdot \phi_s}} \cdot \frac{W_{eff}}{L_{eff}} \cdot V_{tm}^2 \cdot \exp\left(\frac{V_{gs} - V_{th} - V_{off} + DIBL \cdot V_{ds}}{n \cdot V_{tm}}\right)$$

subthMod=2

$$I_{ds} = u0 \cdot \sqrt{\frac{q \cdot \epsilon_{si} \cdot N_{peak}}{2 \cdot \phi_s}} \cdot \frac{W_{eff}}{L_{eff}} \cdot V_{tm}^2 \cdot \left[1 - \exp\left(\frac{-V_{ds}}{V_{tm}}\right) \right] \cdot \exp\left(\frac{V_{gs} - V_{th} - V_{off} + DIBL \cdot V_{ds}}{n \cdot V_{tm}}\right)$$

Transition Region (for subthMod=2 only)**Model Parameters**

$$V_{gshigh}, V_{gslow}$$

$$I_{ds} = (1-t)^2 \cdot I_{dslow} + 2 \cdot (1-t) \cdot t \cdot I_p + t^2 \cdot I_{dshigh}$$

$$t = \left(\frac{V_p - V_{gslow}}{V_{gslow} - 2 \cdot V_p + V_{gshigh}} \right) \cdot \left(\sqrt{1 + \frac{(V_{gslow} - 2 \cdot V_p + V_{gshigh})(V_{gs} - V_{th} - V_{gslow})}{(V_p - V_{gslow})^2}} - 1 \right)$$

$$V_p = \frac{(g_{mhigh} \cdot V_{gshigh} - g_{mlow} \cdot V_{gslow}) - (I_{dshigh} - I_{dslow})}{g_{mhigh} - g_{mlow}}$$

$$I_p = I_{dslow} + g_{mlow} \cdot (V_p - V_{gslow})$$

Temperature Compensation

Model Parameters

A_p , U_{a1} , U_{b1} , U_{c1} , $KT1$, $KT2$, UTE

$$V_{th}(temp) = V_{th}(tref) + (KT1 + KT2 \cdot V_{bs}) \cdot (T_{ratio} - 1)$$

$$u0(temp) = u0(tref) \cdot (T_{ratio})^{UTE}$$

$$V_{sat}(temp) = V_{sat}(tref) - A_t \cdot (T_{ratio} - 1)$$

$$U_a(temp) = U_a(tref) + U_{a1} \cdot (T_{ratio} - 1)$$

$$U_b(temp) = U_b(tref) + U_{b1} \cdot (T_{ratio} - 1)$$

$$U_c(temp) = U_c(tref) + U_{c1} \cdot (T_{ratio} - 1)$$

PMOS Model

In the following example of a PMOS model for the Level 47 MOSFET, V_{TH0} is negative.

```
.model pch PMOS Level=47
+ Tnom=27.0
+ Npeak=1.5E+23 Tox=7.0E-09 Xj=1.0E-07
+ dl=0.2E-06 dw=-0.1E-06
+ SatMod=2 SubthMod=2 BulkMod=1
+ Vth0=-.8 Phi=.7 K1=.5 K2=0.03 K3=0
+ Dvt0=48 Dvt1=.6 Dvt2=-5e-4
+ Nlx=0 W0=0
+ Vsat=9E6 Ua=1E-09 Ub=0 Uc=-3E-02
+ Rds0=180 Rdsw=0 U0=7E-03
+ A0=.87
+ Voff=-.07 NFactor=1.5 Cit=-3E-05
+ Cdsc=6E-02 Vglow=-.12 Vghigh=.12
+ Pclm=77 Pdibl1=0 Pdibl2=2E-011
+ Drout=0 Pscbe1=0 Pscbe2=1E-28
+ Eta=0 Litl=4.5E-08
+ Em=0 Ldd=0
+ kt1=-.3 kt2=-.03
+ At=33000
+ Ua1=4E-09 Ub1=7E-18 Uc1=0
```

Level 49 and 53 BSIM3v3 MOS Models

The Synopsys Level 49 and Level 53 models are based on the BSIM3v3 MOS model from UC Berkeley.

- Level 49 is an HSPICE-enhanced version of BSIM3v3. Level 49 maintains compliance with the UC Berkeley release of BSIM3v3 with the following three exceptions:
 - Default parameter values—To eliminate differences in default parameter values, Level 49 explicitly assigns the `CAPMOD` and `XPART` parameters, and sets `ACM=10`. In addition, the default in Level=53 for `XPART` is “0” whereas in Level=49 it is “1”.
 - Parameter range limits—Provides parameter range limits that are identical to that of the Berkeley release. Differences occur only in the severity of the warning for five parameters. Level 49 issues a warning that the model exceeded the parameter range, but continues with the simulation.
 - However, the Berkeley release issues a fatal error, and aborts the simulation. These five parameters are `NGATE`, `DVT1W`, `DVT1`, `DSUB`, and `DROUT`. (See [Parameter Range Limits on page 459](#) for more details.)
 - Improvements in numerical stability—Provides improvements in numerical stability. In most practical situations, these improvements do not affect compliance with the Berkeley release, but improve the convergence and the simulation time.
- Level 53 maintains full compliance with the Berkeley release, including numerically-identical model equations, identical parameter default values, and identical parameter range limits.
- Level 49 and 53 both support the following instance parameters, along with the `DELVTO` instance parameter for local mismatch and NBTI (negative bias temperature instability) modeling:
 - `MULU0`, low-field mobility (`U0`) multiplier. Default=1.0.
 - `MULUA`, first-order mobility degradation coefficient (`UA`) multiplier.
 - `MULUB`, second-order mobility degradation coefficient (`UB`) multiplier.

Both Levels 49 and 53 support a superset of model parameters that include HSPICE-specific parameters. For Level 53, in all cases, HSPICE-specific parameters default to OFF. The single exception in Level 49 is that `ACM` defaults to 0. To achieve Level 49 compliance with Berkeley BSIM3v3, set `ACM=10`.

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Level 49 and 53 BSIM3v3 MOS Models

If you set any of the following parameter values for MOSFET Level 49 and 53, simulation reports a warning:

- $L_{\text{eff}} \leq 5\text{e-}8$
- $W_{\text{eff}} \leq 1\text{e-}7$
- $L_{\text{eff}}\text{CV} \leq 5\text{e-}8$
- $W_{\text{eff}}\text{CV} \leq 1\text{e-}7$

Simulation aborts if you set L_{eff} or $W_{\text{eff}} \leq 0.0$.

For Level=49 and 53, LINT is used in the ACM model to calculate R_{Deff} and R_{Seff} for BSIM3v3 (LD gets the LINT value).

The following sections discuss these topics:

- [Selecting Model Versions](#)
- [Version 3.2 Features](#)
- [Version 3.3 Features](#)
- [Enhanced Diode Model DC Equations with HSPICE BSIM3](#)
- [Nonquasi-Static \(NQS\) Model](#)
- [HSPICE Junction Diode Model and Area Calculation Method](#)
- [TSMC Diode Model](#)
- [BSIM3v3 STI/LOD](#)
- [BSIM3v3 WPE Model](#)
- [BSIM3v3 \$I_g\$ Model](#)
- [Charge Models](#)
- [Printback](#)
- [Mobility Multiplier](#)
- [Using BSIM3v3](#)
- [Level 49, 53 Model Parameters](#)
- [Parameter Range Limits](#)
- [Level 49, 53 Equations](#)
- [.MODEL CARDS NMOS Model](#)
- [PMOS Model](#)

Selecting Model Versions

Recommended BSIM3v3 Version

The recommended BSIM3v3 model specification is `LEVEL=49`, `VERSION=3.3.0`. This version provides the most stable and up-to-date representation of the UCB BSIM3v3 model.

However, do not change the `VERSION` specification in existing model cards without consulting the foundry or model extraction group that created the model cards.

See [Version 3.3 Features](#) for a description of improvements over V. 3.2.4.

[Table 117](#) lists the available BSIM3v3 models and their release dates from UC Berkeley and the equivalent HSPICE versions.

Table 117 Parameter Settings for Berkeley Releases, MOSFET Levels 49/53

Berkeley Release	Version	HSPVER
Version 3.3.0 (July, 2005)	3.3.0	06.03
Version 3.2.2 (April 20, 1999)	3.22	99.2
	3.23	01.4
	3.2.4	02.2
Version 3.2.1 (April 20, 1999)	3.21	99.2
Version 3.2 (June 16, 1998)	3.2	98.2
Version 3.1 with June 1998 bug fixes	3.1	98.2
Version 3.1 (December 1996)	3.1	98.0
Version 3.0 with June 1998 bug fixes	3.0	98.2
Version 3.0 (October 1995)	3.0	98.0

As of the 99.2 release, there are multiple BSIM3v3 releases from Berkeley and several Level 49 releases. For additional release information from the UCB group, see the BSIM3 home page:

<http://www-device.EECS.Berkeley.EDU/~bsim3/>

To minimize confusion and maintain backward compatibility, you can select the `VERSION` and `HSPVER` model parameters. `VERSION` selects the Berkeley

Chapter 6: MOSFET Models (BSIM): Levels 47 through 72

Level 49 and 53 BSIM3v3 MOS Models

release version; HSPVER selects the Synopsys release version. For example, HSPVER=97.2 and VERSION=3.1 reproduce results from HSPICE 97.2 using the BSIM3 Version 3.1 model. For detailed discussion of how HSPVER relates to the UCB VERSION, see [Using BSIM3v3 on page 442](#).

HSPVER defaults to the current release that you are using. The VERSION model parameter selects among the various Berkeley releases of BSIM3v3 as follows:

- Version 3.0 Berkeley release (October 30, 1995) default for HSPICE96.1,96.2,96.3.

Simulation invokes this version if you specify VERSION=3.0 and HSPVER=98.0. To invoke the Synopsys model version that most accurately represents the Berkeley release of October 1995, specify the VERSION=3.0 and HSPVER=98.0 parameters.
- Version 3.1 Berkeley (December 9, 1997) default for HSPICE97.1,97.2,97.4.

Simulation invokes this version if you specify VERSION=3.1 or 3.11 and HSPVER=98.0. To invoke the Synopsys model version that most accurately represents the Berkeley release of December 1996, specify the VERSION=3.1 or 3.11 and HSPVER=98.0 parameters.
- Berkeley Version 3.0, 3.1 bug fixes. Berkeley corrected several Version 3.0 and 3.1 bugs in the June, 1998 release. These fixes are incorporated into HSPICE98.2, which simulation uses if you specify VERSION=3.0 or VERSION=3.1 and HSPVER=98.2. As a result of bug fixes, you might notice some differences between Version 3.0/3.1 in HSPICE98.2 and previous Version 3.0/3.1 releases. Notably, differences occur if you specify PD and PS perimeter factors that are less than W_{eff} ($PD, PS < W_{eff}$ no longer clamp to W_{eff} in Version 3.1) and if DLC and LINT are not identical ($L_{eff}CV$ calculation bug in Versions 3.0 and 3.1).

For a complete list of bug fixes, see the BSIM3 web site:

<http://www-device.eecs.berkeley.edu/~bsim3>

Note: Version 3.11 was introduced in HSPICE97.4. This version represents Berkeley Version 3.1 (Dec., 1996) with HSPICE bug fixes. This model maintains backward compatibility. Starting with HSPICE98.2, Version 3.1 and 3.11 are identical, and represent Version 3.1 with Berkeley June, 1998 bug fixes.

- Version 3.2 Berkeley release (June 16, 1998). Simulation invokes this version if you specify `VERSION=3.2` and `HSPVER=98.2`.
- Version 3.2.1 Berkeley release (April 20, 1999). Simulation invokes this version if you specify `VERSION=3.21` and `HSPVER=99.2`.
- Version 3.2.2 Berkeley release (April 20, 1999). Simulation invokes this version if you specify `VERSION=3.22` and `HSPVER=99.2`.
- For the latest HSPICE improvements, use `VERSION=3.3.0` and `HSPVER=06.03`.

Note: Versions 3.2.1 and 3.2.2 are identical, except BSIM3v3.2.1 uses a bias-dependent V_{fb} and BSIM3v3.2.2 uses a bias-independent V_{fb} for the `CAPMOD=1` and `2` capacitance models. Versions 3.2.3 and 3.2.4 provide various model fixes, compared to Version 3.2.2.

Version 3.2 Features

In June 1998, Berkeley released BSIM3 Version 3.2, which includes the following new features:

- A new intrinsic capacitance model, `CAPMOD=3`, includes finite charge layer thickness effects; `CAPMOD` now defaults to 3 (new parameters: `CAPMOD=3`, `ACDE`, and `MOIN`).
- Improved modeling of C-V characteristics at the weak-to-strong inversion transition (new parameters: `NOFF` and `VOFFCV`).
- V_{th} dependence on T_{ox} (new parameter: `TOXM`).
- Flatband voltage parameter more accurately models different gate materials (new parameter: `VFB`).
- Improved substrate current scalability with channel length (new parameter: `APLHA1`).
- Restructured nonquasi-static (NQS) model includes pole-zero analysis and bug fixes. `NQSMOD` is a BSIM3 element parameter. HSPICE supports the model (but not the element) parameter.
- Junction diode model temperature dependence (new parameters: `TCJ`, `TCJSW`, `TCJSWG`, `TPB`, `TPBSW`, and `TPBSWG`).
- Adjustable current limiting in the junction diode current model (new parameter: `IJTH`).

Chapter 6: MOSFET Models (BSIM): Levels 47 through 72

Level 49 and 53 BSIM3v3 MOS Models

- Use C-V inversion charge equations ($CAPMOD=0,1,2,3$) to calculate the thermal noise if $NOIMOD=2$ or 4.
- Eliminated the small negative capacitance values (C_{gs} and C_{gd}) in the accumulation-depletion regions.
- Separate set of length/width dependence parameters for the CV model (LLC , LWC , $LWLC$, WLC , WWC , and $WWLC$ parameters).
- Additional parameter checking.
- Bug fixes.

Note: If you use the defaults for all new Version 3.2 parameters, Version 3.2 and Version 3.1 (with June, 1998 bug fixes) return identical DC results. However, transient and AC results generally differ. This discrepancy arises only from differences in the flatband voltage calculations used in the intrinsic charge/capacitance models. These differences occur in all $CAPMOD$ models 1-3.

- Level 53 resets $HSPVER < 98.0$ to 98.0.
- $HSPVER < 98.2$ resets to 98.2 if $VERSION \geq 3.2$ for Levels 49/53.
- Version 3.0, 3.1, and 3.11 in HSPICE do not support $NQSMOD$ and $CAPMOD=3$. Only Version 3.2 supports them.
- Version 3.24 added R_{ds} noise to the thermal noise model. Simulation smooths out the unified flicker noise, from the linear region to the saturation region. You might need to re-extract the parameters for the unified flicker noise model.

For more information about the Berkeley releases, see the BSIM3 web site:

<http://www-device.eecs.berkeley.edu/~bsim3>

Version 3.3 Features

In July 2005, Berkeley released BSIM3 Version 3.3, which includes the following new features:

- A new small-signal AC charge-deficit ACNQS model that enables the NQS effect in AC simulation. This can be turned on by setting `acnqsMod=1` and off by setting `acnqsMod=0`.
- A new channel thermal noise model “SPICE2new” that the thermal noise coefficient varies smoothly between 4 to $8/3$ as the device moves from a linear to a saturation region. The new `noiMod` model flags are:
 - `noiMod=5`: Flicker noise model—SPICE2; Thermal noise model—SPICE2new
 - `noiMod=6`: Flicker noise model—BSIM3v3; Thermal noise model—SPICE2new
- Addition of a `LINTNOI` parameter that introduces an offset to the length reduction parameter (`Lint`) to improve the accuracy of the flicker noise model.
- Changed the `Rds0` source drain current contact resistance check model.
- Fixed bugs in BSIM3V3.2.4.

For more information about the Berkeley releases, see the BSIM3 web site:
<http://www-device.eecs.berkeley.edu/~bsim3>

Enhanced Diode Model DC Equations with HSPICE BSIM3

BSIM3 diode IV equations, considering carrier recombination and trap-assisted tunneling current to improve the `Ioff`-related value. This section describes the use model for this enhancement.

Usage Model and Syntax

The model parameter `bsim4diode` invokes the feature. In addition, 30 related model parameters are also added for this enhancement: `jtss`, `jtsd`, `jtssws`, `jtsswd`, `jtsswgs`, `jtsswgd`, `njts`, `njtssw`, `njtsswg`, `xtss`, `xtsd`, `xtssws`, `xtsswd`, `xtsswgs`, `xtsswgd`, `tnjts`, `tnjtssw`, `tnjtsswg`, `vtss`, `vtsd`, `vtssws`, `vtsswd`, `vtsswgs`, `vtsswgd`, `njtssd`, `njtsswd`, `njtsswgd`, `tnjtssd`, `tnjtsswd`, `tnjtsswgd`. This diode model is only available under `AMC=12` for version ≥ 3.2 .

```
.model nch nmos level=49 ...
+ bsim4diode=1 acm=12 version=3.2....
```

Equations

These equations come from BSIM4.

Chapter 6: MOSFET Models (BSIM): Levels 47 through 72

Level 49 and 53 BSIM3v3 MOS Models

$$\begin{aligned}
 I_{bs_total} = & I_{bs} - W_{effcj} \cdot JTSSWGS(T) \cdot \left(e^{\frac{-V_{bs}}{NJTSSWG(T) \cdot V_{tm0}} \cdot \frac{VTSSWGS}{VTSSWGS - V_{bs}}} - 1 \right) \\
 & - P_{s_eff} \cdot JTSSWS(T) \cdot \left(e^{\frac{-V_{bs}}{NJTSSW(T) \cdot V_{tm0}} \cdot \frac{VTSSWS}{VTSSWGS - V_{bs}}} - 1 \right) \\
 & - A_{s_eff} \cdot JTSS(T) \cdot \left(e^{\frac{-V_{bs}}{NJTS(T) \cdot V_{tm0}} \cdot \frac{VTSS}{VTSS - V_{bs}}} - 1 \right) \\
 I_{bd_total} = & I_{bd} - W_{effcj} \cdot JTSSWGD(T) \cdot \left(e^{\frac{-V_{bd}}{NJTSSWG(T) \cdot V_{tm0}} \cdot \frac{VTSSWGD}{VTSSWGS - V_{bd}}} - 1 \right) \\
 & - P_{d_eff} \cdot JTSSWD(T) \cdot \left(e^{\frac{-V_{bd}}{NJTSSW(T) \cdot V_{tm0}} \cdot \frac{VTSSWD}{VTSSWD - V_{bd}}} - 1 \right) \\
 & - A_{s_eff} \cdot JTSD(T) \cdot \left(e^{\frac{-V_{bd}}{NJTS(T) \cdot V_{tm0}} \cdot \frac{VTSS}{VTSD - V_{bd}}} - 1 \right)
 \end{aligned}$$

where

$$JTSSWGS(T) = JTSSWGS \cdot e^{\frac{XTSSWGS \cdot \frac{Eg0}{V_{tm} \cdot \frac{Temp}{Tnom} - 1}}{}}$$

$$JTSSWS(T) = JTSSWS \cdot e^{\frac{XTSS \cdot \frac{Eg0}{V_{tm} \cdot \frac{Temp}{Tnom} - 1}}{}}$$

$$JTSS(T) = JTSS \cdot e^{\frac{XTSSWGS \cdot \frac{Eg0}{V_{tm} \cdot \frac{Temp}{Tnom} - 1}}{}}$$

$$JTSSWGD(T) = JTSSWGD \cdot e^{\frac{XTSSWGD \cdot \frac{Eg0}{V_{tm} \cdot \frac{Temp}{Tnom} - 1}}{}}$$

$$JTSSWD(T) = JTSSWD \cdot e^{\frac{XTSSWD \cdot \frac{Eg0}{V_{tm} \cdot \frac{Temp}{Tnom} - 1}}{}}$$

$$JTSSTD = JTSSTD \cdot e^{\frac{XTSD \cdot \frac{Eg0}{V_{tm} \cdot \frac{Temp}{Tnom} - 1}}{}}$$

$$NJTSSWG(T) = NJTSSWG \cdot \left[1 + TNJTSSWG \cdot \left(\frac{Temp}{Tnom} - 1 \right) \right]$$

$$NJTSSW(T) = NJTSSW \cdot \left[1 + TNJTSSW \cdot \left(\frac{Temp}{Tnom} - 1 \right) \right]$$

$$NJTS(T) = NJTS \cdot \left[1 + TNJTS \cdot \left(\frac{Temp}{Tnom} - 1 \right) \right]$$

Notes:

These notes apply for this upgrade:

1. The BSIM3 model does not have BSIM4-like equations for Aseff/ADeff/Pseff/Pdeff equations. In the above equations, they are replaced by
->BSIM3sourceArea, ->BSIM3drainArea,
->BSIM3sourcePerimeter, and ->BSIM3drainPerimeter.
2. Model parameter JTWEFF and related equations are not implemented for BSIM3.
3. Eg0-related model parameters including MTRLMOD and BG0SUB / BGASUB / BGBSUB are not implemented for BSIM3.

Nonquasi-Static (NQS) Model

You can also select the Berkeley NonQuasi-Static (NQS) model for Levels 49 and 53. This model provides a first-order correction to the quasi-static charge models. See M.Chan, K.- Y. Hui, C. Hu, and P.-K. Ko, IEEE Trans. Electron Devices, vol. ED-45, pp.834-841, 1998.

The Level 49/53 MOSFET model supports only the model parameter implementation.

To invoke the NQS model, specify the `NQSMOD=1` parameter in the model card. You can use `NQSMOD` with any of the `CAPMOD` Levels (0-3) but only with Version 3.2. Version 3.0 and 3.1 do not support NQS.

HSPICE Junction Diode Model and Area Calculation Method

You can use two junction diode models with both Levels 49 and 53: the HSPICE junction model and the Berkeley junction model.

- For the HSPICE junction model, specify the `ACM=0,1,2`, or `3` model parameter value.
- For the Berkeley junction model, specify `ACM=10,11,12`, or `13`.

The default `ACM` value is `0` for Levels 49 or `10` for Level 53. For the junction current, junction capacitance, and parasitic resistance equations corresponding to `ACM=0,1,2,3` see [MOSFET Diode Models on page 701](#).

Set `ACM=10,11,12`, or `13` to enable the Berkeley junction diodes and to add parasitic resistors to the MOSFET. The parasitic resistor equations for `ACM=10-13` correspond to the `ACM=0-3` parasitic resistor equations. `ACM=10-13` all use the Berkeley junction capacitance model equations:

```
(Bulk-source capacitance)
if (Ps >Weff)
    Cbs=AS * Cjbs + (PS - Weff) * Cjbssw + Weff *
    Cjbsswg
else
    Cbs=AS * Cjbs + PS * Cjbsswg
```

The `AS` and `PS` area and perimeter factors default to `0`, if you do not specify them on the element line.

```

if (Vbs < 0)
    Cjbs=Cj * (1 - (Vbs/Pb)) -Mj
    Cjbssw=Cjsw * (1 - (Vbs/Pbsw))
-Mjsw

    Cjbsswg=Cjswg * (1 - (Vbs/Pbswg)) -Mjswg
else
    Cjbs=Cj * (1 + Mj * (Vbs/Pb))
    Cjbssw=Cjsw * (1 + Mjsw * (Vbs/Pbsw))
    Cjbsswg=Cjswg * (1 + Mjswg * (Vbs/Pbswg))

```

Bulk-drain equations are analogous. ACM=10,11,12,13 do not use the HSPICE equations for AS, PS, AD, and PD. In accordance with the BSIM3v3 model, the default values for these area and perimeter factors are zero. To invoke the HSPICE calculations for AS, PS, AD, and PD, specify the CALCACM=1 model parameter.

Note: Simulation invokes CALCACM only if ACM=12. The calculations used in ACM=10, 11, and 13 are not consistent with the Berkeley diode calculations.

CALCACM=1 and ACM=12 invoke the following area and perimeter calculations:

If you do not specify AD on the element line:

```

    AD=2 * HDIFeff * Weff
else:
    AD=AD * WMLT^2

```

If you do not specify AS on the element line:

```

    AS=2 * HDIFeff * Weff
else:
    AS=AS * WMLT^2

```

If you do not specify PS on the element line:

```

    PS=4 * HDIFeff + 2 * Weff
else:
    PS=PS * WMLT

```

If you do not specify PD on the element line:

```

    PD=4 * HDIFeff + 2 * Weff
else:
    PD=PD * WMLT

```

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Level 49 and 53 BSIM3v3 MOS Models

Note: W_{eff} is not the same W_{eff} used in the BSIM3v3, and Levels 49 and 53 I-V, C-V model equations.

The preceding equations use the following simple forms:

$$W_{\text{eff}} = W * WMLT + XW$$
$$HDIF_{\text{eff}} = HDIF * WMLT$$

Parameter	Description
W	Width specified on the element line
HDIF	Heavy diffusion length specified in the model card
WMLT	Shrink factor specified in the model card
XW	Etch/mask effect factor specified in the model card

Note: These equations ignore the *SCALM*, *SCALE*, and *M* factor effects. See [Using an ACM=2 MOS Diode on page 712](#) (ACM=2) for further details.

Reverse Junction Breakdown Model

Starting with HSPICE version 2009.09 HSPICE MOSFET Level 49-53 (BSIM Level 3.2 or later) supports the Reverse Junction Breakdown model (introduced with BSIM4.6.4). This functionality uses use similar diode model equations as for BSIM4.6.4 DIOMOD=2. Refer to Equation (11.5) of the BSIM4.6.4 manual for details. Note that the equation for forward biased region is affected accordingly.

Parameter	Default	Description
breakmod	0 (off)	Flag to turn on/off reverse junction breakdown model, set to 1 to turn on
bvs	10 (V)	Source diode breakdown voltage
bvd	bvs	Drain diode breakdown voltage

Parameter	Default	Description
ijthsrev	0.1 (A)	Reverse source diode forward limiting current
ijthdrev	ijthsrev	Reverse drain diode forward limiting current
xjbvs	1.0 (no unit)	Fitting parameter for source diode breakdown current
xjbvd	xjbvs	Fitting parameter for drain diode breakdown current

If the above parameters are less than or equal to zero, the parameters are reset to 0.0 and warnings are issued as follows:

- If (bvs \leq 0.0), "bvs reset to 0.0".
- If (bvd \leq 0.0), "bvd reset to 0.0".
- If (ijthsrev \leq 0.0), "ijthsrev reset to 0.0".
- If (ijthdrev \leq 0.0), "ijthdrev reset to 0.0".
- If (xjbvs \leq 0.0), "xjbvs reset to 0.0".
- If (xjbvd \leq 0.0), "xjbvd reset to 0.0".

TSMC Diode Model

Starting in HSPICE version 2003.09, HSPICE MOSFET Level 49 ($A_{CM}=12$, BSIM3 version 3.2 or later) supports a TSMC diode model. You can use this TSMC diode model to simulate the breakdown effect, the resistance-induced non-ideality factor, and geometry-dependent reverse current of a diode.

Order this model directly from Taiwan Semiconductor Manufacturing Company (TSMC), not from Synopsys. See the TSMC web site: <http://www.tsmc.com>

BSIM3v3 STI/LOD

HSPICE BSIM3v3 (Level=49 and 53) supports UC Berkeley's STI/LOD stress effect model (see [Table 118](#)). To turn on this stress effect model in BSIM3v3, specify `STIMOD=1` in your model cards.

Table 118 Supported HSPICE BSIM3v3 STI/LOD Parameters

Parameter	Unit	Default	Bin?	Description
SA (instance parameter)		0.0		Distance between S/D diffusion edge to poly gate edge from one side. If not given, or, if (≤ 0), the stress effect is turned off.
SB (instance parameter)		0.0		Distance between S/D diffusion edge to poly gate edge from the other side. If not given, or, if (≤ 0), the stress effect is turned off
STIMOD (Also instance parameter)		0.0		STI model selector, which gives priority to the instance parameter. <ul style="list-style-type: none"> 0: No STI effect. 1: IDB's STI model 2: GSHUNT's STI model
SAREF	M	1e-06	No	Reference distance for SA, >0.0
SBREF	M	1e-06	No	Reference distance for SB, >0.0
WLOD	M	0.0	No	Width parameter for stress effect
KU0	M	0.0	No	Mobility degradation/enhancement coefficient for stress effect
KVSAT	M	0.0	No	Saturation velocity degradation/enhancement parameter for stress effect. $1.0 \leq kvsat \leq 1.0$
TKU0		0.0	No	Temperature coefficient of KU0
LKU0		0.0	No	Length dependence of KU0
WKU0		0.0	No	Width dependence of KU0
LLODKU0		0.0	No	Length parameter for U0 stress effect, >0

Table 118 Supported HSPICE BSIM3v3 STI/LOD Parameters

Parameter	Unit	Default	Bin?	Description
WLODKU0		0.0	No	Width parameter for U0 stress effect, >0
KVTH0	V*m	0.0	No	Threshold shift parameter for stress effect
WKVTH0		0.0	No	Width dependence of KVTH0
PKVTH0		0.0	No	Cross-term dependence of KVTH0
LLODVTH		0.0	No	Length parameter for Vth stress effect, >0
WLODVTH		0.0	No	Width parameter for Vth stress effect, >0
STK2		0.0	No	K2 shift factor related to VTh0 change
LODK2	m	1.0	No	K2 shift modification factor for stress effect, >0
STETA0		0.0	No	ETA0 shift factor related to VTH0 change
LODETA0	M	1.0	No	ETA0 shift modification factor for stress effect, >0

Parameter Differences

Some parameter names differ between the Synopsys model and the Berkeley junction models. The Synopsys models ($ACM=0-3$) do not recognize the following BSIM3v3 parameters:

- NJ (ignored, use N instead)
- CJSWG (ignored, use CJGATE instead)
- MJSWG (ignored; HSPICE has no equivalent parameter, and simulation sets the gate sidewall grading coefficient=MJSW)
- PBSW (ignored, use PHP instead)
- PBSWG (ignored; HSPICE has no equivalent parameter, and simulation sets the gate sidewall contact potential=PHP)

The Berkeley model ($ACM=10,11,12,13$) does not recognize the following parameters:

- CJGATE (ignored, use CJSWG instead)
- PHP (ignored, use PBSW instead)

Noise Model

The HSPICE `NLEV` parameter overrides the BSIM3v3 `NOIMOD` parameter. Specifying `NLEV` invokes the HSPICE noise model. See [MOSFET Noise Models on page 729](#) for more information. If you do not specify `NLEV`, simulation invokes the Berkeley noise equations.

Performance Improvements

To improve the performance of Levels 49 and 53 reduce the complexity of model equations, replacing some calculations with spline functions and compiler optimization. For Level 49, the result is a reduction in simulation time of up to 40% compared to releases before 97.4 while maintaining accuracy to 5 digits or better. To use the spline functions, set the `SFVTFLAG=1` model parameter in the model card. `SFVTFLAG=0`, the default value, disables the spline functions. For Level 53, all BSIM3v3 non-compliant features default to off.

Reduced Parameter Set BSIM3v3 Model (BSIM3-lite)

Setting the `LITE=1` model parameter in Level 49 to invoke the BSIM3v3-lite reduced parameter set model. Use it with model binning. Without binning to account for geometry effects, the full BSIM3v3 model specifies several model parameters. However, it is often difficult to extract a “global” BSIM3v3 model that is accurate over the entire geometry range.

To improve accuracy over a range of geometries, you can bin the model parameters. That is, this model divides the entire length-width geometry range into rectangular regions or bins. Simulation extracts a different set of parameters for each bin. The built-in bilinear parameter interpolation scheme maintains continuity (over length-width) at the boundaries between bins. Because many BSIM3 model parameters account for MOSFET geometry effects, these geometry-effect parameters are redundant. You can eliminate them when you use binning.

The BSIM3-lite model parameter set was created in response to the question: What BSIM3 parameters should be excluded when using a binned model? To invoke the BSIM3-lite model, specify the `LITE=1` model parameter in the model card.

Simulation checks the model card to determine if it conforms to the BSIM3-lite parameter set. BSIM3-lite takes advantage of the smaller number of calculations, and reduces simulation times by up to 10% compared to the full parameter set BSIM3 model. Only Level 49 supports `LITE=1`.

Table 119 lists model parameters (total 49) that the BSIM3-lite model excludes. Either exclude all parameters in this list from the model card or explicitly set them to the default value specified in the list. In some cases, as noted, the BSIM3-lite default value differs from the standard BSIM3v3 default value. You should also exclude *WR*, *ALPHA0*, and *CIT*, but the BSIM3-lite model card does not require this exclusion.

Table 119 Parameters Excluded from BSIM3-Lite

Parameter	Comments
mobmod	Recommended default or set=1
nqsmod	Recommended default or set=0
toxrn	default=tox
ll	default=0
lln	default=1
lw	default=0
lwn	default=1
lwl	default=0
wl	default=0
wln	default=1
ww	default=0
wwn	default=1
wwl	default=0
dwg	default=0
dwb	default=0
llc	default=0
lwc	default=0
lwc	default=0

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Table 119 Parameters Excluded from BSIM3-Lite

Parameter	Comments
wlc	default=0
wwc	default=0
wwlc	default=0
b0	default=0
b1	default=0
vbx	do not define
vbm	do not define
xt	do not define
nsub	do not define
nlx	default=0, std default=1.74e-7
gamma1	do not define
gamma2	do not define
ngate	Recommended default or set=0
k3	default=0, std default=80
k3b	default=0
w0	no effect
dvt0	default=0, std default=2.2
dvt1	default=0, std default=0.53
dvt2	default=0, std default=-0.032
dvt0w	default=0
dvt1w	default=0, std default=5.3e6

Table 119 Parameters Excluded from BSIM3-Lite

Parameter	Comments
dvt2w	default=0, std default=-0.032
dsub	default=0
prwg	default=0
prwb	default=0
wr	Recommended default or set=1
drout	default=0, std default=0.56
pdiblc1	default=0, std default=0.39
cit	Recommended default or set=0
alpha0	Recommended default or set=0 for Version 3.2
kt1l	default=0

Parameter Binning

To support parameter binning, Berkeley BSIM3v3 specifies L_{WP} parameters. To bilinearly interpolate a subset of model parameters over $1/L_{eff}$ and $1/W_{eff}$, you specify four terms:

- X_o parameter
- X length term
- X_w width term
- X_p product term

The simulation then interpolates the parameter value at specified L, W .

$$X = X_o + X_l/L_{eff} + X_w/W_{eff} + X_p/L_{eff}/W_{eff}$$

See [Parameter Range Limits on page 459](#) to determine whether you can bin a parameter. Simulation adds the L_{MIN} , L_{MAX} , W_{MIN} , W_{MAX} , L_{REF} , and W_{REF} parameters to allow multiple cell binning. L_{MIN} , L_{MAX} , W_{MIN} , W_{MAX} define the cell boundary. L_{REF} and W_{REF} are offset values that provide a convenient

interpolation scheme. The simulation uses the `LREF` and `WREF` offsets if you define both values and you specify the `BINFLAG > 0.9` model parameter.

The simulation then interpolates the parameter value at a specified `L,W`:

$$X = X_o + X_l * (1/L_{eff} - 1/LREF) + X_w * (1/W_{eff} - 1/WREF) + X_p / (1/L_{eff} - 1/LREF) / (1/W_{eff} - 1/WREF)$$

To select micron units for the `lwp` geometry parameters, set the `BINUNIT=1` model parameter. For other choices of `BINUNIT`, the lengths are in units of meters. Simulation handles the `XL`, `XLREF`, `XW`, and `XWREF` parameters in a manner consistent with other Synopsys MOSFET models, and they produce shifts in parameter values without disrupting the continuity across the bin boundaries.

BSIM3v3 WPE Model

HSPICE BSIM3V3 (Level=49, BSIM3 Version 3.22 or later) supports UC Berkeley's BSIM4.5 WPE (well-proximity effects) model (see [Table 120](#) and [Table 121 on page 439](#)). To turn on this WPE model in BSIM3v3, specify `WPEMOD=1` in your model cards.

Table 120 Supported HSPICE BSIM3v3 WPE model parameters

Name	Default	Min	Max	Binnable	Description
WPEMOD	0	0	1	No	Flag for WPE model (WPEMOD=1 to activate this model)
SCREF	1.0e-6	0.0		No	Reference distance to calculate SCA, SCB and SCC
WEB	0.0			No	Coefficient for SCB
WEC	0.0			No	Coefficient for SCC
KVTH0WE	0.0			Yes	Threshold shift factor for well-proximity effect
K2WE	0.0			Yes	K2 shift factor for well-proximity effect
KU0WE	0.0			Yes	Mobility degradation factor for well-proximity effect

Table 121 Integrals to calculate distribution functions/distances

Name	Default	Min	Max	Description
SCA	0.0	0.0		Integral of the first distribution function for scattered well dopant
SCB	0.0	0.0		Integral of the second distribution function for scattered well dopant
SCC	0.0	0.0		Integral of the third distribution function for scattered well dopant
SC	0.0	0.0		Distance to a single well edge

BSIM3v3 Ig Model

HSPICE BSIM3V3 (Level=49, BSIM3 Version 3.22 or later) supports UC Berkeley's BSIM4.5 Ig (gate direct tunneling currents) model ([Table 122](#)). To turn on this Ig model in BSIM3v3, specify IGCMOD=1 and/(or) IGBMOD=1 in your model cards.

Table 122 Supported HSPICE BSIM3v3 Ig model parameters

Name	Default	Min	Max	Binnable	Description
IGCMOD	0	0	2	No	Gate-to-channel Ig model selector
IGBMOD	0	0	1	No	Gate-to-body Ig model selector
TEMPMOD	0	0	2	No	Temperature model selector
NIGC	1.0	0.0		Yes	Parameter for Igc slope
AIGC	NMOS:1.36e-2/ PMOS:9.80e-3			Yes	Parameter for Igc
BIGC	NMOS:1.71e-3/ PMOS:7.59e-4			Yes	Parameter for Igc
CIGC	NMOS:0.075/ PMOS:0.03			Yes	Parameter for Igc
AIGBACC	1.36e-2			Yes	Parameter for Igb

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Table 122 Supported HSPICE BSIM3v3 Ig model parameters

Name	Default	Min	Max	Binnable	Description
BIGBACC	1.71e-3			Yes	Parameter for Igb
CIGBACC	0.075			Yes	Parameter for Igb
NIGBACC	1.0	0.0		Yes	Parameter for Igbacc slope
AIGBINV	1.11e-2			Yes	Parameter for Igb
BIGBINV	9.49e-4			Yes	Parameter for Igb
CIGBINV	0.006			Yes	Parameter for Igb
EIGBINV	1.1			Yes	Parameter for the Si bandgap for Igbinv
NIGBINV	3.0	0.0		Yes	Parameter for Igbinv slope
TOXE	TOX	0.0		No	Electrical gate oxide thickness in meters
NTOX	1.0			Yes	Exponent for Tox ratio
TOXREF	30.0e-10	0.0		No	Target tox value
PIGCD	1.0	0.0		Yes	Parameter for Igc partition
NSD	1.0e20			Yes	S/D doping concentration
VFBSDOFF	0.0			Yes	S/D flatband voltage offset
TVFBSDOFF	0.0			Yes	Temperature parameter for vfbsdoff
POXEDGE	1.0	0.0		Yes	Factor for the gate edge Tox
DLCIG	0.0			No	Delta L for Ig model
AIGSD	NMOS:1.36e-2/ PMOS:9.80e-3			Yes	Parameter for Igs,d
BIGSD	NMOS:1.71e-3/ PMOS:7.59e-4			Yes	Parameter for Igs,d

Table 122 Supported HSPICE BSIM3v3 Ig model parameters

Name	Default	Min	Max	Binnable	Description
CIGSD	NMOS:0.075/ PMOS:0.03			Yes	Parameter for Igs,d

Charge Models

In BSIM3v3, the BSIM1 capacitance model is $CAPMOD=0$. Simulation replaces this with a modified BSIM1 capacitance model, based on the $CAPOP=13$ model in Level 49. Level 53 uses the Berkeley BSIM1 capacitance model for $CAPMOD=0$. Table 123 lists $CAPMOD$ defaults for the Berkeley BSIM3v3 model, and for Levels 49 and 53.

Table 123 MOSFET Charge Model Versions

Version	BSIM3v3	Level 49	Level 53
3.0	1	1	1
3.1	2	0	2
3.2	3	3	3
3.3	3	3	3

VFBFLAG

The $CAPMOD=0$ capacitance model normally calculates the threshold voltage as $V_{th}=v_{fbc} + \phi + k_1 * \sqrt{\phi - v_{bs}}$, where v_{fbc} is the V_{FBCV} model parameter. This eliminates any dependence on the V_{TH0} parameter. To allow capacitance dependence on V_{TH0} , set the $V_{FBFLAG}=1$ model parameter. The $CAPMOD=0$ capacitance model calculates the threshold voltage as $V_{th}=v_{th0} + k_1 * \sqrt{\phi - v_{bs}} - k_1 * \sqrt{\phi}$. The V_{FBFLAG} default value is 0.

Printback

You can printback all model parameters with units. The printback also indicates whether Berkeley or Synopsys model junction diodes and noise models are

invoked, and which parameters are not used (for example, simulation does not use `CJGATE` if `ACM=0-3`).

Mobility Multiplier

You can define mobility multiplier parameters in the BSIM3V3 instance line.

Name	Default	Description
mulu0	1.0	Low-field mobility (U0) multiplier
mulua	1.0	First-order mobility degradation coefficient (UA) multiplier
mulub	1.0	Second-order mobility degradation coefficient (UB) multiplier

When HSPICE prints back a MOSFET element summary (`.OPTION LIST`), it identifies the BSIM3V3 MOSFET, and prints back these three additional instance parameters.

Using BSIM3v3

Note the following points when you use BSIM3v3 with a Synopsys circuit simulator:

- Use either the Level 49 or Level 53 model. Level 53 fully complies with the Berkeley BSIM3v3 release. In most cases Level 49 returns the same results as Level 53, runs as fast or faster, shows better convergence, and allows a wider range of parameter specifications.
- Explicitly set all Berkeley-specific BSIM3 model parameters in the model card. This minimizes problems resulting from version changes and compatibility with other simulators. You do not explicitly set all lwp binning parameters.
- To match results with simulations from previous HSPICE versions, use the `HSPVER=YY.N` model parameter, such as `HSPVER=97.4`. Do not use the full year specification (such as 1997.4). The patch version number format is `HSPVER=YY.NN` (for example, `HSPVER=98.21` is release 98.2.1).

- Levels 49 and 53 support the `TNOM` model parameter name as an alias for `TREF`. The conventional terminology in HSPICE is `TREF`, which all Synopsys model MOS levels support as a model parameter. Both Levels 49 and 53 support the `TNOM` alternative name for compatibility with SPICE3.

The default room temperature is 25°C in Synopsys circuit simulators, but is 27°C in SPICE3. If you specify the BSIM3 model parameters at 27°C, add `TNOM=27` to the model so that simulation correctly interprets the model parameters. To set the nominal simulation temperature to 27, add `.OPTION TNOM=27` to the netlist when you test the Synopsys model versus SPICE3.

You can use `DELVTO` and `DTEMP` on the element line with Levels 49 and 53. The following equation converts the temperature setup between the Synopsys model and SPICE3:

```
SPICE3:      .OPTION TEMP=125
             .MODEL NCH NMOS Level=8
             + TNOM=27 ...
Synopsys Model:      .TEMP 125
             .MODEL NCH NMOS Level=49
             + TNOM=27 ...
```

- To automatically calculate the drain, source area, and perimeter factors for Berkeley junction diode models, use `ACM=12` with `CALCACM=1`. Normally, `ACM=10-13` defaults the area and perimeter factors to 0. To override this value for `ACM=12`, specify `CALCACM=1`. Define the HSPICE-specific parameter (`HDIF`) in the model card. If you do not want parasitic `Rs` and `Rd` with the BSIM3v3 internal `Rsd`, either do not specify the `RSH`, `RSC`, `RDC`, `RS`, and `RD` HSPICE parameters (default is 0) or set them to 0.
- Simulation and analysis either warns or aborts with a fatal error if certain model parameter values are out of a normal range. To view all warnings, you might need to increase the `.OPTION WARNLIMIT` value (default=1). To turn on full parameter range checking, set the `PARAMCHK=1` model parameter (default is 0). If you use `PARAMCHK=0`, simulation checks a smaller set of parameters. (See Note below; also see [Parameter Range Limits on page 459](#) for more details about parameter limits.) Use the `APWARN=1` model parameter (default=0) to turn off `PS,PD < Weff` warnings.
- Use `NQSMOD` only with Version 3.2, and specify it only in the model card.

Note: The default setting of `PARAMCHK` can influence MOSFET behavior in HSPICE in not checking and/or enforcing the range limits for some MOSFET model parameters.

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Level 49 and 53 BSIM3v3 MOS Models

`PARAMCHK` selects between a default and enhanced level of MOSFET parameter checks. If set to 0, only default checks are performed.

If set to 1, an enhanced set of parameter checks are performed and certain parameters will be reset to nominal values if they are found to be out of range.

Because the default setting of `PARAMCHK` can vary between model levels (e.g., 49/53=0 and 54=1), it is important to implicitly set `PARAMCHK` in your model file or insure it has been set by the model vendor. A failure to do so can cause unexpected variations in simulation results and a failure to correlate with other simulators that may have different default settings.

Level 49, 53 Model Parameters

The following tables describe all Level 49 and Level 53 model parameters, including:

- parameter name
- units
- default value
- whether you can bin the parameter
- a description

These tables are a superset of the BSIM3v3 model parameter set, and include HSPICE parameters. These HSPICE parameters are noted in the description column, and always default (for Level 53) to maintain compliance with the BSIM3v3 standard. These parameters also apply to Level 49 with the following exceptions:

Table 124 Model Flags for MOSFET Levels 49/53

Name	Unit	Default	Bin	Description
VERSION	-	3.3	No	Selects from BSIM3 Versions 3.0, 3.1, 3.2, and 3.3. Issues a warning if you do not explicitly set it.

Table 124 Model Flags for MOSFET Levels 49/53

Name	Unit	Default	Bin	Description
HSPVER	-	98.2	No	Selects from HSPICE Versions: 98.2, 97.4, 97.2, 96.4, 96.3, 96.1
PARAMCHK	-	0	No	PARAMCHK=1 checks the model parameters for range compliance
APWARN	-	0	No	When >0 turns off the warning message for PS,PD < Weff (HSPICE specific)
BINFLAG	-	0	No	Uses wref, Iref if you set this flag >0.9 (HSPICE)
MOBMOD	-	1	No	Selects a mobility model
CAPMOD	-	3	No	Selects from the 0,1,2,3 charge models Level 49 CAPMOD defaults to 0.
CAPOP	-	-	No	Obsolete for Levels 49 and 53. HSPICE ignores it (HSPICE specific) in all versions.
NOIMOD	-	1	No	Berkeley noise model flag
NLEV	-	-(off)	No	The noise model flag (non-zero overrides NOIMOD) (HSPICE specific). See MOSFET Noise Models on page 729 for more information.
NQSMOD	-	0 (off)	No	NQS Model flag
SFVTFLAG	-	0 (off)	No	Spline function for Vth (HSPICE specific)
VFBFLAG	-	0 (off)	No	VFB selector for CAPMOD=0 (HSPICE specific)
ACNQSMOD	-	0	No	AC small-signal NQS model selector

Table 125 Basic Model Parameters, MOSFET Levels 49/53

Name	Unit	Default	Bin	Description
VGSLIM	V	0	No	Asymptotic Vgs value, The Min value is 5V. 0—value indicates an asymptote of infinity. (HSPICE and Level 49 specific)

Chapter 6: MOSFET Models (BSIM): Levels 47 through 72

Level 49 and 53 BSIM3v3 MOS Models

Table 125 Basic Model Parameters, MOSFET Levels 49/53

Name	Unit	Default	Bin	Description
TOX	m	150e-10	No	Gate oxide thickness
XJ	m	0.15e-6	Yes	Junction depth
NGATE	cm ⁻³	0	Yes	Poly gate doping concentration
VTH0 (VTHO)	V	0.7 NMOS -0.7 PMOS	Yes	Threshold voltage of the long channel device at $V_{bs}=0$ and small V_{ds}
NSUB	cm ⁻³	6.0e16	Yes	Substrate doping concentration
NCH	cm ⁻³ See (6)	1.7e17	Yes	Peak doping concentration near the interface
NLX	m	1.74e-7	Yes	Lateral nonuniform doping along the channel
K1	V ^{1/2}	0.50	Yes	First-order body effect coefficient
K2	-	-0.0186	Yes	Second-order body effect coefficient
K3	-	80.0	Yes	Narrow width effect coefficient
K3B	1/V	0	Yes	Body width coefficient, narrow width effect
W0	m	2.5e-6	Yes	Narrow width effect coefficient
DVT0W	1/m	0	Yes	Narrow width coefficient 0 for V_{th} , small L
DVT1W	1/m	5.3e6	Yes	Narrow width coefficient 1 for V_{th} , small L
DVT2W	1/V	-0.032	Yes	Narrow width coefficient 2 for V_{th} , small L
DVT0	-	2.2	Yes	Short channel effect coefficient 0 for V_{th}
DVT1	-	0.53	Yes	Short channel effect coefficient 1 for V_{th}
DVT2	1/V	-0.032	Yes	Short channel effect coefficient 2 for V_{th}

Table 125 Basic Model Parameters, MOSFET Levels 49/53

Name	Unit	Default	Bin	Description
ETA0	-	0.08	Yes	DIBL (drain induced barrier lowering) coefficient for the subthreshold region
ETAB	1/V	-0.07	Yes	DIBL coefficient for the subthreshold region
DSUB	-	DROUT	Yes	DIBL coefficient exponent in the subthreshold region
VBM	V	-3.0	Yes	Maximum substrate bias for calculating V_{th}
U0	cm ² /V/sec	670 nmos 250 pmos	Yes	Low field mobility at T=TREF=TNOM
UA	m/V	2.25e-9	Yes	First-order mobility degradation coefficient
UB	m ² /V ²	5.87e-19	Yes	Second-order mobility degradation coefficient
UC	1/V	-4.65e-11 or -0.0465	Yes	Body bias sensitivity coefficient of mobility -4.65e-11 for MOBMOD=1,2 or, -0.0465 for MOBMOD=3
A0	-	1.0	Yes	Bulk charge effect coefficient, channel length
AGS	1/V	0.0	Yes	Gate bias coefficient of Abulk
B0	m	0.0	Yes	Bulk charge effect coefficient, channel width
B1	m	0.0	Yes	Bulk charge effect width offset
KETA	1/V	-0.047	Yes	Body-bias coefficient of the bulk charge effect
VOFF	V	-0.08	Yes	Offset voltage in the subthreshold region

Chapter 6: MOSFET Models (BSIM): Levels 47 through 72

Level 49 and 53 BSIM3v3 MOS Models

Table 125 Basic Model Parameters, MOSFET Levels 49/53

Name	Unit	Default	Bin	Description
VSAT	m/sec	8e4	Yes	Saturation velocity of the carrier at T=TREF=TNOM
A1	1/V	0	Yes	First nonsaturation factor
A2	-	1.0	Yes	Second nonsaturation factor
RDSW	ohm · μm	0.0	Yes	Parasitic source drain resistance per unit width
PRWG	1/V	0	Yes	Gate bias effect coefficient of RDSW
PRWB	$1/V^{1/2}$	0	Yes	Body effect coefficient of RDSW
WR	-	1.0	Yes	Width offset from Weff for the Rds calculation
NFACTOR	-	1.0	Yes	Subthreshold region swing
CIT	F/m ²	0.0	Yes	Interface state capacitance
CDSC	F/m ²	2.4e-4	Yes	Drain/source and channel coupling capacitance
CDSCD	F/Vm ²	0	Yes	Drain bias sensitivity of CDSC
CDSCB	F/Vm ²	0	Yes	Body coefficient for CDSC
PCLM	-	1.3	Yes	Coefficient of the channel length modulation values ≤ 0 result in an error message and program exit.
PDIBLC1	-	0.39	Yes	Coefficient 1 for the DIBL (drain-induced barrier lowering) effect
PDIBLC2	-	0.0086	Yes	Coefficient 2 for the DIBL effect
PDIBLCB	1/V	0	Yes	Body effect coefficient of the DIBL effect coefficients

Table 125 Basic Model Parameters, MOSFET Levels 49/53

Name	Unit	Default	Bin	Description
DROUT	-	0.56	Yes	Length dependence coefficient of the DIBL correction parameter in R_{out}
PSCBE1	V/m	4.24e8	Yes	Exponent 1 for the substrate current induced body effect
PSCBE2	V/m	1.0e-5	Yes	Coefficient 2 for the substrate current induced body effect
PVAG	-	0	Yes	Gate dependence of Early voltage
DELTA	V	0.01	Yes	Effective V_{ds} parameter
ALPHA0	m/V	0	Yes	First parameter of the impact ionization current
BETA0	V	30	Yes	Second parameter of the impact ionization current
RSH	0.0	ohm/square	No	Source/drain sheet resistance in ohm per square

Table 126 AC and Capacitance Parameters, MOSFET 49/53

Name	Unit	Default	Bin	Description
XPART	-	0	No	Charge partitioning rate flag (default deviates from BSIM3V3=0) Level 49 XPART defaults to 1
CGSO	F/m	p1 See (1)	No	Non-LDD region source-gate overlap capacitance per unit channel length
CGDO	F/m	p2 See (2)	No	Non-LDD region source-gate overlap capacitance per unit channel length
CGBO	F/m	0	No	Gate-bulk overlap capacitance per unit channel length
CGS1	F/m	0.0	Yes	Lightly-doped source-gate overlap region capacitance

Chapter 6: MOSFET Models (BSIM): Levels 47 through 72

Level 49 and 53 BSIM3v3 MOS Models

Table 126 AC and Capacitance Parameters, MOSFET 49/53

Name	Unit	Default	Bin	Description
CGD1	F/m	0.0	Yes	Lightly-doped drain-gate overlap region capacitance
CKAPPA	F/m	0.6	Yes	Coefficient for the lightly-doped region overlap capacitance fringing field capacitance
CF	F/m	See (3)	Yes	Fringing field capacitance
CLC	m	0.1e-6	Yes	Constant term for short channel model
CLE	-	0.6	Yes	Exponential term, short channel model
VFBCV	V	-1.0	Yes	Flat band voltage, used only in CAPMOD=0 C-V calculations

Table 127 Length and Width Parameters, MOSFET 49/53

Name	Unit	Default	Bin	Description
WINT	m	0.0	No	Width offset fitting parameter from I-V without bias
WLN	-	1.0	No	Power of the length dependence of the width offset
WW	m^{WWN}	0.0	No	Coefficient of the width dependence for the width offset
WWN	-	1.0	No	Power of the width depends on the width offset.
WWL	$m^{WWN} * m^{WLN}$	0.0	No	Coefficient of the length and width cross term for the width offset
DWG	m/V	0.0	Yes	Coefficient of the gate dependence for W_{eff}
DWB	$m/V^{1/2}$	0.0	Yes	Coefficient of the substrate body bias dependence for W_{eff}
LINT	m	0.0	No	Length offset fitting the parameter from the I-V without the bias
LL	m^{LLN}	0.0	No	Coefficient of the length dependence for the length offset

Table 127 Length and Width Parameters, MOSFET 49/53

Name	Unit	Default	Bin	Description
LLN	-	1.0	No	Power of the length dependence of the length offset
LW	m^{LWN}	0.0	No	Coefficient of the width dependence for the length offset
LWN	-	1.0	No	Power of the width dependence of the length offset
LWL	$m^{LWN} * m^{LLN}$	0.0	No	Coefficient of the length and width cross term for the length offset
DLC	m	LINT	No	Length offset fitting parameter from CV
DWC	m	WINT	No	Width offset fitting parameter from CV

Table 128 Temperature Parameters, MOSFET Levels 49/53

Name	Unit	Default	Bin	Description
KT1	V	-0.11	Yes	Temperature coefficient for Vth
KT1L	m-V	0.0	Yes	Temperature coefficient for the channel length dependence of Vth
KT2	-	0.022	Yes	Body bias coefficient of the Vth temperature effect
UTE	-	-1.5	Yes	Mobility temperature exponent
UA1	m/V	4.31e-9	Yes	Temperature coefficient for UA
UB1	$(m/V)^2$	-7.61e-18	Yes	Temperature coefficient for UB
UC1	m/V^2	-5.69e-11	Yes	Temperature coefficient for UC
AT	m/sec	3.3e4	Yes	Temperature coefficient for the saturation velocity
PRT	ohm-um	0	Yes	Temperature coefficient for RDSW
XTI	-	3.0	No	Junction current temperature exponent

Chapter 6: MOSFET Models (BSIM): Levels 47 through 72

Level 49 and 53 BSIM3v3 MOS Models

Table 129 Bin Description Parameters, MOSFET Levels 49/53

Name	Unit	Default	Bin	Description
LMIN	m	0.0	No	Minimum channel length
LMAX	m	1.0	No	Maximum channel length
WMIN	m	0.0	No	Minimum channel width
WMAX	m	1.0	No	Maximum channel width
BINUNIT				Assumes that W _{EFF} , L _{EFF} , W _{REF} , I _{ref} units are in microns if BINUNIT=1, or, in meters, otherwise

Table 130 Process Parameters, MOSFET Levels 49/53

Name	Unit	Default	Bin	Description
DTOXCV (capmod=3 only)				Difference between the electrical and physical gate oxide thicknesses, due to the effects of the gate poly-depletion and finite channel charge layer thickness.
GAMMA1	\sqrt{V}	See (8)	Yes	Body effect coefficient near the surface
GAMMA2	\sqrt{V}	See (9)	Yes	Body effect coefficient in the bulk
VBX	V	See (10)	Yes	VBX at which the depletion region width equals XT
XT	m	1.55e-7	Yes	Doping depth

Table 131 Noise Parameters, MOSFET Levels 49/53

Name	Unit	Default	Bin	Description
NIOA	-	1.0e20 nmos 9.9e18 pmos	No	Body effect coefficient near the surface
NOIB	-	5.0e4 nmos 2.4e3 pmos	No	Body effect coefficient in the bulk

Table 131 Noise Parameters, MOSFET Levels 49/53

Name	Unit	Default	Bin	Description
NOIC	-	-1.4e-12 nmos 1.4e-12 pmos	No	VBX at which the depletion region width equals XT
EM	V/m	4.1e7	No	Flicker noise parameter
AF	-	1.0	No	Flicker noise exponent
KF	-	0.0	No	Flicker noise coefficient
EF	-	1.0	No	Flicker noise frequency exponent
LINTNOI	m	0.0	No	Length reduction parameter offset

Note: See also [MOSFET Noise Models on page 729](#) for HSPICE noise model usage (the NLEV parameter for HSPICE overrides the Berkeley NOIMOD parameter).

Table 132 Junction Parameters, MOSFET Levels 49/53

Name	Unit	Default	Bin	Description
ACM	-	10	No	Area calculation method selector (HSPICE specific) <ul style="list-style-type: none"> ACM=0-3 uses the HSPICE junction models ACM=10-13 uses the Berkeley junction models Level 49 ACM defaults to 0
JS	A/m2	0.0	No	Bulk junction saturation current. (Default deviates from BSIM3v3=1.0e ⁻⁴)
JSW	A/m	0.0	No	Sidewall bulk junction saturation current
NJ	-	1	No	Emission coefficient (use only with the Berkeley junction model: ACM=10-13)
N	-	1	No	Emission coefficient (HSPICE-specific), (use only with the HSPICE junction model, ACM=0-3)

Chapter 6: MOSFET Models (BSIM): Levels 47 through 72
Level 49 and 53 BSIM3v3 MOS Models

Table 132 Junction Parameters, MOSFET Levels 49/53

Name	Unit	Default	Bin	Description
CJ	F/m ²	5.79e-4	No	Zero-bias bulk junction capacitance (Default deviates from BSIM3v3=5.0e ⁻⁴)
CJSW	F/m	0.0	No	Zero-bias sidewall bulk junction capacitance (Default deviates from BSIM3v3=5.0e ⁻¹⁰)
CJSWG	F/m	CJSW	No	Zero-bias gate-edge sidewall bulk junction capacitance (use only with the Berkeley junction model, ACM=10-13)
CJGATE	F/m	CJSW	No	Zero-bias gate-edge sidewall bulk junction capacitance (HSPICE-specific) (use only if ACM=3)
PB, PHIB	V	1.0	No	Bulk junction contact potential
PBSW	V	1.0	No	Sidewall bulk junction contact potential
PHP	V	1.0	No	Sidewall bulk junction contact potential (HSPICE) (use only with the HSPICE junction model: ACM=0-3)
PBSWG	V	PBSW	No	Gate-edge sidewall bulk junction contact potential (use only with the Berkeley junction model, ACM=10-13). HSPICE has no equivalent parameter. Gate-edge contact potential is always set to PHP for the HSPICE junction model.
MJ	-	0.5	No	Bulk junction grading coefficient
MJSW	-	0.33	No	Sidewall bulk junction grading coefficient

Table 132 Junction Parameters, MOSFET Levels 49/53

Name	Unit	Default	Bin	Description
MJSWG	-	MJSW	No	Gate-edge sidewall bulk junction grading coefficient (use only with the Berkeley junction model: ACM=10-13) HSPICE has no equivalent parameter. Always set the gate-edge grading coefficient to MJSW for the HSPICE junction model.

Note: See [MOSFET Diode Models on page 701](#) for HSPICE junction diode model usage.

Table 133 NonQuasi-Static (NQS) Parameters, MOSFET 49/53

Name	Unit	Default	Bin	Description
ELM	-	5.0	Yes	Elmore constant

Table 134 MOSFET Levels 49/53 Version 3.2 Parameters

Name	Unit	Default	Bin	Description
TOXM	m	TOX	No	Reference gate oxide thickness
VFB	V	See (11)	Yes	DC flatband voltage
NOFF	-	1.0	Yes	I-V parameter, weak to strong inversion transition
VOFFCV	-	0.0	Yes	C-V parameter, weak to strong inversion transition
JTH	A	0.1	No	Diode limiting current
ALPHA1	V-1	0.0	Yes	Substrate current parameter

Chapter 6: MOSFET Models (BSIM): Levels 47 through 72

Level 49 and 53 BSIM3v3 MOS Models

Table 134 MOSFET Levels 49/53 Version 3.2 Parameters

Name	Unit	Default	Bin	Description
ACDE	m/V	1.0	Yes	Exponential coefficient for the charge thickness in the accumulation and depletion regions
MOIN	m/V	15.0	Yes	Coefficient, gate-bias dependent surface potential
TPB	V/K	0.0	No	Temperature coefficient of PB
TPBSW	V/K	0.0	No	Temperature coefficient of PBSW
TPBSWG	V/K	0.0	No	Temperature coefficient of PBSWG
TCJ	V/K	0.0	No	Temperature coefficient of CJ
TCJSW	V/K	0.0	No	Temperature coefficient of CJSW
TCJSWG	V/K	0.0	No	Temperature coefficient of CJSWG
LLC	mln	LL	No	Coefficient of the length dependence for the C-V channel length offset
LWC	mlwn	LW	No	Coefficient of the width dependence for the C-V channel length offset
LWLC	mln+lwn	LWL	No	Coefficient of the length and width for the C-V channel length offset
WLC	mwln	WL	No	Coefficient of the length dependence for the C-V channel width offset
WWC	mwwn	WW	No	Coefficient of the width dependence for the C-V channel width offset
WWLC	mwln+ wwn	WWL	No	Coefficient of the length and width cross terms for the C-V channel width offset

Level 49/53 Notes:

1. If you do not specify C_{gso} , simulation calculates it as follows:

- If you specify a dlc value that is greater than 0.0, then,

$$cgso=p1=\max(0, dlc*cox - cgs1)$$

$$\text{Otherwise, } cgso=0.6*xj*cox$$

2. If you do not specify C_{gdo} , simulation calculates it as follows:

- if you specify a dlc value that is greater than 0.0, then,

$$cgdo=p2=\max(0, dlc*cox - cgd1)$$

$$\text{Otherwise } cgdo=0.6*xj*cox$$

3. If you do not specify C_f , simulation calculates it using:

$$C_f = \frac{2\epsilon_{ox}}{\pi} \log\left(1 + \frac{4 \times 10^{-7}}{T_{ox}}\right)$$

4. If you do not specify V_{th0} in the .MODEL statement, simulation calculates it with $V_{fb}=-1$, using:

$$V_{th0} = V_{fb} + \phi_s + K_1 \sqrt{\phi_s}$$

5. If you do not specify K_1 and K_2 , simulation calculates it using:

$$K_1 = GAMMA_2 + 2K_2 \sqrt{\phi_s - V_{bs}}$$

$$K_2 = \frac{(GAMMA_2 - GAMMA_1)(\sqrt{\phi_s - V_{bs}} - \sqrt{\phi_s})}{2\sqrt{\phi_s}(\sqrt{\phi_s - V_{bm}} - \sqrt{\phi_s}) + V_{bm}}$$

6. If you do not specify n_{ch} , but you specify GAMMA1, then simulation calculates n_{ch} from:

$$n_{ch} = \frac{GAMMA_1^2 C_{OX}^2}{2q\epsilon_{si}}$$

7. If you do not specify n_{ch} or GAMMA1, then n_{ch} defaults to 1.7e17 per cubic meter and simulation calculates GAMMA1 from n_{ch} .
8. If you do not specify PHI, simulation calculates it using:

$$\phi_s = 2 \frac{k_B T}{q} \log\left(\frac{n_{ch}}{n_i}\right)$$

$$n_i = 1.45 \times 10^{10} \left(\frac{T}{300.15}\right)^{1.5} \exp\left(21.5565981 - \frac{qE_g(T)}{2k_B T}\right)$$

$$E_g(T) = 1.16 - \frac{7.02 \times 10^{-4} T^2}{T + 1108}$$

9. If you do not specify GAMMA1, simulation calculates it using:

$$GAMMA_1 = \frac{\sqrt{2q\epsilon_{si}n_{ch}}}{C_{ox}}$$

10. If you do not specify GAMMA2, simulation calculates it using:

$$GAMMA_2 = \frac{\sqrt{2q\epsilon_{si}n_{sub}}}{C_{ox}}$$

11. If you do not specify V_{bx} , simulation calculates it using:

$$V_{bx} = \phi_s - \frac{qn_{ch}X_t^2}{2\epsilon_{si}}$$

12. The BSIM3 model can calculate V_{th} in any of three ways:

- Using K1 and K2 values that you specify
- Using GAMMA1, GAMMA2, VBM, and VBX values that you enter in the .MODEL statement
- Using NPEAK, NSUB, XT, and VBM values that you specify

You can enter the U0 model parameter in meters or centimeters. Simulation converts U0 to m²/Vsec as follows: if U0 is greater than 1, it is multiplied by 1e-4. You must enter the NSUB parameter in cm⁻³ units.

Specify a negative value of VTH0 for the p-channel in the .MODEL statement.

The PSCBE1 and PSCBE2 model parameters determine the impact ionization current, which contributes to the bulk current.

Parameter Range Limits

Simulation reports either a warning or a fatal error if BSIM3v3 parameters fall outside predefined ranges. These range limitations prevent (or at least warn of) potential numerical problems. Level 53 follows exactly the BSIM3v3 range limit reporting scheme. Level 49 deviates from the BSIM3v3 scheme as noted in the comments column of [Table 135](#).

To control the maximum number of simulation warning messages printing to the output file, use:

```
.OPTION WARNLIMIT=#
```

In the preceding `.OPTION` statement, # is the maximum number of warning messages that simulation reports. The default `WARNLIMIT` value is 1. In some cases (as noted in [Table 135](#)), simulation checks parameters only if you set the `PARMAMCHK=1` model parameter.

Table 135 Model Parameter Range Limit, Levels 49/53

Name	Limits	Comments
TOX	Min value=5e-10 <=0 Fatal < 10-9 Warn if parmchk=1	BSIM3tox < 5e-10 is automatically reset to min value 5e-10
TOXM	<=0 Fatal < 10-9 Warn if parmchk=1	
XJ	<=0 Fatal	
NGATE	< 0 Fatal > 10 ²⁵ Fatal <=10 ¹⁸ Fatal if parmchk=1	if >10 ²³ simulation multiplies NGATE by 10 ⁻⁶ before the other limit checks. Level 49 returns: < 0 Fatal > 10 ²⁵ Warn <=10 ¹⁸ Warn if paramchk==1
NSUB	<=0 Fatal <=10 ¹⁴ Warn if parmchk=1 >=10 ²¹ Warn if parmchk=1	Ignores NSUB if k1,k2 are defined

Chapter 6: MOSFET Models (BSIM): Levels 47 through 72
Level 49 and 53 BSIM3v3 MOS Models

Table 135 Model Parameter Range Limit, Levels 49/53 (Continued)

Name	Limits	Comments
NLX	< -Leff Fatal < 0 Warn if parmchk=1	
NCH	<=0 Fatal <=10 ¹⁵ Warn if parmchk=1 ≥10 ²¹ Warn if parmchk=1	if >10 ²⁰ simulation multiplies NCH by 10 ⁻⁶ before the other limit checks.
DVT1W	< 0 Fatal	< 0 Level 49 reports a warning
DVT0	< 0 Warn if paramchk=1	
DVT1	< 0 Fatal	< 0 Level 49 reports a warning
ETA0	<=0 Warn if paramchk=1	
DSUB	< 0 Fatal	< 0 Level 49 reports a warning
VBM		Ignored if you defined K1 and K2
U0	<=0 Fatal	
B1	=-Weff Fatal B1 + Weff < 10 ⁻⁷ Warn if paramchk=1	
VSAT	<=0 Fatal < 10 ³ Warn if paramchk==1	
A1	-	See A2 conditions on the next line
A2	<ul style="list-style-type: none"> ▪ < 0.01 Warn and reset a2=0.01 if paramchk=1 ▪ > 1 Warn and reset a2=1,a1=0 if paramchk=1 	
DELTA	< 0 Fatal	
RDSW	< 0.001 Warn if paramchk=1 and reset rds=0	
NFACTOR	< 0 Warn if paramchk=1	

Table 135 Model Parameter Range Limit, Levels 49/53 (Continued)

Name	Limits	Comments
CDSC	< 0 Warn if paramchk=1	
CDSCD	< 0 Warn if paramchk=1	
PCLM	<=0 Fatal	
PDIBLC1	< 0 Warn if paramchk=1	
PDIBLC2	< 0 Warn if paramchk=1	
PS	< Weff Warn	
W0	=-Weff Fatal $w0 + Weff < 10^{-7}$ Warn if paramchk==1	
DROUT	< 0 Fatal if paramchk=1	Level 49 reports a warning
PSCBE2	<=0 warn if paramchk=1	
CGS0	< 0 Warn and reset to 0 if paramchk=1	
CGD0	< 0 Warn and reset to 0 if paramchk=1	
CGB0	< 0 Warn and reset to 0 if paramchk=1	
ACDE	< 0.4, >1.6 Warn	
MOIN	< 5.0, >25 Warn	
IJTH	< 0 Fatal	
NOFF	< 0.1, >4.0 Warn	

Table 136 Element Parameter Range Limit, Levels 49/53

Name	Limits	Comments
PD	< Weff, Warn	

Table 136 Element Parameter Range Limit, Levels 49/53

PS	< Weff, Warn
Leff	< 5.0 x 10 ⁻⁸ Fatal
Weff	< 1.0 x 10 ⁻⁷ Fatal
LeffCV	< 5.0 x 10 ⁻⁸ Fatal
WeffCV	< 1.0 x 10 ⁻⁷ Fatal

For a list of output template parameters in the MOSFET models, and which parameters this model supports, see [Table 4 on page 22](#).

Level 49, 53 Equations

The effective channel length and width in all model equations are:

$$L_{eff} = L_{drawn} - 2dL$$

$$W_{eff} = W_{drawn} - 2dW$$

$$W'_{eff} = W_{drawn} - 2dW'$$

$$W_{drawn} = W * WMULT + XW$$

$$L_{drawn} = L * LMULT + XL$$

- The unprimed W_{eff} is bias-dependent.
- The primed quantity is bias-independent.

$$dW = dW' + dW_g V_{gseff} + dW_b (\sqrt{\phi_s - V_{bseff}} - \sqrt{\phi_s})$$

$$dW' = W_{int} + \frac{W_L}{L^{WLN}} + \frac{W_W}{W^{WWN}} + \frac{W_{WL}}{L^{WLN} W^{WWN}}$$

$$dL = L_{int} + \frac{L_L}{L^{LLN}} + \frac{L_W}{W^{LWN}} + \frac{L_{WL}}{L^{LLN} W^{LWN}}$$

C-V calculations replace dW' with:

$$dW' = DWC + \frac{W_{LC}}{L^{WLN}} + \frac{W_{WC}}{W^{WWN}} + \frac{W_{WLC}}{L^{WLN} W^{WWN}}$$

C-V also replaces dL' with:

$$dL = DLC + \frac{L_{LC}}{L^{LLN}} + \frac{L_{WC}}{W^{LWN}} + \frac{L_{WLC}}{L^{LLN} W^{LWN}}$$

Note: For details of BSIM3 Version 3 equations, see the web site:

<http://www-device.eecs.berkeley.edu/~bsim3/get.html>

.MODEL CARDS NMOS Model

This is an example of a NMOS model for the Level 49 MOSFET. V_{TH0} is positive.

```
.model nch nmos Level=49
+ Tnom=27.0
+ nch=1.024685E+17 tox=1.00000E-08 xj=1.00000E-07
+ lint=3.75860E-08 wint=-2.02101528644562E-07
+ vth0=.6094574 k1=.5341038 k2=1.703463E-03 k3=-17.24589
+ dvt0=.1767506 dvt1=.5109418 dvt2=-0.05
+ nlx=9.979638E-08 w0=1e-6
+ k3b=4.139039
+ vsat=97662.05 ua=-1.748481E-09 ub=3.178541E-18 uc=1.3623e-10
+ rdsw=298.873 u0=307.2991 prwb=-2.24e-4
+ a0=.4976366
+ keta=-2.195445E-02 a1=.0332883 a2=.9
+ voff=-9.623903E-02 nFactor=.8408191 cit=3.994609E-04
+ cdsc=1.130797E-04
+ cdsch=2.4e-5
+ eta0=.0145072 etab=-3.870303E-03
+ dsub=.4116711
+ pclm=1.813153 pdiblc1=2.003703E-02 pdiblc2=.00129051
+ pdiblc3=-1.034e-3
+ drout=.4380235 pscbe1=5.752058E+08 pscbe2=7.510319E-05
+ pvag=.6370527 prt=68.7 ngate=1.e20 alpha0=1.e-7 beta0=28.4
+ prwg=-0.001 ags=1.2
+ dvt0w=0.58 dvt1w=5.3e6 dvt2w=-0.0032
+ kt1=-.3 kt2=-.03
+ at=33000
+ ute=-1.5
+ ua1=4.31E-09 ub1=7.61E-18 uc1=-2.378e-10
```

Chapter 6: MOSFET Models (BSIM): Levels 47 through 72

Level 49 and 53 BSIM3v3 MOS Models

```
+ kt1l=1e-8
+ wr=1 b0=1e-7 b1=1e-7 dwg=5e-8 dwb=2e-8 delta=0.015
+ cgd1=1e-10 cgsl=1e-10 cgbo=1e-10 xpart=0.0
+ cgdo=0.4e-9 cgso=0.4e-9
+ clc=0.1e-6
+ cle=0.6
+ ckappa=0.6
```

PMOS Model

Example of a PMOS model for the Level 49 MOSFET. V_{TH0} is negative.

```
.model pch PMOS Level=49
+ Tnom=27.0
+ nch=5.73068E+16 tox=1.00000E-08 xj=1.00000E-07
+ lint=8.195860E-08 wint=-1.821562E-07
+ vth0=-.86094574 k1=.341038 k2=2.703463E-02 k3=12.24589
+ dvt0=.767506 dvt1=.65109418 dvt2=-0.145
+ nlx=1.979638E-07 w0=1.1e-6
+ k3b=-2.4139039
+ vsat=60362.05 ua=1.348481E-09 ub=3.178541E-19 uc=1.1623e-10
+ rdsw=498.873 u0=137.2991 prwb=-1.2e-5
+ a0=.3276366
+ keta=-1.8195445E-02 a1=.0232883 a2=.9
+ voff=-6.623903E-02 nFactor=1.0408191 cit=4.994609E-04
+ cdsc=1.030797E-3
+ cdsb=2.84e-4
+ eta0=.0245072 etab=-1.570303E-03
+ dsub=.24116711
+ pclm=2.6813153 pdiblc1=4.003703E-02 pdiblc2=.00329051
+ pdiblc3=-2.e-4
+ drout=.1380235 pscbe1=0 pscbe2=1.e-28
+ pvag=-.16370527
+ prwg=-0.001 ags=1.2
+ dvt0w=0.58 dvt1w=5.3e6 dvt2w=-0.0032
+ kt1=-.3 kt2=-.03 prt=76.4
+ at=33000
+ ute=-1.5
+ ua1=4.31E-09 ub1=7.61E-18 uc1=-2.378e-10
+ kt1l=0
+ wr=1 b0=1e-7 b1=1e-7 dwg=5e-8 dwb=2e-8 delta=0.015
+ cgd1=1e-10 cgsl=1e-10 cgbo=1e-10 xpart=0.0
+ cgdo=0.4e-9 cgso=0.4e-9
+ clc=0.1e-6
+ cle=0.6
+ ckappa=0.6
```

Level 54 BSIM4 Model

The UC Berkeley BSIM4 model explicitly addresses many issues in modeling sub-0.13 micron CMOS technology and RF high-speed CMOS circuit simulation. The Level 54 model is based on the UC Berkeley BSIM4 MOS model. BSIM4.5 is fully supported in this release. For details, see the BSIM web site:

<http://www-device.eecs.berkeley.edu/~bsim3/bsim4.html>

The following sections discuss these topics:

- [Version 4.5 Features](#)
- [Other Noise Sources Modeled in v. 4.5](#)
- [General Syntax for BSIM4 Model](#)
- [Improvements Over BSIM3v3](#)
- [Parameter Range Limit for BSIM4 Level 54](#)
- [TSMC Diode Model](#)
- [BSIM4 Juncap2 Model](#)
- [BSIM4 STI/LOD](#)
- [Version 4.6 Features](#)
- [Version 4.6.2 Features and Updates](#)
- [Version 4.6.3 Update](#)
- [Level 54 BSIM4 Template Output List](#)

See [.OPTION PHD](#) in the *HSPICE Reference Manual: Commands and Control Options* for the PHD flow that can generally help large case HSPICE DC OP convergence for BSIM4 testcases.

The following sections discuss these topics:

- [Version 4.5 Features](#)
- [General Syntax for BSIM4 Model](#)
- [Improvements Over BSIM3v3](#)
- [Parameter Range Limit for BSIM4 Level 54](#)
- [TSMC Diode Model](#)
- [BSIM4 Juncap2 Model](#)

- [BSIM4 STI/LOD](#)
- [HSPICE Junction Diode Model and ACM](#)
- [Version 4.6 Features](#)
- [Version 4.6.1 Features](#)
- [Version 4.6.2 Features and Updates](#)
- [Version 4.6.3 Update](#)
- [Level 54 BSIM4 Template Output List](#)

Version 4.5 Features

In July 2005, Berkeley released BSIM4 Version 4.5, which includes the following features:

- The gate resistance parameters `XGW` and `NGCON` are now available as both model and instance parameters.
- Four modes are added or enhanced:
 - `RBODYMOD=2`: substrate resistance model that is scalable with channel length, channel width and number fingers
 - `IGCMOD=2`: implements full BSIM4 V_{th} model into IGC enables accurate predictions of IGC V_{bs} dependence
 - `TEMPMOD=2`: enhances `TEMPMOD` so $V_{th}(DITS)$ and gate tunneling models are functions of nominal temperature and adds the temperature dependence of zero-bias flat-band voltage
 - `WPEMOD=1`: adds a new well-proximity effect model developed by CMC.
- Adds a new mobility model that accounts for Coulomb scattering effect as well as the channel length dependence of mobility due to heavy halo-doping.
- Adds additional temperature dependence of model parameters `VOFF` and `VFBSDOFF`.
- A fatal error message is issued when a model parameter `VTSS`, `VTSD`, `VTSSWS`, or `VTSSWGD` is negative. A warning message was issued previously.

- A warning message is issued if model parameter `CGBO` is negative. In which case, `CGBO` is set to 0.
- Fixed bugs in BSIM 4.4.

Note: BSIM4 Version 4.5 officially supports instance parameter `DELVT0`, which is used to represent threshold variations. This parameter has been supported in HSPICE since the 2002.12 version.

Other Noise Sources Modeled in v. 4.5

BSIM4 models the thermal noise due to the substrate, electrode gate, and source/drain resistances. Shot noise due to various gate tunneling components is modeled as well.

HSPICE can print out `rg`, `rbps`, `rbpd`, `rbpb`, `rbsb`, `rbdb`, `igs`, `igd`, `igb` noise information. You can add the following noise parameters to the model card.

Output Parameters	Turns On...
+ <code>rgatemod=1</code>	The <code>rg</code> noise output
+ <code>rbodymod=1</code>	The <code>rbps</code> , <code>rbpb</code> noise output
+ <code>igbmod=1</code>	The <code>igb</code> noise output
+ <code>igcmod=1</code>	The <code>igs</code> and <code>igd</code> noise output
+ <code>rbsbx0=1</code> <code>rbsby0=1</code> <code>rbdbx0=1</code> <code>rbdb0=1</code> <code>rbodymod=1</code>	The <code>rbsb</code> and <code>rbdb</code> noise output

General Syntax for BSIM4 Model

The general syntax for including a BSIM4 model element in a netlist is:

```
Mxxx nd ng ns [nb] mname [L=val] [W=val] [M=val]
+ [VER_CONTROL=0|1] [AD=val] [AS=val] [PD=val] [PS=val]
+ [RGATEMOD=val] [RBODYMOD=val] [TRNQSMOD=val]
+ [ACNQSMOD=val] [GEOMOD=val] [RGEOMOD=val]
+ [NRS=val] [NRD=val] [RBPB=val] [RBDP=val]
+ [RBPS=val] [RBDB=val] [RBSB=val] [NF=val]
+ [MIN=val] [RDC=val] [RSC=val] [DELVT0=val]
+ [MULU0=val] [DELK1=val] [DELNFCT=val]
```

Chapter 6: MOSFET Models (BSIM): Levels 47 through 72

Level 54 BSIM4 Model

```
+ [DELTOX=val] [OFF] [IC=Vds, Vgs, Vbs]  
+ [WNFLAG=val] [MULID0=val]
```

Parameter	Description
ACNQSMOD	AC small-signal NQS model selector.
AD	Drain diffusion area.
AS	Source diffusion area.
DELK1	Shift in body bias coefficient (K1).
DELNFCT	Shift in subthreshold swing factor (NFACTOR).
DELTOX	Shift in gate electrical and physical oxide thickness (TOXE and TOXP). That is, the difference between the electrical and physical gate oxide/insulator thicknesses.
DELVTO (DELVT0)	Shift in the VTH0 zero-bias threshold voltage.
GEOMOD	Geometry-dependent parasitics model selector—specifies how the end S/D diffusions connect.
IC	Initial guess in the order
L	BSIM4 MOSFET channel length in meters.
MIN	Whether to minimize the number of drain or source diffusions for even-number fingered device.
<i>mname</i>	MOSFET model name reference.
MULU0	Low-field mobility (U0) multiplier.
<i>nb</i>	Bulk terminal node name.
<i>nd</i>	Drain terminal node name.
NF	Number of device fingers.
<i>ng</i>	Gate terminal node name.

Parameter	Description
NRD	Number of drain diffusion squares.
NRS	Number of source diffusion squares.
<i>ns</i>	Source terminal node name.
OFF	Sets the initial condition to OFF in DC analysis.
PD	Perimeter of the drain junction: <ul style="list-style-type: none"> ▪ If PERMOD=0, it excludes the gate edge. ▪ Otherwise, it includes the gate edge.
PS	Perimeter of the source junction: <ul style="list-style-type: none"> ▪ If PERMOD=0, it excludes the gate edge. ▪ Otherwise, it includes the gate edge.
RBDB	Resistance connected between dbNode and bNode.
RBODYMOD	Substrate resistance network model selector.
RBPB	Resistance connected between bNodePrime and bNode.
RBPB	Resistance connected between bNodePrime and dbNode.
RBPS	Resistance connected between bNodePrime and sbNode.
RBSB	Resistance connected between sbNode and bNode.
RDC	Drain contact resistance for per-finger device.
RGATEMOD	Gate resistance model selector.
RGEOMOD	Source/drain diffusion resistance and contact model selector—specifies the end S/D contact type: point wide or merged) and how to compute the S/D parasitics resistance.
RSC	Source contact resistance for per-finger device.
TRNQSMOD	Transient NQS model selector.
W	BSIM4 MOSFET channel width in meters.

Parameter	Description
WNFLAG	Turn on to select bin model based on width per NF for multi-finger devices.
MULID0	Scaling factor of drain current, the default is 1.0.
VER_CONTROL	<ul style="list-style-type: none"> ▪ VER_CONTROL=0: (Default) Version control is off ▪ VER_CONTROL=1: Version control is on; the simulation will abort for non-supported version

Improvements Over BSIM3v3

BSIM4 includes the following major improvements and additions over BSIM3v3:

- An accurate new model of the intrinsic input resistance (R_{ii}) for both RF, high-frequency analog, and high-speed digital applications
- A flexible substrate resistance network for RF modeling
- A new accurate channel thermal noise model, and a noise partition model for the induced gate noise
- A non-quasi-static (NQS) model consistent with the R_{ii} -based RF model, and a consistent AC model that accounts for the NQS effect in both transconductances and capacitances
- An accurate gate direct tunneling model
- A comprehensive and versatile geometry-dependent parasitics model for source/drain connections and multi-finger devices
- An improved model for steep vertical retrograde doping profiles
- A better model for pocket-implanted devices in V_{th} , the bulk charge effect model, and R_{out}
- An asymmetrical and bias-dependent source/drain resistance, either internal or external to the intrinsic MOSFET
- Accepts either the electrical or physical gate oxide thickness as the model input in a physically accurate manner
- A quantum mechanical charge-layer-thickness model for both IV and CV
- A more accurate mobility model for predictive modeling

- A gate-induced drain leakage (GIDL) current model, not available in earlier BSIM models
- An improved unified flicker (1/f) noise model, which is smooth over all bias regions, and which considers the bulk charge effect
- Different diode IV and CV characteristics for the source and drain junctions
- A junction diode breakdown with or without current limiting
- A dielectric constant of the gate dielectric as a model parameter
- `.OPTION LIST` now prints the total capacitances, instead of just the intrinsic capacitances for the BSIM4 (Level 54) MOSFET model

BSIM4.2.1 has the following improvements over BSIM4.2.0:

- A new GISL (Gate Induced Source Leakage) current component corresponds to the same current at the drain side (GIDL).
- The warning limits for effective channel length, channel width, and gate oxide thickness have been reduced to avoid unnecessary warnings if you use BSIM4 aggressively, beyond the desired model card application ranges.
- The DELTOX parameter in the MOS active element (M) models the relative variation on the trans conductance (oxide thickness) of the MOS in Monte Carlo analysis.
- `.OPTION LIST` can now print an element summary for the MOSFET Level=54 model

Parameter Range Limit for BSIM4 Level 54

Simulation reports either a warning or a fatal error if BSIM3v3 parameters fall outside predefined ranges. These range limitations prevent (or at least warn of) potential numerical problems.

To control the maximum number of simulation warning messages printing to the output file, use:

```
.OPTION WARNLIMIT=#
```

In the preceding `.OPTION` statement, # is the maximum number of warning messages that simulation reports. The default `WARNLIMIT` value is 1. In some

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Level 54 BSIM4 Model

cases (as noted in [Table 137](#) below), simulation checks parameters only if you set the `PARAMCHK=1` model parameter.

Table 137 Model Parameter Range Limit, Level 54

Parameter	Limits	Comment
toxref	≤ 0 fatal	
lpe0	$< -\text{leff}$, fatal	
lintnoi	$> \text{leff}/2$, fatal	if (version) ≥ 4.399999
lpeb	$< -\text{leff}$, fatal	
phin	< -0.4 fatal	if (version) ≥ 4.4 phin ≤ 0 fatal
ndep	≤ 0 fatal	
nsub	≤ 0 fatal	
ngate	$< 0, > 1.0\text{e}25$ fatal	
xj	≤ 0 fatal	
dvt1	< 0 fatal	
dvt1w	< 0 fatal	
w0	$w0 = -\text{weff}$ fatal	
dsub	< 0 fatal	
b1	$b1 = -\text{weff}$ fatal	
delta	< 0 fatal	
pclm	≤ 0 fatal	
drout	< 0 fatal	
pscbe2	≤ 0 fatal	
nf	< 1 fatal	
ngcon	< 1 fatal	If ngcon $\neq 1, 2$ warn and set 1

Table 137 Model Parameter Range Limit, Level 54

Parameter	Limits	Comment
gbmin	< 1.0e-20 warn	
noff	=0 warn and set 1; < 0.1 warn	if (version < 4.2999 stiMod=2) noff > 4 warn
voffcv	< -0.5 warn	if (version<4.2999 stiMod=2) voffcv > 0.5 warn
clc	< 0 fatal	
moin	< 5.0, > 25 warn	
acde	< 0.1, > 1.6 warn	if (version < 4.29999) acde<0.4 warn
ckappas	< 0.02 warn and set 0.02	if (version >= 4.299999 &&stiMod != 2) version < 4.299999)
ckappad	< 0.02 warn and set 0.02	if (version >= 4.299999 &&stiMod != 2) version < 4.299999)
if paramchk=1 the following parameter limit range is added		
leff	<= 1e-9 warn	
leffcv	<= 1e-9 warn	
weff	<= 1e-9 warn	
weffcv	<= 1e-9 warn	
toxe	Toxe + Delttox < 1e-10 warn	
toxp	Toxp + Delttox < 1e-10 warn	
toxm	< 1e-10 warn	
ndep	<= 1e12, >= 1e21 warn	
nsub	<= 1e14, >= 1e21 warn	

Table 137 Model Parameter Range Limit, Level 54

Parameter	Limits	Comment
ngate	$0 < \text{ngate} \leq 1 \text{e}18$ warn	
dvt0	< 0 warn	
w0	$w0 + w_{\text{eff}} < 1 \text{e}-7$ warn	if (version ≥ 4.39999) $w0 + w_{\text{eff}} < 1 \text{e}-9$ warn
nfactor	< 0 warn	
cdsc	< 0 warn	
cdscd	< 0 warn	
eta0	< 0 warn	
b1	$b1 + w_{\text{eff}} < 1 \text{e}-7$ warn	if (version ≥ 4.39999) $b1 + w_{\text{eff}} < 1 \text{e}-9$ warn
a2	< 0.01 warn, set 0.01; > 1.0 warn, set 1 and a1 set 0	- If the total calculated A2 (including binnings) is smaller than 0.01, then it is set to 0.01. - If the total A2 is larger than 1, it is set to 1.
prwg	< 0 warn, set 0	
rdsw	< 0 warn, set 0	
rds0	< 0 warn, set 0	
rdswmin	< 0 warn, set 0	
vsattemp	$< 1 \text{e}3$ warn	
lambda	$> 1 \text{e}-9$ warn	if (version ≥ 4.3)
vth	$< 6 \text{e}4$ warn	if (version ≥ 4.3)
xn	< 3	if (version ≥ 4.3)
lc	< 0	if (version ≥ 4.3)

Table 137 Model Parameter Range Limit, Level 54

Parameter	Limits	Comment
prout	< 0 fatal	
pdits	< 0 fatal	
pditsl	< 0 fatal	
pdibl1	< 0 warn	
pdibl2	< 0 warn	
lodk2	<= 0 warn	if (version>= 4.4)
lodeta0	<= 0 warn	if (version>= 4.4)
nigbinv	<= 0 fatal	
nigbacc	<= 0 fatal	
nigc	<= 0 fatal	
poxedge	<= 0 fatal	
pigcd	<= 0 fatal	
rshg	<= 0 warn	if (version >= 4.299999 && stiMod != 2)
xrcrg1	<=0 warn	if (version >= 4.299999 && stiMod != 2)
sl	< 1e-7 warn; < 0 fatal	
sw	< 1e-7 warn; < 0 fatal	
sa	< 0 fatal	
sb	< 0 fatal	
sd	< 0 fatal	If nf>1
sa0	<= 0 fatal	
sb0	<= 0 fatal	

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Table 137 Model Parameter Range Limit, Level 54

Parameter	Limits	Comment
wlod	< 0 fatal	
kvsat	< -1.0, > 1.0 fatal	
lodk2	<= 0	
lodeta0	<= 0	
nf	>1 fatal	if (stiMod == 2)
cgdo	< 0 warn	
cgso	< 0 warn	
cgbo	< 0 warn	if (version >4.4999)
tnoia	< 0 warn	
tnob	< 0 warn	
rnoia	< 0 warn	
rnoib	< 0 warn	
ntnoi	< 0 warn	
Njs	< 0 warn	
Njd	< 0 warn	
Njts	< 0 warn	
Njtssw	< 0 warn	
Njtsswg	< 0 warn	
Njtstd	< 0 warn	
Njtsswd	< 0 warn	
Njtsswgd	< 0 warn	

Table 137 Model Parameter Range Limit, Level 54

Parameter	Limits	Comment
Vtss	< 0 warn	
Vtsd	< 0 warn	
vtssws	< 0 warn	
vtsswd	< 0 warn	
vtsswgs	< 0 warn	
vtsswgd	< 0 warn	
mjs	>= 0.99 warn	
mjsws	>= 0.99 warn	
mjswgs	>= 0.99 warn	
mjd	>= 0.99 warn	
mjswd	>= 0.99 warn	
mjswgd	>= 0.99 warn	
scref	< 0 warn	if (wpemod=1)
sca	< 0 warn	if (wpemod=1)
scb	< 0 warn	if (wpemod=1)
scc	< 0 warn	if (wpemod=1)
sc	< 0 warn	if (wpemod=1)

TSMC Diode Model

HSPICE MOSFET Level 54 (BSIM4) supports a TSMC junction diode model. You can use this TSMC junction diode model to simulate the temperature dependence, source/body, and drain/body currents of a junction diode.

Note: For a complete description of this effect model, visit the official UCB BSIM web site:

<http://www-device.eecs.berkeley.edu/~bsim3/>

You can order either of these models directly from Taiwan Semiconductor Manufacturing Company (TSMC)—not from Synopsys. See the TSMC web site: <http://www.tsmc.com>

BSIM4 Juncap2 Model

HSPICE BSIM4 support for the juncap2 junction model is based on Philips' JUNCAP2 model in BSIM4 version 4.2 and later. You use the flag `JUNCAP=0` to turn on the built-in BSIM4 default junction model. You can use `JUNCAP=1` to switch to the Juncap1 model and `JUNCAP=2` to access the Juncap2 model. The Juncap2 model has 2 versions, 200.0 and 200.1, which can be toggled using the `JCAP2VERSION` flag.

Table 138 BSIM4 Juncap2 Model Parameters

Parameter	Unit	Default	Description
JUNCAP	-	0	Flag to turn on juncap diode model, 1 for juncap1, 2 for juncap2
JCAP2VERSION	-	200.1	Juncap2 model version (200.0, 200.1)
IMAX	A	1000	Maximum current up to which forward current behaves exponentially
CJORBOT	F/m ²	1.00E-003	Zero-bias capacitance per unit-of-area of bottom component
CJORSTI	F/m ²	1.00E-009	Zero-bias capacitance per unit-of-length of STI-edge component
CJORGAT	F/m ²	1.00E-009	Zero-bias capacitance per unit-of-length of gate-edge component
VBIRBOT	V	1	Built-in voltage at the reference temperature of bottom component

Table 138 BSIM4 Juncap2 Model Parameters (Continued)

Parameter	Unit	Default	Description
VBIRSTI	V	1	Built-in voltage at the reference temperature of TI-edge component
VBIRGAT	V	1	Built-in voltage at the reference temperature of gate-edge component
PBOT	-	0.5	Grading coefficient of bottom component
PSTI	-	0.5	Grading coefficient of STI-edge component
PGAT	-	0.5	Grading coefficient of gate-edge component
PHIGBOT	V	1.16	Zero-temperature bandgap voltage of bottom component
PHIGSTI	V	1.16	Zero-temperature bandgap voltage of STI-edge component
PHIGGAT	V	1.16	Zero-temperature bandgap voltage of gate-edge component
IDSATRBOT	A/m ²	1.00E-012	Saturation current density at the reference temperature of bottom component
IDSATRSTI	A/m	1.00E-018	Saturation current density at the reference temperature of STI-edge component
IDSATRGAT	A _m	1.00E-018	SATURATION current density at the reference temperature of gate-edge component
CSRHBOT	A/m ²	1.00E+002	Shockley-Read-Hall prefactor of bottom component
CSRHSTI	A/m ²	1.00E-004	Shockley-Read-Hall prefactor of STI-edge component
CSRHGAT	A/m ²	1.00E-004	Shockley-Read-Hall prefactor of gate-edge component
XJUNSTI	m	1.00E-007	Junction depth of STI-edge component
XJUNGAT	m	1.00E-007	junction depth of gate-edge component
CTATBOT	A/m ³	1.00E+002	Trap-assisted tunneling prefactor of bottom component

Table 138 BSIM4 Juncap2 Model Parameters (Continued)

Parameter	Unit	Default	Description
CTATSTI	A/m ²	1.00E-004	Trap-assisted tunneling prefactor of STI-edge component
CTATGAT	A/m ²	1.00E-004	Trap-assisted tunneling prefactor of gate-edge component
MEFFTATBOT	-	0.25	Effective mass (in units of m0) for trap-assisted tunneling of bottom component
MEFFTATSTI	-	0.25	Effective mass (in units of m0) for trap-assisted tunneling of STI-edge component
MEFFTATGAT	-	0.25	Effective mass (in units of m0) for trap-assisted tunneling of gate-edge component
CBBTBOT	AV ⁻³	1.00E-012	Band-to-band tunneling prefactor of bottom component
CBBTSTI	AV ⁻³ m	1.00E-018	Band-to-band tunneling prefactor of STI-edge component
CBBTGAT	AV ⁻³ m	1.00E-018	Band-to-band tunneling prefactor of gate-edge component
FBBTRBOT	V/m	1.00E+009	Normalization field at the reference temperature for band-to-band tunneling of bottom component
FBBTRSTI	V/m	1.00E+009	Normalization field at the reference temperature for band-to-band tunneling of STI-edge component
FBBTRGAT	V/m	1.00E+009	Normalization field at the reference temperature for band-to-band tunneling of gate-edge component
STFBBTBOT	1/K	-1.00E-003	temperature scaling parameter for band-to-band tunneling of bottom component
STFBBTSTI	1/K	-1.00E-003	temperature scaling parameter for band-to-band tunneling of STI-edge component
STFBBTGAT	1/K	-1.00E-003	temperature scaling parameter for band-to-band tunneling of gate-edge component

Table 138 BSIM4 Juncap2 Model Parameters (Continued)

Parameter	Unit	Default	Description
VBRBOT	V	10	breakdown voltage of bottom component
VBRSTI	V	10	breakdown voltage of STI-edge component
VBRGAT	V	10	breakdown voltage of gate-edge component
PBRBOT	V	4	breakdown onset tuning parameter of bottom component
PBRSTI	V	4	breakdown onset tuning parameter of STI-edge component
PBRGA	V	4	breakdown onset tuning parameter of gate-edge component

BSIM4 STI/LOD

HSPICE BSIM4 supports the full STI (Shallow Trench Isolation) or LOD (Length of Oxide Definition) induced mechanical stress-effect model (for version 4.3 or later), which was first released in the UCB BSIM4.3.0 model version. HSPICE BSIM4 turns on the simulation of this effect when the following conditions (consistent with those of the UCB BSIM4 model) are satisfied:

```
if (VERSION >=4.3)
{
  if ((SA > 0 and SB > 0 and NF==1) or ( SA > 0 and SB > 0 and (
NF >1 and SD > 0 )))
  { UCB's STI/LOD model is turned on}
}
```

If $VERSION \geq 4.3$, the STI model is not dependent on $STIMOD=0$ or 1 . In this case, the STI model is applied to the model similar to the UCB STI model (see [Table 139](#)). When parameter values that satisfy $SA > 0$, $SB > 0$, $NF > 1$, and $SD = 0$ are given in model cards, no evaluation of such effect is performed.

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Level 54 BSIM4 Model

Table 139 Supported HSPICE BSIM4 STI/LOD Parameters

Parameter	Unit	Default	Bin?	Description
SA (instance parameter)		0.0		Distance between S/D diffusion edge to poly gate edge from one side. If not given, or, if (≤ 0), the stress effect is turned off.
SB (instance parameter)		0.0		Distance between S/D diffusion edge to poly gate edge from the other side. If not given or, if (≤ 0), the stress effect is turned off
SD (instance parameter)		0.0		Distance between neighboring fingers. For $NF > 1$, If not given or (≤ 0), stress effect is turned off
STIMOD (Also instance parameter)		0.0 ($V < 4.3$) 1.0 ($V \geq 4.3$)		STI model selector, which gives priority to the instance parameter. <ul style="list-style-type: none"> 0: No STI effect. 1: UCB's STI model 2: TSMC's STI model
SAREF	M	1e-06	No	Reference distance for SA, > 0.0
SBREF	M	1e-06	No	Reference distance for SB, > 0.0
WLOD	M	0.0	No	Width parameter for stress effect
KU0	M	0.0	No	Mobility degradation/enhancement coefficient for stress effect
KVSAT	M	0.0	No	Saturation velocity degradation/enhancement parameter for stress effect. $1.0 \leq kvsat \leq 1.0$
TKU0		0.0	No	Temperature coefficient of KU0
LKU0		0.0	No	Length dependence of KU0
WKU0		0.0	No	Width dependence of KU0
LLODKU0		0.0	No	Length parameter for U0 stress effect, > 0

Table 139 Supported HSPICE BSIM4 STI/LOD Parameters

Parameter	Unit	Default	Bin?	Description
WLODKU0		0.0	No	Width parameter for U0 stress effect, >0
KVTH0	V*m	0.0	No	Threshold shift parameter for stress effect
WKVTH0		0.0	No	Width dependence of KVTH0
PKVTH0		0.0	No	Cross-term dependence of KVTH0
LLODVTH		0.0	No	Length parameter for Vth stress effect, >0
WLODVTH		0.0	No	Width parameter for Vth stress effect, >0
STK2		0.0	No	K2 shift factor related to VTh0 change
LODK2	m	1.0	No	K2 shift modification factor for stress effect, >0
STETA0		0.0	No	ETA0 shift factor related to VTH0 change
LODETA0	M	1.0	No	ETA0 shift modification factor for stress effect, >0

LMLT and WMLT in BSIM4

You can use `LMLT` and `WMLT` to shrink the length and width in memory design. The `LMLT` and `WMLT` parameters are unitless, and are used to scale (usually scale down) MOSFET drawn length and width (specified in BSIM4 MOSFET instance lines), respectively. This makes memory design and netlist creation quite convenient because most (if not all) memory circuits use the smallest feature sizes as the process capability improves, even within the same generation of CMOS technology.

The shrunken device length and width will then be further offset (by `XL` and `XW`, respectively) to the actual device size in lithography and etching process steps, and finally to the electrical size as a result of subsequent ion implementation and annealing steps.

Name (Alias)	Default	Description
LMLT	1.0	Channel length shrinking factor
WMLT	1.0	Device width shrinking factor

Both LMLT and WMLT must be greater than 0; if not, simulation resets them to 1.0 (default) and issues a warning message.

To use these two parameters, add them in the model cards, without any other modifications. For example:

```
.model nmos nmos
+ level=54 lmlt=0.85 wmlt=0.9
```

- The drawn channel length (L) is multiplied by LMLT.
- The drawn channel width (W) is multiplied by WMLT,

BSIM4 evaluates the effective length and width, L_{eff} and W_{eff} , as:

```
Leff=Lnew - 2.0 * dL
Weff=Wnew - 2.0 * dW
```

L_{new} and W_{new} are evaluated as:

```
Lnew=L + XL
Wnew=W + XW
```

dL and dW are evaluated with L_{new} and W_{new}:

```
T0=pow(Lnew, LLN)
T1=pow(Wnew, LWN)
dL=LINT + LL/T0 + LW / T1 + LWL / (T0*T1)
T2=pow(Lnew, WLN)
T3=pow(Wnew, WWN)
dW=WINT + WL / T2 + WW / T3 + WWL / (T2*T3)
```

Similarly, the preceding equations determine the L_{dlc}, L_{dlcig}, L_{effCV} , W_{dwc}, W_{dwcig}, W_{effCV} , W_{effCJ} , g_{rgeltd}, and W_{new} model variables and quantities.

When multiplied by the LMLT and WMLT parameters, L_{eff} and W_{eff} become:

```
Leff=Lnew' - 2.0 * dL
Weff=Wnew' - 2.0 * dL
```

L_{new}' and W_{new}' are evaluated as:

$$L_{new}' = L * L_{MLT} + XL$$

$$W_{new}' = W * W_{MLT} + XW$$

Similarly, dL , dW , L_{dlc} , L_{dlcig} , L_{effCV} , W_{dwc} , W_{dwcig} , W_{effCV} , W_{effCJ} , and $grgeltd$ are all evaluated from L_{new}' and W_{new}' .

HSPICE Junction Diode Model and ACM

BSIM4 now supports Area Calculation Method (ACM) similar to BSIM3v3 for the following models and corresponding ACM values:

- For the HSPICE junction model, specify $ACM=0,1,2$, or 3 .
- For the Berkeley BSIM4 junction model, specify $ACM=10,11,12$, or 13 .

For the junction current, junction capacitance, and parasitic resistance equations corresponding to $ACM=0,1,2,3$ see [MOSFET Diode Models on page 701](#).

Table 140 MOSFET Level 54 Parameters

Parameter	Description
nf	Number of device fingers
min	Whether to minimize the number of drain or source diffusions for even-number fingered device
rbdb	Resistance connected between the internal drain-side body node and the external body node
rbsb	Resistance connected between the internal source-side body node and the external body node
rbpb	Resistance connected between the internal reference body node and the external body node
rbps	Resistance connected between the internal reference body node and the internal drain-side body node
rbpd	Resistance connected between the internal reference body node and the internal source-side body node
trnqsmod	Transient NQS model selector

Table 140 MOSFET Level 54 Parameters

Parameter	Description
acnqsmode	AC small-signal NQS model selector
rbodysmod	Substrate resistance network model selector
rgatemod	Gate resistance model selector
geomod	Geometry-dependent parasitics model selector
rgeomod	Source/Drain diffusion resistance and contact model selector

MOSFET Level 54 uses the generic MOSFET model parameters described in [Chapter 2, Common MOSFET Model Parameters](#). It also uses the parameters described in this section, which apply only to MOSFET Level 54.

The simulation calculates R_d and R_s as follows:

$$R_d(TEMP) = R_d(TNOM) * (1 + TRD * (TEMP - TNOM))$$

$$R_s(TEMP) = R_s(TNOM) * (1 + TRS * (TEMP - TNOM))$$

Table 141 Instance Parameters, Level 54

Parameter	Unit	Default	Description
RDC	ohm	0.0	Drain contact resistance for the per-finger device
RSC	ohm	0.0	Source contact resistance for the per-finger device
DELVTO (DELVT0)	V	0.0	Shift in the zero-bias threshold voltage (VTH0)
MULU0		1.0	Low-field mobility (U0) multiplier
DELK1	$V^{1/2}$		Shift in the body bias coefficient (K1)
DELNFCT		0.0	Shift in subthreshold swing factor (NFACTOR)

Table 142 Model Selectors/Controllers, Level 54

Parameter	Default	Binnable	Description
VERSION	4.5	NA	Model version number
BINUNIT	1	NA	Binning unit selector
PARAMCHK	1	NA	Switch for the parameter check
MOBMOD	1	NA	Mobility model selector
RDSMOD	0	NA	Bias-dependent source/drain resistance model selector
IGCMOD	0	NA	Gate-to-channel tunneling current model selector
IGBMOD	0	NA	Gate-to-substrate tunneling current model selector
CAPMOD	2	NA	Capacitance model selector
RGATEMOD	0 (no gate resistance)		Gate resistance model selector
RBODYMOD	0 (network off)	NA	Substrate resistance network model selector
TRNQSMOD	0	NA	Transient NQS model selector
ACNQSMOD	0	NA	AC small-signal NQS model selector
FNOIMOD	1	NA	Flicker noise model selector
TNOIMOD	0	NA	Thermal noise model selector
DIOMOD	1	NA	Source/drain junction diode IV model selector
TEMPMOD	0	NA	Temperature mode selector

Chapter 6: MOSFET Models (BSIM): Levels 47 through 72**Level 54 BSIM4 Model***Table 142 Model Selectors/Controllers, Level 54*

Parameter	Default	Binnable	Description
PERMOD	1	NA	PS/PD includes/excludes the gate-edge perimeter
GEOMOD	0 (isolated)	NA	Geometry-dependent parasitics model selector
RGEOMOD	0 (no S/D diffusion resistance)	NA	Source/drain diffusion resistance and contact model selector
WPEMOD	0	NA	Flag for WPE model (WPEMOD=1 to activate this model)

Table 143 Level 54 Process Parameters, Level 54

Parameter	Default	Binnable	Description
EPSROX	3.9 (SiO ₂)	No	Gate dielectric constant relative to vacuum
TOXE	3.0e-9m	No	Electrical gate equivalent oxide thickness
TOXP	TOXE	No	Physical gate equivalent oxide thickness
TOXM	TOXE	No	Tox at which simulation extracts parameters
DTOX	0.0m	No	Defined as (TOXE-TOXP)
XJ	1.5e-7m	Yes	S/D junction depth
GAMMA1 (γ_1 in equation)	calculated ($V^{1/2}$)	Yes	Body-effect coefficient near the surface
GAMMA2 (γ_2 in equation)	calculated ($V^{1/2}$)	Yes	Body-effect coefficient in the bulk
NDEP	1.7e17cm ⁻³	Yes	Channel doping concentration at the depletion edge for the zero body bias

Table 143 Level 54 Process Parameters, Level 54 (Continued)

Parameter	Default	Binnable	Description
NSUB	$6.0\text{e}16\text{cm}^{-3}$	Yes	Substrate doping concentration
NGATE	0.0cm^{-3}	Yes	Poly Si gate doping concentration
NSD	$1.0\text{e}20\text{cm}^{-3}$	Yes	Source/drain doping concentration
VBX	calculated (v)	No	V_{bs} at which the depletion region width equals X_T
XT	$1.55\text{e-}7\text{m}$	Yes	Doping depth
RSH	0.0ohm/square	No	Source/drain sheet resistance
RSHG	0.1ohm/square	No	Gate electrode sheet resistance

Table 144 Basic Model Parameters, Level 54

Parameter	Default	Binnable	Description
A0	1.0	Yes	Coefficient of the channel-length dependence of the bulk charge effect
A1	0.0V^{-1}	Yes	First non-saturation effect parameter
A2	1.0	Yes	Second non-saturation factor
AGS	0.0V^{-1}	Yes	Coefficient of the V_{gs} dependence of the bulk charge effect
B0	0.0m	Yes	Bulk charge effect coefficient for the channel width
B1	0.0m	Yes	Bulk charge effect width offset
CDSC	$2.4\text{e-}4\text{F/m}^2$	Yes	Coupling capacitance between the source/drain and the channel
CDSCB	$0.0\text{F}/(\text{Vm}^2)$	Yes	Body-bias sensitivity of CDSC

Table 144 Basic Model Parameters, Level 54 (Continued)

Parameter	Default	Binnable	Description
CDSCD	0.0(F/Vm ²)	Yes	Drain-bias sensitivity of DCSC
CIT	0.0F/m2	Yes	Interface trap capacitance
DELTA δ (in equation)	0.01V	Yes	Parameter for DC V_{dseff}
DROUT	0.56	Yes	Channel-length dependence of the DIBL effect on R_{out}
DSUB	DROUT	Yes	DIBL coefficient exponent in the subthreshold region
DVT0	2.2	Yes	First coefficient of the short-channel effect on V_{th}
DVT0W	0.0	Yes	First coefficient of the narrow width effect on V_{th} for a small channel length
DVT1	0.53	Yes	Second coefficient of the short-channel effect on V_{th}
DVT1W	5.3e6m ⁻¹	Yes	Second coefficient of the narrow width effect on V_{th} for a small channel length
DVT2	-0.032V ⁻¹	Yes	Body-bias coefficient of the short-channel effect on V_{th}
DVT2W	-0.032V ⁻¹	Yes	Body-bias coefficient of narrow width effect for small channel length
DVTP0	0.0m	Yes	First coefficient of the drain-induced V_{th} shift due to long-channel pocket devices
DVTP1	0.0V ⁻¹	Yes	First coefficient of the drain-induced V_{th} shift due to long-channel pocket devices
DWB	0.0m/V ^{1/2}	Yes	Coefficient of the body bias dependence of the Weff bias dependence

Table 144 Basic Model Parameters, Level 54 (Continued)

Parameter	Default	Binnable	Description
DWG	0.0m/V	Yes	Coefficient of gate bias dependence of W_{eff}
ETA0	0.08	Yes	DIBL coefficient in the subthreshold region
ETAB	-0.07V ⁻¹	Yes	Body-bias coefficient for the DIBL effect for the subthreshold
EU	1.67 (NMOS); 1.0 (PMOS)	No	Exponent for the mobility degradation of MOBMOD=2
FPROUT	0.0V/m ^{0.5}	Yes	Effect of the pocket implant on R_{out} degradation
K1	0.5V ^{1/2}	Yes	First-order body bias coefficient
K2	0.0	Yes	Second-order body bias coefficient
K3	80.0	Yes	Narrow width coefficient
K3B	0.0V ⁻¹	Yes	Body effect coefficient of K3
KETA	-0.047V ⁻¹	Yes	Body-bias coefficient of the bulk charge effect
LINT	0.0m	No	Channel-length offset parameter
LP	1e-8(m)	Yes	Mobility channel length degradation of MOBMOD=2
LPE0	1.74e-7m	Yes	Lateral non-uniform doping parameter
LPEB	0.0m	Yes	Lateral non-uniform doping effect on K1
MINV	0.0	Yes	V_{gsteff} fitting parameter for the moderate inversion condition
NFACTOR	1.0	Yes	Subthreshold swing factor
PCLM	1.3	Yes	Channel-length modulation parameter

Chapter 6: MOSFET Models (BSIM): Levels 47 through 72

Level 54 BSIM4 Model

Table 144 Basic Model Parameters, Level 54 (Continued)

Parameter	Default	Binnable	Description
PDIBLC1	0.39	Yes	Parameter for the DIBL effect on R_{out}
PDIBLC2	0.0086	Yes	Parameter for the DIBL effect on R_{out}
PDIBLCB	$0.0V^{-1}$	Yes	Body bias coefficient of the DIBL effect on R_{out}
PDITS	$0.0V^{-1}$	Yes	Impact of the drain-induced V_{th} shift on R_{out}
PDITSD	$0.0V^{-1}$	Yes	V_{ds} dependence of the drain-induced V_{th} shift for R_{out}
PDITSL	$0.0m^{-1}$	No	Channel-length dependence of the drain-induced V_{th} shift for R_{out}
PHIN	0.0V	Yes	Non-uniform vertical doping effect on the surface potential
PSCBE1	4.24e8V/m	Yes	First substrate current induced body-effect parameter
PSCBE2	1.0e-5m/V	Yes	Second substrate current induced body-effect parameter
PVAG	0.0	Yes	Gate-bias dependence of Early voltage
U0	$0.067m^2/(Vs)$ (NMOS); $0.025m^2/(Vs)$ (PMOS)	Yes	Low-field mobility
UA	1.0e-9m/V for $MOBMOD=0$ and 1; 1.0e-15m/V for $MOBMOD=2$	Yes	Coefficient of the first-order mobility degradation due to the vertical field
UB	$1.0e-19m^2/V^2$	Yes	Coefficient of the second-order mobility degradation due to the vertical field

Table 144 Basic Model Parameters, Level 54 (Continued)

Parameter	Default	Binnable	Description
UC	-0.0465V ⁻¹ for MOB-MOD=1; -0.0465e-9 m/V ² for MOBMOD=0 and 2	Yes	Coefficient of the mobility degradation due to the body-bias effect
UD	1e14(1/m ²)	Yes	Mobility coulomb scattering coefficient
UP	0(1/m ²)	Yes	Mobility channel length coefficient
VBM	-3.0V	Yes	Maximum applied body bias in the VTH0 calculation
VFB	-1.0V	Yes	Flat-band voltage (PHIN)
VOFF	-0.08V	Yes	Offset voltage in subthreshold region for large W and L
VOFFL	0.0mV	No	Channel-length dependence of VOFF
VSAT	8.0e4m/s	Yes	Saturation velocity
VTH0 or VTHO	0.7V (NMOS) -0.7V (PMOS)	Yes	Long-channel threshold voltage at V _{bs} =0
W0	2.5e-6m	Yes	Narrow width parameter
WINT	0.0m	No	Channel-width offset parameter

Table 145 Parameters for Asymmetric and Bias-Dependent Rds Model, Level 54

Parameter	Default	Binnable	Description
PRWB	0.0V-0.5	Yes	Body-bias dependence of the LDD resistance
PRWG	1.0V-1	Yes	Gate-bias dependence of the LDD resistance

Chapter 6: MOSFET Models (BSIM): Levels 47 through 72**Level 54 BSIM4 Model***Table 145 Parameters for Asymmetric and Bias-Dependent Rds Model, Level 54*

Parameter	Default	Binnable	Description
RDSW	200.0 ohm(μ m)WR	Yes	Zero bias LLD resistance per unit width for RDSMOD=0
RDSWMIN	0.0 ohm(μ m)WR	No	LDD resistance per unit width at high V_{gs} and zero V_{bs} for RDSMOD=0
RDW	100.0 ohm(μ m)WR	Yes	Zero bias lightly-doped drain resistance $R_d(v)$ per unit width for RDSMOD=1
RSW	100.0 ohm(μ m)WR	Yes	Zero bias lightly-doped source resistance $R_s(V)$ per unit width for RDSMOD=1
RSWMIN	0.0 ohm(μ m)WR	No	Lightly-doped source resistance per unit width at high V_{gs} and zero V_{bs} for RDSMOD=1
WR	1.0	Yes	Channel-width dependence of the LDD resistance
NRS	1.0	No	Number of source diffusion squares
NRD	1.0	No	Number of drain diffusion squares

Table 146 Impact Ionization Current Model Parameters, Level 54

Parameter	Default	Binnable	Description
ALPHA0	0.0Am/V	Yes	First parameter of the impact ionization current
ALPHA1	0.0A/V	Yes	Isup parameter for length scaling
BETA0	30.0V	Yes	Second parameter for the impact ionization current

Table 147 Gate-Induced Drain Leakage Model Parameters, Level 54

Parameter	Default	Binnable	Description
AGIDL	0.0ohm	Yes	Pre-exponential coefficient for GIDL
AGISL	0.0	Yes	Pre-exponential coefficient for GISL
BGIDL	2.3e9V/m	Yes	Exponential coefficient for GIDL
BGISL	2.3e9V/m	Yes	Exponential coefficient for GISL
CGIDL	0.5V3	Yes	Parameter for the body-bias effect on GIDL
EGIDL	0.8V	Yes	Fitting parameter for band bending for GIDL
EGISL	0.8V	Yes	Fitting parameter for Bandbending

Table 148 Gate Dielectric Tunneling Current Model Parameters, Level 54

Parameter	Default	Binnable	Description
AIGS	1.36e-2(NMOS) and 9.8e-3(PMOS)	Yes	Parameter for I_{gs}
AIGBACC	$0.43 (F_s^2/\epsilon_g)^{0.5} m^{-1}$	Yes	Parameter for I_{gb} in the accumulation
AIGBINV	$0.35 (F_s^2/\epsilon_g)^{0.5} m^{-1}$	Yes	Parameter for I_{gb} in the inversion
AIGC	0.054 (NMOS) and 0.31 (PMOS) $(F_s^2/\epsilon_g)^{0.5} m^{-1}$	Yes	Parameter for I_{gcs} and I_{gcd}
AIGD	1.36e-2(NMOS) and 9.8e-3(PMOS)	Yes	Parameter for I_{gd}
AIGSD	0.43 (NMOS) and 0.31 (PMOS) $(F_s^2/\epsilon_g)^{0.5} m^{-1}$	Yes	Parameter for I_{gs} and I_{gd}

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Level 54 BSIM4 Model

Table 148 Gate Dielectric Tunneling Current Model Parameters, Level 54

Parameter	Default	Binnable	Description
BIGBACC	$0.054 (F_s^2/\epsilon_g)^{0.5} \text{ m}^{-1}\text{V}^{-1}$	Yes	Parameter for I_{gb} in the accumulation
BIGBINV	$0.03 (F_s^2/\epsilon_g)^{0.5} \text{ m}^{-1}\text{V}^{-1}$	Yes	Parameter for I_{gb} in the inversion
BIGC	0.054 (NMOS) and 0.024 (PMOS) $(F_s^2/\epsilon_g)^{0.5} \text{ m}^{-1}\text{V}^{-1}$	Yes	Parameter for I_{gcs} and I_{gcd}
BIGD	1.71e-3(NMOS) and 7.59e-4(PMOS)	Yes	Parameter for I_{gd}
BIGS	1.71e-3(NMOS) and 7.59e-4(PMOS)	Yes	Parameter for I_{gs}
BIGSD	0.054 (NMOS) and 0.024 (PMOS) $(F_s^2/\epsilon_g)^{0.5} \text{ m}^{-1}\text{V}^{-1}$	Yes	Parameter for I_{gs} and I_{gd}
CIGBACC	0.075 V^{-1}	Yes	Parameter for I_{gb} in the accumulation
CIGBINV	0.0006 V^{-1}	Yes	Parameter for I_{gb} in the inversion
CIGC	0.075 (NMOS) and 0.03(PMOS) V^{-1}	Yes	Parameter for I_{gcs} and I_{gcd}
CIGD	0.075(NMOS) and 0.03(PMOS)	Yes	Parameter for I_{gd}
CIGS	0.075(NMOS) and 0.03(PMOS)	Yes	Parameter for I_{gs}
CIGSD	0.075 (NMOS) and 0.03 (PMOS) V^{-1}	Yes	Parameter for I_{gs} and I_{gd}
DLCIG	LINT	Yes	Source/drain overlap length for I_{gs} and I_{gd}

Table 148 Gate Dielectric Tunneling Current Model Parameters, Level 54

Parameter	Default	Binnable	Description
EIGBINV	1.1V	Yes	Parameter for I_{gb} in the inversion
NIGBACC	1.0	Yes	Parameter for I_{gb} in the accumulation
NIGBINV	3.0	Yes	Parameter for I_{gb} in the inversion
NIGC	1.0	Yes	Parameter for I_{gcs} , I_{gcd} , I_{gs} and I_{gd}
NTOX	1.0	Yes	Exponent for the gate oxide ratio
PIGCD	1.0	Yes	V_{ds} dependence of I_{gcs} and I_{gcd}
POXEDGE	1.0	Yes	Factor for the gate oxide thickness in the source/drain overlap regions
TOXREF	3.0e-9m	No	Nominal gate oxide thickness for the gate dielectric tunneling current model only
VFBSDOFF	0.0V	Yes	Flatband voltage offset parameter

Table 149 Charge/Capacitance Model Parameters, Level 54

Parameter	Default	Binnable	Description
ACDE	1.0m/V	Yes	Exponential coefficient for the charge thickness in CAPMOD=2 for the accumulation and depletion regions
CF	calculated (F/m)	Yes	Fringing field capacitance
CGBO	0.0 (F/m)	No	Gate-bulk overlap capacitance per unit channel length
CGDL	0.0F/m	Yes	Overlap capacitance between gate and lightly-doped source region
CGDO	calculated (F/m)	No	Non LDD region drain-gate overlap capacitance per unit channel width

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Level 54 BSIM4 Model

Table 149 Charge/Capacitance Model Parameters, Level 54

Parameter	Default	Binnable	Description
CGSL	0.0F/m	Yes	Overlap capacitance between the gate and the lightly-doped source region
CGSO	calculated (F/m)	No	Non LDD region source-gate overlap capacitance per unit channel width
CKAPPAD	CKAPPAS	Yes	Coefficient of bias-dependent overlap capacitance for the drain side
CKAPPAS	0.6V	Yes	Coefficient of the bias-dependent overlap capacitance for the source side
CLC	1.0e-7m	Yes	Constant term for the short channel model
CLE	0.6	Yes	Exponential term for the short channel model
DLC	LINT (m)	No	Channel-length offset parameter for the CV model
DWC	WINT (m)	No	Channel-width offset parameter for the CV model
MOIN	15.0	Yes	Coefficient for the gate-bias dependent surface potential
NOFF	1.0	Yes	CV parameter in $V_{gsteff,CV}$ for weak to strong inversion
VFBCV	-1.0V	Yes	Flat-band voltage parameter (for CAPMOD=0 only)
VOFFCV	0.0V	Yes	CV parameter in $V_{gsteff,CV}$ for weak to strong inversion
XPART	0.0	No	Charge partition parameter

Table 150 High-Speed/RF Model Parameters, Level 54

Parameter	Default	Binnable	Description
GBMIN	1.0e-12mho	No	Conductance in parallel with each of the five substrate resistances to avoid potential numerical instability due to an unreasonably large substrate resistance

Table 150 High-Speed/RF Model Parameters, Level 54

Parameter	Default	Binnable	Description
RBDB	50.0 ohm	No	Resistance between dbNode and dbNode
RBDBX0	100 ohms	No	Scaling prefactor for RBDBX
RBDBY0	100 ohms	No	Scaling prefactor for RBDBY
RBPB	50.0 ohm	No	Resistance between bNodePrime and bNode
RBPBX0	100 ohms	No	Scaling prefactor for RBPBX
RBPBXL	0.0	No	Length Scaling parameter for RBPBX
RBPBXNF	0.0	No	Number of fingers Scaling parameter for RBPBX
RBPBXW	0.0	No	Width Scaling parameter for RBPBX
RBPBY0	100 ohms	No	Scaling prefactor for RBPBY
RBPBYL	0.0	No	Length Scaling parameter for RBPBY
RBPBYNF	0.0	No	Number of fingers Scaling parameter for RBPBY
RBPBYW	0.0	No	Width Scaling parameter for RBPBY
RBPD	50.0 ohm	No	Resistance between bNodePrime and dbNode
RBPD0	50 ohms	No	Scaling prefactor for RBPD
RBPDL	0.0	No	Length Scaling parameter for RBPD
RBPDNF	0.0	No	Number of fingers Scaling parameter for RBPD
RBPDW	0.0	No	Width Scaling parameter for RBPD
RBPS	50.0 ohm	No	Resistance between bNodePrime and sbNode
RBPS0	50 ohms	No	Scaling prefactor for RBPS
RBPSL	0.0	No	Length Scaling parameter for RBPS
RBPSNF	0.0	No	Number of fingers Scaling parameter for RBPS

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Level 54 BSIM4 Model

Table 150 High-Speed/RF Model Parameters, Level 54

Parameter	Default	Binnable	Description
RBPSW	0.0	No	Width Scaling parameter for RBPS
RBSB	50.0 ohm	No	Resistance between sbNode and bNode
RBSBX0	100 ohms	No	Scaling prefactor for RBSBX
RBSBY0	100 ohms	No	Scaling prefactor for RBSBY
RBSDBXL	0.0	0.0	Length Scaling parameter for RBSBX and RBDBX
RBSDBXNF	0.0	No	Number of fingers Scaling parameter for RBSBX and RBDBX
RBSDBXW	0.0	No	Width Scaling parameter for RBSBX and RBDBX
RBSDBYL	0.0	No	Length Scaling parameter for RBSBY and RBDBY
RBSDBYNF	0.0	No	Number of fingers Scaling parameter for RBSBY and RBDBY
RBSDBYW	0.0	No	Width Scaling parameter for RBSBY and RBDBY
XRCRG1	12.0	Yes	Parameter for the distributed channel-resistance effect for both intrinsic-input resistance and charge-deficit NQS models
XRCRG2	1.0	Yes	Parameter to account for the excess channel diffusion resistance for both intrinsic input resistance and charge-deficit NQS models

Table 151 Flicker and Thermal Noise Model Parameters, Level 54

Parameter	Default	Binnable	Description
AF	1.0	No	Flicker noise exponent
EF	1.0	No	Flicker noise frequency exponent
EM	4.1e7V/m	No	Saturation field

Table 151 Flicker and Thermal Noise Model Parameters, Level 54

Parameter	Default	Binnable	Description
KF	$0.0 \text{ A}^{2-\text{EF}} \text{ s}^{1-\text{EF}} \text{ F}$	No	Flicker noise coefficient
NOIA	6.25e41 (eV) ⁻¹ s ^{1-EF} m ⁻³ for NMOS; 6.188e40 (eV) ⁻¹ s ^{1-EF} m ⁻³ for PMOS	No	Flicker noise parameter A
NOIB	3.125e26 (eV) ⁻¹ s ^{1-EF} m ⁻¹ for NMOS; 1.5e25 (eV) ⁻¹ s ^{1-EF} m ⁻¹ for PMOS	No	Flicker noise parameter B
NOIC	$8.75 \text{ (eV)}^{-1} \text{ s}^{1-\text{EF}} \text{ m}$	No	Flicker noise parameter C
NTNOI	1.0	No	Noise factor for short-channel devices for TNOIMOD=0 only
TNOIA	1.5	No	Coefficient of the channel-length dependence of the total channel thermal noise
TNOIB	3.5	No	Channel-length dependence parameter for partitioning the channel thermal noise

Table 152 Layout-Dependent Parasitics Model Parameters, Level 54

Parameter	Default	Binnable	Description
DMCG	0.0m	No	Distance from the S/D contact center to the gate edge
DMCGT	0.0m	No	DMCG of the test structures
DMCI	DMCG	No	Distance from the S/D contact center to the isolation edge in the channel-length direction

Chapter 6: MOSFET Models (BSIM): Levels 47 through 72

Level 54 BSIM4 Model

Table 152 Layout-Dependent Parasitics Model Parameters, Level 54

Parameter	Default	Binnable	Description
DMDG	0.0m	No	Same as DMCG, but for merged devices only
DWJ	DWC (in CVmodel)	No	Offset of the S/D junction width
MIN	0	No	Minimize the number of drain or source diffusions for even-number fingered device
NF	1	No	Number of device figures
NGCON	1	No	Number of gate contacts
XGL	0.0m	No	Offset of the gate length due to variations in patterning
XGW	0.0m	No	Distance from the gate contact to the channel edge

Table 153 Asymmetric Source/Drain Junction Diode Model Parameters, Level 54

Parameter	Default	Binnable	Description
BVD	BVD=BVS	No	Breakdown voltage
BVS	BVS=10.0V	No	Breakdown voltage
CJD	CJD=CJS	No	Bottom junction capacitance per unit area at zero bias
CJS	CJS=5.0e-4 F/m ²	No	Bottom junction capacitance per unit area at zero bias
CJSWD	CJSWD=CJSWS	No	Isolation-edge sidewall junction capacitance per unit length
CJSWGD	CJSWGD=CJSWS	No	Gate-edge sidewall junction capacitance per unit length

Table 153 Asymmetric Source/Drain Junction Diode Model Parameters,
Level 54

Parameter	Default	Binnable	Description
CJSWGS	CJSWGS=CJSWS	No	Gate-edge sidewall junction capacitance per unit length
CJSWS	CJSWS=5.0e-10 F/m	No	Isolation-edge sidewall junction capacitance per unit length
IJTHDFWD	IJTHDFWD=IJTHSFWD	No	Limiting current in the forward bias region
IJTHDREV	IJTHDREV=IJTHSREV	No	Limiting current in the reverse bias region
IJTHSFWD	IJTHSFWD=0.1A	No	Limiting current in the forward bias region
IJTHSREV	IJTHSREV=0.1A	No	Limiting current in the reverse bias region
JSD	JSD=JSS	No	Bottom junction reverse saturation current density
JSS	JSS=1.0e-4A/m ²	No	Bottom junction reverse saturation current density
JSWD	JSWD=JSWS	No	Isolation-edge sidewall reverse saturation current density
JSWGD	JSWGD=JSWGS	No	Gate-edge sidewall reverse saturation current density
JSWGS	JSWGS=0.0A/m	No	Gate-edge sidewall reverse saturation current density
JSWS	JSWS=0.0A/m	No	Isolation-edge sidewall reverse saturation current density
MJD	MJD=MJS	No	Bottom junction capacitance grading coefficient
MJS	MJS=0.5	No	Bottom junction capacitance grading coefficient

Chapter 6: MOSFET Models (BSIM): Levels 47 through 72

Level 54 BSIM4 Model

Table 153 Asymmetric Source/Drain Junction Diode Model Parameters, Level 54

Parameter	Default	Binnable	Description
MJSWD	MJSWD=MJSWS	No	Isolation-edge sidewall junction capacitance grading coefficient
MJSWGD	MJSWGD=MJSWS	No	Gate-edge sidewall junction capacitance grading coefficient
MJSWGS	MJSWGS=MJSWS	No	Gate-edge sidewall junction capacitance grading coefficient
MJSWS	MJSWS=0.33	No	Isolation-edge sidewall junction capacitance grading coefficient
PBD	PBD=PBS	No	Bottom junction built-in potential
PBS	PBS=1.0V	No	Bottom junction built-in potential
PBSWD	PBSWD=PBSWS	No	Isolation-edge sidewall junction built-in potential
PBSWGD	PBSWGD=PBSWS	No	Gate-edge sidewall junction built-in potential
PBSWGS	PBSWGS=PBSWS	No	Gate-edge sidewall junction built-in potential
PBSWS	PBSWS=1.0V	No	Isolation-edge sidewall junction built-in potential
XJBVD	XJBVD=XJBVS	No	Fitting parameter for the diode breakdown
XJBVS	XJBVS=1.0	No	Fitting parameter for the diode breakdown

Table 154 Temperature Dependence Parameters, Level 54

Parameter	Default	Binnable	Description
AT	3.3e4m/s	Yes	Temperature coefficient for the saturation velocity

Table 154 Temperature Dependence Parameters, Level 54

Parameter	Default	Binnable	Description
KT1	-0.11V	Yes	Temperature coefficient for the threshold voltage
KT1L	0.0Vm	Yes	Channel length dependence of the temperature coefficient for the threshold voltage
KT2	0.022	Yes	Body-bias coefficient of the V_{th} temperature effect
NJS, NJD	NJS=1.0; NJD=NJS	No	Emission coefficients of junction for the source and drain junctions
PRT	0.0ohm-m	Yes	Temperature coefficient for R _{dsw}
TCJ	0.0K ⁻¹	No	Temperature coefficient of C _J
TCJSW	0.0K ⁻¹	No	Temperature coefficient of C _{JSW}
TCJSWG	0.0K ⁻¹	No	Temperature coefficient of C _{JSWG}
TNOM	27° X	No	Temperature at which simulation extracts parameters
TPB	0.0V/K	No	Temperature coefficient of P _B
TPBSW	0.0V/K	No	Temperature coefficient of P _{BSW}
TPBSWG	0.0V/K	No	Temperature coefficient of P _{BSWG}
TRD	0.0 1K ⁻¹	No	Temperature coefficient for the drain diffusion and the R _d contact resistances.
TRS	0.0 1/K	No	Temperature coefficient for the source diffusion and the R _s contact resistances.
TVFBSDOFF	0.0K ⁻¹	Yes	Temperature coefficient of V _{FBSDOFF}
TVOFF	0.0K ⁻¹	Yes	Temperature coefficient of V _{OFF}

Chapter 6: MOSFET Models (BSIM): Levels 47 through 72

Level 54 BSIM4 Model

Table 154 Temperature Dependence Parameters, Level 54

Parameter	Default	Binnable	Description
UA1	1.0e-9m/V	Yes	Temperature coefficient for UA
UB1	-1.0e-18 (m/V ²)	Yes	Temperature coefficient for UB
UC1	0.056/V ⁻¹ for MOBMOD=1; 0.056e-9m/V ² for MOBMOD=0 and 2	Yes	Temperature coefficient for UC
UD1	0.0(1/m) ²	Yes	Temperature coefficient for UD
UTE	-1.5	Yes	Mobility temperature exponent
XTIS, XTID	XTIS=3.0; XTID=XTIS	No	Junction current temperature exponents for the source and drain junctions

Table 155 Well Proximity Effect Parameters, Level 54

Parameter	Default	Binnable	Description
K2WE	0.0	Yes	K2 shift factor for well proximity effect
KU0WE	0.0	Yes	Mobility degradation factor for well proximity effect
KVTH0WE	0.0	Yes	Threshold shift factor for well proximity effect
SC	0.0[m]	No	Distance to a single well edge
SCA	0.0	No	Integral of the first distribution function for scattered well dopant
SCB	0.0	No	Integral of the second distribution function for scattered well dopant
SCC	0.0	No	Integral of the third distribution function for scattered well dopant
SCREF	1e-6[m]	No	Reference distance to calculate SCA, SCB, and SCC

Table 155 Well Proximity Effect Parameters, Level 54

Parameter	Default	Binnable	Description
WEB	0.0	No	Coefficient for SCB
WEC	0.0	No	Coefficient for SCC

Table 156 dW and dL Parameters, Level 54

Parameter	Default	Binnable	Description
LL	0.0mLLN	No	Coefficient of the length dependence for the length offset
LLC	LL	No	Coefficient of the length dependence for the CV channel length offset
LLN	1.0	No	Power of the length dependence for the length offset
LW	0.0mLWN	No	Coefficient of the width dependence for the length offset
LWC	LW	No	Coefficient of the width dependence for the CV channel length offset
LWL	0.0 mLWN+LLN	No	Coefficient of the length and width cross term dependence for the length offset
LWLC	LWL	No	Coefficient of the length and width cross-term dependence for the CV channel length offset
LWN	1.0	No	Power of the width dependence, length offset
WL	0.0 $\mu\Omega\Lambda$ N	No	Coefficient of the length dependence of the width offset
WLC	WL	No	Coefficient of the length dependence for the CV channel width offset
WLN	1.0	No	Power of the length dependence of the width offset

Table 156 dW and dL Parameters, Level 54

Parameter	Default	Binnable	Description
WW	0.0mWWN	No	Coefficient of the width dependence of the width offset
WWC	WW	No	Coefficient of the width dependence for the CV channel width offset
WWL	0.0 mWWN+WLN	No	Coefficient of the length and width cross term dependence for the width offset
WWLC	WWL	No	Coefficient of the length and width cross-term dependence for the CV channel width offset
WWN	1.0	No	Power of the width dependence of the width offset

Table 157 Range Parameters for Model Application, Level 54

Parameter	Default	Binnable	Description
LMIN	0.0μ	No	Minimum channel length
LMAX	1.0m	No	Maximum channel length
WMIN	0.0m	No	Minimum channel width
WMAX	1.0m	No	Maximum channel width

Version 4.6 Features

The current HSPICE release supports BSIM version 4.6.0, including the following features:

- The IGISL and IGIDL modules have independent model parameters (as opposed to v. 4.5, in which the GIDL and GISL leakage current modules shared the parameter set).
- The parameters for the source and drain side junction diode current due to the trap-assisted tunneling current in space-change region are fully separated.
- The parameters for the gate tunneling current in the S/D overlap diffusion regions (lgs/lgd) are separated.

In addition three bug fixes are implemented in this version.

- The implementation of coulomb scattering in mobility model has been changed to avoid the non-monotonicity in drain current as a function of gate voltage. Also the default value of parameter has been changed to 0.
- The accuracy of RgateMod = 2 has been improved by accounting correctly the contribution from Rgate to overall noise. The change has been made in b4noi.c
- The default value for the model parameter VFB was missing. The default value of the parameter VFB has been now set to -1.0V in b4set.c

Version 4.6.1 Features

Compared with BSIM4.6.0, several new features are added in this version.

- New material model is introduced for the predictive modeling of Non-SiO₂ insulator, Non-Poly Silicon gate and Non-silicon channel. The following new parameters are added:
 - MTRLMOD: New material model selector
 - PHIG, EPSRGATE: non-poly silicon gate parameters
 - EOT, VDDEOT: non-SiO₂ gate dielectric
 - EASUB, EPSRSUB, NI0SUB, BG0SUB, TBGASUB, TBGBSUB, ADOS, BDOS: Non-silicon channel parameters

- Mobility model (MOBMOD = 0 and MOBMOD = 1) has been improved through predictive modeling of vertical electric field. The improved mobility model is selected through MTRLMOD = 1 for backward compatibility.
- GIDL/GISL models are improved through an improved definition of flatband voltages at S/D ends. The improved GISL/GIDL model is selected through MTRLMOD = 1 for backward compatibility.
- The Poly-depletion model is modified to account for new gate and gate-insulator materials.
- C-V model has been improved by adding a new VgsteffCV definition through CVCHARGEMOD = 1. Six new parameters have been added: CVCHARGEMOD, MINVVCV, LMINVVCV, WMINVCV, PMINVCV and VOFFCVL
- The following bugs have been fixed:
 - An error in the derivative calculation of $dV_{dseffCV}/dV_b$ has been fixed for CAPMOD = 1 and CAPMOD = 2 in b4ld.c
 - The warning limits for NOFF and VOFFCV have been removed from b4check.c.

Version 4.6.2 Features and Updates

The v. 4.6.2 release added the following features and bug fixes:

- Mobility model (mobMod=3) added to enhance the modeling of Coulombic scattering in the high-k/metal gate transistors.
- Trap assisted tunneling (TAT) has been improved to include the width dependence. A new model parameter JTWEFF is introduced and set to zero to maintain the backward compatibility.
- Bug fixes include:
 - Output Conductance Model: VASCBE: A division by zero bug in the output conductance calculation is fixed.
 - Thermal Noise Model (tnoiMod=0): The scaling factor NF is added to the equivalent resistance R_{ds}/NF .
 - Negative Thermal Noise (tnoiMod=1) The noise spectral density will not be negative now.

- Source/Drain Bulk Junction Capacitance: The source/drain bulk junction capacitance will not be discontinuous when V_{bs}/V_{bd} is zero. The S/D junction sidewall capacitance along the isolation edge is set to zero if they are negative.
- Derivative Issue in Capacitance Model (capMod=0): An error in the derivative calculation of $dV_{gs_eff_dVg}$ has been fixed.
- Toxp Calculation (mtrlMod=1): The physical oxide thickness should be lay-out independent.
- Source/Drain Resistance: A division by zero bug in the R_{end} calculation is fixed.
- Typo of SC: SCA is a typo of SC in b4.c
- Drain/Body Breakdown Voltage: The reset value of drain/body breakdown voltage will not cause non-convergence now. Some other similar bugs have also been fixed.

Version 4.6.3 Update

The only change in BSIM4.6.3 compared with BSIM4.6.2 was the refinement of the calculation below.

```
pParam->BSIM4lit1 = sqrt(3.0 * 3.9 / epsrox * pParam->BSIM4xj
* tox)
```

Level 54 BSIM4 Template Output List

For a list of output template parameters in the MOSFET models, and which parameters this model supports, see [Table 4 on page 22](#).

Level 57 UC Berkeley BSIM3-SOI Model

The UC Berkeley SOI model (BSIM3SOI) supports Fully Depleted (FD), Partially Depleted (PD), and Dynamically Depleted (DD) SOI devices of which BSIM3PD2.0.1 for PD SOI devices is Synopsys MOSFET Level 57. For a description of this model, see the *BSIM3PD2.0 MOSFET MODEL User's Manual*.

Level 57 uses the UCB Version 2.2.3 model, which includes a separate set of the geometry-dependence parameters (L_{LC} , L_{WC} , L_{WLC} , W_{LC} , W_{WC} , and W_{WLC}) to calculate $L_{eff}CV$ and $W_{eff}CV$.

Level 57 also includes a new Full-Depletion (FD) module ($soiMod=1$). This module provides a better fit to FD SOI devices. As $soiMod=0$ (default), the model is identical to previous BSIMSOI PD models. This module also includes gate to channel/drain/source tunneling currents and overlap components.

The following enhancements to the BSIMSOI PD version were made starting in the BSIMSOI 3.0 version:

- If the self-heating model is on, simulation calculates the channel surface potential.
- NDIF includes parameter Compared with BSIM4.6.1, several new features are added in this version.
- An error in the derivative calculation of $dV_{gs_eff_dVg}$ has been fixed.
- The reset value of drain/body breakdown voltage will not cause non-convergence now. Some other similar bugs have also been fixed.
- The $DELTOX$ parameter in the MOS active element (M) models the relative variation on the trans conductance (oxide thickness) of the MOS in Monte Carlo analysis.

The following sections discuss these topics:

- [General Syntax for BSIM3-SOI Model](#)
- [Level 57 Model Parameters](#)
- [Parameter Range Limit for BSIM4SOI Level 57](#)
- [Level 57 Template Output](#)
- [Level 57 Updates to BSIM3-SOI PD versions 2.2, 2.21, and 2.22](#)
- [UCB BSIMSOI3.1](#)
- [New Features in BSIMSOIv3.2](#)

General Syntax for BSIM3-SOI Model

The general syntax for including a BSIM3-SOI model element in a netlist is:

```
Mxxx nd ng ns ne [np] [nb] [nT] mname [L=val] [W=val]
+ [M=val] [NRD=val] [AD=val] [AS=val] [PD=val] [PS=val]
+ [VER_CONTROL=0|1] [NRS=val] [NRB=val] [RTH0=val] [NBC=val]
```



```

+ [NSEG=val] [PDBCP=val] [PSBCP=val] [AGBCP=val]
+ [AEBCP=val] [VBSUSR=val] [DELTOX=val] [TNODEOUT]
+ [off] [FRBODY] [BJToff=val] [IC=Vds, Vgs, Vbs, Ves]
+ [SOIMOD=val] [SOIQ0=val] [MULID0=val]

```

Parameter	Description
AD	Drain diffusion area. Overrides .OPTION DEFAD statement. Default=DEFAD.
AEBCP	Parasitic body-to-substrate overlap area for the body contact.
AGBCP	Parasitic gate-to-body overlap area for the body contact.
AS	Source diffusion area. Overrides .OPTION DEFAS statement. Default=DEFAS.
BJTOFF	Turning off BJT if equal to 1.
CTH0	Thermal capacitance per unit width: <ul style="list-style-type: none"> ▪ If you do not specify CTH0, simulation extracts it from the model card. ▪ If you specify CTH0, it overrides CTH0 in the model card.
DELTOX	Shift in gate oxide thickness (TOX). That is, the difference between the electrical and physical gate oxide/insulator thicknesses.
FRBODY	Coefficient of the distributed body resistance effects. Default=1.0
IC	Initial guess in the order (drain, front gate, internal body, back gate, external voltage). (ignores Vps for 4-terminal devices) Use these only if you specify UIC in the .TRAN statement. The .IC statement overrides it.
L	SOI MOSFET channel length in meters. This parameter overrides DEFL in an OPTIONS statement. Default=DEFL with a maximum of 0.1m.
M	Multiplier to simulate multiple SOI MOSFETs in parallel. The M setting affects all channel widths, diode leakages, capacitances, and resistances. Default=1.
mname	MOSFET model name reference.

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Level 57 UC Berkeley BSIM3-SOI Model

Parameter	Description
Mxxx	SOI MOSFET element name. Must begin with M, followed by up to 1023 alphanumeric characters.
nb	Internal body node name or number.
NBC	Number of body contact isolation edge.
nd	Drain terminal node name or number.
ne	Back gate (or substrate) node name or number.
ng	Front gate node name or number.
np	External body contact node name or number.
NRB	Number of squares for the body series resistance.
NRD	NRD (Number of squares of drain diffusion for resistance calculations) overrides .OPTION DEFNRD. For nonCMI models such as BSIM3 etc... Default=DEFNRD, if you set ACM=0 or 1 model parameter. Default=0.0, if you set ACM=2 or 3 For CMI models such as BSIM4 etc... Default=1.0
NRS	NRS (Number of squares of source diffusion for resistance calculations) overrides .OPTION DEFNRS. For nonCMI models such as BSIM3 etc... Default=DEFNRS, if you set ACM=0 or 1 model parameter. Default=0.0, if you set ACM=2 or 3 For CMI models such as BSIM4 etc... Default=1.0
ns	Source terminal node name or number.
NSEG	Number of segments for partitioning the channel width.
nT	Temperature node name or number.
OFF	Sets the initial condition of the element to OFF in DC analysis.
PD	Drain junction perimeter, including channel edge. Overrides .OPTION DEFPD.
PDBCP	Parasitic perimeter length for the body contact a the drain side.

Parameter	Description
PS	Source junction perimeter including channel edge. Overrides .OPTION DEFPS.
PSBCP	Parasitic perimeter length for the body contact at the source side.
RTH0	Thermal resistance per unit width: <ul style="list-style-type: none"> ▪ If you do not specify RTH0, simulation extracts it from the model card. ▪ If you specify RTH0, it overrides RTH0 in the model card.
SOIMOD	SOI model selector If SOIMOD is not specified, it's extracted from the model card If SOIMOD is specified, it overrides SOIMOD in the model card
SOIQ0	Floating body charge initialization. This parameter is set for the BQI algorithm of a floating body node.
TNODEOUT	Temperature node flag indicating the use of the T node.
VBSUSR	Optional initial Drain/Body Breakdown Voltage of Vbs that you specify for transient analysis.
W	MOSFET channel width in meters. This parameter overrides DEFW in an OPTIONS statement. Default=DEFW.
MULID0	Scaling factor of drain current, the default is 1.0.
VER_CONTROL	<ul style="list-style-type: none"> ▪ VER_CONTROL=0: (Default) Version control is off ▪ VER_CONTROL=1: Version control is on; the simulation will abort for non-supported version

- If you do not set `TNODEOUT`, you can specify four nodes for a device to float the body. Specifying five nodes implies that the fifth node is the external body contact node with a body resistance between the internal and external terminals. This configuration applies to a distributed body resistance simulation.
- If you set `TNODEOUT`, simulation interprets the last node as the temperature node. You can specify five nodes to float the device. Specifying six nodes implies body contact. Seven nodes is a body-contacted case with an accessible internal body node. You can use the temperature node to simulate thermal coupling.

Level 57 Model Parameters

Table 158 Model Control Parameters, Level 57

Parameter	Unit	Default	Description
capmod	-	2	Flag for the short channel capacitance model
MOBMOD	-	1	Mobility model selector
noimod	-	1	Flag for the noise model
SHMOD	-	0	Flag for self-heating: 0 - no self-heating 1 - self-heating

Table 159 Process Parameters, Level 57

Parameter	Unit	Default	Description
DTOXCV (capmod=3 only)			Difference between the electrical and physical gate oxide thicknesses, due to the effects of the gate poly-depletion and the finite channel charge layer thickness.
Nch	1/cm3	1.7e17	Channel doping concentration
Ngate	1/cm3	0	Poly gate doping concentration

Table 159 Process Parameters, Level 57

Parameter	Unit	Default	Description
Nsub	1/cm ³	6.0e16	Substrate doping concentration
Tbox	m	3.0e-7	Buried oxide thickness
Tox	m	1.0e-8	Gate oxide thickness
Tsi	m	1.0e-7	Silicon film thickness
Xj	m	-	S/D junction depth

Table 160 DC Parameters, Level 57

Parameter	Unit	Default	Description
a0	-	1.0	Bulk charge effect coefficient for the channel length
A1	1/V	0.0	First non-saturation effect parameter
A2	-	1.0	Second non-saturation effect parameter
Aely	V/m	0	Channel length dependency of the early voltage for the bipolar current
Agidl	1/W	0.0	GIDL constant
ags	1/V	0.0	Gate bias coefficient of A_{bulk}
Ahli	-	0	High-level injection parameter for the bipolar current
alpha0	m/V	0.0	First parameter of the impact ionization current
b0	m	0.0	Bulk charge effect coefficient for the channel width
b1	m	0.0	Bulk charge effect width offset

Table 160 DC Parameters, Level 57

Parameter	Unit	Default	Description
beta0	1/V	0.0	First V_{ds} dependence parameter of the impact ionization current
beta1	-	0.0	Second V_{ds} dependence parameter of the impact ionization current
beta2	V	0.1	Third V_{ds} dependence parameter of the impact ionization current
Bgidl	V/m	0.0	GIDL exponential coefficient
cdsc	F/m2	2.4e-4	Drain/source to the channel coupling capacitance
cdscb	F/m2	0	Body-bias sensitivity of cdsc
cdscd	F/m2	0	Drain-bias sensitivity of cdsc
cit	F/m2	0.0	Interface trap capacitance
delta	-	0.01	Effective V_{ds} parameter
drout	-	0.56	L dependence coefficient of the DIBL correction parameter in Rout
dsub	-	0.56	DIBL coefficient exponent
Dvt0	-	2.2	First coefficient of the short-channel effect on Vth
dvt0w	-	0	First coefficient of the narrow width effect on Vth for a small channel length
dvt1	-	0.53	Second coefficient of the short-channel effect on Vth
dvt1w	-	5.3e6	Second coefficient of the narrow width effect on Vth for a small channel length
dvt2	1/V	-0.032	Body-bias coefficient of the short-channel effect on Vth

Table 160 DC Parameters, Level 57

Parameter	Unit	Default	Description
dvt2w	1/V	-0.032	Body-bias coefficient of the narrow width effect on V_{th} for a small channel length
dwb	m/V ^{1/2}	0.0	Coefficient of the substrate body bias dependence of W_{eff}
dwbc	m	0.0	Width offset for the body contact isolation edge
dwg	m/V	0.0	Coefficient of the gate dependence of W_{eff}
esati	V/m	1.e7	Saturation channel electric field for the impact ionization current
eta0	-	0.08	DIBL coefficient in the subthreshold region
etab	1/V	-0.07	Body-bias coefficient for the DIBL effect in the subthreshold region
fbjtii	-	0.0	Fraction of the bipolar current affecting the impact ionization
lsbjt	A/m ²	1.0e-6	BJT injection saturation current
lsdif	A/m ²	0	Body to source/drain injection saturation current
lsrec	A/m ²	1.0e-5	Recombination in the depletion saturation current
lstun	A/m ²	0.0	Reverse tunneling saturation current
k1	V ^{1/2}	0.6	First-order body effect coefficient
k1w1	m	0	First-order effect width dependent parameter
k1w2	m	0	Second-order effect width dependent parameter
k2	-	0	Second-order body effect coefficient
k3	-	0	Narrow coefficient

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Level 57 UC Berkeley BSIM3-SOI Model

Table 160 DC Parameters, Level 57

Parameter	Unit	Default	Description
k3b	1/V	0	Body effect coefficient of k3
kb1	-	1	Backgate body charge coefficient
keta	1/V	-0.6	Body-bias coefficient of the bulk charge effect
Ketas	V	0.0	Surface potential adjustment for the bulk charge effect
Lbjt0	m	0.2e-6	Reference channel length for the bipolar current
lii	-	0	Channel length dependence parameter for the impact ionization current
lint	m	0.0	Length offset fitting parameter from I-V without bias
Ln	m	2.0e-6	Electron/hole diffusion length
Nbjt	-	1	Power coefficient of the channel length dependency for the bipolar current
NdioDE	-	1.0	Diode non-ideality factor
nfactor	-	1	Subthreshold swing factor
Ngidl	V	1.2	GIDL V_{ds} enhancement coefficient
nlx	m	1.74e-7	Lateral non-uniform doping parameter
Nrecf0	-	2.0	Recombination non-ideality factor at the forward bias
Nrecr0	-	10	Recombination non-ideality factor at the reversed bias
Ntun	-	10.0	Reverse tunneling non-ideality factor
pclm	-	1.3	Channel length modulation parameter

Table 160 DC Parameters, Level 57

Parameter	Unit	Default	Description
PDIBLC1	-	0.39	Correction parameter for the DIBL effect of the first output resistance
pdiblc2	-	0.0086	Correction parameter for the DIBL effect of the second output resistance
prwb	1/V1	0	Body effect coefficient of R _{dsw}
prwg	1/V1/2	0	Gate-bias effect coefficient of R _{dsw}
pvag	-	0.0	Gate dependence of the Early voltage
Rbody	ohm/m2	0.0	Intrinsic body contact sheet resistance
Rbsh	ohm/m2	0.0	Extrinsic body contact sheet resistance
rdsw	$\Omega \cdot \mu\text{m}^{\text{wr}}$	100	Parasitic resistance per unit width
rsh	ohm/ square	0.0	Source/drain sheet resistance in ohm per square
sii0	1/V	0.5	First V_{gs} dependence parameter for the impact ionization current
sii1	1/V	0.1	Second V_{gs} dependence parameter for the impact ionization current
sii2	1/V	0	Third V_{gs} dependence parameter for the impact ionization current
siid	1/V	0	V_{ds} dependence parameter of the drain saturation voltage for the impact ionization current
tii	-	0	Temperature dependence parameter for the impact ionization current
u0	$\text{cm}^2/(\text{V} \cdot \text{sec})$	NMOS-670 PMOS-250	Mobility at Temp=T _{nom}

Table 160 DC Parameters, Level 57

Parameter	Unit	Default	Description
ua	m/V	2.25e-9	First-order mobility degradation coefficient
ub	(m/V) ²	5.87e-19	Second-order mobility degradation coefficient
uc	1/V	-0.0465	Body-effect of the mobility degradation coefficient
Vabjt	V	10	Early voltage for the bipolar current
vdsatii0	V	0.9	Nominal drain saturation voltage at threshold for the impact ionization current
VECB	v	0.026v	Electron tunneling from the conduction band
VEVB	v	0.075v	Electron tunneling from the valence band
voff	v	-0.08	Offset voltage in the subthreshold region for large W and L
Vrec0	V	0.0	Voltage dependent parameter for the recombination current
vsat	m/sec	8e4	Saturation velocity at Temp=Tnom
vth0	v	NMOS 0.7 PMOS -0.7	Threshold voltage @ Vbs=0 for a long, wide device
Vtun0	V	0.0	Voltage dependent parameter for the tunneling current
w0	m	0	Narrow width parameter
wint	m	0.0	Width offset fitting parameter from I-V without bias
wr	-	1	Width offset from Weff for the Rds calculation

Table 161 AC and Capacitance Parameters, Level 57

Parameter	Unit	Default	Description
acde	m/V	1.0	Exponential coefficient for the charge thickness in the CapMod=3 for the accumulation and depletion regions
asd	V	0.3	Smoothing parameter for the source/drain bottom diffusion
cf	F/m	cal.	Fringing field capacitance of the gate-to-source/drain
cgdl	F/m	0.0	Overlap capacitance for the lightly-doped drain-gate region
cgdo	F/m	0	Non LDD region drain-gate overlap capacitance per channel length
CGEO	F/m	0	Gate substrate overlap capacitance per unit channel length
cgsi	F/m	0.0	Overlap capacitance for the lightly-doped source-gate region
cgso	F/m	calculate d	Non LDD region source-gate overlap capacitance per channel length
cjswg	F/m ²	1.e-10	Source/drain (gate side) sidewall junction capacitance per unit width (normalized to 100nm Tsi)
ckappa	F/m	0.6	Coefficient for the fringing field capacitance for the overlap capacitance in the lightly-doped region
clc	m	0.1e-7	Constant term for the short-channel model
cle	-	0.0	Exponential term for the short-channel model
csdesw	F/m	0.0	Fringing capacitance per unit length for the source/drain sidewall
csdmin	V	cal.	Minimum capacitance for the source/drain bottom diffusion
delvt	V	0.0	Threshold voltage adjustment for C-V

Table 161 AC and Capacitance Parameters, Level 57

Parameter	Unit	Default	Description
dlbg	m	0	Length offset fitting parameter for the backgate charge
dlc	m	lint	Length offset fitting parameter for the gate charge
dlcb	m	lint	Length offset fitting parameter for the body charge
dwc	m	wint	Width offset fitting parameter from C-V
fbody	-	1.0	Scaling factor for the body charge
Ldif0	-	1	Channel length dependency coefficient of the diffusion cap.
mjswg	V	0.5	Grading coefficient of the source/drain (gate side) sidewall junction capacitance
moin	V ^{1/2}	15.0	Coefficient for the gate-bias dependent surface potential
Ndif	-	-1	Power coefficient of the channel length dependency for the diffusion capacitance
pbswg	V	0.7	Built-in potential of the source/drain (gate side) sidewall junction capacitance
tt	second	1ps	Diffusion capacitance transit time coefficient
vsdfb	V	cal.	Flatband voltage for the source/drain bottom diffusion capacitance
vsdth	V	cal.	Threshold voltage for the source/drain bottom diffusion capacitance
xpart	-	0	Charge partitioning rate flag

Table 162 Temperature Parameters, Level 57

Parameter	Unit	Default	Description
at	m/sec	3.3e4	Temperature coefficient for U_a
cth0	$m^{\circ}C/(W*s)$	0	Normalized thermal capacity
kt1	V	-0.11	Temperature coefficient for the threshold voltage
kt2	-	0.022	Body-bias coefficient of the threshold voltage temperature effect
ktil	V*m	0	Channel length dependence of the temperature coefficient for the threshold voltage
Ntrecf	-	0	Temperature coefficient for N_{recf}
Ntreocr	-	0	Temperature coefficient for N_{reocr}
prt	Ω_{-um}	0	Temperature coefficient for R_{dsw}
rth0	$m^{\circ}C/W$	0	Normalized thermal resistance
tcjswg	1/K	0	Temperature coefficient of C_{jswg}
tnom	$^{\circ}C$	25	Temperature at which simulation expects parameters
tpbswg	V/K	0	Temperature coefficient of P_{bswg}
ua1	m/V	4.31e-9	Temperature coefficient for U_a
ub1	$(m/V)^2$	-7.61e-18	Temperature coefficient for U_b
uc1	1/V	-0.056	Temperature coefficient for U_c
ute	-	-1.5	Mobility temperature exponent
xbjt	-	1	Power dependence of j_{bjt} on the temperature
xdif	-	XBJT	Power dependence of j_{dif} on the temperature
xrec	-	1	Power dependence of j_{rec} on the temperature

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Level 57 UC Berkeley BSIM3-SOI Model

Table 162 Temperature Parameters, Level 57

Parameter	Unit	Default	Description
xtun	-	0	Power dependence of j_{tun} on the temperature

The parameters in [Table 163](#) improve the BSIM3SOI model to address parasitic BJT-induced avalanche impact ionization current. Contact Synopsys for details.

Table 163 Avalanche Impact Ionization Parameters, Level 57

Parameter	Unit	Default	Description	Notes
IIMOD	-	0 (original II model)	Impact ionization model selector	=1 selects the new II model
EBJTII	1/V	0.0	Impact ionization parameter for BJT part	-
CBJTII	m/V	0.0	Length scaling parameter for II BJT part	-
VBCI	V	0.7	Internal B-C built-in potential	-
ABJTII	-	0.0	Exponent factor for avalanche current	-
MBJTII	-	0.4	Internal B-C grading coefficient	-
TVBCI	-	0.0	Temperature coefficient for VBCI	-

Level 57 Notes:

- BSIMPD2.01 supports capmod=2 and 3 only. It does not support capmod=0 and 1.
- Modern SOI technology commonly uses source/drain extension or LDD. The source/drain junction depth (X_j) can be different from the silicon film thickness (T_{si}). By default, if you do not specify X_j , simulation sets it to T_{si} . X_j cannot be greater than T_{si} .
- BSIMPD refers the substrate to the silicon below the buried oxide (not to the well region in BSIM3) to calculate the backgate flatband voltage (V_{fb}) and the parameters related to the source/drain diffusion bottom capacitance (V_{sdth} , V_{sdfb} , C_{sdmin}).
 - Positive n_{sub} means the same type of doping as the body.

- Negative n_{sub} means the opposite type of doping.
- **New W_{0FLK} Parameter:**
The following equation models the SPICE2 flicker noise current density, used in both UCB SOI code and the Synopsys Level=57 MOSFET model for $noiMod=1$ and 4:

$$S_{id,f}[I_2/Hz] = K_F * I_{ds}^{AF} / (C_{ox} * L_{eff}^2 * f^{EF}) \quad -- \quad (1)$$

However, if AF is not equal to unity, it does not scale properly with W_{eff} , because I_{ds} is approximately proportional to W_{eff} . Also, without the HSPICE multiplicity factor (M factor) in equation (1), this model cannot simulate multiple transistors in parallel.

To solve these problems, HSPICE 2002.2 added a W_{0FLK} (width normalizing) parameter, and corrects equation (1) as:

$$M * K_F * [(W_{eff}/W_{0FLK})^{(1-AF)}] * I_{ds}^{AF} / (C_{ox} * L_{eff}^2 * f^{EF}) \quad -- \quad (2)$$

The default value of W_{0FLK} is -1.0 to switch off the new width-scaling model. The unit is in meters.

The next equation handles the flicker noise model ($noiMod=1$ & 4), depending on whether you specify W_{0FLK} .

If $W_{0FLK} \leq 0.0$ (the default case), then the flicker noise model of $noiMod=1$ and 4 uses this equation for backward compatibility.

$$\begin{aligned} & M * K_F * I_{ds}^{AF} / (C_{ox} * L_{eff}^2 * f^{EF}) \quad -- \quad (3) \\ \text{ELSE} \\ & M * K_F * [(W_{eff}/W_{0FLK})^{(1-AF)}] * I_{ds}^{AF} / (C_{ox} * L_{eff}^2 * f^{EF}) \end{aligned}$$

Parameter Range Limit for BSIM4SOI Level 57

Simulation reports either a warning or a fatal error if BSIM3v3 parameters fall outside predefined ranges. These range limitations prevent (or at least warn of) potential numerical problems.

To control the maximum number of simulation warning messages printing to the output file, use:

```
.OPTION WARNLIMIT=#
```

In the preceding `.OPTION` statement, `#` is the maximum number of warning messages that simulation reports. The default `WARNLIMIT`

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Level 57 UC Berkeley BSIM3-SOI Model

The source/drain bulk junction capacitance will not be discontinuous when V_{bs}/V_{bd} is zero. The S/D junction sidewall capacitance along the isolation edge is set to zero if they are negative.

value is 1. In some cases (as noted in [Table 164](#) below), simulation checks parameters only if you set the `PARAMCHK=1` model parameter.

Table 164 Model Parameter Range Limit, Level 57

Parameter	Limits	Comment
<code>nlx</code>	$< -leff$ fatal	
<code>tox</code>	$tox+deltox < 0$ fatal	
<code>toxm</code>	$toxm+deltox < 0$ fatal	
<code>tbox</code>	≤ 0 fatal	
<code>npeak</code>	≤ 0 fatal	
<code>ngate</code>	$< 0, > 1e25$ fatal	
<code>dvt1</code>	< 0 fatal	
<code>dvt1w</code>	< 0 fatal	
<code>w0</code>	$w0+weff = 0$ fatal	
<code>dsub</code>	< 0 fatal	
<code>b1</code>	$b1+weff = 0$ fatal	
<code>u0</code>	≤ 0 fatal	
<code>delta</code>	< 0 fatal	
<code>vsat</code>	≤ 0 fatal	
<code>pclm</code>	≤ 0 fatal	
<code>drout</code>	< 0 fatal	
<code>clc</code>	< 0 fatal	
<code>noff</code>	$= 0$ warn, set 1.0	If (version>3.1999) $< 0.1, > 4.0$ warn

Table 164 Model Parameter Range Limit, Level 57

Parameter	Limits	Comment
moin	< 5, > 25 warn	
acde	< 0.1, > 1.6 warn	if (2.2299 < version < 3.1099) acde < 0.4 warn
moinFD	< 5.0 warn	if (version > 2.9999)
if paramchk=1 following parameter limit range is added		
leff	<= 5e-8 warn	
leffcv	<= 5e-8 warn	
weff	<= 1e-7 warn	
weffcv	<= 1e-7 warn	
nlx	< 0 warn	
tox	tox+delttox < 0 warn	
npeak	<= 1e15, >= 1e21 warn	
nsub	>= 1e21 warn	
ngate	0 < ngate <= 1e18 warn	
dvt0	< 0 warn	
w0	w0+weff < 1e-7 warn	
cdsc	< 0 warn	
nfactor	< 0 warn	
cdscd	< 0 warn	
eta0	<0 warn	
b1	b1+weff<1e-7 warn	
a2	< 0.01, > 1 warn	

Table 164 Model Parameter Range Limit, Level 57

Parameter	Limits	Comment
rdsw	< 0 warn	
rds0	> 0, < 0.001 warn	
vsattemp	< 1e3 warn	
pdibl1	< 0 warn	
pdibl2	< 0 warn	
cgdoi	< 0 warn	
cgsoi	< 0 warn	
cgeo	< 0 warn	
ntun	< 0 warn	
ndiode	< 0 warn	
isbjt	< 0 warn	
isdif	< 0 warn	
isrec	< 0 warn	
istun	< 0 warn	
Tt	< 0 warn	
csdmin	< 0 warn	
csdesw	< 0 warn	
asd	< 0 warn	
rth0	< 0 warn	
cth0	<0 warn	
rbody	< 0 warn	

Table 164 Model Parameter Range Limit, Level 57

Parameter	Limits	Comment
rbsh	< 0 warn	
nigc	<= 0 fatal	if (version > 2.9999)
poxedge	<= 0 fatal	if (version > 2.9999)
pigcd	<= 0 fatal	if (version > 2.9999)
wth0	< 0 warn	
rhalo	< 0 warn	
ntox	< 0 warn	
toxtref	< 0 warn	
ebg	< 0 warn	
nevb	< 0 warn	
vevb	< 0 warn	
alphaGB1	< 0 warn	
BetaGB1	< 0 warn	
vgb1	< 0 warn	
necb	< 0 warn	
vecb	< 0 warn	
alphaGB2	< 0 warn	
vgb2	< 0 warn	
toxqm	<= 0 warn	
voxh	< 0 warn	
deltavox	<= 0 warn	

Table 164 Model Parameter Range Limit, Level 57

Parameter	Limits	Comment
k1w1	< 0 warn	
k1w2	< 0 warn	
ketas	< 0 warn	
dwbc	< 0 warn	
beta0	< 0 warn	
beta1	< 0 warn	
beta2	< warn	
tii	< 0 warn	
lii	< 0 warn	
sii1	< 0 warn	
sii2	< 0 warn	
siid	< 0 warn	
fbjtii	< 0 warn	
vrec0	< 0 warn	
vtun0	< 0 warn	
nbjt	< 0 warn	
aely	< 0 warn	
ahli	< 0 warn	
rbody	< 0 warn	
rbsh	< 0 warn	
ntred	< 0 warn	

Table 164 Model Parameter Range Limit, Level 57

Parameter	Limits	Comment
ntrecf	< 0 warn	
ndif	< 0 warn	if (version <= 2.9999)
tcjswg	< 0 warn	if (version <= 2.9999)
tpbswg	< 0 warn	if (version <= 2.9999)
acde	< 0.4, > 1.6 warn	if (version > 3.1099) acde < 0.1 warn
moin	< 5, > 25 warn	
dlbg	< 0 warn	
agidl	< 0 warn	
bgidl	< 0 warn	
ngidl	< 0 warn	
esatii	< 0 warn	Should be within (0,1)
xj	> tsi warn	
capmod	< 2 warn	

Level 57 Template Output

For a list of output template parameters in the MOSFET models, and which parameters this model supports, see [Table 4 on page 22](#).

Level 57 Updates to BSIM3-SOI PD versions 2.2, 2.21, and 2.22

- BSIM PD version 2.2 enhances the model flexibility and accuracy from PD version 2.0, and the following are its major features.
 - Gate-body tunneling (substrate current) enhances the model accuracy.
 - Body contact resistance improves the modeling accuracy.
 - Binning enhances the model flexibility.
- BSIM PD version 2.21 updates the PD version 2.2 for bug fixes and S/D swapping for the gate current components.
- BSIM PD version 2.22 updates the 2.21 version for bug fixes and enhancements. The major features include:
 - FRBODY instance parameter
 - Improved temperature dependence of the gate direct tunneling model
 - Two new model parameters, `VEVB` and `VECB`
 - UC Berkeley code no longer supports the `NECB` and `NEVB` model parameters. Version 2.22 accepts these parameters for backwards compatibility, but they have no effect.

- `.OPTION LIST` prints an element summary for the MOSFET Level=57 model.

Element	Description
bjtoff	BJT on/off flag (Turn off BJT if equal to 1)
rth0	Thermal Resistance per unit width
cth0	Thermal Capacitance per unit width
nrb	Number of squares for the body series resistance
frbody	Coefficient of the distributed body resistance effects
nbcb	Number of body contact isolation edge
nseg	Number of segments for channel width partitioning
pdbcp	Parasitic perimeter length for the body contact at the drain side
psbcp	Parasitic perimeter length for the body contact at the source side
agbcp	Parasitic gate-to-body overlap area for the body contact
aebcp	Parasitic body-to-substrate overlap area for the body contact
vbsusr	Optional initial value of Vbs, which you specify for transient analysis

- BSIM PD version 2.23 includes several bug fixes and enhancements from version 2.2.
 - Adds geometric dependency in CV delta L and delta W.
 - Fixes a gate-body-tunneling residue problem in the low-bias region.
 - Provides an additional parameter (dtoxcv) in CAPMOD=3 for flexibility
 - Other bug fixes

Using BSIM3-SOI PD

To use BSIM3-SOI PD versions 2.0, 2.2, 2.21, or 2.22 in simulation, apply the `VERSION` model parameter. For example:

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Level 57 UC Berkeley BSIM3-SOI Model

- Invokes PD2.0 if VERSION=2.0
- Invokes PD2.2 and PD2.21 if VERSION=2.2
- Invokes PD2.22 if VERSION=2.22
- Invokes PD2.23 if VERSION=2.23.

For gate-body tunneling, set the IGMOD model parameter to 1.

Example

```
mckt drain gate source bulk nch L=10e-6 W=10e-6
.model nch nmos Level=57 igmod=1 version=2.2
+ tnom=27 tox=4.5e-09 tsi=.0000001 tbox=8e-08
+ mobmod=0 capmod=2 shmod=0 paramchk=0
+ wint=0 lint=-2e-08 vth0=.42 k1=.49
+ k2=.1 k3=0 k3b=2.2 nlx=2e-7
+ dvt0=10 dvt1=.55 dvt2=-1.4 dvt0w=0
+ dvt1w=0 dvt2w=0 nch=4.7e+17 nsub=-1e+15
+ ngate=1e+20 agidl=1E-15 bgidl=1E9 ngidl=1.1
+ ndiode=1.13 ntun=14.0 nrecf0=2.5 nrecr0=4
+ vrec0=1.2 ntrecf=.1 ntrecr=.2 isbjt=1E-4
+ isdif=1E-5 istun=2E-5 isrec=4E-2 xbjt=.9
+ xdif=.9 xrec=.9 xtun=0.01 ahli=1e-9
+ lbjt0=0.2e-6 ln=2e-6 nbjt=.8 ndif=-1
+ aely=1e8 vabjt=0 u0=352 ua=1.3e-11
+ ub=1.7e-18 uc=-4e-10 w0=1.16e-06 ags=.25
+ A1=0 A2=1 b0=.01 b1=10
+ rdsw=0 prwg=0 prwb=-.2 wr=1
+ rbody=1E0 rbsh=0.0 a0=1.4 keta=0.1
+ ketas=0.2 vsat=135000 dwg=0 dwb=0
+ alpha0=1e-8 beta0=0 betal=0.05 beta2=0.07
+ vdsatii0=.8 esatii=1e7 voff=-.14 nfactor=.7
+ cdsc=.00002 cdsch=0 cdschd=0 cit=0
+ pclm=2.9 pvag=12 pdiblc1=.18 pdiblc2=.004
+ pdiblc3=-.234 drout=.2 delta=.01 eta0=.05
+ etab=0 dsub=.2 rth0=.005 clc=.0000001
+ cle=.6 cf=1e-20 ckappa=.6 cgd1=1e-20
+ cgsl=1e-20 kt1=-.3 kt1l=0 kt2=.022
+ ute=-1.5 ual=4.31e-09 ubl=-7.61e-18 ucl=-5.6e-11
+ prt=760 at=22400 cgso=1e-10 cgdo=1e-10
+ cjswg=1e-12 tt=3e-10 asd=0.3 csdesw=1e-12
+ tcjswg=1e-4 mjswg=.5 pbswg=1
```


UCB BSIMSOI3.1

In addition to BSIMSOI3.0, the MOSFET Level 57 model also supports the UCB BSIMSOI3.1 model version, which includes the following new features that are not available in BSIMSOI3.0.

Ideal Full-Depletion (FD) Modeling

BSIMSOI3.0 supports the modeling of these two families of SOI MOSFETs with a `SOIMOD` switching model flag.

- `SOIMOD=0` for partially depleted devices (PD).
- `SOIMOD=1` for devices that tend to operate in a mixed mode of PD and FD.

V3.1 also provides an ideal full-depletion (FD) module (`SOIMOD=2`), not available in V3.0 to model FD SOI devices that literally exhibit no floating-body behavior. As in BSIMSOI3.0, the default `SOIMOD` value is 0 for BSIMSOI3.1.

The following physical modeling components, related to the internal SOI body node, are critical for accurately modeling PD SOI devices, but are not needed for the ideal FD module. Thus, for the ideal FD module, HSPICE ignores these components, which makes SOI MOSFET modeling much easier than for PD devices, or non-ideal FD devices.

- Source/Drain to body diode currents
- Source-Body-Drain parasitic BJT currents
- Impact ionization currents
- Gate-body direct currents
- Body-related capacitances.

Gate Resistance Modeling

BSIMSOI3.1 uses the same gate resistance models as in the BSIM4 model with four options for various gate-resistance modeling topologies.

Table 165 BSIMSOI3.1 Gate Resistance Modeling Topologies

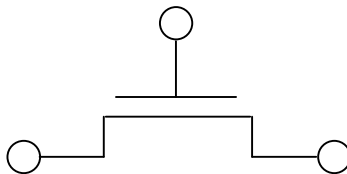
Name	Unit	Default	Bin	Description
NGCON	-	-	N	Number of gate contacts

Table 165 BSIMSOI3.1 Gate Resistance Modeling Topologies

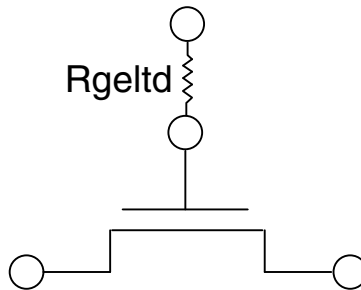
Name	Unit	Default	Bin	Description
RGATEMOD	-	0	N	Gate resistance model selector <ul style="list-style-type: none"> RGATEMOD=0: No gate resistance RGATEMOD=1: Constant gate resistance RGATEMOD=2: Rii model with variable resistance RGATEMOD=3: Rii model with two nodes
RSHG	Ohm/Sq	0.1	N	Gate electrode sheet resistance
XGL	m	0	N	Offset of the gate length due to variations in patterning
XGW	m	0	N	Distance from the gate contact to the channel edge in the W direction
XRCRG1	-	12	Y	Parameter for distributed channel-resistance effect for intrinsic input resistance
XRCRG2	-	1	Y	Parameter to account for the excess channel diffusion resistance for intrinsic input resistance

Gate Resistance Equivalent Circuit

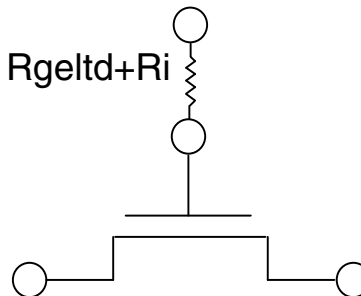
RGATEMOD=0: No gate resistance (default)



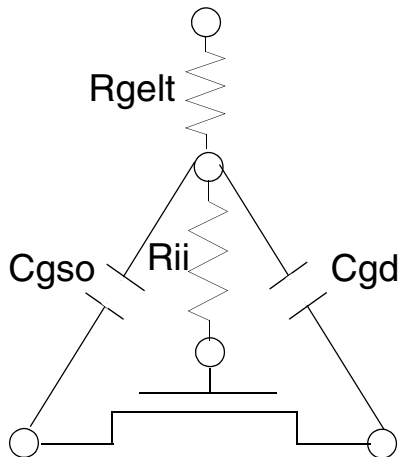
RGATEMOD=1: Constant gate resistance



RGATEMOD=2: variable resistance with Rii model



RGATEMOD=3: Rii model with two nodes



R_{geltd} : (Poly) gate electrode resistance, bias independent.

R_{ii} : Intrinsic input gate resistance, reflected to the gate from the intrinsic channel region. It is bias-dependent and a first-order non-quasi static model for RF and rapid transient MOSFET operations.

Enhanced Binning Capability

Model parameters for the following components are now binnable for better accuracy and scalability:

- Junction depth
- Gate-tunneling current
- Temperature dependence of threshold voltage, mobility, saturation velocity, parasitic resistance, and diode currents.

Bug Fixes

The BSIMSOI3.1 from UC Berkeley fixes the following bugs in the BSIMSOI3.0 model:

- The model now takes NSEG into account when calculating the gate-channel tunneling current.
- The G_{MIN} connecting gate and drain is now multiplied by $1e-6$ to reduce false leakage current.
- A swapping error in the source/drain overlap capacitance stamping.
- The bulk charge effect coefficient (A_{bulkCV}) is now corrected for Q_{inv} and its derivatives in $CAPMOD=2$.

New Features in BSIMSOIv3.2

Level 57 UC Berkeley BSIM3SOI Model

The model selector, `SoiMod`, is an instance parameter and a model parameter. `SoiMod` will determine the operation of BSIMSOI.

If `SoiMod=0` (default), the model equation is identical to the BSIMPD equation.

If `SoiMod=1` (unified model for PD&FD) or `SoiMod=2` (ideal FD), the following equations (FD module) are added on top of BSIMPD.

$$V_{bs0} = \frac{C_{Si}}{C_{Si} + C_{BOX}} \cdot \left(\phi_i - \frac{qN_{ch}(1 + N_{LX}/L_{eff})}{2\epsilon_{Si}} \cdot T_{Si}^2 + V_{nonideal} + \Delta V_{DIBL} \right) + \eta_e \frac{C_{BOX}}{C_{Si} + C_{BOX}} \cdot (V_{es} - V_{FBb})$$

where $C_{Si} = \frac{\epsilon_{Si}}{T_{Si}}, C_{BOX} = \frac{\epsilon_{OX}}{T_{BOX}}, C_{OX} = \frac{\epsilon_{OX}}{T_{OX}}$

$$\Delta V_{DIBL} = D_{vbd0} \left(\exp \left(-D_{vbd1} \frac{L_{eff}}{2l} \right) + 2 \exp \left(-D_{vbd1} \frac{L_{eff}}{l} \right) \right) \cdot (V_{bi} - 2\Phi_B)$$

$$\eta_e = K_{1b} - K_{2b} \cdot \left(\exp \left(-D_{k2b} \frac{L_{eff}}{2l} \right) + 2 \exp \left(-D_{k2b} \frac{L_{eff}}{l} \right) \right)$$

$$\phi_i = \phi_{iON} - \frac{C_{OX}}{C_{OX} + (C_{Si}^{-1} + C_{BOX}^{-1})^{-1}} \cdot N_{OFF,FD} V_t \cdot \ln \left(1 + \exp \left(\frac{V_{th,FD} - V_{gs,eff} - V_{OFF,FD}}{N_{OFF,FD} V_t} \right) \right)$$

$$\phi_{iON} = 2\Phi_B + V_t \ln \left(1 + \frac{V_{gsteff,FD} (V_{gsteff,FD} + 2K1\sqrt{2\Phi_B})}{MoinFD \cdot K1 \cdot V_t^2} \right),$$

$$V_{gsteff,FD} = N_{OFF,FD} V_t \cdot \ln \left(1 + \exp \left(\frac{V_{gs,eff} - V_{th,FD} - V_{OFF,FD}}{N_{OFF,FD} V_t} \right) \right)$$

BSIMSOIv3.2 Equation List Copyright© 2004, UC Berkeley

Here N_{ch} is the channel doping concentration. N_{LX} is the lateral non-uniform doping coefficient to account for the lateral non-uniform doping effect. V_{FBb} is the backgate flatband voltage. $V_{th,FD}$ is the threshold voltage at $V_{bs}=V_{bs0}(\phi_i=2\Phi_B)$. V_t is thermal voltage. $K1$ is the body effect coefficient.

If $SoiMod=1$, the lower bound of V_{bs} (SPICE solution) is set to V_{bs0} . If $SoiMod=2$, V_{bs} is pinned at V_{bs0} . Notice that there is no body node and body leakage/charge calculation in $SoiMod=2$.

The zero field body potential that will determine the transistor threshold voltage, V_{bsmos} , is then calculated by

$$V_{bsmos} = V_{bs} - \frac{C_{Si}}{2qN_{ch}T_{Si}}(V_{bs0}(T_{OX} \rightarrow \infty) - V_{bs})^2 \text{ if } V_{bs} \leq V_{bs0}(T_{OX} \rightarrow \infty)$$

$$= V_{bs} \text{ else}$$

The subsequent clamping of V_{bsmos} will use the same equation that was utilized in BSIMPD. You can download the BSIMPD manual at:

<http://www-device.eecs.Berkeley.edu/~bsimsoi>

If $\text{SoiMod}=3$ is specified, BSIMSOI will select the operation mode for the user based on the estimated value of V_{bs0} at $\phi=2\Phi_B$ (bias independent), V_{bs0t} :

- If $V_{bs0t} > V_{bs0fd}$, BSIMSOI will be in the ideal FD mode ($\text{SoiMod}=2$).
- If $V_{bs0t} < V_{bs0pd}$, BSIMSOI will be in the BSIMPD mode ($\text{SoiMod}=0$).

Otherwise, BSIMSOI will be operated under $\text{SoiMod}=1$.

Notice that both V_{bs0fd} and V_{bs0pd} are model parameters.

A new model parameter, T_{OXM} , is introduced to represent the T_{OX} dependence for the model parameters $K1$ and $K2$ (compatible to BSIM3v3.2).

A new model parameter, N_{OFF} , is introduced in $V_{gsteff,cv}$ to adjust the CV curve around the threshold (compatible to BSIM3v3.2).

BSIMSOI3.2 Noise Model

The BSIMSOI3.2 version implements a flicker noise and thermal noise model compatible with BSIM4. In addition, the new noise model includes gate tunneling-induced shot noise and thermal noise due to gate electrode resistance. (1) Flicker noise models

Note: For output noise parameters, see [Chapter 10, MOSFET Noise Models](#).

Simple and Unified Flicker Noise Models

BSIMSOI3.2 provides two flicker noise models. When the model selector fnoiMod is set to 0, a simple flicker noise model which is convenient for hand calculation is invoked. A unified physical flicker noise model, which is the default model, will be used if $\text{fnoiMod}=1$. These two modes come from BSIMSOI3.1, but the unified model has many improvements. For instance, it is now smooth over all bias regions and considers the bulk charge effect.

- fnoiMOd = 0 (simple model)

$$S_{id}(f) = \frac{K_f f_{ds}^{af}}{C_{OX} L_{eff}^2 f^{ef}}$$

The noise density is:

- fnoiMOd = 1 (unified model)

The physical mechanism for the flicker noise is trapping/de-trapping related charge fluctuation in oxide traps, which results in fluctuations of both mobile carrier numbers and mobility in the channel. The unified flicker noise model captures this physical process.

The noise density in inversion region is given by:

$$S_{id,inv}(f) = \frac{k_B T q^2 \mu_{eff} I_{ds}}{C_{oxe} L_{eff}^2 A_{bulk} f^{ef} \cdot 10^{10}} \left(NOIA \log \left(\frac{N_0 + N^*}{N_l + N^*} \right) + NOIB (N_0 - N_l) + \frac{NOIC}{2} (N_0^2 - N_l^2) \right) \\ + \frac{k_B T I_{ds}^2 \Delta L_{clm}}{W_{eff} L_{eff}^2 f^{ef} \cdot 10^{10}} \frac{NOIA + NOIB \cdot N_l + NOIC \cdot N_l^2}{(N_l + N^*)^2}$$

where μ_{eff} is the effective mobility at the given bias condition, and L_{eff} and W_{eff} are the effective length and width, respectively. The parameter N_0 is the charge density at the source side given by:

$$N_0 = \frac{C_{OX} V_{gsteff}}{q}$$

The parameter N_l is the charge density at the source side given by:

$$N_l = \frac{C_{ox} V_{gsteff}}{q} \left(1 - \frac{A_{bulk} V_{dseff}}{V_{gsteff} + 2V_t} \right)$$

N^* is given by:

$$N^* = K_B T \cdot \frac{(C_{ox} + C_d + CIT)}{q_2}$$

where CIT is a model parameter from DC IV and C_d is the depletion capacitance. ΔL_{clm} is the channel length reduction due to channel length modulation and given by:

$$\Delta L_{clm} = Litl \cdot \log \frac{\frac{V_{ds} - V_{dseff}}{Litl} + EM}{E_{sat}}$$

$$E_{sat} = \frac{2VSAT}{\mu_{eff}}$$

In the subthreshold region, the noise density is written as:

$$S_{id, subvt}(f) = \frac{NOIA \cdot k_B T \cdot I_{ds}^2}{W_{eff} L_{eff} f^{EF} N^{*2} \cdot 10^{10}}$$

The total flicker noise density is:

$$S_{id}(f) = \frac{S_{id, inv}(f) \times S_{id, insubvt}(f)}{S_{id, inv}(f) + S_{id, insubvt}(f)}$$

Thermal noise models

There are two channel thermal noise models in BSIMSOI3.2 version. One is the charge based model (default) similar to that used in BSIMSOI3.1. The other is the holistic model. These two models can be selected through the model selector `tnoiMod`.

- `tnoiMod = 0` (charge based)

The noise current is given by:

$$\overline{i_d^2} = \frac{4k_B T \Delta f}{L_{eff}^2} \cdot \frac{NTNOI}{R_{ds} + \frac{L_{eff}}{\mu_{eff} |Q_{inv}|}}$$

where R_{ds} is the source/drain resistance, and the parameter $NTNOI$ is introduced from more accurate fitting of short-channel devices. Q_{inv} is the inversion channel charge computed from the capacitance models.

- `tnoiMod = 1` (holistic)

In this thermal noise model, all the short-channel effects and velocity saturation effects incorporated in the IV model are automatically included, hence the name “holistic thermal noise model.” In addition, the amplification of the channel thermal noise through G_m and G_{mbs} as well as the induced- gate noise

with partial correlation to the channel thermal noise are all captured in the new “noise partition” model.

The noise voltage source partitioned to the source side is given by:

$$\overline{v_d^2} = 4k_B T \cdot \theta_{moi}^2 \frac{V_{dseff} \Delta f}{I_{ds}}$$

and the noise current source put in the channel region with gate and body amplification is given by:

$$\overline{v_d^2} = 4k_B T \frac{V_{dseff} \Delta f}{I_{ds}} [G_{ds} + \beta_{moi} \cdot (G_m + G_{mbs})]^2 - \overline{v_d^2} \cdot (G_m + G_{ds} + G_{mbs})^2$$

where

$$\theta_{moi} = RNOIB \left[1 + TNOIB \cdot L_{eff} \left(\frac{V_{gsteff}}{E_{sat} L_{eff}} \right)^2 \right]$$

$$\beta_{moi} = RNOIA \left[1 + TNOIA \cdot L_{eff} \left(\frac{V_{gsteff}}{E_{sat} L_{eff}} \right)^2 \right]$$

Model Parameters in BSIMSOIv3.2

Table 166 Parameter Listing for BSIMSOIv3.2

Symbols Used in Equation	Symbol used in SPICE	Description	Unit	Default
SoiMod	SoiMod	SOI model selector (instance) SoiMOd=0 BSIMPD SoiMOd=1 Unified model for PD & FD SoiMod=2 ideal FD SoiMod=3 Auto selection by SIMSOI	-	0
T _{OXM}	toxm	Gate oxide thickness used in extraction	μ	T _{ox}
N _{OFF}	noff	CV parameter for V _{gsteff,cv}	-	1.0
V _{bs0fd}	vbs0fd	Upper bound of built-in potential lowering for ideal FD operation	V	0.0

Table 166 Parameter Listing for BSIMSOIv3.2

Symbols Used in Equation	Symbol used in SPICE	Description	Unit	Default
V_{bs0fd}	vbs0fd	Lowering bound of built- in potential lowering for ideal FD operation	V	0.5
fnoiMod	fnoiMod	Flicker noise model selector	-	1
tnoiMod	tnoiMod	Thermal noise model selector	-	0
NTNOI	ntnoi	Noise factor for short-channel devices for TNOIMOD=0 only	-	1.0
TNOIA	tnoia	Coefficient of channel-length dependence of total channel thermal noise	-	1.5
TNOIB	tnoib	Channel-length dependence parameter for channel thermal noise partitioning	-	3.5
RNOIA	rnoia	Thermal noise parameter		0.577
RNOIB	rnoib	Thermal noise parameter		0.37

Level 59 UC Berkeley BSIM3-SOI FD Model

The UC Berkeley SOI (BSIM3-SOI) Fully Depleted (FD) model is Level 59 in the Synopsys MOSFET models. For a description of this model, see the *BSIM3SOI FD2.1 MOSFET MODEL User Manual*, at:

<http://www-device.eecs.berkeley.edu/~bsim3soi>

The following sections discuss these topics:

- [General Syntax for BSIM3-SOI FD Model](#)
- [Level 59 Model Parameters](#)
- [Level 59 Template Output](#)

General Syntax for BSIM3-SOI FD Model

The general syntax for including a BSIM3-SOI FD MOSFET element in a netlist is:

```
Mxxx nd ng ns ne [np] mname [L=val]
+ [W=val] [M=val] [AD=val] [AS=val] [PD=val] [PS=val]
+ [NRD=val] [NRS=val] [NRB=val] [RTH0=val] [CTH0=val]
+ [off] [BJToff=val] [IC=Vds, Vgs, Vbs, Ves, Vps]
```

Parameter	Description
Mxxx	SOI MOSFET element name. Must begin with M, followed by up to 1023 alphanumeric characters.
nd	Drain terminal node name or number.
ng	Front gate node name or number.
ns	Source terminal node name or number.
ne	Back gate (or substrate) node name or number.
np	Optional external body contact node name or number.
mname	MOSFET model name reference.
L	SOI MOSFET channel length in meters. This parameter overrides DEFL in an OPTIONS statement. Default=DEFL with a maximum of 0.1m.
W	MOSFET channel width in meters. This parameter overrides DEFW in an OPTIONS statement. Default=DEFW.
M	Multiplier to simulate multiple SOI MOSFETs in parallel. The M setting affects all channel widths, diode leakages, capacitances, and resistances. Default=1.
AD	Drain diffusion area. Overrides DEFAD in the OPTIONS statement. Default=DEFAD.
AS	Source diffusion area. Overrides DEFAS in the OPTIONS statement. Default=DEFAS.
PD	Perimeter of the drain junction, including the channel edge. Overrides DEFPD in the OPTIONS statement.

Chapter 6: MOSFET Models (BSIM): Levels 47 through 72

Level 59 UC Berkeley BSIM3-SOI FD Model

Parameter	Description
PS	Perimeter of the source junction, including the channel edge. Overrides DEFPS in the OPTIONS statement.
NRD	Number of squares of drain diffusion for the drain series resistance. Overrides DEFNRD in the OPTIONS statement.
NRS	Number of squares of source diffusion for the source series resistance. Overrides DEFNRS in the OPTIONS statement.
NRB	Number of squares for the body series resistance.
RTH0	Thermal resistance per unit width: <ul style="list-style-type: none">▪ If you do not specify RTH0, simulation extracts it from the model card.▪ If you specify RTH0, it overrides RTH0 in the model card.
CTH0	Thermal capacitance per unit width <ul style="list-style-type: none">▪ If you do not specify CTH0, simulation extracts it from the model card.▪ If you specify CTH0, it overrides CTH0 in the model card.
OFF	Sets the initial condition to OFF for this element in DC analysis.
BJTOFF	Turns off BJT if equal to 1.
IC	Initial guess in the order (drain, front gate, internal body, back gate, external voltage). (ignores Vps in a 4-terminal device) Simulation uses these settings if you specify UIC in the .TRAN statement. The .IC statement overrides them.

Level 59 Model Parameters

Table 167 Model Control Parameters, Level 59

Parameter	Unit	Default	Description
CAPMOD	-	2	Flag for the short channel capacitance model
Level	-	-	Level 59 for BSIM3SOI

Table 167 Model Control Parameters, Level 59

Parameter	Unit	Default	Description
MOBMOD	-	1	Mobility model selector
NOIMOD	-	1	Flag for the Noise model
SHMOD	-	0	Flag for self-heating: <ul style="list-style-type: none"> ▪ 0=no self-heating ▪ 1=self-heating

Table 168 Process Parameters, Level 59

Parameter	Unit	Default	Description
NCH	1/cm ³	1.7e17	Channel doping concentration
NGATE	1/cm ³	0	Poly gate doping concentration
NSUB	1/cm ³	6.0e16	Substrate doping concentration
TBOX	m	3.0e-7	Buried oxide thickness
TOX	m	1.0e-8	Gate oxide thickness
TSI	m	1.0e-17	Silicon film thickness

Table 169 DC Parameters, Level 59

Parameter	Unit	Default	Description
A0	-	1.0	Bulk charge effect coefficient for the channel length
A1	1/V	0.0	First non-saturation effect parameter
A2	-	1.0	Second non-saturation effect parameter
ABP	-	1.0	Coefficient of A _{beff} dependency on V _{gst}
ADICE0	-	1	DICE bulk charge factor

Chapter 6: MOSFET Models (BSIM): Levels 47 through 72

Level 59 UC Berkeley BSIM3-SOI FD Model

Table 169 DC Parameters, Level 59 (Continued)

Parameter	Unit	Default	Description
AGIDL	1/W	0.0	GIDL constant
AGS	1/V	0.0	Gate bias coefficient of A_{bulk}
AI1	1/V	0.0	First V_{dsat} parameter for the L_{eff} dependence
ALPHA0	m/V	0.0	First parameter of the impact ionization current
ALPHA1	1/V	1.0	Second parameter of the impact ionization current
B0	m	0.0	Bulk charge effect coefficient for the channel width
B1	m	0.0	Width offset for the bulk charge effect
BGIDL	V/m	0.0	GIDL exponential coefficient
BI1	m/V	0.0	Second V_{dsat} parameter for the L_{eff} dependence
CDSC	F/m ²	2.4e-4	Drain/source to the channel coupling capacitance
CDSCB	F/m ²	0	Body-bias sensitivity of cdsc
CDSCD	F/m ²	0	Drain-bias sensitivity of cdsc
CI1	-	0.0	First V_{dsat} parameter for the V_{ds} dependence
CIT	F/m ²	0.0	Interface trap capacitance
DELP	V	0.02	Constant for limiting V_{bseff} to the surface potential
DELTA	-	0.01	Effective V_{ds} parameter
DI1	V	-1.0	Second V_{dsat} parameter for the V_{ds} dependence
DROUT	-	0.56	L dependence coefficient of the DIBL correction parameter in R_{out}
DSUB	-	0.56	DIBL coefficient exponent

Table 169 DC Parameters, Level 59 (Continued)

Parameter	Unit	Default	Description
DVBD0	V	0	First coefficient of the V_{ds} 0 dependency on Le_{ff}
DVBD1	V	0	Second coefficient of the V_{ds} 0 dependency on Le_{ff}
DVT0	-	2.2	First coefficient of the short-channel effect on V_{th}
DVT0W	-	0	First coefficient of the narrow-width effect on V_{th} for a small channel length
DVT1	-	0.53	Second coefficient of the short-channel effect on V_{th}
DVT1W	-	5.3e6	Second coefficient of the narrow-width effect on V_{th} for a small channel length
DVT2	1/V	-0.032	Body-bias coefficient of the short-channel effect on V_{th}
DVT2W	1/V	-0.032	Body-bias coefficient of the narrow width effect on V_{th} for small channel length
DWB	$m/V^{1/2}$	0.0	Coefficient of the substrate body bias dependence for We_{ff}
DWG	m/V	0.0	Coefficient of the gate dependence for We_{ff}
EDL	m	2e-6	Electron diffusion length
ETA0	-	0.08	DIBL coefficient in the subthreshold region
ETAB	1/V	-0.07	Body-bias coefficient for the DIBL effect in the subthreshold region
ISBJT	A/m^2	1.0e-6	BJT injection saturation current
ISDIF	A/m^2	0	Body to source/drain injection saturation current
ISREC	A/m^2	1.0e-5	Recombination in the depletion saturation current

Chapter 6: MOSFET Models (BSIM): Levels 47 through 72

Level 59 UC Berkeley BSIM3-SOI FD Model

Table 169 DC Parameters, Level 59 (Continued)

Parameter	Unit	Default	Description
ISTUN	A/m ²	0.0	Reverse tunneling saturation current
K1	V ^{1/2}	0.6	Coefficient for the first-order body effect
K2	-	0	Coefficient for the second-order body effect
K3	-	0	Narrow coefficient
K3B	1/V	0	Body-effect coefficient of k3
KB1	-	1	Coefficient of the V_{bs0} dependency on V_{gbs}
KB3	-	1	Coefficient of the V_{bs0} dependency on V_{gs} at subthreshold region
KBJT1	m/V	0	Parasitic bipolar Early effect coefficient
KETA	m	-0.6	Body-bias coefficient of the bulk charge effect
LINT	m	0.0	Length-offset fitting parameter from I-V without bias
MXC	-	-0.9	Fitting parameter for calculating A_{beff}
NDIODE	-	1.0	Diode non-ideality factor
NFACTOR	-	1	Subthreshold swing factor
NGIDL	V	1.2	GIDL V_{ds} enhancement coefficient
NLX	m	1.74e-7	Lateral non-uniform doping parameter
NTUN	-	10.0	Reverse tunneling non-ideality factor
PCLM	-	1.3	Channel length modulation parameter
PDIBL1	-	0.39	First correction parameter for the DIBL effect of the output resistance
PDIBL2	-	0.0086	Second correction parameter for the DIBL effect of the output resistance

Table 169 DC Parameters, Level 59 (Continued)

Parameter	Unit	Default	Description
PRWB	$1/V$	0	Body effect coefficient of R_{dsw}
PRWG	$1/V^{1/2}$	0	Gate bias effect coefficient of R_{dsw}
PVAG		0.0	Gate dependence of the Early voltage
RBODY	ohm/ m^2	0.0	Intrinsic body contact sheet resistance
RBSH	ohm/ m^2	0.0	Extrinsic body contact sheet resistance
RDSW	$\Omega \cdot \mu m^{wr}$	100	Parasitic resistance per unit width
RSH	ohm/square	0.0	Source/drain sheet resistance in ohm per square
U0	$cm^2/(V \cdot sec)$	NMOS-670 PMOS-250	Mobility at Temp= T_{nom}
UA	m/V	2.25e-9	First-order coefficient for mobility degradation
UB	$(m/V)^2$	5.87e-19	Second-order coefficient for mobility degradation
UC	$1/V$	-0.0465	Body-effect coefficient for mobility degradation
VBSA	V	0	Transition body voltage offset
VOFF	v	-0.08	Offset voltage in the subthreshold region for large W and L values
VSAT	m/sec	8e4	Saturation velocity at Temp= T_{nom}
VTH0	v	NMOS 0.7 PMOS -0.7	Threshold voltage @ $V_{bs}=0$ for a long, wide device
W0	m	0	Narrow width parameter
WINT	m	0.0	Width offset fitting parameter from I-V without bias
WR	-	1	Width offset from W_{eff} for calculating R_{ds}

Chapter 6: MOSFET Models (BSIM): Levels 47 through 72

Level 59 UC Berkeley BSIM3-SOI FD Model

Table 170 AC and Capacitance Parameters, Level 59

Parameter	Unit	Default	Description
ASD	V	0.3	Smoothing parameter for the source/drain bottom diffusion
CF	F/m	cal.	Gate to source/drain fringing field capacitance
CGDL	F/m	0.0	Lightly-doped drain-gate region overlap capacitance
CGDO	F/m	calculated	Non-LDD region drain-gate overlap capacitance per channel length
CGEO	F/m	0.0	Gate-substrate overlap capacitance per channel length
CGSL	F/m	0.0	Lightly-doped source-gate region overlap capacitance
CGSO	F/m	calculated	Non-LDD region source-gate overlap capacitance per channel length
CJSWG	F/m ²	1.e-10	Source/drain (gate side) sidewall junction capacitance per unit width (normalized to 100nm Tsi)
CKAPPA	F/m	0.6	Coefficient for lightly-doped region overlap capacitance fringing field capacitance
CLC	m	0.1e-7	Constant term for the short channel model
CLE	-	0.0	Exponential term for the short channel model
CSDESW	F/m	0.0	Source/drain sidewall fringing capacitance per unit length
CSDMIN	V	cal.	Source/drain bottom diffusion minimum capacitance
DLC	m	lint	Length offset fitting parameter for the gate charge
DWC	m	wint	Width offset fitting parameter from C-V
MJSWG	V	0.5	Source/drain (gate side) sidewall junction capacitance grading coefficient
PBSWG	V	0.7	Built-in potential for the source/drain (gate side) sidewall junction capacitance

Table 170 AC and Capacitance Parameters, Level 59

Parameter	Unit	Default	Description
TT	second	1ps	Diffusion capacitance transit time coefficient
VSDFB	V	cal.	Flatband voltage for the source/drain bottom diffusion capacitance
VSDTH	V	cal.	Threshold voltage for the source/drain bottom diffusion capacitance
XPART	-	0	Charge partitioning rate flag

Table 171 Temperature Parameters, Level 59

Parameter	Unit	Default	Description
AT	m/sec	3.3e4	Temperature coefficient for U_a
CTH0	m°C/(W*s)	0	Normalized thermal capacity
KT1	V	-0.11	Temperature coefficient for the threshold voltage
KT2	-	0.022	Body-bias coefficient for the temperature effect of the threshold voltage
KTIL	V*m	0	Channel length dependence of the temperature coefficient for the threshold voltage
PRT	Ω -um	0	Temperature coefficient for R_{dsw}
RTH0	m°C/W	0	Normalized thermal resistance
TNOM	°C	25	Temperature at which simulation expects parameters
UA1	m/V	4.31e-9	Temperature coefficient for U_a
UB1	(m/V) ²	-7.61e-18	Temperature coefficient for U_b
UC1	1/V	-0.056	Temperature coefficient for U_c

Table 171 Temperature Parameters, Level 59

Parameter	Unit	Default	Description
UTE	-	-1.5	Mobility temperature exponent
XBJT	-	1	Power dependence of j_{bjt} on the temperature
XDIF	-	XBJT	Power dependence of j_{dif} on the temperature
XREC	-	1	Power dependence of j_{rec} on the temperature
XTUN	-	0	Power dependence of j_{tun} on the temperature

Note: BSIMFD refers the substrate to the silicon below the buried oxide, not to the well region in BSIM3. It calculates the backgate flatband voltage (V_{fbb}) and the parameters related to the bottom capacitance of the source/drain diffusion (V_{sdth} , V_{sdfb} , C_{sdmin}).

- Positive n_{sub} means the same type of doping as the body.
- Negative n_{sub} means opposite type of doping.

Level 59 Template Output

For a list of output template parameters in the MOSFET models, and which parameters this model supports, see [Table 4 on page 22](#).

Level 60 UC Berkeley BSIM3-SOI DD Model

The UC Berkeley SOI model (BSIM3SOI) supports Fully Depleted (FD), Partially Depleted (PD), and Dynamically Depleted (DD) SOI devices. BSIM3DD2.2 for DD SOI devices is Level 60 in the Synopsys MOSFET models. For a description of this model, see the *BSIM3DD2.1 MOSFET MODEL User's Manual*, at

<http://www-device.eecs.berkeley.edu/~bsim3>

BSIM3DD2.1 includes many advanced concepts for dynamic and continuous transition between PD and FD operation. These concepts are collectively named Dynamic Depletion.

The following sections discuss these topics:

- [Model Features](#)
- [General Syntax for BSIM3-SOI DD Model](#)
- [Level 60 BSIMSOI Model Parameters](#)

Model Features

- Simulation applies dynamic depletion to both I-V and C-V. Tbox and Tsi continuously scale the charge and drain current.
- Supports external body bias and backgate bias; a total of 6 nodes.
- Real floating body simulation in both I-V and C-V. Diode and C-V formulation properly bind the body potential.
- Improved self-heating.
- Improved impact ionization current model.
- Various diode leakage components and parasitic bipolar current.
- Depletion charge model (EBCI) for better accuracy in predicting capacitive coupling. The BSIM3v3 based model is also improved.
- Dynamic depletion can suit different requirements for SOI technologies.
- Single I-V expression as in BSIM3v3.1 to assure continuities of I_{ds} , G_{ds} , G_m and their derivatives for all bias conditions.

General Syntax for BSIM3-SOI DD Model

The general syntax for a BSIM3SOI MOSFET element in a netlist is:

```
Mxxx nd ng ns ne [np] mname [L=val] [W=val] [M=val]
+ [AD=val] [AS=val] [PD=val] [PS=val] [NRD=val] [NRS=val]
+ [NRB=val] [RTHO=val] [CTHO=val] [off] [BJToff=val]
+ [IC=Vds, Vgs, Vbs, Ves, Vps] [SOIQ0=val]
```

Chapter 6: MOSFET Models (BSIM): Levels 47 through 72

Level 60 UC Berkeley BSIM3-SOI DD Model

Parameter	Description
Mxxx	SOI MOSFET element name. Must begin with M, followed by up to 1023 alphanumeric characters.
nd	Drain terminal node name or number.
ng	Front gate node name or number.
ns	Source terminal node name or number.
ne	Back gate (or Substrate) node name or number.
np	External body contact node name or number.
mname	MOSFET model name reference.
L	SOI MOSFET channel length in meters. This parameter overrides DEFL in an .OPTION statement. Default=DEFL with a maximum of 0.1m.
W	SOI MOSFET channel width in meters. This parameter overrides DEFW in an .OPTION statement. Default=DEFW with a maximum of 0.1m.
M	Multiplier to simulate multiple SOI MOSFETs in parallel. The M setting affects all channel widths, diode leakages, capacitances, and resistances. Default=1.
AD	Drain diffusion area. Overrides DEFAD in the .OPTION statement: Default=DEFAD
AS	Source diffusion area. Overrides DEFAS in the .OPTION statement: Default=DEFAS
PD	Perimeter of the drain junction, including the channel edge. Overrides DEFPD in the .OPTION statement.
PS	Perimeter of the source junction, including the channel edge. Overrides DEFPS in the .OPTION statement.
NRD	Number of squares of the drain diffusion for the drain series resistance. Overrides DEFNRD in the .OPTION statement.

Parameter	Description
NRS	Number of squares of the source diffusion for the source series resistance. Overrides DEFNRS in the.OPTION statement.
NRB	Number of squares for the body series resistance.
RDC	Additional drain resistance due to the contact resistance in units of ohms. This value overrides the RDC setting in the model specification. Default=0.0.
RSC	Additional source resistance due to the contact resistance in units of ohms. This value overrides the RDC setting in the model specification. Default=0.0.
RTHO	Thermal resistance per unit width: <ul style="list-style-type: none"> ▪ If you do not specify RTHO, simulation extracts it from the model card. ▪ If you specify RTHO, it overrides RTHO in the model card.
CTHO	Thermal capacitance per unit width: <ul style="list-style-type: none"> ▪ If you do not specify CTHO, simulation extracts it from the model card. ▪ If you specify CTHO, it overrides CTHO in the model card.
OFF	Sets the initial condition to OFF for this element in DC analysis.
BJTOFF	Turns off BJT if equal to 1.
IC	Initial guess in the order (drain, front gate, internal body, back gate, external voltage). Simulation ignores Vps in a 4-terminal device. Use these settings if you specify UIC in the .TRAN statement. The .IC statement overrides it.
SOIQ0	Floating body charge initialization. This parameter is set for the BQI algorithm of a floating body node.

Level 60 BSIMSOI Model Parameters

Table 172 Control Parameters, Level 60

SPICE Symbol	Description	Unit	Default	Notes See Table 177
shMod	Flag for self-heating <ul style="list-style-type: none"> ▪ 0=no self-heating ▪ 1=self-heating 	-	0	
mobMod	Mobility model selector	-	1	-
capMod	Flag for the short channel capacitance model	-	2	nl-1
noiMod	Flag for the noise model	-	1	-

Table 173 Process Parameters, Level 60

SPICE Symbol	Description	Unit	Default	Notes See Table 177
Tsi	Silicon film thickness	m	10 ⁻⁷	-
Tbox	Buried oxide thickness	m	3x10 ⁻⁷	-
Tox	Gate oxide thickness	m	1x10 ⁻⁸	-
Nch	Channel doping concentration	1/cm ³	1.7x10 ¹⁷	-
Nsub	Substrate doping concentration	1/cm ³	6x10 ¹⁶	nl-2
ngate	Poly gate doping concentration	1/cm ³	0	-

Table 174 DC Parameters, Level 60

SPICE Symbol	Description	Unit	Default	Notes See Table 177
vth0	Threshold voltage @ $V_{bs}=0$ for the long and wide device	V	0.7 for N -0.7 for P	nl-3

Table 174 DC Parameters, Level 60

SPICE Symbol	Description	Unit	Default	Notes See Table 177
k1	First order body effect coefficient	$\sqrt{V}^{1/2}$	0.5	-
k2	Second order body-effect coefficient	-	0	-
k3	Narrow width coefficient	-	0	-
k3b	Body-effect coefficient of k3	1/V	0	-
Vbsa	Transition body voltage offset	V	0	-
delp	Constant for limiting Vbseff to fs	V	0.02	-
Kb1	Coefficient of Vbs0 dependency on Ves	-	1	-
Dvbd0	First coefficient of Vbs0, Leff dependency	V	0	-
Dvbd1	Second coefficient of Vbs0, Leff dependency	V	0	-
w0	Narrow width parameter	m	0	-
nlx	Lateral non-uniform doping parameter	m	1.74e-7	-
dvt0	First coefficient of the short-channel effect on Vth	-	2.2	-
dvt1	Second coefficient of the short-channel Vth effect	-	0.53	-
dvt2	Body-bias coefficient of the short-channel Vth effect	1/V	-0.032	-
dvt0w	First coefficient of the narrow-width effect on Vth for a small channel length	-	0	-
dvt1w	Second coefficient of the narrow-width effect on Vth for a small channel length	-	5.3e6	-
dvt2w	Body-bias coefficient of the narrow-width effect on Vth for a small channel length	1/V	-0.032	-

Table 174 DC Parameters, Level 60

SPICE Symbol	Description	Unit	Default	Notes See Table 177
u0	Mobility at Temp=Tnom <ul style="list-style-type: none"> ▪ NMOSFET ▪ PMOSFET 	cm ² /(V-sec)	670 250	-
ua	First-order mobility degradation coefficient	m/V	2.25e-9	-
ub	Second-order mobility degradation coefficient	(m/V) ²	5.9e-19	-
uc	Body-effect of the mobility degradation coefficient	1/V	-.0465	-
vsat	Saturation velocity at Temp=Tnom	m/sec	8e4	-
a0	Bulk charge effect coefficient for the channel length	-	1.0	-
ags	Gate bias coefficient of A _{bulk}	1/V	0.0	-
b0	Bulk charge effect coefficient for the channel width	m	0.0	-
b1	Bulk charge effect width offset	m	0.0	-
keta	Body-bias coefficient of the bulk charge effect	m	-0.6	-
Abp	Coefficient of the Abeff dependency on Vgst	-	1.0	-
mxcc	Fitting parameter for calculating Abeff	-	-0.9	-
adice0	DICE bulk charge factor	-	1	-
A1	First non-saturation effect parameter	1/V	0.0	-
A2	Second non-saturation effect parameter	0	1.0	-
rdsw	Parasitic resistance per unit width	Ω-mm ^{Wr}	100	-

Table 174 DC Parameters, Level 60

SPICE Symbol	Description	Unit	Default	Notes See Table 177
prwb	Body-effect coefficient of R _{dsw}	1/V	0	-
prwg	Gate bias effect coefficient of R _{dsw}	1/V ^{1/2}	0	-
wr	Width offset from W _{eff} for calculating R _{ds}	-	1	-
wint	Width offset fitting parameter of I-V without bias	m	0.0	-
lint	Length offset fitting parameter of I-V without bias	m	0.0	-
dwg	Coefficient of the gate dependence of W _{eff}	m/V	0.0	-
dwb	Coefficient, substrate body bias dependence, W _{eff}	m/V ^{1/2}	0.0	-
voff	Offset voltage in the subthreshold region for large W and L values	V	-0.08	-
nfactor	Subthreshold swing factor	-	1	-
eta0	DIBL coefficient in the subthreshold region	-	0.08	-
etab	Body-bias coefficient for subthreshold DIBL effect	1/V	-0.07	-
dsub	DIBL coefficient exponent	-	0.56	-
cit	Interface trap capacitance	F/m ²	0.0	-
cdsc	Drain/Source to the channel coupling capacitance	F/m ²	2.4e-4	-
cdscb	Body-bias sensitivity of C _{dsc}	F/m ²	0	-
cdscd	Drain-bias sensitivity of C _{dsc}	F/m ²	0	-
pclm	Channel length modulation parameter	-	1.3	-

Table 174 DC Parameters, Level 60

SPICE Symbol	Description	Unit	Default	Notes See Table 177
pdibl1	Correction parameter for the DIBL effect of the first output resistance	-	.39	-
pdibl2	Correction parameter for the DIBL effect of the second output resistance	-	0.086	-
drout	L dependence coefficient of the DIBL correction parameter in Rout	-	0.56	-
pvag	Gate dependence of the Early voltage	-	0.0	-
delta	Effective V_{ds} parameter	-	0.01	-
aii	First V_{dsat} parameter for the L_{eff} dependence	1/V	0.0	-
bii	Second V_{dsat} parameter for the L_{eff} dependence	m/V	0.0	-
cii	First V_{dsat} parameter for the V_{ds} dependence	-	0.0	-
dii	Second V_{dsat} parameter for the V_{ds} dependence	V	-1.0	-
alpha0	First parameter of the impact ionization current	m/V	0.0	-
alpha1	Second parameter of the impact ionization current	1/V	1.0	-
beta0	Third parameter of the impact ionization current	V	30	-
Agidl	GIDL constant	Ω^{-1}	0.0	-
Bgidl	GIDL exponential coefficient	V/m	0.0	-
Ngidl	GIDL V_{ds} enhancement coefficient	V	1.2	-

Table 174 DC Parameters, Level 60

SPICE Symbol	Description	Unit	Default	Notes See Table 177
ntun	Reverse tunneling non-ideality factor	-	10.0	-
Ndiode	Diode non-ideality factor	-	1.0	-
Isbjt	BJT injection saturation current	A/m2	1e-6	-
Isdif	Body to source/drain injection saturation current	A/m2	0.0	-
Isrec	Recombination in the depletion saturation current	A/m2	1e-5	-
Istun	Reverse tunneling saturation current	A/m2	0.0	-
Edl	Electron diffusion length	m	2e-6	-
Kbjt1	Parasitic bipolar early effect coefficient	m/V	0	-
Rbody	Intrinsic body contact sheet resistance	ohm/m2	0.0	-
Rbsh	Extrinsic body contact sheet resistance	ohm/m2	0.0	-
rsh	Source drain sheet resistance in ohm per square	Ω /square	0.0	-

Table 175 AC and Capacitance Parameters, Level 60

SPICE Symbol	Description	Unit	Default	See Table 177
xpart	Charge partitioning rate flag	-	0	
cgso	Non-LDD region source-gate overlap capacitance per channel length	F/m	calculated	nC-1
cgdo	Non-LDD region drain-gate overlap capacitance per channel length	F/m	calculated	nC-2
cgeo	Gate substrate overlap capacitance per unit channel length	F/m	0.0	-

Table 175 AC and Capacitance Parameters, Level 60

SPICE Symbol	Description	Unit	Default	See Table 177
cjswg	Source/Drain (gate side) sidewall junction Capacitance per unit width (normalized to 100nm T _{si})	F/m ²	1e-10	-
pbswg	Built-in potential for the Source/Drain (gate side) sidewall junction capacitance	V	.7	-
mjswg	Grading coefficient for the Source/Drain (gate side) sidewall junction capacitance	V	0.5	-
tt	Coefficient for the diffusion capacitance transit time	second	1ps	-
vsdfb	Flatband voltage for the source/drain bottom diffusion capacitance	V	calculated	nC-3
vsdth	Threshold voltage for the source/drain bottom diffusion capacitance	V	calculated	nC-4
csdmin	Minimum capacitance of the source/drain bottom diffusion	V	calculated	nC-5
asd	Smoothing parameter for the source/drain bottom diffusion	-	0.3	-
csdesw	Source/drain sidewall fringing capacitance per unit length	F/m	0.0	-
cgs1	Overlap capacitance for the lightly-doped source-gate region	F/m	0.0	-
cgd1	Overlap capacitance for the lightly-doped drain-gate region	F/m	0.0	-
ckappa	Coefficient of the fringing field capacitance for the overlap capacitance in the lightly-doped region	F/m	0.6	-

Table 175 AC and Capacitance Parameters, Level 60

SPICE Symbol	Description	Unit	Default	See Table 177
cf	Fringing field capacitance for the gate-to-source/drain	F/m	calculated	nC-6
clc	Constant term for the short-channel mode	m	0.1×10^{-7}	-
cle	Exponential term for the short-channel mode	none	0.0	-
dlc	Length offset fitting parameter from C-V	m	lint	-
dwc	Width offset fitting parameter from C-V	m	wint	-

Table 176 Temperature Parameters, Level 60

SPICE Symbol	Description	Unit	Default	See Table 177
tnom	Temperature at which simulation expects parameters	°C	27	-
ute	Mobility temperature exponent	none	-1.5	-
kt1	Temperature coefficient for the threshold voltage	V	-0.11	-
kt11	Channel length dependence of the temperature coefficient for the threshold voltage	V*m	0.0	-
kt2	Body-bias coefficient of the V_{th} temperature effect	none	0.022	-
ua1	Temperature coefficient for U_a	m/V	4.31e-9	-
ub1	Temperature coefficient for U_b	(m/V) ²	-7.61e-18	-
uc1	Temperature coefficient for U_c	1/V	-.056	nT-1
at	Temperature coefficient for the saturation velocity	m/sec	3.3e4	-

Table 176 Temperature Parameters, Level 60

SPICE Symbol	Description	Unit	Default	See Table 177
cth0	Normalized thermal capacity	moC/(W*sec)	0	-
prt	Temperature coefficient for R _{dsw}	$\Omega\text{-}\mu\text{m}$	0	-
rth0	Normalized thermal resistance	moC/W	0	-
xbjt	Power dependence of j _{bjt} on the temperature	none	2	-
xdif	Power dependence of j _{dif} on the temperature	none	2	-
xrec	Power dependence of j _{rec} on the temperature	none	20	-
xtun	Power dependence of j _{tun} on the temperature	none	0	-

Table 177 MOSFET Level 60 Model Parameter Notes

Note	Explanation
nl-1	<i>Capmod</i> 0 and 1 do not calculate the dynamic depletion. Therefore, ddMod does not work with <i>capmod</i> .
nl-2	BSIMSOI refers to a substrate of the silicon below the buried oxide, not the well region in BSIM3. It calculates the backgate flatband voltage (V_{fbb}) and the parameters related to the source/drain diffusion bottom capacitance (V_{sdth} , V_{sdfb} , C_{sdmin}). <ul style="list-style-type: none"> Positive n_{sub} is the same type of doping as the body. Negative n_{sub} is the opposite type of doping.
nC-1	If you do not specify <i>cgso</i> , simulation calculates it: <ul style="list-style-type: none"> if you specify <i>d/c</i> greater than 0, then $cgso=pl=(dlc*cox)-cgs1$ if the previously-calculated $cgso<0$, then $cgso=0$ else $cgso=0.6*Tsi*cox$
nC-2	Calculates <i>Cgdo</i> similar to <i>Csdo</i>

Table 177 MOSFET Level 60 Model Parameter Notes

Note	Explanation
nC-3	<p>If nsub is positive, then:</p> $V_{sdfb} = -\frac{kT}{q} \log\left(\frac{10^{20} \cdot n_{sub}}{n_i \cdot n_i}\right) - 0.3 \text{ else: } V_{sdfb} = -\frac{kT}{q} \log\left(\frac{10^{20}}{n_{sub}}\right) + 0.3$
nC-4	<p>If nsub is positive, then:</p> $\phi_{sd} = 2\frac{kT}{q} \log\left(\frac{n_{sub}}{n_i}\right), \Upsilon_{sd} = \frac{5.753 \times 10^{-12} \sqrt{n_{sub}}}{C_{box}} \quad V_{sdth} = V_{sdfb} + \phi_{sd} + \Upsilon_{sd} \sqrt{\phi_{sd}} \text{ else:}$ $\phi_{sd} = 2\frac{kT}{q} \log\left(-\frac{n_{sub}}{n_i}\right), \Upsilon_{sd} = \frac{5.753 \times 10^{-12} \sqrt{-n_{sub}}}{C_{box}} \quad V_{sdth} = V_{sdfb} - \phi_{sd} + -\Upsilon_{sd} \sqrt{\phi_{sd}}$
nC-5	$X_{sdddep} = \sqrt{\frac{2\epsilon_{si}\phi_{sd}}{q n_{sub} \cdot 10^6 }}, C_{sdddep} = \frac{\epsilon_{si}}{X_{sdddep}}, C_{sdmin} = \frac{C_{sdddep}C_{box}}{C_{sdddep} + C_{box}}$
nC-6	<p>If you do not specify cf, then simulation calculates it:</p> $CF = \frac{2\epsilon_{ox}}{\pi} \ln\left(1 + \frac{4 \times 10^{-7}}{T_{ox}}\right)$
nT-1	<p>For mobmod=1 and 2, the unit is m/V². Default is -5.6E-11. For mobmod=3, the unit is 1/V and the default is -0.056.</p>

Level 65 SSIMSOI Model

Level 65 is a surface-potential, charge-based, and partially depleted SOI MOSFET model developed by Motorola semiconductor.

The following sections discuss these topics:

- [Using Level 65 with Synopsys Simulators](#)
- [General Syntax for SSIMSOI](#)

Using Level 65 with Synopsys Simulators

To simulate using the SSIMSOI model:

1. Set LEVEL=65 to identify the model as the SSIMSOI model.
2. Set the correct simulator room temperature.

The default room temperature is 25C in Synopsys circuit simulators, but is 27C in most other simulators. When comparing to other simulators, use `TEMP 27` or `.OPTION TNOM=27` to set the simulation temperature to 27 in the netlist.

3. Set DTEMP on the element line.

You can use DTEMP with this model to increase the temperature of individual elements, relative to the circuit temperature. If you do not specify DTEMP, simulation extracts TRISE from the model card. If you do specify DTEMP, it overrides TRISE in the model card.

General Syntax for SSIMSOI

```
Mxxx nd ng ns ne [np] mname [L=val] [W=val]
+ [M=val] [AD=val] [AS=val] [PD=val] [PS=val]
+ [BODYTYPE=val] [IGATE=val] [AB=val] [PB=val] [LXB=val]
+ [WXB=val] [LPE=val] [DTEMP=val]
```

Parameter	Description
Mxxx	SSIMSOI element name. Must begin with M, followed by up to 1023 alphanumeric characters.
nd	Drain terminal node name or number.
ng	Front gate node name or number.
ns	Source terminal node name or number.
ne	Back gate (or Substrate) node name or number.
np	External body contact node name or number.
mname	SSIMSOI model name reference.

Parameter	Description
L	SSIMSOI channel length in meters. Default is 5.0 um.
W	SSIMSOI channel width in meters. Default is 5.0 um.
M	Multiplier to simulate multiple SSIMSOIs in parallel. Default=1.
AD	Drain diffusion area. Default=0.
AS	Source diffusion area. Default=0.
PD	Drain diffusion perimeter. Default=0.
PS	Source diffusion perimeter. Default=0.
BODYTYPE	Flag to choose floating(0) or Tgate(2). Default=0.
IGATE	Flag to turn on/off(0/1) gate current calculations. Default=1.
AB	Body diffusion area. Default=0.
PB	Body diffusion perimeter (Body Contacted). Default=0.
LXB	Extrinsic Gate Length (Body Contacted). Default=0.
WXB	Extrinsic Gate Width (Body Contacted). Default=0.
LPE	Flag to turn on/off lpe-related parasitics.
DTEMP	Increases the temperature.

Table 178 SSIMSOI Model intrinsic Parameters (Geometry Modifiers and Threshold Voltage)

Name	Parameter	Units	Default
tox	Gate oxide thickness.	Angstrom	250
tbox	Back oxide thickness.	Angstrom	250
tsi	Silicon film thickness.	cm	0.2e-4

Chapter 6: MOSFET Models (BSIM): Levels 47 through 72
Level 65 SSIMSOI Model

Table 178 SSIMSOI Model intrinsic Parameters (Geometry Modifiers and Threshold Voltage)

Name	Parameter	Units	Default
vth0	Linear region vth, reference (large) MOSFET, Vbs=0	v	0.8 (nmos) -0.8 (pmos)
tcv	Temperature coefficient of threshold voltage.	1/K	0
vfb	Reference (large) MOSFET flatband voltage	v	calc
tcvfb	Temperature coefficient of flatband voltage	1/K	
ng	Poly gate doping density	1/cm ³	
ngf	Gate oxide fixed charge density	1/cm ²	0
pbias	Length modifier (use with odif)	micron	0
dlivcv	Length modified for capacitance model	micron	0
odif	Outdiffusion of s/d under gate	micron	0
odifs	Outdiffusion of s under gate (asymmetric)	micron	oidf
abias	Width modifier	micron	0
lidd	Ldd spacer width	micron	0
lg2ct	Distance from contact to poly edge	micron	1.0
dbias	Diffusion resistor processing bias	micron	0
nfs	Fast surface state density	1/V-cm ²	0
n1	Surface region doping density	1/cm ³	5.0e16
n2	Bulk region doping density	1/cm ³	2.0e16
wbrk	Depth of surface region	micron	0.2
vfbll	Length dependence parameter of vth0		0
vfble	Exponent for length dependence of vth0		-1

Table 178 SSIMSOI Model intrinsic Parameters (Geometry Modifiers and Threshold Voltage)

Name	Parameter	Units	Default
vfbwl	Width dependence parameter of vth0		0
vfbwe	Exponent for width dependence of vth0		-1
dphii	Norm. error in phi at extro. Vth0		0
cs1ll	I-dependence parameter of n1		0
cs1le	Exponent for I-dependence of n1		-1
cs2ll	I-dependence parameter of n2		0
cs2le	Exponent for I-dependence of n2		-1
cs1wl	W-dependence parameter of n1		0
cs1we	Exponent for w-dependence of n1		-1
cs2wl	W-dependence parameter of n2		0
cs2we	Exponent for w-dependence of n2		-1
dibl	I-dependence parameter of dibl		0
dible	Exponent for I-dependence of dibl		-2
gp1	Bulk charge coefficient		1.744
gp2	Bulk charge coefficient	1/V	0.8364
shrink	Linear size reduction	%	0
shrink2	Modified areal size reduction	%	0

Chapter 6: MOSFET Models (BSIM): Levels 47 through 72

Level 65 SSIMSOI Model

Table 179 SSIMSOI Model Intrinsic Parameters (Mobility and Saturation, Output Conductance)

Name	Parameter	Units	Default
ubref	Mobility parameter	cm ² /V-s	700 (nmos) 300 (pmos)
ubred	Mobility filed reduction factor	(cm/V) ^{egvexp}	100
eavfac	Effective field coefficient		0.5
eavfwl	Width dependence of eavfac		0.0
eavfwe	Exponent of width dependence of eavfac		-2.0
eavexp	Exponent of mobility field function		1.0
ubvds	Drain dependence of eff. field		0.5
vsat	Channel carrier saturation velocity	cm/sec	1.0e-7
esat0	Vsat divisor, velocity field model		2
esat1	Divisor, carrier velocity at sat.		1
lc00	Mult. For channel length modulation		0.2
lc01	Length dependence of lc00	1/micron	0
lc1	Bias dependence of channel length modulation	1/V	0
wlmod	Mult. for channel width modulation		0
dv2	Par. for lin/sat transition region		0.05
dv3	Length dependence of dv2		0
exb	Temperature exponent of ubref		1.5

Table 180 SSIMSOI Model Parasitic Parameters

Name	Parameter	Units	Default
aimp0	Impact ionization parameter		0

Table 180 SSIMSOI Model Parasitic Parameters

Name	Parameter	Units	Default
aimpl	Length dependence of aimp0	micron	0
aimpw	Width dependence of aimp0	micron	0
aimpt	Temperature dependence of aimp0	1/K	0
bimp0	Exponent for impact ionization	1/V	28.0
bimpl	Length dependence of bimp0	micron	0
bimp2	Width dependence of bimp0	micron	0
fsat1	Bias dependence of impact ionization	1/V	0
onkink	Voltage adjustment for onset of the kink	V	0
gtundeltox	Intrinsic region delta tox (electrical vs physical)	angstrom	(off)
gtundtoxovl	S/D overlap region delta tox (electrical vs physical)	angstrom	(off)
gtunstoxovl	S overlap region delta tox (asymmetric)	angstrom	gundtoxovl
gtunwdep	Accumulation 2-D fringing parameter	micron	0
gtunecbm	ECB effective mass		0.4
gtunecba	ECB fitting parameter		0.6
gtunecbb	ECB barrier height	V	3.1
gtunecbbo	ECB barrier height	V	3.1
gtunhvbm	HWB effective mass		0.3
gtunhvba	HVB fitting parameter		1.0
gtunhvbb	HVB barrier height	V	4.5
gtunhvbbbo	HVB barrier height	V	4.5
gtunevbeg	EVB energy bandgap	V	1.12

Table 180 SSIMSOI Model Parasitic Parameters

Name	Parameter	Units	Default
gtunevbm	EVB effective mass		0.32
gtunevba	EVB fitting parameter		0.4
gtunevbb	EVB barrier height	V	4.2
gtunevbbo	EVB barrier height	V	3.1
nbit	Effective doping parameter for I-bit		1.0
ndif	Effective doping parameter for Q-diffusion		1.0
cjch	S/D zero-bias junction channel-side capacitance	F/m	0.0
mich	S/D junction channel-side grading coefficient		0.5
pbch	S/D junction channel-side built-in pot.	V	0.8
tcppbch	S/D temperature coefficient for pbch	V/K	calculated
seff	S/D diode QNR recombination velocity	cm/s	1e5
seffl	I-dependence parameter for seff		0
seffle	Exponent for I-dependence for seff		0
seffwl	W-dependence parameter for seff		0
seffwe	Exponent for w-dependence for seff		0
sefft	Temperature adjustment coefficient for seff		0
jro	S/D diode SCR recombination coef	A/cm ²	1e6
jroll	I-dependence parameter for jro		0
jrole	Exponent for I-dependence for jro		0
jrowl	W-dependence parameter for jro		0
jrowe	Exponent for w-dependence for jro		0

Table 180 SSIMSOI Model Parasitic Parameters

Name	Parameter	Units	Default
jrot	Temperature adjustment coefficient for jro		calculated
m	S/D diode recombination slope factor		2.0
jgo	S/D diode SCR generation coefficient	A/cm ²	0
jgoll	I-dependence parameter for jgo		0
lgole	Exponent for I-dependence for jgo		0
jgowl	Exponent for I-dependence for jgo		0
jgowe	Exponent for w-dependence for jgo		0
jgot	Temperature adjustment coefficient for jgo		0
mg	S/D diode generation slope factor		2.0
seffs	S diode QNR recombination velocity (asymmetrical)	cm/s	seff
seffsll	I-dependence parameter for seffs		seffll
seffsle	Exponent for dependence for seffs		seffle
seffswl	W-dependence parameter for seffs		seffwl
seffswe	Exponent for w-dependence for seffs		seffwe
seffst	Temperature adjustment coefficient for seffs		sefft
jros	S diode SCT recombination coefficient (asymmetrical)	A/cm ²	jro
jrosll	I-dependence parameter for jro		jroll
jrosle	Exponent for I-dependence for jro		jrole
jroswl	W-dependence parameter for jro		jrowl
jroswe	Exponent for w-dependence for jro		jrowe
jrost	Temperature adjustment coefficient for jro		jrot

Table 180 SSIMSOI Model Parasitic Parameters

Name	Parameter	Units	Default
ms	S diode recombination slope factor (asymmetrical)		m
jgos	S diode SCR generation coefficient (asymmetrical)	A/cm ²	jgo
jgosll	I-dependence parameter for jgo		jgoll
jgosle	Exponent for I-dependence for jgo		jgole
jgoswl	W-dependence parameter for jgo		jgowl
jgoswe	Exponent for w-dependence for jgo		jgowe
jgost	Temperature adjustment coefficient for jgo		jgot
mgs	S diode generation slope factor		mg
gidla	GIDL pre-exponential parameter	A/m	(off)
gidlb	GIDL exponential parameter	m/V	3.0e9
gidlc	GIDL bulk-dependence parameter	V ³	8.0
gidle	GIDL bandgap	V	calculated
gidlt	GIDL temperature-dependence parameter		calculated
gisla	GISL pre-exponential parameter	A/m	gidla
gislb	GISL exponential parameter	m/V	gidlb
gislc	GISL bulk-dependence parameter	V ³	gidlc
gisle	GISL bandgap	V	gidle
gislt	GISL temperature-dependence parameter		gidlt
rshmin	Sheet res. of s/d-gate overlap	ohm/sq	0
tcmn	Temperature coefficient for rshmin	1/K	0
rshmins	Sheet res. of s-gate overlap (asymmetrical)	ohm/sq	rshmin

Table 180 SSIMSOI Model Parasitic Parameters

Name	Parameter	Units	Default
tcmns	Temperature coefficient for rshims (asymmetrical)	1/K	tcmn
rshpls	Sheet res. of heavily doped S/D	ohm/sq	0
tcpls	Temperature coefficient for rshpls	1/K	0
rshbody	Sheet res. of intrinsic body	ohm/sq	3000
rshbodyext	Sheet res. of extrinsic body	ohm/sq	3000
tcbody	Temperature coefficient for rshbody and rshbodyext	1/K	0
cfr	Gate to S/D fringing capacitance	F/micron	0
cfrs	Gate to s-fringing capacitance (asymmetrical)	F/micron	cfr
foc	Bias dependence of overlap capacitance		1.0
voc	Bias dependence of overlap capacitance	V	0
cfrb	Gate to body overlap capacitance	F/micron	0
cfrbox	Back-gate to S/D fringing capacitance	F/micron	0
odifact	S/D active diffusion	micron	0
odifbc	Body contact diffusion	micron	0
ccp	Contact-to-poly capacitance	F/micron	0
ccpr	Ccp error in RCE netlist	F/micron	0
ccc	Contact-to-contact capacitance	F/micron	0
cccr	Ccc error in RCE netlists	F/micron	0
ccx	Contact-to-soisub capacitance	F/micron	0
cpx	Poly-to-soisub capacitance	F/micron	0
wfr	Additional contact width	micron	0

Table 180 SSIMSOI Model Parasitic Parameters

Name	Parameter	Units	Default
nlev	Flicker noise equation level		0
kf	Flicker noise coefficient		0.0
af	Flicker noise exponent		1.0
cexp	Flicker noise cox exponent		1.0
fexp	Flicker noise frequency exponent		1.0

Level 66 HSPICE HVMOS Model

The HSPICE Level 66 model is Synopsys' proprietary model for high-voltage CMOS integrated circuits design and simulation. It is accurate in modeling the high-voltage device physics and robust in SPICE simulation. It is designed for various high-voltage CMOS processes, technology nodes, and device structures, including both widely-employed LDMOS (Laterally Diffused MOS) and EDMOS (Extended Drain MOS) transistors that may have any field plate oxide layer which helps the drain engineering. In addition, applications can be whole power management ICs such as switch power supply controllers, flash memory, hot-swap chips, and chips used in the automotive and medical industries.

This HSPICE HVMOS model is fully supported by Synopsys' parameter extraction tool, Aurora, and it has been widely adopted for production by many semiconductor companies and major foundries.

The model has been developed based on BSIM4, with high accuracy in geometrical, bias, and temperature scaling. It explicitly and accurately considers the following physical effects: independent bias-dependent drain/source resistances, quasi-saturation, self-heating, Gm fall-off in the saturation region, symmetric and asymmetrical source and drain structures, and many other high-voltage operation-related unique device behaviors.

For the details and usage, contact the Synopsys support teams.

General Syntax for the Level 66 Model

The general syntax for including a LEVEL 66 model element in a netlist is:

```

Mxxx nd ng ns [nb] mname [L=val] [W=val] [M=val]
+ [AD=val] [AS=val] [PD=val] [PS=val]
+ [RGATEMOD=val] [RBODYMOD=val]
+ [ACNQSMOD=val] [GEOMOD=val] [RGEOMOD=val]
+ [NRS=val] [NRD=val] [RBPB=val] [RBPB=val]
+ [RBPS=val] [RBSB=val]
+ [MIN=val] [RDC=val] [RSC=val] [DELVTO=val]
+ [MULU0=val] [DELK1=val]
+ [DELTOX=val] [OFF] [IC=Vds, Vgs, Vbs]
+ [WNFLAG=val]

```

The following table lists and describe the HVMOS Level 66 general parameters.

Note: For Level 66, the following list only presents the HSPICE proprietary model parameters, while the rest are the same as BSIM4.

Table 181 General Parameters for the Level 66 Model

Parameter	Description
ACNQSMOD	AC small-signal NQS model selector.
AD	Drain diffusion area.
AS	Source diffusion area.
DELK1	Shift in body bias coefficient (K1).
DELNFCT	Shift in subthreshold swing factor (NFACTOR).
DELTOX	Shift in gate electrical and physical oxide thickness (TOXE and TOXP). That is, the difference between the electrical and physical gate oxide/insulator thicknesses.
DELVTO (DELVTO)	Shift in the VTH0 zero-bias threshold voltage.
GEOMOD	Geometry-dependent parasitics model selector—specifies how the end S/D diffusions connect.
IC	Initial guess in the order
L	MOSFET channel length in meters.

Table 181 General Parameters for the Level 66 Model (Continued)

Parameter	Description
MIN	Whether to minimize the number of drain or source diffusions for even-number fingered device.
mname	MOSFET model name reference.
MULU0	Low-field mobility (U0) multiplier.
nb	Bulk terminal node name.
nd	Drain terminal node name.
NF	Number of device fingers.
ng	Gate terminal node name.
NRD	Number of drain diffusion squares.
NRS	Number of source diffusion squares.
ns	Source terminal node name.
OFF	Sets the initial condition to OFF in DC analysis.
PD	Perimeter of the drain junction: <ul style="list-style-type: none"> ▪ If PERMOD=0, it excludes the gate edge. ▪ Otherwise, it includes the gate edge.
PS	Perimeter of the source junction: <ul style="list-style-type: none"> ▪ If PERMOD=0, it excludes the gate edge. ▪ Otherwise, it includes the gate edge.
RBDB	Resistance connected between dbNode and bNode.
RBODYMOD	Substrate resistance network model selector.
RBPB	Resistance connected between bNodePrime and bNode.
RBPD	Resistance connected between bNodePrime and dbNode.
RBPS	Resistance connected between bNodePrime and sbNode.

Table 181 General Parameters for the Level 66 Model (Continued)

Parameter	Description
RBSB	Resistance connected between sbNode and bNode.
RDC	Drain contact resistance for per-finger device.
RGATEMOD	Gate resistance model selector.
RGEOMOD	Source/drain diffusion resistance and contact model selector—specifies the end S/D contact type: point wide or merged) and how to compute the S/D parasitics resistance.
RSC	Source contact resistance for per-finger device.
TRNQSMOD	Transient NQS model selector.
W	MOSFET channel width in meters.
WNFLAG	Turn on to select bin model based on width per NF for multi-finger devices.

Note: To print the substrate current when using the Level=66 model, you need to turn on the instance parameter RBODYMOD to output the substrate current.

For example:

```
MN VD VG VS VB nmod w=1 l=0.2 RBODYMOD=1
```

HSPICE prints mobility parameters for Level 66 and Level 68.

Level 70 BSIMSOI4.x Model Parameters

The UC Berkeley SOI model (BSIMSOI4.0) addresses several issues in modeling sub-0.13 micron CMOS/SOI high-speed and RF circuit simulations. Many inputs from the Compact Model Council (CMC) meetings were incorporated into the model. This model is fully backward compatible with its previous 3.X versions. For a description of this model, see the *BSIMSOI4.0 MOSFET Model User's Manual* at

<http://www-device.eecs.berkeley.edu/~bsimsoi/get.html>

The BSIMSOI4.0 model provides the following major improvements and additions over the BSIMSOI3.2 model:

- A scalable stress effect model for process induced stress effect; device performance thus becomes a function of the active area geometry and the location of the device in the active area.
- An asymmetric current/capacitance model S/D diode and asymmetric S/D resistance.
- An improved GIDL model with BSIM4 GIDL compatibility.
- Noise model improvements, such as:
 - Improved width/length dependence on flicker noise
 - SPICE2 thermal noise model is introduced as `TNOIMOD=2` with parameter `NTNOI` that adjusts the magnitude of the noise density
 - Body contact resistance induced thermal noise
 - Thermal noise induced by the body resistance network
 - Shot noises induced by `Ibs` and `Ibd` separated
- A two resistance body resistance network introduced for RF simulation.
- Threshold voltage model enhancement, such as:
 - Long-channel DIBL effect model added
 - Channel-length dependence of body effect improved
- Drain-induced threshold shift (DITS) model introduced in output conductance.
- Improved model accuracy in moderate inversion region with BSIM4 compatible `Vgsteff`.
- Multi-finger device with instance parameter `NF`.
- A new instance parameter `AGBCPD` to improve gate current for body contact.
- A new instance parameter `DELVTO` representing threshold voltage variation.
- Instance `FRBODY` is both an instance and a model parameter.

The following sections discuss these topics:

- [BSIMSOI4.3.1 Update](#)
- [BSIMSOI4.2, 4.3 Updates](#)
- [BSIMOI4.1 Update](#)

- [General Syntax for BSIMSOI4.x Model](#)
- [BSIMOI4.x Model Parameters](#)
- [Parameter Range Limit for BSIM4SOI4 Level 70](#)

BSIMSOI4.3.1 Update

In BSIMSOI4.3.1 the following updates are added:

1. The temperature derivative expressions are greatly improved.
2. Bugfixes related to `mtrlMod=1` are incorporated.
3. Thermal noise NF issue is fixed in SOI4.3.1.

For a description of this model, see the *BSIMSOI4..3.1 MOSFET Model User's Manual* at

<http://www-device.eecs.berkeley.edu/~bsimsoi/get.html>

BSIMSOI4.2, 4.3 Updates

In BSIMSOI versions 4.2 and 4.3, the following features were added:

1. Some bugs such as charge derivative issues are fixed in version 4.2.
2. The charge derivative issues in v4.2 and earlier versions are greatly improved in version 4.3.
3. Many expressions and derivatives are greatly improved in version 4.3, such as GISL.
4. A model parameter `BSOIUPDATE=0|1` has been added using a flag to control thermal noise nf fix for v. 4.3. Its default value is 0, providing “No fix” for backward compatibility. Setting `BSOIUPDATE=1` turns on the HSPICE thermal noise nf fix.

BSIMOI4.1 Update

In BSIMSOI4.1, the following features were added:

- A new material model (`mtrlMod`)
- Asymmetric GIDL/GISL model and new GIDL/GISL model (`gidlMod`)
- A new impact-ionization current model

- An improved Coulombic scattering model for high k/metal gate
- An improved body-contact model to characterize the opposite-type gate
- A new ΔV_{bi} model to simplify the parameter extraction
- A new VgsteffCV model for C-V, which is similar to Vgsteff in I-V
- A new gate current component in body contact region
- An improved DITS model with more flexibility and better fit

For a description of this model, see the *BSIMSOI4.1 MOSFET Model User's Manual* at <http://www-device.eecs.berkeley.edu/~bsimsoi/get.html>

Model parameter range limits for SSIMSOI4 are listed in [Table 194 on page 607](#).

General Syntax for BSIMSOI4.x Model

The general syntax for a BSIMSOI4.0 MOSFET element in a netlist is:

```
MXXX nd ng ns ne [np] [nb] [nT] mname [L=val] [W=val]
+ [M=val] [AD=val] [AS=val] [PD=val] [PS=val] [NRD=val]
+ [NRS=val] [NRB=val] [RTH0=val] [CTH0=val] [NBC=val]
+ [NSEG=val] [PDBCP=val] [PSBCP=val] [AGBCP=val] [AEBCP=val]
+ [VBSUSR=val] [DELTOX=val] [TNODEOUT] [off] [FRBODY=val]
+ [BJTOFF=val] [IC=vds, vgs, vbs, ves, vps] [dtemp=val]
+ [soimod=val] [rgatemod=val] [nf=val] [sa=val] [sb=val]
+ [sd=val] [rbdb=val] [rbsb=val] [delvto=val] [agbcpd=val]
+ [rbodymod=val] [mulu0=val] [SOIQ0=val]
+ [DELSVAT=val] [MULSVAT=val]
```

Parameter	Description
Mxxx	SOI MOSFET element name. Must begin with M, followed by up to 1023 alphanumeric characters.
nd	Drain terminal node name or number.
ng	Front gate node name or number.
ns	Source terminal node name or number.
ne	Back gate (or Substrate) node name or number.

Parameter	Description
np	External body contact node name or number. If 'body node' is to be checked in a <code>.biaschk</code> command, use keyword 'np' as in the BSIM3 SOI model.
nb	Internal body node name or number.
nT	Temperature node name or number.
mname	SOI MOSFET model name reference.
L	SOI MOSFET channel length in meters. The default is 5e-6.
W	SOI MOSFET channel width in meters. The default is 5e-6.
M	Multiplier to simulate multiple SOI MOSFETs in parallel. The M setting affects all channel widths, diode leakages, capacitances, and resistances. The default is 1.
AD	Drain diffusion area. The default is 0.
AS	Source diffusion area. The default is 0.
PD	Perimeter of the drain junction, including the channel edge. The default is 0.
PS	Perimeter of the source junction, including the channel edge. The default is 0.
NRD	Number of squares of drain diffusion for the drain series resistance. The default is 1.
NRS	Number of squares of source diffusion for the source series resistance. The default is 1.
NRB	Number of squares for the body series resistance. The default is 1.
FRBODY	Coefficient of the distributed body resistance effects. <ul style="list-style-type: none"> ▪ If FRBODY is not specified, it's extracted from the model card ▪ If FRBODY is specified, it overrides FRBODY in the model card
RTH0	Thermal resistance per unit width. <ul style="list-style-type: none"> ▪ If RTH0 is not specified, it's extracted from the model card ▪ If RTH0 is specified, it overrides RTH0 in the model card
CTH0	Thermal capacitance per unit width. <ul style="list-style-type: none"> ▪ If CTH0 is not specified, it's extracted from the model card ▪ If CTH0 is specified, it overrides RTH0 in the model card
NBC	Number of body contact isolation edge. The default is 0
NSEG	Number of segments for partitioning the channel width. The default is 1
PDBCP	Parasitic perimeter length for the body contact at the drain side. The default is 0

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Level 70 BSIMSOI4.x Model Parameters

Parameter	Description
PSBCP	Parasitic perimeter length for the body contact at the source side. The default is 0
AGBCP	Parasitic gate-to-body overlap area for the body contact. The default is 0
AEBCP	Parasitic body to substrate overlap area for the body contact. The default is 0
VBSUSR	Optional initial value of Vbs that you specify for transient analysis.
DELTOX	Shift in gate oxide thickness (TOX), that is, the difference between the electrical and physical gate oxide/insulator thickness. The default is 0
TNODEOUT	Temperature node flag indicating the use of the T node. If you do not set TNODEOUT, you can specify four nodes for a device to float the body. Specifying five nodes implies that the fifth node is the external body contact node with a body resistance between the internal and external terminals. This configuration applies to a distributed body resistance simulation. If you set TNODEOUT, simulation interprets the last node as the temperature node. You can specify five nodes to float the device. Specifying six nodes implies body contact. Seven nodes is a body-contacted case with a accessible internal body node. You can use the temperature node to simulate thermal coupling.
OFF	Sets the initial condition to OFF for this element in DC analysis.
BJTOFF	Turns off BJT if equal to 1.
IC	Initial guess in the order (drain, front gate, internal body, back gate, external voltage). Simulation ignores Vps in a 4-terminal device. Use these settings if you specify UIC in the .TRAN statement. The .IC statement overrides it.
DTEMP	Increase in temperature. The default is 0.
SOIMOD	SOI model selector. <ul style="list-style-type: none">▪ If SOIMOD is not specified, it's extracted from the model card▪ If SOIMOD is specified, it overrides SOIMOD in the model card
RGATEMOD	Gate resistance model selector. <ul style="list-style-type: none">▪ If RGATEMOD is not specified, it's extracted from the model card▪ If RGATEMOD is specified, it overrides RGATEMOD in the model card
NF	Number of fingers. The default is 1.
SA	Distance between OD edge to poly from one side. The default is 0.
SB	Distance between OD edge to poly from another side. The default is 0.
SD	Distance between neighboring fingers. The default is 0.

Parameter	Description
RBDB	Resistance between dbNode and bNode. <ul style="list-style-type: none"> ▪ If RBDB is not specified, it's extracted from the model card ▪ If RBDB is specified, it overrides RBDB in the model card
RBSB	Resistance between sbNode and bNode. <ul style="list-style-type: none"> ▪ If RBSB is not specified, it's extracted from the model card ▪ If RBSB is specified, it overrides RBSB in the model card
DELVTO	Zero bias threshold voltage variation. The default is 0.
AGBCPD	Parasitic gate to body overlap area for body contact in DC. The default is 0.
RBODYMOD	Body resistance model selector. <ul style="list-style-type: none"> ▪ If RBODYMOD is not specified, it's extracted from the model card ▪ If RBODYMOD is specified, it overrides RBODYMOD in the model card
MULU0	Low-field mobility (U0) multiplier($U0_{eff} = MULU0 * U0$), the default is 1.0
SOIQ0	Floating body charge initialization. This parameter is set for the BQI algorithm of a floating body node.
DELSVAT	Shift in Saturation velocity (VSAT).
MULSVAT	Scaling factor of Saturation velocity (VSAT), the default is 1.0.

BSIMOI4.x Model Parameters

The following tables list and describe the BSIMSOI4.0 model parameters.

- [Control Parameters, Level 70](#)
- [Process Parameters, Level 70](#)
- [DC Parameters, Level 70](#)
- [Gate-to-body Tunneling Parameters, Level 70](#)
- [AC and Capacitance Parameters, Level 70](#)
- [Temperature Parameters, Level 70](#)
- [Built-in Potential Lowering Model Parameters, Level 70](#)
- [Gate Resistance Parameters, Level 70](#)
- [Body Resistance Parameters, Level 70](#)
- [Noise Parameters, Level 70](#)

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Level 70 BSIMSOI4.x Model Parameters

- [Stress Model Parameters, Level 70](#)
- [Avalanche Impact Ionization Parameters, Level 70](#)

Table 182 Control Parameters, Level 70

Parameter	Description	Unit	Default	Bin
VERSION	Mode version number	-	4.3.1	N
BSOIUPDATE	Flag for fixing thermal noise NF issue in versions 4.0-4.3 <ul style="list-style-type: none">▪ 0 = Does not fix noise NF issue▪ 1 = Fixes noise NF issue		0	N
SHMOD	Flag for self-heating <ul style="list-style-type: none">▪ 0=no self-heating▪ 1=self-heating	-	0	N
MOBMOD	Mobility model selector	-	1	N
CAPMOD	Flag for the short channel capacitance model CAPMOD=2 and 3 are supported, CAPMOD=0 and 1 are not supported.	-	2	N
IGCMOD	Gate to channel tunneling current model selector	-	0	N
RDSMOD	Bias-dependent S/D resistance model selector	-	0	N

Table 183 Process Parameters, Level 70

Parameter	Description	Unit	Default	Bin
TSI ¹	Silicon film thickness	m	1e-7	N
TBOX	Buried oxide thickness	m	3e-7	N
TOX	Gate oxide thickness	m	1e-8	N
TOXM	Oxide thickness used in extraction	m	TOX	N
NCH	Channel doping concentration	cm ⁻³	1.7e17	Y
NSUB ²	Substrate doping concentration	cm ⁻³	6e16	Y

Table 183 Process Parameters, Level 70

Parameter	Description	Unit	Default	Bin
NGATE	Poly gate doping concentration	cm ⁻³	0	Y

1. In modern SOI technology, source/drain extension or LDD are commonly used. As a result, the source/drain junction depth (XJ) can be different from the silicon film thickness (TSI). By default, if XJ is not given, it is set to TSI. XJ is not allowed to be greater than TSI.

2. BSIMSOI4.0 refers the substrate to the silicon below the buried oxide (not to the well region in BSIM4) to calculate the backgate flatband voltage (V_{fb}) and the parameters related to the source/drain diffusion bottom capacitance (V_{sdth}, V_{sdfb}, and C_{sdmin})

– Positive NSUB means the same type of doping as the body

– Negative NSUB means the opposite type of doping.

Table 184 DC Parameters, Level 70

Parameter	Description	Unit	Default	Bin
VTH0 (VTO)	Threshold voltage @ V _{bs} =0 for the long and wide device	V	0.7 for N -0.7 for P	Y
K1	First order body effect coefficient	V ^{-1/2}	0.6	Y
K1W1	First body effect width dependent parameter	m	0	Y
K1W2	Second body effect width dependent parameter	m	0	Y
K2	Second order body-effect coefficient	-	0	Y
K3	Narrow width coefficient	-	0	Y
K3B	Body effect coefficient	V ⁻¹	0	Y
KB1	Backgate body charge coefficient	-	1	Y
W0	Narrow width parameter	m	0	Y
LPE0 (NLX)	Lateral non-uniform doping parameter	m	1.74e-7	Y
LPEB	Lateral non-uniform doping effect for body bias	m	0	Y
DVT0	First coefficient of the short-channel effect on V _{th}	-	2.2	Y

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Level 70 BSIMSOI4.x Model Parameters

Table 184 DC Parameters, Level 70

Parameter	Description	Unit	Default	Bin
DVT1	Second coefficient of the short-channel Vth effect	-	0.53	Y
DVT2	Body-bias coefficient of the short-channel Vth effect	V^{-1}	-0.032	Y
DVT0W	First coefficient of the narrow-width effect on Vth for a small channel length	-	0	Y
DVT1W	Second coefficient of the narrow-width effect on Vth for a small channel length	-	5.3e6	Y
DVT2W	Body-bias coefficient of the narrow-width effect on Vth for a small channel length	V^{-1}	-0.032	Y
U0	Mobility at Temp=TNOM	$cm^2/(V\cdot sec)$	670 for N 250 for P	Y
UA	First-order mobility degradation coefficient	m/V	2.25e-9	Y
UB	Second-order mobility degradation coefficient	$(m/V)^2$	5.9e-19	Y
UC	Body-effect of the mobility degradation coefficient	V^{-1}	-.0465	Y
VSAT	Saturation velocity at T=TNOM	m/sec	8e4	Y
A0	Bulk charge effect coefficient for channel length	-	1	Y
AGS	Gate bias coefficient of A_{bulk}	V^{-1}	0	Y
B0	Bulk charge effect for channel width	m	0	Y
B1	Bulk charge effect width offset	m	0	Y
KETA	Body-bias coefficient of bulk charge effect	V^{-1}	-0.6	Y
KETAS	Surface potential adjustment for bulk charge effect	V	0	Y
A1	First non-saturation effect parameter	V^{-1}	0	Y
A2	Second non-saturation effect parameter	-	1	Y

Table 184 DC Parameters, Level 70

Parameter	Description	Unit	Default	Bin
RDSW	Parasitic resistance per unit width	$\Omega\text{-}\mu\text{m}^{\text{WR}}$	100	Y
PRWB	Body-effect coefficient of R _{dsw}	V^{-1}	0	Y
PRWG	Gate bias effect coefficient of R _{dsw}	$\text{V}^{-1/2}$	0	Y
WR	Width offset from W _{eff} for calculating RDS	-	1	Y
NFACTOR	Subthreshold swing factor	-	1	Y
WINT	Width offset fitting parameter of I-V without bias	m	0	N
LINT	Length offset fitting parameter of I-V without bias	m	0	N
DWG	Coefficient of W _{eff} 's gate bias dependence	m/V	0	Y
DWB	Coefficient of W _{eff} 's body bias dependence	$\text{m}/\text{V}^{1/2}$	0	Y
DWBG	Width offset for body contact isolation edge	m	0	N
VOFF	Offset voltage in the subthreshold region for large W and L values	V	-0.08	Y
ETA0	DIBL coefficient in the subthreshold region	-	0.08	Y
ETAB	Body-bias coefficient for subthreshold DIBL effect	V^{-1}	-0.07	Y
DSUB	DIBL coefficient exponent	-	0.56	Y
CIT	Interface trap capacitance	F/m^2	0	Y
CDSC	Drain/Source to the channel coupling capacitance	F/m^2	2.4e-4	Y
CDSCB	Body-bias sensitivity of C _{dsc}	F/m^2	0	Y
CDSCD	Drain-bias sensitivity of C _{dsc}	F/m^2	0	Y
PCLM	Channel length modulation parameter	-	1.3	Y

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Level 70 BSIMSOI4.x Model Parameters

Table 184 DC Parameters, Level 70

Parameter	Description	Unit	Default	Bin
PDIBLC1	First output resistance DIBL effect correction parameter	-	0.39	Y
PDIBLC2	Second output resistance DIBL effect correction parameter	-	0.086	Y
DROUT	L dependence coefficient of the DIBL correction parameter in Rout	-	0.56	Y
PVAG	Gate dependence of the Early voltage	-	0	Y
DELTA	Effective V_{ds} parameter	-	0.01	Y
ALPHA0	First parameter of impact ionization current	-	0	Y
FBJTII	Fraction of bipolar current affecting the impact ionization	V^{-1}	0	Y
BETA0	First V_{ds} dependent parameter of impact ionization current	V^{-1}	0	Y
BETA1	Second V_{ds} dependent parameter of impact ionization current	-	0	Y
BETA2	Third V_{ds} dependent parameter of impact ionization current	V	0.1	Y
VDSATII0	Nominal drain saturation voltage at threshold for impact ionization current	V	0.9	Y
TII	Temperature dependent parameter for impact ionization current	-	0	N
LII	Length dependent parameter for impact ionization current	-	0	Y
ESATII	Saturation channel electric field for impact ionization current	V/m	1e7	Y
SII0	First V_{gs} dependent parameter for impact ionization current	V^{-1}	0.5	Y

Table 184 DC Parameters, Level 70

Parameter	Description	Unit	Default	Bin
SI1	Second V_{gs} dependent parameter for impact ionization current	V^{-1}	0.1	Y
SI2	Third V_{gs} dependent parameter for impact ionization current	-	0	Y
SIID	V_{ds} dependent parameter of drain saturation voltage for impact ionization current	V^{-1}	0	Y
AGIDL	Pre-exponent GIDL constant	Ω^{-1}	0	Y
BGIDL	GIDL exponential coefficient	V/m	2.3e9	Y
GDIDL	Body-bias effect on GIDL parameter	V^{-3}	0.5	Y
EGIDL (NGIDL)	Fitting parameter for band bending for GIDL	V	1.2	Y
NTUN	Reverse tunneling non-ideality factor for source	-	10	Y
NTUND	Reverse tunneling non-ideality factor for drain	-	NTUN	Y
NDIODE	Diode non-ideality factor for source	-	1	Y
NRECF0	Recombination non-ideality factor at forward bias for source	-	2	Y
NRECF0D	Recombination non-ideality factor at forward bias for drain	-	NRECF0	Y
NRECR0	Recombination non-ideality factor at reverse bias for source	-	10	Y
NRECR0D	Recombination non-ideality factor at reverse bias for drain	-	NRECR0	Y
ISBJT	BJT injection saturation current	A/m^2	1e-6	Y
IDBJT	BJT injection saturation current	A/m^2	ISBJT	Y

Chapter 6: MOSFET Models (BSIM): Levels 47 through 72
Level 70 BSIMSOI4.x Model Parameters

Table 184 DC Parameters, Level 70

Parameter	Description	Unit	Default	Bin
ISDIF	Body to source/drain injection saturation current	A/m ²	0	Y
IDDIF	Body to source/drain injection saturation current	A/m ²	ISDIF	Y
ISREC	Recombination in the depletion saturation current	A/m ²	1e-5	Y
IDREC	Recombination in the depletion saturation current	A/m ²	ISREC	Y
ISTUN	Reverse tunneling saturation current	A/m ²	0	Y
IDTUN	Reverse tunneling saturation current	A/m ²	ISTUN	Y
LN	Electron/hole diffusion length	m	2e-6	N
VREC0	Voltage-dependent parameter for recombination current for source	V	0	Y
VREC0D	Voltage-dependent parameter for recombination current for drain	V	VREC0	Y
VTUN0	Voltage-dependent parameter for tunneling current for source	V	0	Y
VTUN0D	Voltage-dependent parameter for tunneling current for drain	V	VTUN0	Y
NBJT	Power coefficient of channel length dependency for bipolar current	-	1	Y
LBJT0	Reference channel length for bipolar current	m	0.2e-6	Y
VABJT	Early voltage for bipolar current	V	10	Y
AELY	Channel-length dependency of early voltage for bipolar current	V/m	0	Y
AHLI	High-level injection parameter for bipolar current for source	-	0	Y

Table 184 DC Parameters, Level 70

Parameter	Description	Unit	Default	Bin
AHLID	High-level injection parameter for bipolar current for drain	-	AHLI	Y
RBODY	Intrinsic body contact sheet resistance	Ω/square	0	N
RBSH	Extrinsic body contact sheet resistance	Ω/square	0	N
RSH	Source drain sheet resistance in ohm per square	Ω/square	0	N
RHALO	Body halo sheet resistance	Ω/m	1e15	N
RSW	Zero bias lightly-doped source resistance per unit width for RDSMOD=1	$\Omega\text{-}\mu\text{m}^{\text{WR}}$	50	Y
RDW	Zero bias lightly-doped drain resistance per unit width for RDSMOD=1	$\Omega\text{-}\mu\text{m}^{\text{WR}}$	50	Y
RSWMIN	Lightly-doped source resistance per unit width at V_{gs} and zero V_{bs} for RDSMOD=1	$\Omega\text{-}\mu\text{m}^{\text{WR}}$	0	N
RDWMIN	Lightly-doped drain resistance per unit width at V_{gs} and zero V_{bs} for RDSMOD=1	$\Omega\text{-}\mu\text{m}^{\text{WR}}$	0	N
FRBODY	Layout-dependent RBODY multiplier	-	1	N
DVTP0	First parameter for V_{th} shift due to pocket	m	0	Y
DVTP1	Second parameter for V_{th} shift due to pocket	V^{-1}	0	Y
PDITS	Coefficient for drain-induced V_{th} shifts	V^{-1}	1e-20	Y
PDITSL	Length dependence of drain-induced V_{th} shifts	m^{-1}	0	N
PDITSD	V_{ds} dependence of drain-induced V_{th} shifts	V^{-1}	0	Y
FPROUT	Effect of pocket implant on ROUT degradation	$\text{V}/\text{m}^{0.5}$	0	Y
MINV	VGST_{eff} fitting parameter for moderate inversion	-	0	Y

Chapter 6: MOSFET Models (BSIM): Levels 47 through 72**Level 70 BSIMSOI4.x Model Parameters***Table 185 Gate-to-body Tunneling Parameters, Level 70*

Parameter	Description	Unit	Default	Bin
IGBMOD(I GMOD)	Gate to body tunneling current model selector	-	0	N
TOXQM	Oxide thickness for IGB calculation	m	TOX	N
NTOX	Power term of gate current	-	1	N
TOXREF	Target oxide thickness	m	2.5e-9	N
EBG	Effective bandgap in gate current calculation	V	1.2	N
ALPHAGB1	First VOX dependent parameter for gate current in inversion	V^{-1}	3.5	Y
BETAGB1	Second VOX dependent parameter for gate current in inversion	V^{-2}	0.03	Y
VGB1	Third VOX dependent parameter for gate current in inversion	V	300	N
VEVB	VAUX parameter for valence band electron tunneling	-	0.075	N
ALPHAGB2	First VOX dependent parameter for gate current in accumulation	V^{-1}	0.43	Y
BETAGB1	Second VOX dependent parameter for gate current in accumulation	V^{-2}	0.05	Y
VGB2	Third VOX dependent parameter for gate current in accumulation	V	17	N
VECB	VAUX parameter for conduction band electron tunneling	-	0.026	N

Table 186 AC and Capacitance Parameters, Level 70

Parameter	Description	Unit	Default	Bin
XPART	Charge partitioning rate flag	-	0	N
CGSO	Non-LDD region source-gate overlap capacitance per channel length	F/m	calculate	N

Table 186 AC and Capacitance Parameters, Level 70

Parameter	Description	Unit	Default	Bin
CGDO	Non-LDD region drain-gate overlap capacitance per channel length	F/m	calculate	N
CGEO	Gate substrate overlap capacitance per unit channel length	F/m	0	N
CJSWG	Source/Drain (gate side) sidewall junction capacitance per unit width (normalized to 100nm T_{si})	F/m ²	1e-10	N
CJSWGD	Drain (gate side) sidewall junction capacitance per unit width (normalized to 100 nm T_{si})	F/m ²	CJSWG	N
PBSWG	Source (gate side) sidewall junction capacitance built-in potential	V	0.7	N
PBSWGD	Drain (gate side) sidewall junction capacitance built-in potential	V	PBSWG	N
MJSWG	Source (gate side) sidewall junction capacitance grading coefficient	V	0.5	N
MJSWGD	Drain (gate side) sidewall junction capacitance grading coefficient	V	MJSWG	N
TT	Diffusion capacitance transit time coefficient	s	1e-12	N
NDIF	Power coefficient of channel length dependency for diffusion capacitance	-	-1	Y
LDIF0	Channel length dependency coefficient of diffusion capacitance	-	1	N
VSDFB	Source/drain bottom diffusion capacitance flatband voltage	V	calculate	Y
VSDTH	Source/drain bottom diffusion capacitance threshold voltage	V	calculate	Y
CSDMIN	Source/drain bottom diffusion minimum capacitance	V	calculate	N

Chapter 6: MOSFET Models (BSIM): Levels 47 through 72**Level 70 BSIMSOI4.x Model Parameters***Table 186 AC and Capacitance Parameters, Level 70*

Parameter	Description	Unit	Default	Bin
ASD	Source/drain bottom diffusion smoothing parameter f	-	0.3	N
CSDESW	Source/drain sidewall fringing capacitance per unit length	F/m	0	N
CGSL	Lightly-doped source-gate region overlap capacitance	F/m	0	Y
CGDL	Lightly-doped drain-gate region overlap capacitance	F/m	0	Y
CKAPPA	Coefficient lightly-doped region overlap capacitance fringing field capacitance	F/m	0.6	Y
CF	Gate-to-source/drain fringing field capacitance	F/m	calculate	N
CLC	Constant term for the short-channel mode	m	0.1e-7	N
CLE	Exponential term for the short-channel mode	-	0	N
DLC	Length offset fitting parameter from C-V	m	LINT	N
DLCB	Length offset fitting parameter for body charge	m	0	N
DLBG	Length offset fitting parameter for backgate charge	m	0	N
DWC	Width offset fitting parameter from C-V	m	WINT	N
DELVT	Threshold voltage adjust for C-V	V	0	Y
FBODY	Scaling factor for body charge	0	1	N
ACDE	Exponential coefficient for charge thickness in CAPMOD=3 for accumulation and depletion regions	m/V	1	Y
MOIN	Coefficient for the gate-bias dependent surface potential	$V^{-1/2}$	5	Y

Table 187 Temperature Parameters, Level 70

Parameter	Description	Unit	Default	Bin
TNOM	Temperature at which simulation expects parameters	°C	27	N
UTE	Mobility temperature exponent	-	-1.5	Y
KT1	Temperature coefficient for the threshold voltage	V	-0.11	Y
KT1L	Channel length dependence of the temperature coefficient for the threshold voltage	V*m	0	Y
KT2	Body-bias coefficient of the V_{th} temperature effect	-	0.022	Y
UA1	Temperature coefficient for U_a	m/V	4.31e-9	Y
UB1	Temperature coefficient for U_b	(m/V) ²	-7.61e-18	Y
UC1	Temperature coefficient for U_c	V ⁻¹	-0.056	Y
AT	Temperature coefficient for the saturation velocity	m/sec	3.3e4	Y
TCJSWG	Temperature coefficient of CJSWGS	K ⁻¹	0	N
TCJSWGD	Temperature coefficient of CJSWGD	K ⁻¹	TCJSWG	N
TPBSWG	Temperature coefficient of PBSWGS	V/K	0	N
TPBSWGD	Temperature coefficient of PBSWGD	V/K	TPBSWG	N
CTH0	Normalized thermal capacity	(W-sec)/mC	1e5	N
RTH0	Normalized thermal resistance	mC/W	0	N
PRT	Temperature coefficient for RDSW	Ω-μm	0	Y
NTRECF	Temperature coefficient for NRECF	-	0	Y

Chapter 6: MOSFET Models (BSIM): Levels 47 through 72
Level 70 BSIMSOI4.x Model Parameters

Table 187 Temperature Parameters, Level 70

Parameter	Description	Unit	Default	Bin
NTRECR	Temperature coefficient for NRECR	-	0	Y
XBJT	Power dependence of JBJT on the temperature	-	1	Y
XDIF	Power dependence of JDIF on the temperature	-	XBJT	Y
XDIFD	Power dependence of JDIFD on temperature	-	XDIF	Y
XREC	Power dependence of JREC on the temperature	-	1	Y
XRECD	Power dependence of JRECD on temperature	-	XREC	Y
XTUN	Power dependence of JTUN on the temperature	-	0	Y
ZTUND	Power dependence of JRECD on temperature	-	XTUN	Y
WTH0	Minimum width for thermal resistance calculation	m	0	N
SOIMOD	SOI model selector <ul style="list-style-type: none"> ▪ SOIMOD=0: BSIMPD ▪ SOIMOD=1: unified model for PD&FD ▪ SOIMOD=2: ideal FD ▪ SOIMOD=3: auto selection by BSIMSOI 	-	0	N
VBSA	Offset voltage due to non-idealities	V	0	N
NOFFFD	Smoothing parameter in FD module	-	1	N
VOFFFD	Smoothing parameter in FD module	V	0	N
K1B	First backgate body effect parameter	-	1	N
K2B	Second backgate body effect parameter for short channel effect	-	0	N
DK2B	Third backgate body effect parameter for short channel effect	-	0	N

Table 187 Temperature Parameters, Level 70

Parameter	Description	Unit	Default	Bin
DVBD0	First short channel effect parameter in FD module	-	0	N
DVBD1	Second short channel effect parameter in FD module	-	0	N
MOINFD	Gain bias dependence coefficient of surface potential in FD module	-	1e3	N
VBS0PD	Upper bound of built-in potential lowering for BSIMPD operation	V	0	N
VBS0FD	Upper bound of built-in potential lowering for ideal FD operation	V	0.5	N

Table 188 Built-in Potential Lowering Model Parameters, Level 70

Parameter	Description	Unit	Default	Bin
SOIMOD	SOI model selector <ul style="list-style-type: none"> SOIMOD=0: BSIMPD SOIMOD=1: unified model for PD&FD SOIMOD=2: ideal FD SOIMOD=3: auto selection by BSIMSOI 	-	0	N
VBSA	Offset voltage due to non-idealities	V	0	N
NOFFFD	Smoothing parameter in FD module	-	1	N
VOFFFD	Smoothing parameter in FD module	V	0	N
K1B	First backgate body effect parameter	-	1	N
K2B	Second backgate body effect parameter for short channel effect	-	0	N
DK2B	Third backgate body effect parameter for short channel effect	-	0	N

Chapter 6: MOSFET Models (BSIM): Levels 47 through 72**Level 70 BSIMSOI4.x Model Parameters***Table 188 Built-in Potential Lowering Model Parameters, Level 70*

Parameter	Description	Unit	Default	Bin
DVBD0	First short channel effect parameter in FD module	-	0	N
DVBD1	Second short channel effect parameter in FD module	-	0	N
MOINFD	Gain bias dependence coefficient of surface potential in FD module	-	1e3	N
VBS0PD	Upper bound of built-in potential lowering for BSIMPD operation	V	0	N
VBS0FD	Upper bound of built-in potential lowering for ideal FD operation	V	0.5	N

Table 189 Gate Resistance Parameters, Level 70

Parameter	Description	Unit	Default	Bin
RGATEMOD	Gate resistance model selector <ul style="list-style-type: none"> ▪ 0: No gate resistance ▪ 1: Constant gate resistance ▪ 2: Rii model with variable resistance ▪ 3: Rii model with two nodes 	-	0	N
RSHG	Gate electrode sheet resistance	0.1	Ω/square	N
XRCRG1	Parameter for distributed channel resistance effect for intrinsic input resistance	12	-	Y
XRCRG2	Parameter to account for the excess channel diffusion resistance for intrinsic input resistance	1	-	Y
NGCON	Number of gate contacts	1	-	N
XGW	Distance from the gate contact to the channel edge	0	m	N
XGL	Offset of the gate length due to variations in patterning	0	m	N

Table 190 Body Resistance Parameters, Level 70

Parameter	Description	Unit	Default	Bin
RBODYMOD	Body resistance model selector <ul style="list-style-type: none"> ▪ 0: No body resistance model ▪ 1: Two-resistor body resistance model 	-	0	N
GBMIN	Conductance parallel with RBSB/RBDB	Ohm	1e-12	N
RBDB	Resistance between dbNode and bNode	Ohm	50	N
RBSB	Resistance between sbNode and bNode	Ohm	50	N

Table 191 Noise Parameters, Level 70

Parameter	Description	Unit	Default	Bin
FNOIMOD	Flicker noise model selector	-	1	N
TNOIMOD	Thermal noise model selector	-	0	N
NTNOI	Noise factor for short-channel devices for TNOIMOD=0 or 2	-	1	N
TNOIA	Coefficient of channel length dependence of total channel thermal noise	-	1.5	N
TONIB	Channel length dependence parameter for channel thermal noise partitioning	-	3.5	N
RNOIA	Thermal noise parameter	-	0.577	N
RNOIB	Thermal noise parameter	-	0.37	N
BF	Flicker noise length dependence exponent	-	2	N
W0FLK	Flicker noise width dependence parameter	-	-1	N

Chapter 6: MOSFET Models (BSIM): Levels 47 through 72**Level 70 BSIMSOI4.x Model Parameters***Table 192 Stress Model Parameters, Level 70*

Parameter	Description	Unit	Default	Bin
SAREF	Reference distance between OD and edge to poly of one side	m	1e-6	N
SBREF	Reference distance between OD and edge to poly of another side	m	1e-6	N
WLOD	Width parameter for stress effect	m	0	N
KU0	Mobility degradation/enhancement	m	0	Y
KVSAT	Saturation velocity degradation/enhancement parameter for stress effect	m	0	N
KVTH0	Threshold shift parameter for stress effect	V-m	0	Y
TKU0	Temperature coefficient of KU0	-	0	N
LLODKU0	Length parameter for KU0 stress effect	-	0	N
WLODKU0	Width parameter for KU0 stress effect	-	0	N
LLODVTH	Length parameter for Vth stress effect	-	0	N
WLODVTH	Width parameter for Vth stress effect	-	0	N
STK2	K2 shift factor related to Vth0 change	m	0	N
LODK2	K2 shift modification factor for stress effect	-	1	N
STETA0	Eta0 shift factor related to Vth0 change	m	0	N
LODETA0	Eta0 shift modification factor for stress effect	-	1	N

The parameters in [Table 193](#) improve the BSIM4SOI model to address parasitic BJT-induced avalanche impact ionization current. Contact Synopsys for details.

Table 193 Avalanche Impact Ionization Parameters, Level 70

Parameter	Description	Unit	Default	Notes
IIMOD	Impact ionization model selector	-	0 (original II model)	=1 selects the new II model

Table 193 Avalanche Impact Ionization Parameters, Level 70

Parameter	Description	Unit	Default	Notes
EBJTII	Impact ionization parameter for BJT part	1/V	0.0	-
CBJTII	Length scaling parameter for II BJT part	m/V	0.0	-
VBCI	Internal B-C built-in potential	V	0.7	-
ABJTII	Exponent factor for avalanche current	-	0.0	-
MBJTII	Internal B-C grading coefficient	-	0.4	-
TVBCI	Temperature coefficient for VBCI	-	0.0	-

Parameter Range Limit for BSIM4SOI4 Level 70

Simulation reports either a warning or a fatal error if BSIMSOI4 parameters fall outside predefined ranges. These range limitations prevent (or at least warn of) potential numerical problems.

To control the maximum number of simulation warning messages printing to the output file, use:

```
.OPTION WARNLIMIT=#
```

In the preceding `.OPTION` statement, # is the maximum number of warning messages that simulation reports. The default `WARNLIMIT` value is 1. In some cases (as noted in [Table 194](#) below), simulation checks parameters only if you set the `PARAMCHK=1` model parameter.

Table 194 Model Parameter Range Limit, Level 70

Parameter	Limit
wlod	< 0 warn
kvsat	< -1.0, >1.0 warn
Lpe0	< -leff fatal
saref	<= 0 fatal

Chapter 6: MOSFET Models (BSIM): Levels 47 through 72
Level 70 BSIMSOI4.x Model Parameters

Table 194 Model Parameter Range Limit, Level 70

Parameter	Limit
sbref	≤ 0 fatal
Lpeb	$< -leff$ fatal
fprout	< 0 fatal
pdits	< 0 fatal
pditsl	< 0 fatal
tox	$tox + deltox \leq 0$ fatal
toxm	$toxm + deltox \leq 0$ fatal
nf	< 1 fatal
tbox	≤ 0 fatal
npeak	≤ 0 fatal
ngate	$< 0, > 1e25$ fatal
dvt1	< 0 fatal
dvt1w	< 0 fatal
w0	$w0 + weff = 0$ fatal
dsub	< 0 fatal
b1+weff	$b1 + weff = 0$ fatal
u0	≤ 0 fatal
delta	< 0 fatal
vsat	≤ 0 fatal
pclm	≤ 0 fatal
drout	< 0 fatal

Table 194 Model Parameter Range Limit, Level 70

Parameter	Limit
pd	< w warn
ps	< w warn
clc	< 0 fatal
noff	< 0.1, > 4.0 warn
lodk2	<= 0 warn
lodeta0	<= 0 warn
moin	< 5, > 25 warn
moinfd	< 5 warn
acde	< 0.1, > 1.6 warn
if paramchk=1 following parameter limit range is added	
leff	<= 5e-8 warn
leffcv	<= 5e-8 warn
weff	<= 1e-7 warn
weffcv	<= 1e-7 warn
lpe0	< 0 warn
npeak	<= 1e15, >= 1e21 warn
nsub	<= -1e21, >= 1e21 warn
ngate	< 1e18 warn
dvt0	< 0 warn
w0	w0+weff < 1e-7 warn
nfactor	< 0 warn

Chapter 6: MOSFET Models (BSIM): Levels 47 through 72
Level 70 BSIMSOI4.x Model Parameters

Table 194 Model Parameter Range Limit, Level 70

Parameter	Limit
cdsc	< 0 warn
cdscd	< 0 warn
eta0	< 0 warn
b1	$b1 + weff < 1e-7$ warn
a2	< 0.01, > 1 warn
rdsw	< warn
rds0	< 0.001 warn
vsattemp	< 1e3 warn
pdibl1	< 0 warn
pdibl2	< 0 warn
cgdo	< 0 warn
cgso	< 0 warn
cgeo	< 0 warn
ntun	< 0 warn
ntund	< 0 warn
ndiode	< 0 warn
ndioded	< 0 warn
isbjt	< 0 warn
idbjt	< 0 warn
isdiff	< 0 warn
iddiff	< 0 warn

Table 194 Model Parameter Range Limit, Level 70

Parameter	Limit
isrec	< 0 warn
idrec	< 0 warn
istun	< 0 warn
idtun	< 0 warn
tt	< 0 warn
csdmin	< 0 warn
csdesw	< 0 warn
asd	< 0 warn
rth0	< 0 warn
cth0	< 0 warn
rbody	< 0 warn
rbsh	< 0 warn
nigc	<= 0 warn
poxedge	<= 0 warn
pigcd	<= 0 warn
wth0	< 0 warn
rhalo	< 0 warn
ntox	< 0 warn
toxref	< 0 warn
ebg	< 0 warn
vevb	< 0 warn

Chapter 6: MOSFET Models (BSIM): Levels 47 through 72
Level 70 BSIMSOI4.x Model Parameters

Table 194 Model Parameter Range Limit, Level 70

Parameter	Limit
alphagb1	< 0 warn
betagb1	< 0 warn
vgb1	< 0 warn
vecb	< 0 warn
alphagb2	< 0 warn
betagb2	< 0 warn
vgb2	< warn
toxqm	< 0 warn
voxh	< 0 warn
beltavox	<= 0 warn
k1w1	< 0 warn
k1w2	< 0 warn
ketas	< 0 warn
dwbc	< 0 warn
beta0	< 0 warn
beta1	< 0 warn
beta2	< 0 warn
tii	< 0 warn
lii	< 0 warn
sii1	< 0 warn
sii2	< 0 warn

Table 194 Model Parameter Range Limit, Level 70

Parameter	Limit
siid	< 0 warn
fbjtii	< 0 warn
vrec0	< 0 warn
vrec0d	< 0 warn
vtun0	< 0 warn
vtun0d	< 0 warn
nbjt	< 0 warn
aely	< 0 warn
ahli	< 0 warn
ahlid	< 0 warn
rbody	< 0 warn
rbsh	< 0 warn
ntrecf	< 0 warn
ntrecr	< 0 warn
tcjswg	< 0 warn
tpbswg	< 0 warn
tcjswgd	< 0 warn
tpbswgd	< 0 warn
acde	< 0.1, > 1.6 warn
moin	< 5, > 25 warn
dlbg	< 0 warn

Table 194 Model Parameter Range Limit, Level 70

Parameter	Limit
agidl	< 0 warn
bgidl	< 0 warn
cgidl	< 0 warn
egidl	< 0 warn
esatii	<= 0 warn
xj	> tsi warn
capmod	< 2 warn

Level 71 TFT Model

Thin-film transistor (TFT) process technology has been the industry mainstream technology of choice to implement various flat-panel display applications. While there exist many similarities in the electrical terminal characteristics between TFTs and their crystalline silicon counterparts, unique charge trapping/de-trapping and charge carrier transport mechanisms associated with the grains and grain boundaries in the channel region have led to significant technical challenges in TFT device modeling for accurate and scalable SPICE simulations.

The Level 71 TFT model is a unified model. It is used for polycrystalline silicon (p-si), but it is also applicable to amorphous silicon (a-si). The model has been developed based on BSIMSOI, with high accuracy in geometrical, bias, and temperature scaling. It explicitly and accurately considers the following physical effects: non-ideality of the subthreshold swing, quasi-saturation, bias-dependent source/drain resistance, kink in the saturation region, self heating, large leakage current, and many other related device behaviors.

This HSPICE TFT model is fully supported by Synopsys' parameter extraction tool, Aurora. For detail on usage, contact the Synopsys support teams.

The following sections discuss these topics:

- General Syntax for the Level 71 Model

General Syntax for the Level 71 Model

The general syntax for including a LEVEL 71 model element in a netlist is:

```
Mxxx nd ng ns ne [np] [nb] [nT] mname [L=val]
+ [M=val] [AS=val] [PS=val] [NRD=val]
+ [NRS=val] [NRB=val] [CTH0=val]
+ [NSEG=val] [PDBCP=val] [PSBCP=val] [AGBCP=val]
+ [AEBCP=val] [DELTOX=val] [TNODEOUT]
+ [off] [FRBODY] [BJToff=val] [IC=Vds, Vgs, Vbs, Ves, Vps]
```

Argument Descriptions

Table 195 TFT Model Arguments and Options

Argument	Description
Mxxx	TFT element name. Must begin with M, followed by up to 1023 alphanumeric characters.
nd	Drain terminal node name or number.
ng	Front gate node name or number.
ns	Source terminal node name or number.
ne	Back gate (or substrate) node name or number.
np	External body contact node name or number.
nb	Internal body node name or number.
nT	Temperature node name or number.
mname	MOSFET model name reference.
L	TFT channel length in meters. This parameter overrides DEFL in an OPTIONS statement. Default=DEFL with a maximum of 0.1m.

Chapter 6: MOSFET Models (BSIM): Levels 47 through 72

Level 71 TFT Model

Table 195 TFT Model Arguments and Options (Continued)

Argument	Description
W	MOSFET channel width in meters. This parameter overrides DEFW in an OPTIONS statement. Default=DEFW.
M	Multiplier to simulate multiple TFT in parallel. The M setting affects all channel widths, diode leakages, capacitances, and resistances. Default=1.
AD	Drain diffusion area. Overrides .OPTION DEFAD statement. Default=DEFAD.
AS	Source diffusion area. Overrides .OPTION DEFAS statement. Default=DEFAS.
PD	Drain junction perimeter, including channel edge. Overrides .OPTION DEFPD.
PS	Source junction perimeter including channel edge. Overrides .OPTION DEFPS.
NRD	Number of squares of drain diffusion for the drain series resistance. Overrides .OPTION DEFNRD.
NRS	Number of squares of source diffusion for the source series resistance. Overrides .OPTION DEFNRS.
NRB	Number of squares for the body series resistance.
FRBODY	Coefficient of the distributed body resistance effects. Default=1.0
RTH0	Thermal resistance per unit width: If you do not specify RTH0, simulation extracts it from the model card. If you specify RTH0, it overrides RTH0 in the model card.
CTH0	Thermal capacitance per unit width: If you do not specify CTH0, simulation extracts it from the model card. If you specify CTH0, it overrides CTH0 in the model card.
NBC	Number of body contact isolation edge.
NSEG	Number of segments for partitioning the channel width.
PDBCP	Parasitic perimeter length for the body contact a the drain side.

Table 195 TFT Model Arguments and Options (Continued)

Argument	Description
PSBCP	Parasitic perimeter length for the body contact at the source side.
AGBCP	Parasitic gate-to-body overlap area for the body contact.
AEBCP	Parasitic body-to-substrate overlap area for the body contact.
VBSUSR	Optional initial Compared value of Vbs that you specify for transient analysis.
DELTOX	Shift in gate oxide thickness (TOX). That is, the difference between the electrical and physical gate oxide/insulator thicknesses.
TNODEOUT	Temperature node flag indicating the use of the T node. ¹ See footnote below.
OFF	Sets the initial condition of the element to OFF in DC analysis.
BJTOFF	Turning off BJT if equal to 1.
IC	Initial guess in the order (drain, front gate, internal body, back gate, external voltage). (ignores Vps for 4-terminal devices) Use these only if you specify UIC in the .TRAN statement. The .IC statement overrides it.

1. If you do not set TNODEOUT, you can specify 3 nodes for a device to float the body. Specifying 4 nodes implies that the 4th node is the external body contact node with a body resistance between the internal and external terminals. This configuration applies to a distributed body resistance simulation. If you set TNODEOUT, simulation interprets the last node as the temperature node. You can specify 4 nodes to float the device. Specifying 5 nodes implies body contact. 6 nodes is a body-contacted case with an accessible internal body node. You can use the temperature node to simulate thermal coupling.

Level 71 Model Parameters

The following tables describe the Level 71 Model Control, Process, DC, AC and Capacitance, Temperature, and A.4 Bias Control for Source Model parameters.

Table 196 Model Control Parameters

Parameter	Unit	Default	Description
MOBMOD	-	1	Mobility model selector
Noimod	-	1	Flag for the noise model

Chapter 6: MOSFET Models (BSIM): Levels 47 through 72

Level 71 TFT Model

Table 196 Model Control Parameters (Continued)

Parameter	Unit	Default	Description
SHMOD	-	0	Flag for self-heating: 0=no self-heating 1=self-heating
TFTMOD	-	0	Flag for the transistor operation mode: 0=partially depleted 1=dynamic depleted 2=partially depleted

Table 197 Process Parameters

Parameter	Unit	Default	Description
Parameter	Unit	Default	Description
DTOXCV			Difference between the electrical and physical gate oxide thicknesses, due to the effects of the gate poly depletion and the finite channel charge layer thickness.
Nch	1/cm ³	1e15	Channel doping concentration
Ngate	1/cm ³	0	Poly gate doping concentration
Nsub	1/cm ³	6.0e16	Substrate doping concentration
Tox	m	4.5e-8	Gate oxide thickness
Tsi	m	1.0e-8	Silicon film thickness

Table 198 DC Parameters

Parameter	Unit	Default	Description
a0	-	2.5	Bulk charge effect coefficient for the channel length

Table 198 DC Parameters (Continued)

Parameter	Unit	Default	Description
a1	1/V	0.68	First non-saturation effect parameter
a2	-	0.18	Second non-saturation effect parameter
aely	V/m	-0.1	Channel length dependency of the early voltage for the bipolar current
agidl	1/W	1e-7	GIDL constant
ags	1/V	0.15	Gate bias coefficient of Abulk
ahli	-	0.1	High-level injection parameter for the bipolar current
alpha0	m/V	1e-12	First parameter of the impact ionization current
b0	m	4.5e-8	Bulk charge effect coefficient for the channel width
b1	m	1e-7	Bulk charge effect width offset
beta0	1/V	40	First Vds dependence parameter of the impact ionization current
beta1	-	5	Second Vds dependence parameter of the impact ionization current
beta2	V	0	Third Vds dependence parameter of the impact ionization current
betag	-	3	Gate induced grain boundary barrier lowering coefficient
bgidl	V/m	9.5e9	GIDL exponential coefficient
cdsc	F/m ²	-1e-3	Drain/source to the channel coupling capacitance
cdscb	F/m ²	0	Body-bias sensitivity of cdsc
cdscd	F/m ²	1e-3	Drain-bias sensitivity of cdsc
cgidl	-	3.7e-2	Body voltage factor for gidl

Chapter 6: MOSFET Models (BSIM): Levels 47 through 72

Level 71 TFT Model

Table 198 DC Parameters (Continued)

Parameter	Unit	Default	Description
cit	F/m ²	0.0	Interface trap capacitance
delta	-	2.3	Effective Vds parameter
dgidl	-	2.5	Electric field exponent factor for gidl
drout	-	0.2	L dependence coefficient of the DIBL correction parameter in Rout
dsub	-	5	DIBL coefficient exponent
dvt0	-	0	First coefficient of the short-channel effect on Vth
dvt0w	-	0	First coefficient of the narrow width effect on Vth for a small channel length
dvt1	-	1	Second coefficient of the short-channel effect on Vth
dvt1w	-	5.3e6	Second coefficient of the narrow width effect on Vth for a small channel length
dvt2	1/V	-0.032	Body-bias coefficient of the short-channel effect on Vth
dvt2w	1/V	-0.032	Body-bias coefficient of the narrow width effect on Vth for a small channel length
dwb	m/V ^{1/2}	0.0	Coefficient of the substrate body bias dependence of Weff
dwbc	m	0.0	Width offset for the body contact isolation edge
dwg	m/V	2.3e-8	Coefficient of the gate dependence of Weff
esati	V/m	1.e7	Saturation channel electric field for the impact ionization current
eta0	-	0	DIBL coefficient in the subthreshold region
etab	1/V	-0.07	Body-bias coefficient for the DIBL effect in the subthreshold region

Table 198 DC Parameters (Continued)

Parameter	Unit	Default	Description
fbjtii	-	0.0	Fraction of the bipolar current affecting the impact ionization
ggidl	-	6e-1	Gate voltage coefficient for gidl
lsbjt	A/m ²	1.4e-7	BJT injection saturation current
lsdif	A/m ²	5e-5	Body to source/drain injection saturation current
lsrec	A/m ²	1.0e-5	Recombination in the depletion saturation current
lstun	A/m ²	0.0	Reverse tunneling saturation current
k1	V ^{1/2}	0.35	First-order body effect coefficient
k1w1	m	0	First-order effect width dependent parameter
k1w2	m	0	Second-order effect width dependent parameter
k2	-	-2e-2	Second-order body effect coefficient
k3	-	6e-4	Narrow coefficient
k3b	1/V	0	Body effect coefficient of k3
kb1	-	1	Backgate body charge coefficient
keta	1/V	-4.6e-2	Body-bias coefficient of the bulk charge effect
Ketas	V	0.0	Surface potential adjustment for the bulk charge effect
kg	-	1	Offset voltage for gate induced grain boundary barrier lowering
Lbjt0	m	1.3e-7	Reference channel length for the bipolar current
lii	-	2.8e-6	Channel length dependence parameter for the impact ionization current
lint	m	0.0	Length offset fitting parameter from I-V without bias

Chapter 6: MOSFET Models (BSIM): Levels 47 through 72

Level 71 TFT Model

Table 198 DC Parameters (Continued)

Parameter	Unit	Default	Description
lgb1	-	1e-2	Grain boundary factor inducing effective channel length decrease
lgb2	-	7e-4	Depletion near grain boundary inducing effective channel length decrease
lgb3	-	2e-2	Gate voltage factor for effective channel length
ln	m	1.8-6	Electron/hole diffusion length
nbjt	-	1.3	Power coefficient of the channel length dependency for the bipolar current
ndio	-	0.5	Diode non-ideality factor
nln	-	2	Channel length exponent for amplification coefficient of parasitic BJT
nfactor	-	20	Subthreshold swing factor
ngidl	V	-22	GIDL Vds enhancement coefficient
nlx	m	1.5e-6	Lateral non-uniform doping parameter
nrecf0	-	2.0	Recombination non-ideality factor at the forward bias
nrecr0	-	10	Recombination non-ideality factor at the reversed bias
ntun	-	10.0	Reverse tunneling non-ideality factor
pclm	-	9e-4	Channel length modulation parameter
PDIBLC1	-	1	Correction parameter for the DIBL effect of the first output resistance
pdiblc2	-	1.5e-3	Correction parameter for the DIBL effect of the second output resistance
prwb	1/V	-7.7e-7	0
prwg	1/V ^{1/2}	-1e-2	Gate-bias effect coefficient of R _{dsw}

Table 198 DC Parameters (Continued)

Parameter	Unit	Default	Description
pvag	-	5.6e2	Gate dependence of the Early voltage
rbody	ohm/m ²	0.0	Intrinsic body contact sheet resistance
rbsh	ohm/m ²	0.0	Extrinsic body contact sheet resistance
rdsw	ohm/m ²	7e4	Parasitic resistance per unit width
rsh	ohm/square	0.0	Source/drain sheet resistance in ohm per square
sii0	1/V	0.37	First V _{gs} dependence parameter for the impact ionization current
sii1	1/V	0.08	Second V _{gs} dependence parameter for the impact ionization current
sii2	1/V	0.08	Third V _{gs} dependence parameter for the impact ionization current
siid	1/V	5e-3	V _{ds} dependence parameter of the drain saturation voltage for the impact ionization current
tii	-	0	Temperature dependence parameter for the impact ionization current
u0	cm ² /(V-sec)	NMOS-600 PMOS-200	Mobility at Temp=T _{nom}
ua	m/V	9.6e-9	First-order mobility degradation coefficient
ub	(m/V) ²	1e-21	Second-order mobility degradation coefficient
uc	1/V	-4e-11	Body-effect of the mobility degradation coefficient
ug	m ² /(V-sec)	9e-2	Grain boundary barrier scattering mobility at Temp=T _{nom}
vabjt	V	10	Early voltage for the bipolar current
vdsatii0	V	0.6	Nominal drain saturation voltage at threshold for the impact ionization current

Chapter 6: MOSFET Models (BSIM): Levels 47 through 72

Level 71 TFT Model

Table 198 DC Parameters (Continued)

Parameter	Unit	Default	Description
VECB	v	0.026v	Electron tunneling from the conduction band
VEVB	v	0.075v	Electron tunneling from the valence band
voff	v	-0.6	Offset voltage in the subthreshold region for large W and L values
Vrec0	V	0.0	Voltage dependent parameter for the recombination current
vsat	m/sec	5e5	Saturation velocity at Temp=Tnom
vth0	v	NMOS 0.7 PMOS -0.7	Threshold voltage @ Vbs=0 for a long, wide device
Vtun0	V	0.0	Voltage dependent parameter for the tunneling current
w0	m	2.5e-5	Narrow width parameter
wint	m	0.0	Width offset fitting parameter from I-V without bias
wr	-	0.8	Width offset from Weff for the Rds calculation

Table 199 AC and Capacitance Parameters

Parameter	Unit	Default	Description
acde	m/V	1.0	Exponential coefficient for the charge thickness in the CapMod=3 for the accumulation and depletion regions
asd	V	0.3	Smoothing parameter for the source/drain bottom diffusion
cf	F/m	cal.	Fringing field capacitance of the gate-to-source/drain
cgdl	F/m	0.0	Overlap capacitance for the lightly-doped drain-gate region
cgdo	F/m	0	Non LDD region drain-gate overlap capacitance per channel length
CGEO	F/m 0	Gate	Substrate overlap capacitance per unit channel length
cgsi	F/m	0.0	Overlap capacitance for the lightly-doped source-gate region

Table 199 AC and Capacitance Parameters (Continued)

Parameter	Unit	Default	Description
cgso	F/m	cal.	Calculated Non LDD region source-gate overlap capacitance per channel length
cjswg	F/m ²	1.e-10	Source/drain (gate side) sidewall junction capacitance per unit width (normalized to 100nm Tsi)
ckappa	F/m	0.6	Coefficient for the fringing field capacitance for the overlap capacitance in the lightly-doped region
clc	m	0.1e-7	Constant term for the short-channel model
cle	-	0.0	Exponential term for the short-channel model
csdesw	F/m	0.0	Fringing capacitance per unit length for the source/drain sidewall
csdmin	V	cal.	Minimum capacitance for the source/drain bottom diffusion
delvt	V	0.0	Threshold voltage adjustment for C-V
dlbg	m	0	Length offset fitting parameter for the backgate charge
dlc	m	lint	Length offset fitting parameter for the gate charge
dlcb	m	lint	Length offset fitting parameter for the body charge
dwc	m	wint	Width offset fitting parameter from C-V
fbody	-	1.0	Scaling factor for the body charge
Ldif0	-	1	Channel length dependency coefficient of the diffusion cap.
mjswg	V	0.5	Grading coefficient of the source/drain (gate side) sidewall junction capacitance
moin	V ^{1/2}	15.0	Coefficient for the gate-bias dependent surface potential
Ndif	-	-1	Power coefficient of the channel length dependency for the diffusion capacitance
pbswg	V	0.7	Built-in potential of the source/drain (gate side) sidewall junction capacitance

Chapter 6: MOSFET Models (BSIM): Levels 47 through 72

Level 71 TFT Model

Table 199 AC and Capacitance Parameters (Continued)

Parameter	Unit	Default	Description
tt	second	1ps	Diffusion capacitance transit time coefficient
vsdfb	V	cal.	Flatband voltage for the source/drain bottom diffusion capacitance
vsdth	V	cal.	Threshold voltage for the source/drain bottom diffusion capacitance
xpart	-	0	Charge partitioning rate flag

Table 200 Temperature Parameters

Parameter	Unit	Default	Description
at	m/sec	3.3e4	Temperature coefficient for Ua
cth0	m° C/(W*s)	0	Normalized thermal capacity
kt1	V	-0.11	Temperature coefficient for the threshold voltage
kt2	-	0.022	Body-bias coefficient of the threshold voltage temperature effect
ktil	V*m	0	Channel length dependence of the temperature coefficient for the threshold voltage
Ntrecf	-	0	Temperature coefficient for Ntrecf
Ntreocr	-	0	Temperature coefficient for Ntreocr
prt	$\Omega-\mu m$	0	Temperature coefficient for Rdsw
rth0	m° C/W	0	Normalized thermal resistance
tcjswg	1/K	0	Temperature coefficient of Cjswg
tnom	° C	25	Temperature at which simulation expects parameters
tpbswg	V/K	0	Temperature coefficient of Pbswg

Table 200 Temperature Parameters (Continued)

Parameter	Unit	Default	Description
ua1	m/V	4.31e-9	Temperature coefficient for Ua
ub1	(m/V) ²	-7.61e-18	Temperature coefficient for Ub
uc1	1/V	-0.056	Temperature coefficient for Uc
ute	-	-1.5	Mobility temperature exponent
xbjt	-	1	Power dependence of jbjt on the temperature
xdif	-	Same as XBJT	Power dependence of jdif on the temperature
xrec	-	1	Power dependence of jrec on the temperature
xtun	-	0	Power dependence of jtun on the temperature

Table 201 A.4 Parameters for Bias-Dependent Source (Rs)/Drain(Rd) Models

Parameter	Unit	Default	Description
rsw	ohm(um) ^{wr}	100.0	Zero bias lightly-doped source resistance Rs(V) per unit width for RSMOD=1
rswmin	ohm(um) ^{wr}	0.0	Lightly-doped source resistance per unit width at high Vgs and zero Vbs for RSMOD=1
prwbs	V ^{-0.5}	0.0	Body-bias dependence of LDD resistance in source side
prwgs	V ⁻¹	1.0	Gate-bias dependence of LDD resistance in source side
prwss	V ⁻¹	1.0	External source-bias and gate-bias dependence of LDD resistance in source side
ersg1	-	1.0	Gate-bias dependent parameter in PRWGS
ersg2	-	1.0	Gate-bias dependent parameter in PRWSS
erss	-	1.0	External source voltage dependent parameter in PRWSS

Chapter 6: MOSFET Models (BSIM): Levels 47 through 72

Level 71 TFT Model

Table 201 A.4 Parameters for Bias-Dependent Source (Rs)/Drain(Rd) Models

Parameter	Unit	Default	Description
crs		1.0	Coefficient of Rs due to gate and external source bias
rdw	ohm(um)^wr	100.0	Zero bias lightly-doped drain resistance Rd(V) per unit width for RDMOD=1
rdwmin	ohm(um)^wr	0.0	Lightly-doped drain resistance per unit width at high Vgs and zero Vbs for RDMOD=1
prwdb	Same as prwbs		Body-bias dependence of LDD resistance in drain side
prwgd	Same as prwgs		Gate-bias dependence of LDD resistance in drain side
prwdd	Same as prwss		External drain-bias and gate-bias dependence of LDD resistance in drain side
erdg1	Same as ersg1		Gate-bias dependent parameter in PRWGD
erdg2	Same as ersg2		Gate-bias dependent parameter in PRWDD
erdd	Same as erss		External drain voltage dependent parameter in PRWDD
crd	Same as crs		Coefficient of Rd due to gate and external drain bias
rswmin0	Ohm	0.0	Source resistance constant component
rdwmin0	Ohm	0.0	Drain resistance constant component
wr	-	0.0	Width dependence exponent of lightly-doped source and drain resistance
deltavgs	-	1.0e-4	Smoothing parameter for RS dependence on VGS
deltavgd	Same as deltavgs		Smoothing parameter for RD dependence on VGD

Level 72 BSIM-CMG MOSFET Model

The BSIM-CMG model (HSPICE Level 72) is a compact model to describe the behavior of multiple-gate MOSFET devices. There are two sub-modules for this HSPICE built-in model:

- 3-terminal SOIMG module for the BSIM-CMG SOI model
- 4-terminal BULKMG module for the BSIM-CMG BULK model

All important multi-gate transistor behaviors are captured by this model. Volume inversion is included in the solution of Poisson's equation; hence the subsequent I-V formulation automatically captures the volume inversion effect. Analysis of the electrostatic potential in the body of MG MOSFETs provides the model equation for short channel effects (SCE). The extra electrostatic control from the top gate (tri-gate) or top/bottom gates (omega-gate or all-around-gate) is also captured in the short channel model. The SCE model predicts the threshold (V_t) roll-off, drain-induced-barrier lowering (DIBL) and subthreshold slope degradation in close agreement with 2-D device simulation results.

Included in the model are other important effects such as: mobility degradation, multiple surface-orientations, velocity saturation, velocity overshoot, series resistance, channel length modulation, quantum mechanical effects, poly depletion, gate tunneling current, gate-induced-drain-leakage, and parasitic capacitance models.

See also: [Output Templates for BSIMMG \(BSIM-CMG\) Level 72 on page 45](#).

The following sections discuss these topics:

- [BSIM-CMG 104 Updates](#)
- [BSIM-CMG 103 Updates](#)
- [General Syntax for BSIM-CMG Model](#)
- [Deactivating Equations in BSIM-CMG](#)
- [BSIM-CMG Complete Parameter Lists](#)

BSIM-CMG 104 Updates

BSIM-CMG 104.1

The following BSIM-CMG 104.1 updates became available for HSPICE with the HSPICE E-2010.12 release:

1. Asymmetric DIBL parameters supported.
2. Bulk-Charge is made bias independent through correct implementation.
3. CLMMOD=1 case replaced with newer model.
4. Many bug fixes were implemented.

BSIM-CMG 104.0

The following BSIM-CMG 104 updates became available for HSPICE with the HSPICE D-2010.03-SP1 release:

1. Channel length modulation model CLMMOD=1 is added based on the BSIM4 formulation.
2. Instance parameters NRS and NRD and associated equations are added based on the BSIM4 formulation.
3. The equations associated with parameter PVAG are modified to provide more flexibility for output conductance fitting.
4. Added a New Impact Ionization Current Model and Model Switch IIMOD; BSIM4 based Iii model into IIMOD=1 block and BSIMSOI based Iii model into IIMOD=2 block.
5. Improved the Gate Electrode Resistance Model; introduced new parameters RGEXT and RGFIN and removed parameter RGELTD.
6. Changed the Internal Resistance formula.
7. Implemented many bug fixes.

BSIM-CMG 103 Updates

The following BSIM-CMG 103 updates became available for HSPICE with the HSPICE D-2010.03 release:

1. This release supports a Cylindrical gate geometry through GEOMOD = 3 with an associated short channel scale length and quantum effects model.
2. The existing I-V has been enhanced to model Poly-depletion accurately.

3. Self-heating is now supported with addition of a Temperature node.
4. Junction Capacitance and Junction Current equations were revamped with source-drain asymmetry supported. The asymmetry is now also in GIDL/GISL currents.
5. Length-dependent equations have been added for a Global Parameter Extraction without binning.
6. SHMOD, RGATEMOD, NQSMOD and RDSMOD also control the number of internal nodes for faster simulations.
7. Many bug fixes were implemented.

General Syntax for BSIM-CMG Model

The general syntax for including a BSIM-CMG model element in a netlist is:

```
Mxxx nd ng ns [nb] mname [L=val] [M=val]  
.model mname n(p)mos LEVEL=72 VERSION=val ...
```

Level 72 is the BSIM-CMG model in HSPICE. Before BSIMCMG102, the model parameter TECHMOD=0 (default) was used for the BSIM-CMG BULK model and TECHMOD=1 for the BSIM-CMG SOI model. With BSIMCMG102, and going forward, use model parameter BULKMOD=1 (default) for the BSIM-CMG BULK model and BULKMOD=0 for the BSIM-CMG SOI model.

For example, to use the BSIM-CMG model in HSPICE, specify:

```
M1 drain gate source NCH L=1u
```

For the BSIM-CMG BULK model, specify NCH as:

```
.MODEL NCH NMOS LEVEL=72 VERSION=1.01 TECHMOD=0  
.MODEL NCH NMOS LEVEL=72 VERSION=102 BULKMOD=1
```

For the BSIM-CMG SOI model, specify NCH as:

```
.MODEL NCH NMOS LEVEL=72 VERSION=1.01 TECHMOD=1  
.MODEL NCH NMOS LEVEL=72 VERSION=102 BULKMOD=0
```

Deactivating Equations in BSIM-CMG

The following settings for parameters turn off equations in BSIM-CMG:

Table 202 BSIM-CMG Parameter Settings to Turn Off Equations

Parameter	Description
CDSC=0 CDSCD=0 CIT=0	Subthreshold slope degradation
ETA0=0	Drain induced barrier lowering
DVT0=0	Vt roll-off (at low drain bias)
K1RSCE=0	Reverse short channel effect
QMFACTOR=0	Quantum effect
MUE=0 THETAMU=1 (to prevent 0 to the 0'th power) CS=0	Mobility degradation due to vertical field & coulomb scattering
RDSWMIN=0	Source drain resistance
RDSW=0	
KSATIV=1000	Drain saturation voltage and velocity overshoot
VSAT=1e9	
LAMBDA=0	
NGATE=0	Polysilicon Depletion
ALP=0	Channel Length Modulation
ALP1=0	
ALP2=0	

Table 202 BSIM-CMG Parameter Settings to Turn Off Equations (Continued)

Parameter	Description
THETASAT=0	Effect of velocity saturation in the linear region
PDIBL1=0	Output conductance due to DIBL
PDIBL2=0	
LOV=0	Parasitic Capacitance
CF=0	
ALPHA0=0	Impact Ionization
ALPHA1=0	
IGMOD=0	Gate Current
GIDLMOD=0	GIDL Current

BSIM-CMG Complete Parameter Lists

The following tables list all the parameters used for BSIM-CMG model including:

- [BSIM-CMG Instance Parameters](#)
- [Model Controllers and Process Parameters on page 635](#)
- [Basic Model Parameters on page 637](#)
- [Parameters for Temperature Dependence and Self-Heating on page 646](#)

BSIM-CMG Instance Parameters

Note: Binnable parameters are marked as ^(b). Instance parameters which are also model parameters are marked as ^(m).

Table 203 BSIM-CMG Instance Parameters

Parameter	Unit	Default	Description
VERSION		104.1	Latest supported version

Chapter 6: MOSFET Models (BSIM): Levels 47 through 72
Level 72 BSIM-CMG MOSFET Model

Table 203 BSIM-CMG Instance Parameters (Continued)

Parameter	Unit	Default	Description
$L^{(m)}$	m	30e-9	Channel length
NF	-	1	Number of fingers
$NFIN^{(m)}$	-	10	Number of fins per finger
$TFIN^{(m)}$	m	15e-9	Fin (channel) thickness; currently supports $TFIN < 50 \times 10^{-9} \text{m}$; for larger values use BSIM4 or BSIM4SOI.
$D^{(m)}$	m	40e-9	Diameter of cylinder
$AS^{(m)}$	m^2	0	Source area
$AD^{(m)}$	m^2	0	Drain area
$PS1^{(m)}$	m	0	1st part of the source perimeter
$PD1^{(m)}$	m	0	1st part of the drain perimeter
$PS2^{(m)}$	m	0	2nd part of the source perimeter
$PD2^{(m)}$	m	0	2nd part of the drain perimeter
$CGSP^{(m)}$	F	0	Constant gate to source fringe capacitance
$CGDP^{(m)}$	F	0	Constant gate to drain fringe capacitance
$CDSP^{(m)}$	F	0	Constant drain to source fringe capacitance
NRS	-	0	Number of source diuiffion squares
NRD	-	0	Number of drain diuiffion squares

Model Controllers and Process Parameters

Table 204 BSIM-CMG Model Controllers and Process Parameters

Parameter	Unit	Default	Description
BULKMOD	-	1	BULK/SOI model selector (Version102 and later) In Verilog-A the number of terminals cannot be controlled by a model parameter. If you are running the Verilog-A version of this model, select the bulk or SOI module by running bulkmg.va or soimg.va
IGMOD	-	0	Gate current switch; 1=on, 0=off
GIDLMOD	-	0	GIDL/GISL current switch; 1=on, 0=off
RGATEMOD	-	0	Gate electrode resistor switcher; 1=on, 0=off
NQSMOD	-	0	NQS gate resistor switch; 1=on, 0=off
SHMOD	-	0	Self-heating switch; 1=on, 0=off
COREMOD	-	0	Simplified surface potential solution; 0=off, 1= on (lightly-doped or undoped)
GEOMOD	-	1	Structure selector; 0=double gate, 1=triple gate, 2=quadruple gate, 3=cylindrical gate
RDSMOD	-	0	Source/drain resistance selector; 0 = internal, 1 =external
MOBMOD	-	0	Mobility model selector 0 = BSIM-based, 1 = PSP-based
CGEOMOD	-	0	Geometry-dependent parasitic capacitance model selector; 1=on, 0=off
CLMMOD	-	0	Model selector for channel length modulation
IIMOD	-	0	Impact ionization model switch; 0 = OFF, 1 =BSIM4 based, 2 = BSIMSOI based
DEVTYPE		NMOS	NMOS=1, PMOS=0
XL	m	-5e-9	L offset for channel length due to mask/etch e effect
LINT	m	0.0	Channel length reduction parameter

Chapter 6: MOSFET Models (BSIM): Levels 47 through 72

Level 72 BSIM-CMG MOSFET Model

Table 204 BSIM-CMG Model Controllers and Process Parameters

Parameter	Unit	Default	Description
LL	$m^{(LLN+1)}$	0.0	Channel length reduction parameter
LLN	-	1.0	Channel length reduction parameter
LLC	$m^{(LLN+1)}$	0.0	Channel length reduction parameter for CV
DLC	m	0.0	Channel length reduction parameter for CV
EOT	m	0.9e-9	Effective gate dielectric thickness relative to SiO ₂
HFIN	m	35e-9	Fin height; instance parameter, also
FECH	-	1.0	End-channel factor, for different orientation/shape; this parameter handles the mobility difference between the side channel and the top channel
DELTA W	m	0.0	Reduction of effective width due to shape of fin
FECHCV	-	1.0	CV end-channel factor, for different orientation/shape
DELTA WCV	m	0.0	CV reduction of effective width due to shape of fin
NBODY ^(b)	m^{-3}	1e22	Channel doping concentration; model currently supports $NBODY < 5 \times 10^{24} m^{-3}$; for larger values use BSIM4 or BSIM4SOI
PHIG ^(b)	eV	4.61	Work function of gate
EPSROX	-	3.9	Relative dielectric constant of the gate insulator
EPSRSUB	-	11.9	Relative dielectric constant of the channel material
EASUB	eV	4.05	Electron affinity of the substrate material
NIOSUB	m^{-3}	1.1e16	Intrinsic carrier concentration of channel at 300.15K
BG0SUB	eV	1.12	Band gap of the channel material at 300.15K
NC0SUB	m^{-3}	2.86e25	Conduction band density of states at 300.15K

Table 204 BSIM-CMG Model Controllers and Process Parameters

Parameter	Unit	Default	Description
NGATE ^(b)	m ⁻³	0	Parameter for Poly Gate doping; =0 for metal gate

Basic Model Parameters

Table 205 BSIM-CMG Basic Model Parameters

Name	Unit	Default	Min	Max	Description
NSD ^(b)	m ⁻³	2e26	-	-	S/D doping concentration
CIT ^(b)	F/m ²	0	-	-	Parameter for interface trap
CDSC ^(b)	F/m ²	7e-3	0.0	-	Coupling capacitance between S/D and channel
CDSCD ^(b)	F/m ²	7e-3	0.0	-	Drain-bias sensitivity of CDSC
CDSCDR ^(b)	F/m ²	CDSCD	0.0	-	Reverse mode drain-bias sensitivity of CDSC
DVT0 ^(b)	-	0.0	0.0	-	SCE coefficient
DVT1 ^(b)	-	0.60	>0	-	SCE exponent coefficient
PHIN ^(b)	V	0.05	-	-	Nonuniform vertical doping effect on surface potential
ETA0 ^(b)	-	0.60	0.0	-	DIBL coefficient
ETA0R ^(b)	-	ETA0	0.0	-	Reverse mode DIBL coefficient
DSUB ^(b)	-	1.06	>0	-	DIBL exponent coefficient
K1RSCE ^(b)	V ^{1/2}	0.0	-	-	Prefactor for reverse short channel effect
LPE0 ^(b)	m	5e-9	-Leff	-	Equivalent length of pocket region zero bias
QMFACTOR ^(b)	-	0.0	-	-	Prefactor for QM correction

Chapter 6: MOSFET Models (BSIM): Levels 47 through 72
Level 72 BSIM-CMG MOSFET Model

Table 205 BSIM-CMG Basic Model Parameters (Continued)

Name	Unit	Default	Min	Max	Description
VSAT ^(b)	m/s	85000	-	-	Saturation velocity
KSATIV ^(b)	-	1.3	-	-	Parameter for reverse short channel effect
MEXP ^(b)	-	4	2	-	Smoothing function factor for Vdsat
PTWG ^(b)	v^{-2}	0.0	-	-	Correction factor for velocity saturation
THETASAT ^(b)	v^{-1}	2.0	-	-	Velocity saturation parameter
U0 ^(b)	$m^2/V\cdot s$	6e-2	-	-	Low field mobility
ETAMOB ^(b)	-	2.0	-	-	Effective field parameter
UP ^(b)	μm^{LPA}	0.0	-	-	Mobility L coefficient
LPA	-	1.0	-	-	Mobility L power coefficient
UA ^(b)	$(cm/MV)^{EU}$	0.3	>0.0	-	MOBMOD = 0 phonon / surface roughness scattering
EU ^(b)	cm/MV	2.5	>0.0	-	MOBMOD = 0 phonon / surface roughness scattering
UD ^(b)	cm/MV	0.0	>0.0	-	MOBMOD = 0 Coulombic scattering (Experimental)
UCS ^(b)	-	1.0	>0.0	-	MOBMOD = 0 Coulombic scattering (Experimental)
MUE ^(b)	cm/MV	1.2	>0.0	-	MOBMOD=1 Mobility reduction coefficient
THETAMU	-	1.0	>0.0	-	MOBMOD = 1 mobility reduction exponent
CS ^(b)	-	0.0	>0.0	-	Coulombic scattering parameter

Table 205 BSIM-CMG Basic Model Parameters (Continued)

Name	Unit	Default	Min	Max	Description
ALP ^(b)	-	0.013	-	-	CLMMOD = 0 Channel Length Modulation (CLM) prefactor
VP	V	0.0	-	-	CLMMOD = 0 CLM log dependence parameter
PCLM ^(b)	-	0.013	-	-	CLMMOD = 1 Channel Length Modulation parameter
PCLMG	-	0	-	-	CLMMOD = 1 Gate bias dependent parameter for channel Length Modulation (CLM)
VASAT	V	0.2	-	-	CLMMOD = 1 Channel Length Modulation (CLM) parameter
RDSWMIN	$\Omega - \mu_m^{WR}$	0.0	-	-	RDSMOD = 0 S/D extension resistance per unit width at high V_{gs}
RDSW ^(b)	$\Omega - \mu_m^{WR}$	40	0.0	-	RDSMOD = 0 zero bias S/D extension resistance per unit width
RSWMIN	$\Omega - \mu_m^{WR}$	0.0	0.0	-	RDSMOD = 1 source extension resistance per unit width at high V_{gs}
RSW ^(b)	$\Omega - \mu_m^{WR}$	50	0.0	-	RDSMOD = 1 zero bias source extension resistance per unit width
RDWMIN	$\Omega - \mu_m^{WR}$	0.0	0.0	-	RDSMOD = 1 drain extension resistance per unit width at high V_{gs}
RDW ^(b)	$\Omega - \mu_m^{WR}$	50	0.0	-	RDSMOD = 1 zero bias drain extension resistance per unit width

Chapter 6: MOSFET Models (BSIM): Levels 47 through 72
Level 72 BSIM-CMG MOSFET Model

Table 205 BSIM-CMG Basic Model Parameters (Continued)

Name	Unit	Default	Min	Max	Description
PRWG ^(b)	V ⁻¹	0.0	0.0	-	Gate bias dependence of S/D extension resistance
WR ^(b)	-	1.0	-	-	W dependence parameter of S/D extension resistance
RGEXT	Ω	0.0	0.0	-	Effective gate electrode external resistance (Experimental)
RGFIN	Ω	1.0e-3	1.0e-3	-	Effective gate electrode resistance per n per finger
RSHS	Ω	0.0	0.0	-	Source-side sheet resistance
RSHD	Ω	RSHS	0.0	-	Drain-side sheet resistance
PDIBL1	-	1.30	0.0	-	Parameter for DIBL effect on Rout
PDIBL2		2e-4	0.0	-	Parameter for DIBL effect on Rout
DROUT		1.06	>0.0	-	0.56
PVAG ^(b)	-	1.0	-	-	Vgs dependence on early voltage
AIGBINV ^(b)	$(Fs^2/g)^{0.5} m^{-1}$	1.11e-2	-	-	Parameter for Igb in inversion
BIGBINV ^(b)	$(Fs^2/g)^{0.5} m^{-1} V^{-1}$	9.49e-4	-	-	Parameter for Igb in inversion (BULKMOD only)
CIGBINV ^(b)	V ⁻¹	6.00e-3	-	-	Parameter for Igb in inversion (BULKMOD only)
EIGBINV ^(b)	V	1.1	-	-	Parameter for Igb in inversion (BULKMOD only)
NIGBINV ^(b)	-	3.0	> 0.0	-	Parameter for Igb in inversion (BULKMOD only)

Table 205 BSIM-CMG Basic Model Parameters (Continued)

Name	Unit	Default	Min	Max	Description
AIGC ^(b)	$(Fs^2/g)^{0.5}m^{-1}$	1.36e-2	-	-	Parameter for Igc in inversion
BIGC ^(b)	$(Fs^2/g)^{0.5}m^{-1}V^{-1}$	1.71e-3	-	-	Parameter for Igc in inversion
CIGC ^(b)	V ⁻¹	0.075	-	-	Parameter for Igc in inversion
NIGC ^(b)	-	1	>0	-	Parameter for Igc in inversion
DLCIGS	m	0	-	-	Delta L for Igs model
AIGS ^(b)	$(Fs^2/g)^{0.5}m^{-1}$	1.36e2	-	-	Parameter for Igs in inversion
BIGS ^(b)	$(Fs^2/g)^{0.5}m^{-1}V^{-1}$	1.71e-3	-	-	Parameter for Igs in inversion
CIGS ^(b)	V ⁻¹	0.075	-	-	Parameter for Igs in inversion
DLCIGD	m	DLCIGS	-	-	Delta L for Igd model
AIGD ^(b)	$(Fs^2/g)^{0.5}m^{-1}$	1.36e2	-	-	Parameter for Igd in inversion
BIGD ^(b)	$(Fs^2/g)^{0.5}m^{-1}V^{-1}$	1.71e-3	-	-	Parameter for Igd in inversion
CIGD ^(b)	V ⁻¹	0.075	-	-	Parameter for Igd in inversion
POXEDGE ^(b)	-	1	>0	-	Factor for the gate edge Tox
AGIDL ^(b)	Ω^{-1}	6.055	-	-	Pre-exponential coefficient for GIDL
BGIDL ^(b)	V/m	0.3e9	-	-	Exponential coefficient for GIDL
EGIDL ^(b)	V	0.2			Band bending parameter for GIDL
AGISL ^(b)	Ω^{-1}	AIGDL	-	-	Pre-exponential coefficient for GISL

Table 205 BSIM-CMG Basic Model Parameters (Continued)

Name	Unit	Default	Min	Max	Description
BGSL(b)	V/m	BIGDL			Band bending parameter for GISL
EGSL(b)	V	EGIDL	-	-	Pre-exponential coefficient for GISL
ALPHA0 ^(b)	$m \cdot V^{-1}$	0.0	-	-	First parameter of lii
ALPHA1 ^(b)	V^{-1}	0.0	-	-	L scaling parameter of lii
BETA0 ^(b)	V^{-1}	0.0	-	-	Vds dependent parameter of lii
ALPHAII ^(b)	-	0.0	-	-	Pre-exponential constant for lii (IIMOD=2)
BETAII0 ^(b)	V^{-1}	0.0	-	-	Vds dependent parameter of lii (IIMOD=2)
BETAII1 ^(b)	-	0.0	-	-	Vds dependent parameter of lii (IIMOD=2)
BETAII2 ^(b)	V	0.0	-	-	Vds dependent parameter of lii (IIMOD=2)
ESATII ^(b)	V/m	1.0e7	-	-	Saturation channel E-Field for lii (IIMOD=2)
LII ^(b)	V -m	0.5e-9	-	-	Channel length dependent parameter of lii (IIMOD=2)
SII0 ^(b)	V^{-1}	0.0	-	-	Vgs dependent parameter of lii (IIMOD=2)
SII1 ^(b)	-	0.0	-	-	Vgs dependent parameter of lii (IIMOD=2)
SII2 ^(b)	V	0.0	-	-	Vgs dependent parameter of lii (IIMOD=2)
SIID ^(b)	V	0.0	-	-	Vds dependent parameter of lii (IIMOD=2)

Table 205 BSIM-CMG Basic Model Parameters (Continued)

Name	Unit	Default	Min	Max	Description
LOVS ^(b)	m	1.0e-9	0.0	-	Gate-to-source overlap length (for parasitic capacitance calculation)
LOVD ^(b)	m	LOVS	0.0	-	Gate-to-drain overlap length (for parasitic capacitance calculation)
CFS ^(b)	F/m	2.5e-11	0.0	-	Source-side outer fringe cap (for parasitic capacitance calculation)
CFD ^(b)	F/m	CFS	0.0	-	Drain-side outer fringe cap (for parasitic capacitance calculation)
COVS ^(b)	F	0	0.0	-	Constant gate-to-source overlap cap (for parasitic capacitance calculation)
COVD ^(b)	F	COVS	0.0	-	Constant gate-to-drain overlap cap (for parasitic capacitance calculation)
CJS	F/m ²	0.003	0.0	-	Unit area source-side junction capacitance at zero bias
CJD	F/m ²	CJS	0.0	-	Unit area drain-side junction capacitance at zero bias
CJSWS1	F/m	3.0e-10	0.0	-	1st unit length source-side sidewall junction capacitance at zero bias
CJSWD1	F/m	CJSWS1	0.0	-	1st unit length drain-side sidewall junction capacitance at zero bias
CJSWS2	F/m	3.0e-10	0.0	-	2nd unit length source-side sidewall junction capacitance at zero bias

Table 205 BSIM-CMG Basic Model Parameters (Continued)

Name	Unit	Default	Min	Max	Description
CJSWD2	F/m	CJSWS1	0.0	-	2nd unit length drain-side sidewall junction capacitance at zero bias
PBS	V	1.0	0.01	-	Unit area source-side junction capacitance at zero bias
PBD	V	PBS	0.01	-	Unit area drain-side junction capacitance at zero bias
PBSWS1	V	1.0	0.01	-	Built-in potential for 1st source-side sidewall junction capacitance
PBSWD1	V	PBSWS1	0.0	-	Built-in potential for 1st drain-side sidewall junction capacitance
PBSWS2	V	PBSWS1	0.01	-	Built-in potential for 2nd source-side sidewall junction capacitance
PBSWD2	V	PBSWS2	0.01	-	Built-in potential for 2nd drain-side sidewall junction capacitance
MJS	-	0.5	-	-	Source bottom junction capacitance grading coefficient
MJD	-	MJS	-	-	Drain bottom junction capacitance grading coefficient
MJSWS1	-	0.33			1st source sidewall junction capacitance grading coefficient
MJSWD1	-	MJSWS1	-	-	2nd drain sidewall junction capacitance grading coefficient
MJSWS2	-	MJSWS1	-	-	2nd source sidewall junction capacitance grading coefficient

Table 205 BSIM-CMG Basic Model Parameters (Continued)

Name	Unit	Default	Min	Max	Description
MJSWD2	-	MJSWS2	-	-	2nd drain sidewall junction capacitance grading coefficient
JSS	A/m ²	1.0e-4	0.0	-	Bottom source junction reverse saturation current density
JSD	A/m ²	JSS	0.0	-	Bottom drain junction reverse saturation current density
JSWS1	A/m	0	0.0	0.0	Unit length reverse saturation current for 1st sidewall source junction
JSWD1	A/m	JSWS1	0.0	0.0	Unit length reverse saturation current for 1st sidewall drain junction
JSWS2	A/m	JSWS1	0.0	0.0	Unit length reverse saturation current for 2nd sidewall source junction
JSWD2	A/m	JSWS2	0.0	0.0	Unit length reverse saturation current for 2nd sidewall drain junction
NJS	-	1.0	0.0	-	Source junction emission coefficient
NJD	-	NJS	0.0	-	Drain junction emission coefficient
IJTHSFWD	A	0.1	10 I _{sbs}	-	Forward source diode breakdown limiting current
IJTHDFWD	A	IJTHSFWD	10 I _{sbs}	-	Forward drain diode breakdown limiting current
IJTHSREV	A	0.1	10 I _{sbs}	-	Reverse source diode breakdown limiting current
IJTHDREV	A	IJTHSREV			Reverse drain diode breakdown limiting current

Table 205 BSIM-CMG Basic Model Parameters (Continued)

Name	Unit	Default	Min	Max	Description
BVS	V	10.0			Source diode breakdown voltage
BVD	V	BVS			Drain diode breakdown voltage

Parameters for Temperature Dependence and Self-Heating

Table 206 BSIM-CMG Temperature Dependent and Self-Heating Parameters

Name	Unit	Default	Min	Max	Description
TNOM	$^{\circ}K$	300.15	0.9	-	Temperature at which the model is extracted
TBGASUB	$(eV)/(^{\circ}K)$	7.02e-4	-	-	Bandgap temperature coefficient
TBGBSUB	$^{\circ}K$	1108.0	-	-	Bandgap temperature coefficient
KT1	V	-0.3	-	-	V_{th} temperature coefficient
KT1L	V · m	0.0	-	-	V_{th} temperature coefficient
UTE ^(b)	-	-1.4	-	-	Mobility temperature coefficient
UA1 ^(b)	-	-1.1	-	-	Mobility (MOBMOD=0) temperature coefficient
UD1 ^(b)	-	0.0	-	-	Mobility (MOBMOD=0) temperature coefficient (Experimental)
UCSTE ^(b)	-	-4.775e-3	-	-	Mobility (MOBMOD=0) temperature coefficient (Experimental)
STTHETAMU	-	1.5	-	-	Mobility (MOBMOD=0) temperature coefficient
STMUE	-	0.0	-	-	Mobility (MOBMOD=1) temperature coefficient
STCS	-	0.0	-	-	Mobility (MOBMOD=1) temperature coefficient

Table 206 BSIM-CMG Temperature Dependent and Self-Heating Parameters

Name	Unit	Default	Min	Max	Description
AT ^(b)	1/ (°K)	0.005	-	-	Saturation velocity temperature coefficient
TMEXP ^(b)	1/ (°K)	0	-	-	Temperature coefficient for V_{dseff} smoothing
PTWGT ^(b)	1/ (°K)	0.004	-	-	PTWG temperature coefficient
STTHETASAT	-	1.0	-	-	Saturation velocity temperature coefficient
PRT ^(b)	-	0.001	-	-	Series resistance temperature coefficient
IIT ^(b)	-	-0.5	-	-	Impact ionization temperature coefficient(IIMOD=1)
TI ^(b)	-	0.0	-	-	Impact ionization temperature coefficient(IIMOD=2)
TGIDL ^(b)	1/ (°K)	-0.003	-	-	GISL/GIDL temperature coefficient
IGT ^(b)	-	2.5	-	-	Gate current temperature coefficient
TCJ	1/ (°K)	0.0	-	-	Temperature coefficient for cjs/cjd
TCJSW1	1/ (°K)	0.0	-	-	Temperature coefficient for cjsws1/cjdwd1
TCJSW2	1/ (°K)	0.0	-	-	Temperature coefficient for cjsws2/cjdwd2
TPB	1/ (°K)	0.0	-	-	Temperature coefficient for pbs/pbd
TPBSW1	1/ (°K)	0.0	-	-	Temperature coefficient for pbsws1/pbdwd1
TPBSW2	1/ (°K)	0.0	-	-	Temperature coefficient for pbsws2/pbdwd2

Chapter 6: MOSFET Models (BSIM): Levels 47 through 72

Supported Instance Parameters, BSIM3, BSIM4, BSIM3SOI and BSIM4SOI

Table 206 BSIM-CMG Temperature Dependent and Self-Heating Parameters

Name	Unit	Default	Min	Max	Description
XTIS	-	3.0	-	-	Drain junction current temperature exponent
XTID	-	XTIS	-	-	Source junction current temperature exponent
RTH0	Ω	0.01	0.0	-	Thermal resistance for self-heating calculation
CTH0	F	1.0e-5	0.0	-	Thermal capacitance for self-heating calculation
WTH0	m	0.0	0.0	-	Width-dependence coefficient for self-heating calculation

Supported Instance Parameters, BSIM3, BSIM4, BSIM3SOI and BSIM4SOI

The following lists the instance parameters that are currently supported by HSPICE in these four model types:

Table 207 Instance parameters: BSIM3, BSIM4, BSIM3SOI, BSIM4SOI

Instance Parameter	BSIM3	BSIM4	BSIM3SOI	BSIM4SOI
ACNQSMOD	yes	yes	no	no
AD	yes	yes	yes	yes
AS	yes	yes	yes	yes
CTH0	yes	no	yes	yes
DELDVT0	no	yes	no	no
DELK1	yes	yes	no	yes
DELK2	no	yes	yes	no
DELNFCT	yes	yes	no	yes
DELLPE0	no	yes	no	no
DELRSH	no	yes	no	no

Supported Instance Parameters, BSIM3, BSIM4, BSIM3SOI and BSIM4SOI

Table 207 Instance parameters: BSIM3,BSIM4, BSIM3SOI, BSIM4SOI

Instance Parameter	BSIM3	BSIM4	BSIM3SOI	BSIM4SOI
DELRSHG	no	yes	no	no
DELTOX	yes	yes	yes	yes
DELVTO	yes	yes	yes	yes
DELXJ	no	yes	no	no
DTEMP	yes	yes	yes	yes
GEO	yes	yes	no	no
GEOMOD	no	yes	no	no
IC	yes	yes	yes	yes
L	yes	yes	yes	yes
MIN	no	yes	no	no
MULID0	no	yes	yes	yes
MULNGATE	no	yes	no	no
MULU0	yes	yes	yes	yes
MULVSAT	no	yes	no	yes
NF	no	yes	yes	yes
NGCON	no	yes	no	no
NRD	yes	yes	yes	yes
NRS	yes	yes	yes	yes
OFF	yes	yes	yes	yes
PD	yes	yes	yes	yes
PS	yes	yes	yes	yes
RBDB	no	yes	no	yes
RBODYMOD	no	yes	no	yes
RBPB	no	yes	no	yes
RBPD	no	yes	no	no
RBPS	no	yes	no	no
RBSB	no	yes	no	yes
RDC	no	yes	no	no
RGATEMOD	no	yes	yes	yes

Chapter 6: MOSFET Models (BSIM): Levels 47 through 72

Supported Instance Parameters, BSIM3, BSIM4, BSIM3SOI and BSIM4SOI

Table 207 Instance parameters: BSIM3, BSIM4, BSIM3SOI, BSIM4SOI

Instance Parameter	BSIM3	BSIM4	BSIM3SOI	BSIM4SOI
RGEOMOD	no	yes	no	no
RSC	no	yes	no	no
RTH0	yes	no	no	no
SA	yes	yes	no	yes
SA1	yes	yes	no	no
SA10	yes	yes	no	no
SA2	yes	yes	no	no
SA3	yes	yes	no	no
SA4	yes	yes	no	no
SA5	yes	yes	no	no
SA6	yes	yes	no	no
SA7	yes	yes	no	no
SA8	yes	yes	no	no
SA9	yes	yes	no	no
SB	yes	yes	no	yes
SB1	yes	yes	no	no
SB10	yes	yes	no	no
SB2	yes	yes	no	no
SB3	yes	yes	no	no
SB4	yes	yes	no	no
SB5	yes	yes	no	no
SB6	yes	yes	no	no
SB7	yes	yes	no	no
SB8	yes	yes	no	no
SB9	yes	yes	no	no
SC	3.22 or later	yes	no	no
SCA	3.22 or later	yes	no	no
SCB	3.22 or later	yes	no	no
SCC	3.22 or later	yes	no	no

Chapter 6: MOSFET Models (BSIM): Levels 47 through 72
Supported Instance Parameters, BSIM3, BSIM4, BSIM3SOI and BSIM4SOI

Table 207 Instance parameters: BSIM3,BSIM4, BSIM3SOI, BSIM4SOI

Instance Parameter	BSIM3	BSIM4	BSIM3SOI	BSIM4SOI
SD	yes	yes	no	yes
SOIQ0	no	no	yes	yes
STIMOD	yes	yes	no	no
SW1	yes	yes	no	no
SW10	yes	yes	no	no
SW2	yes	yes	no	no
SW3	yes	yes	no	no
SW4	yes	yes	no	no
SW5	yes	yes	no	no
SW6	yes	yes	no	no
SW7	yes	yes	no	no
SW8	yes	yes	no	no
SW9	yes	yes	no	no
TNODEOUT	yes	no	yes	yes
TRNQSMOD	no	yes	no	no
W	yes	yes	yes	yes
XGW	no	yes	no	no

Chapter 6: MOSFET Models (BSIM): Levels 47 through 72

Supported Instance Parameters, BSIM3, BSIM4, BSIM3SOI and BSIM4SOI

MOSFET Capacitance Models

This chapter discusses use of available capacitance models.

HSPICE ships hundreds of examples for your use; see [Listing of Demonstration Input Files](#) for paths to demo files.

These topics are presented in the following sections:

- [MOS Gate Capacitance Models](#)
- [Selecting Capacitor Models](#)
- [Transcapacitance](#)
- [Operating Point Capacitance Printout](#)
- [Element Template Printout](#)
- [Calculating Gate Capacitance](#)
- [MOS Gate Capacitance Model Parameters](#)
- [Specifying XQC and XPART for CAPOP=4, 9, 11, 12, 13](#)
- [Overlap Capacitance Equations](#)
- [CAPOP=0 — SPICE Meyer Gate Capacitances](#)
- [CAPOP=1 — Modified Meyer Gate Capacitances](#)
- [CAPOP=3 — Gate Capacitances \(Simpson Integration\)](#)
- [CAPOP=4—Charge Conservation Capacitance Model](#)
- [CAPOP=5 — No Gate Capacitance](#)
- [CAPOP=6 — AMI Gate Capacitance Model](#)
- [CAPOP=13 — BSIM1-based Charge-Conserving Gate Capacitance Model](#)

- [CAPOP=39 — BSIM2 Charge-Conserving Gate Capacitance Model](#)
- [Calculating Effective Length and Width for AC Gate Capacitance](#)

MOS Gate Capacitance Models

You can use capacitance model parameters with all MOSFET model statements.

Three fixed-capacitance parameters ($CGDO$, $CGSO$, and $CGBO$) represent gate-to-drain, gate-to-source, and gate-to-bulk overlap capacitances to model charge storage, use fixed and nonlinear gate capacitances and junction capacitances. The algorithm used for calculating nonlinear, voltage-dependent MOS gate capacitance depends on the value of the $CAPOP$ model parameter.

To model MOS gate capacitances as a nonlinear function of terminal voltages, use Meyer's piecewise linear model for all MOS levels. The charge conservation model is also available for MOSFET model Levels 2 through 7, 13, and 27. For LEVEL 1, you must specify the TOX model parameter to invoke the Meyer model. The next three sections describe the Meyer, Modified Meyer, and Charge Conservation MOS Gate Capacitance models.

Some of the charge conserving models (Ward-Dutton or BSIM) can cause "timestep too small" errors if you do not specify other nodal capacitances.

Selecting Capacitor Models

When you select a gate capacitance model, you can choose various combinations of capacitor models and DC models. You can incrementally update older DC models with new capacitance equations, without having to move to a new DC model. You can use the $CAPOP$ model parameter to select the gate capacitance and validate the effects of different capacitance models.

The $CAPOP$ capacitance model selection parameter selects the capacitor models to use for modeling the MOS gate capacitance:

- gate-to-drain capacitance
- gate-to- source capacitance
- gate-to-bulk capacitance.

You can use `CAPOP` to select several versions of the Meyer and charge conservation model.

Some capacitor models are tied to specific DC models (DC model level in parentheses below). Other models are designated as general; any DC model can use them.

Parameter	Description
CAPOP=0	SPICE original Meyer gate-capacitance model (general)
CAPOP=1	Modified Meyer gate-capacitance model (general)
CAPOP=2	Parameterized Modified Meyer gate-capacitance model (general default)
CAPOP=3	Parameterized Modified Meyer gate-capacitance model with Simpson integration (general)
CAPOP=4	Charge conservation capacitance model (analytic), Levels 2, 3, 6, 7, 13, 28, and 39 only
CAPOP=5	No capacitor model
CAPOP=6	AMI capacitor model (LEVEL 5)
CAPOP=9	Charge conservation model (LEVEL 3)
CAPOP=11	Ward-Dutton model (specialized, LEVEL 2)
CAPOP=12	Ward-Dutton model (specialized, LEVEL 3)
CAPOP=13	Generic BSIM Charge-Conserving Gate Capacitance model (default for Levels 13, 28, 39)
CAPOP=39	BSIM2 Charge-Conserving Gate Capacitance model (LEVEL 39)

CAPOP=4 selects the recommended charge-conserving model from among CAPOP=11, 12, or 13 for the specified DC model.

Table 208 CAPOP = 4 Selections

MOS Level	Default CAPOP	CAPOP=4 selects
2	2	11
3	2	12
13, 28, 39	13	13
Other levels	2	11

The proprietary models (Levels 5, 17, 21, 22, 25, 31, 33), the SOS model (LEVEL 27), and models higher than 49 have their own built-in capacitance routines.

Transcapacitance

If a capacitor has two terminals (1 and 2) with charges named Q1 and Q2 on the two terminals that sum to zero (for example, $Q1 = -Q2$), then the charge is a function of the voltage difference between the terminals ($V12 = V1 - V2$). One quantity ($C = dQ1/dV12$) completely describes the small-signal characteristics of the device.

If a capacitor has four terminals, the sum of the charges on the four terminals must equal zero ($Q1 + Q2 + Q3 + Q4 = 0$). They can depend only on voltage differences, but they are otherwise arbitrary functions. Because three independent charges (Q1, Q2, Q3) are functions of three independent voltages ($V14, V24, V34$), you must specify nine derivatives to describe the small-signal characteristics.

You can consider the four charges separately as functions of the four terminal voltages, $Q1(V1, V2, V3, V4)$, ... $Q4(V1, V2, V3, V4)$. The derivatives form a four-by-four matrix, dQ_i/dV_j , $i=1,4$, $j=1,4$. Simulation directly interprets this matrix as AC measurements.

If you apply an AC voltage signal to the j terminal and you ground the other terminals to AC, and if you measure AC current into the i terminal, then the current is the imaginary constant times $2\pi \times \text{frequency} \times dQ_i/dV_j$.

- Because the charges add up to zero, each column of this matrix must add up to zero.
- Because the charges can depend only on voltage differences, each row must add up to zero.

In general, the matrix is not symmetrical:

dQ_i/dV_j need not equal dQ_j/dV_i

This is not an expected event because it does not occur for the two-terminal case. For two terminals, because the rows and columns must add up to zero, dQ_1/dV_2 must equal dQ_2/dV_1 .

$$\frac{dQ_1}{dV_1} + \frac{dQ_2}{dV_1} = 0, \quad \frac{dQ_1}{dV_1} + \frac{dQ_2}{dV_2} = 0$$

For three or more terminals, this relation does not generally hold.

The terminal input capacitances are the diagonal matrix entries:

$$C_{ii} = dQ_i/dV_i \quad i=1, .4$$

The transcapacitances are the negative of off-diagonal entries:

$$C_{ij} = -dQ_i/dV_j \quad i \text{ not equal to } j$$

All of the C values are normally positive.

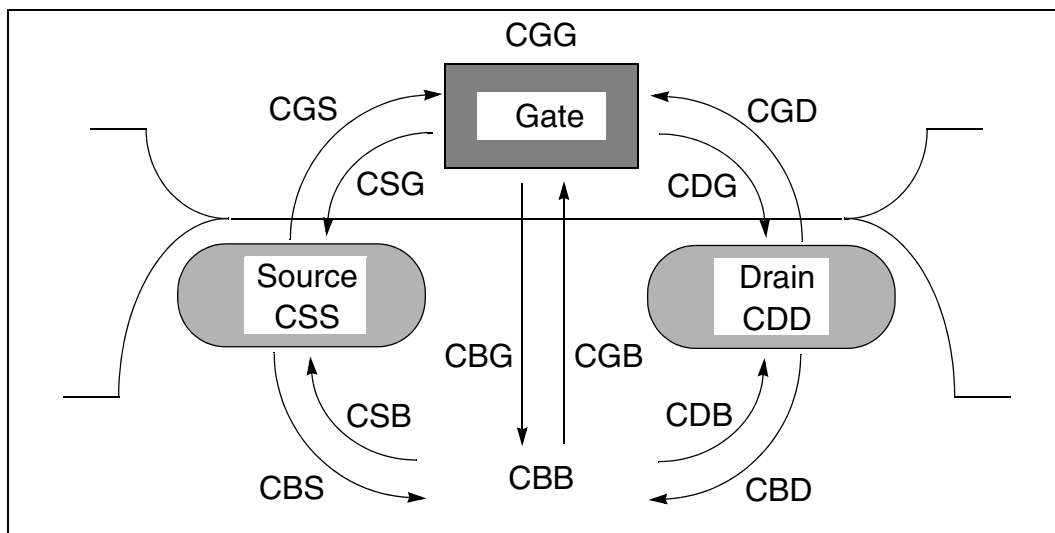


Figure 20 MOS Capacitances

In [Figure 20](#), Cij determines the current transferred out of the i node from a voltage change on the j node. The arrows, representing direction of influence, point from node j to node i.

A MOS device with terminals named D, G, S, and B provides:

$$C_{GG} = \frac{dQ_g}{dV_G}, C_{GD} = -\frac{dQ_g}{dV_D}, C_{DG} = -\frac{dQ_D}{dV_G}$$

- C_{GG} represents input capacitance: a change in gate voltage requires a current equal to $C_{GG}dv_G/dt$ into the gate terminal.
- C_{GD} represents Miller feedback: a change in drain voltage creates a current equal to $C_{GD}dv_D/dt$ out of the gate terminal.
- C_{DG} represents Miller feedthrough, capacitive current out of the drain due to a change in gate voltage.

To show how C_{GD} might not equal C_{DG} , the following example is a simplified model with no bulk charge with a gate charge as a function of V_{GS} only, and with the 50/50 channel charge partitioned into Q_S and Q_D :

$$Q_G = Q(v_{gs}), Q_S = -0.5 \cdot Q(v_{gs}), Q_D = -0.5 \cdot Q(v_{gs}), Q_B = 0$$

Consequently:

$$C_{GD} = -\frac{dQ_G}{dV_D} = 0, C_{DG} = -\frac{dQ_D}{dV_G} = 0.5 \cdot \frac{dQ}{dv_{gs}}$$

Therefore, this model has Miller feedthrough, but no feedback.

Operating Point Capacitance Printout

The operating point printout reports six capacitances:

Table 209 Operating Point Capacitance

Capacitance	Value
cdtot	dQ_D/dV_D
cgtot	dQ_G/dV_G
cstot	dQ_S/dV_S
cbtot	dQ_B/dV_B

Table 209 Operating Point Capacitance

Capacitance	Value
cgs	$-dQ_G/dV_S$
cgd	$-dQ_G/dV_D$

These capacitances include gate-drain, gate-source, and gate-bulk overlap capacitance, and drain-bulk and source-bulk diode capacitance. Drain and source refer to node 1 and 3 of the MOS element (physical instead of electrical).

For the Meyer models, where charges such as Q_D are not well defined, [Table 210](#) shows the printout quantities.

Table 210 Capacitance Printout for Meyer Models

Capacitance	Value
cdtot	$c_{gd} + c_{db}$
cgtot	$c_{gs} + c_{gd} + c_{gb}$
cstot	$c_{gs} + c_{sb}$
cbtot	$c_{gb} + c_{sb} + c_{db}$
cgs	cgs
cgd	cgd

Element Template Printout

The MOS element template printouts for gate capacitance are LX18 to LX23 and LX32 to LX34. From these nine capacitances, you can construct the complete four-by-four matrix of transcapacitances. The nine LX printouts are:

Chapter 7: MOSFET Capacitance Models

Element Template Printout

LX18 (m) = dQ_G/dV_{GB} = CGGBO
LX19 (m) = dQ_G/dV_{DB} = CGDBO
LX20 (m) = dQ_G/dV_{SB} = CGSBO
LX21 (m) = dQ_B/dV_{GB} = CBGBO
LX22 (m) = dQ_B/dV_{DB} = CBDBO
LX23 (m) = dQ_B/dV_{SB} = CBSBO
LX32 (m) = dQ_D/dV_G = CDGBO
LX33 (m) = dQ_D/dV_D = CDDBO
LX34 (m) = dQ_D/dV_S = CDSBO

These capacitances include gate-drain, gate-source, and gate-bulk overlap capacitance, and drain-bulk and source-bulk diode capacitance. Drain and source refer to node 1 and 3 of the MOS element (physical instead of electrical).

For an NMOS device with source and bulk grounded:

- LX18 is the input capacitance.
- LX33 is the output capacitance.
- LX19 is the Miller feedback capacitance (gate current induced by voltage signal on the drain).
- LX32 is the Miller feedthrough capacitance (drain current induced by the voltage signal on the gate).

A device operating with node 3 as electrical drain—for example an NMOS device with node 3 at higher voltage than node 1—is in *reverse mode*.

The LX values are physical, but you can translate them into electrical definitions by interchanging D and S:

$CGG(\text{reverse}) = CGG = LX18$
 $CDD(\text{reverse}) = CSS = dQ_S/dV_S = d(-Q_G - Q_B - Q_D)/dV_S =$
 $-LX20 - LX23 - LX34$
 $CGD(\text{reverse}) = CGS = -LX20$
 $CDG(\text{reverse}) = CSG = -dQ_S/dV_G = d(Q_G + Q_B + Q_D)/dV_G =$
 $LX18 + LX21 + LX32$

For Meyer models, QD and other charges are not well defined. The formulas (such as $LX18 = CGG$, $LX19 = -CGD$) are still true, but the transcapacitances are symmetrical; for example, $CGD = CDG$. In terms of the six independent Meyer capacitances (cgd, cgs, cgb, cdb, csb, and cds), the LX printouts are:

```
LX18 (m) = CGS+CGD+CGB
LX19 (m) = LX32 (m) = -CGD
LX20 (m) = -CGS
LX21 (m) = -CGB LX22 (m) = -CDB
LX23 (m) = -CSB
LX33 (m) = CGD+CDB+CDS
LX34 (m) = -CDS
```

Calculating Gate Capacitance

The following input file example shows a gate capacitance calculation in detail for a BSIM model. τ_{OX} is chosen so that: $\frac{eox}{tox} = 1e - 3F / m^2$

In this example, V_{fb0} , ϕ , and k_1 are chosen so that $v_{th}=1v$. The AC sweep is chosen so that the last point is: $2 \cdot \pi \cdot freq = 1e6s^{-1}$

Input File

This example is based on demonstration netlist calcap.sp, which is available in directory \$<installdir>/demo/hspice/mos:

```
$
m d g 0 b nch l=0.8u w=100u ad=200e-12 as=200e-12
vd d 0 5
vg g 0 5 ac 1
vb b 0 0
.ac dec 1 1.59155e4 1.59155e5
.print CGG=LX18(m) CDD=LX33(m) CGD=par('-LX19(m)')
+ CDG=par('-LX32(m)')
.print ig_imag=ii2(m) id_imag=ii1(m)
.model nch nmos level=13 update=2
+ xqc=0.6 toxm=345.315 vfb0=-1 phi0=1 k1=1.0 muz=600
+ mus=650 acm=2
+ xl=0 ld=0.1u meto=0.1u cj=0.5e-4 mj=0 cjsw=0
.alter
vd d 0 5 ac 1
vg g 0 5
.end
```

Calculations

$$Leff = 0.6\mu$$

$$\frac{eox}{tox} = 1e-3F/m^2$$

$$Cap = \frac{Leff \cdot Weff \cdot eox}{tox} = 60e-15F$$

BSIM equations for internal capacitance in saturation with xqc=0.4:

$$body = 1 + 0.5 \cdot \left(1 - \frac{1}{(1.744 + 0.8364 \cdot (PHI0 + vsb))} \right) \cdot \frac{K1}{\sqrt{(PHI0 + vsb)}}$$

$$1 + 0.5 \cdot \left(1 - \frac{1}{(1.744 + 0.8364)} \right) = 1.3062$$

$$cgg = Cap \cdot \left(1 - \frac{1}{(3 \cdot body)} \right) = Cap \cdot 0.7448 = 44.69F$$

$$cgd = 0$$

$$cdg = \left(\frac{4}{15} \right) \cdot Cap = 16F$$

$$cdd = 0$$

$$\text{Gate-drain overlap} = (ld + meto) \cdot Weff \cdot \frac{eox}{tox} = 20e-15F$$

Adding the overlaps:

$$cgg = 44.69F + 2 \cdot 20F = 84.69F$$

$$cgd = 20F$$

$$cdg = 36F$$

$$cdd = 20F$$

$$\text{Drain-bulk diode cap} = cj \cdot ad = (0.5e-4) \cdot (200e-12) = 10F$$

Adding the diodes:

$$cgg = 84.69F$$

$$c_{gd} = 20F$$

$$c_{dg} = 36F$$

$$c_{dd} = 30F$$

Results

```
subckt
element 0:m
model 0:nch
cdtot 30.0000f
cgtot 84.6886f
cstot 65.9999f
cbtot 43.4213f
cgs 61.2673f
cgd 20.0000f
```

The calculation and simulation results match.

Plotting Gate Capacitances

The following input file shows how to plot gate capacitances as a function of bias. Set `.OPTION DCCAP` to turn on capacitance calculations for a DC sweep. The model used is the same as for the previous gate capacitance calculations.

Example

This example is based on demonstration netlist `gatecap.sp`, which is available in directory `$<installdir>/demo/hspice/mos`:

Calculating Gate Capacitance

Figure 10 is a line graph showing the relationship between LD [Lin] (Y-axis, ranging from 0 to 100.0F) and PDN [Lin] (X-axis, ranging from 0 to 5.0). The graph displays several data series, all labeled as CDB, and one labeled C0. The C0 series starts at 100.0F and decreases to approximately 85.0F at PDN=3.0. The other CDB series show varying trends, with some increasing and others decreasing as PDN increases.

PDN [Lin]	C0	CDB (Top)	CDB (Middle)	CDB (Bottom)
0.0	100.0F	50.0F	50.0F	50.0F
1.0	100.0F	55.0F	50.0F	45.0F
2.0	95.0F	60.0F	48.0F	38.0F
3.0	85.0F	62.0F	45.0F	22.0F
4.0	85.0F	62.0F	45.0F	22.0F
5.0	85.0F	62.0F	45.0F	22.0F

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Capacitance Control Options

The SCALM, CVTOL, DCSTEP, and DCCAP control options affect the CAPOP models.

- SCALM scales the model parameters (ignored in Levels 49 and higher).
- CVTOL controls the error tolerance for convergence for the CAPOP=3 model (see [CAPOP=3 — Gate Capacitances \(Simpson Integration\) on page 681](#)).
- DCSTEP models capacitances with a conductance during DC analysis.
- DCCAP calculates capacitances in DC analysis.

Scaling

.OPTION SCALM scales the CGBO, CGDO, CGSO, COX, LD, and WD parameters according to fixed rules, which are a function of the parameter's units. If the model parameter's units are in meters, simulation multiplies the parameter by SCALM. For example:

- The LD parameter uses units in meters; to obtain its scaled value, simulation multiplies the value of LD by SCALM.
- If the units are in meters squared, simulation multiplies the parameter by $SCALM^2$.
- If the units are in reciprocal meters, the parameter's value is divided by SCALM. For example, because CGBO is in farads/meter, the value of CGBO is divided by SCALM.
- If the units are in reciprocal meters squared, then the parameter is divided by $SCALM^2$.

For the scaling equations specific to each CAPOP level, see the individual CAPOP subsections.

MOS Gate Capacitance Model Parameters

Table 211 Basic Gate Capacitance Parameters

Name (Alias)	Units	Default	Description
CAPOP	-	2.0	Capacitance model selector.
COX (CO)	F/m ²	3.453e-4	Oxide capacitance. If you do not specify COX, simulation calculates it from TOX. The default corresponds to the TOX default of 1e-7: $\text{COXscaled} = \text{COX}/\text{SCALM}^2$
TOX	m	1e-7	Oxide thickness, calculated from COX (if you specify COX). The program uses the default if you do not specify COX. For TOX>1, simulation assumes that the unit is Angstroms. A level-dependent default can override it. See specific MOSFET levels in this manual.

Table 212 Gate Overlap Capacitance Model Parameters

Name (Alias)	Units	Default	Description
CGBO (CGB)	F/m	0.0	Gate-bulk overlap capacitance per meter channel length. If you set WD and TOX, but you do not set CGBO, then simulation calculates CGBO. $\text{CGBOscaled} = \text{CGBO}/\text{SCALM}$
CGDO (CGD, C2)	F/m	0.0	Gate-drain overlap capacitance per meter channel width. If you set LD or METO and TOX, but you do not set CGDO, then simulation calculates CGDO. $\text{CGDOscaled} = \text{CGDO}/\text{SCALM}$

Table 212 Gate Overlap Capacitance Model Parameters

Name (Alias)	Units	Default	Description
CGSO (CGS, C1)	F/m	0.0	Gate-source overlap capacitance per meter channel width. If you set LD or METO and TOX, but you do not set CGSO, then simulation calculates CGSO. $CGSO_{scaled} = CGSO / SCALM$
LD (LATD, DLAT)	m		Lateral diffusion into channel from source and drain diffusion. <ul style="list-style-type: none"> ▪ If you do not specify either LD or XJ, then the LD default=0.0. ▪ If you specify XJ but you do not specify LD, then simulation calculates LD from XJ. ▪ LD default=0.75 · XJ for all levels except LEVEL 4 for which LD default=0.75. $LD_{scaled} = LD \cdot SCALM$ LEVEL 4: $LD_{scaled} = LD \cdot XJ \cdot SCALM$
METO	m	0.0	Fringing field factor for gate-to-source and gate-to-drain overlap capacitance calculation. $METO_{scaled} = METO \cdot SCALM$
WD	m	0.0	Lateral diffusion into channel from bulk along width. $WD_{scaled} = WD \cdot SCALM$

Table 213 Meyer Capacitance Parameters CAPOP=0, 1, 2

Name (Alias)	Units	Default	Description
CF1	V	0.0	Modified MEYER control for transition of cgs from depletion to weak inversion for CGSO (for CAPOP=2 only)
CF2	V	0.1	Modified MEYER control for transition of cgs from weak to strong inversion region (for CAPOP=2 only)
CF3		1.0	Modified MEYER control for the cgs and cgd transition from the saturation region to the linear region as a function of vds (for CAPOP=2 only)
CF4		50.0	Modified MEYER control for the contour of the cgb and cgs smoothing factors
CF5		0.667	Modified MEYER control for the capacitance multiplier for cgs in the saturation region
CF6		500.0	Modified MEYER control for contour of cgd smoothing factor
CGBEX		0.5	cgb exponent (for CAPOP=1 only)

Table 214 Charge Conservation Parameters (CAPOP=4)

Name (Alias)	Units	Default	Description
XQC		0.5	Coefficient of channel charge share attributed to drain; its range is 0.0 to 0.5. This parameter applies only to CAPOP=4 and some of its level-dependent aliases.

Specifying XQC and XPART for CAPOP=4, 9, 11, 12, 13

Parameter rules for the gate capacitance charge sharing coefficient (XQC & XPART) in the saturation region:

- If you do not specify either XPART or XQC, then simulation uses the 0/100 model.
- If you specify both XPART and XQC, then XPART overrides XQC.
- If you specify XPART, but you do not specify XQC, then:
 - XPART=0 →40/60
 - XPART=0.4 →40/60
 - XPART=0.5 →50/50
 - XPART=1 →0/100
 - XPART = any other value less than 1 →40/60
 - XPART >1 →0/100
- If you specify XQC but you do not specify XPART, then:
 - XQC=0 →0/100
 - XQC=0.4 →40/60
 - XQC=0.5 →50/50
 - XQC=1 →0/100
 - XQC = any other value less than 1 →40/60
 - XQC>1 →0/100

The only difference is the treatment of the 0 parameter value.

After you specify XPART/XQC, the gate capacitance ramps from 50/50 at $V_{ds}=0$ volt (linear region) to the value (with V_{ds} sweep) in the saturation region in XPART/XQC. Ramping the charge-sharing coefficient ensures smooth gate capacitance characteristics.

Overlap Capacitance Equations

The overlap capacitors are common to all models. You can input them explicitly or the program can calculate them. Either way, these overlap capacitors must

be added into the respective voltage-variable capacitors before integration, and before the DC operating point reports the combined parallel capacitance.

Gate-to-Bulk Overlap Capacitance

If you specify CGBO, then: $CGBO_{eff} = M \cdot L_{eff} \cdot CGBO_{scaled}$

Otherwise: $CGBO_{eff} = 2 \cdot WD_{scaled} \cdot L_{eff} \cdot COX_{scaled} \cdot M$

Gate-to-Source Overlap Capacitance

If you specify CGSO, then: $CGSO_{eff} = W_{eff} \cdot CGSO_{scaled}$

Otherwise: $CGSO_{eff} = W_{eff} \cdot (LD_{scaled} + METO_{scaled}) \cdot COX_{scaled}$

Gate-to-Drain Overlap Capacitance

If you specify CGDO, then: $CGDO_{eff} = W_{eff} \cdot CGDO_{scaled}$

Otherwise: $CGDO_{eff} = W_{eff} \cdot (LD_{scaled} + METO_{scaled}) \cdot COX_{scaled}$

Simulation calculates the L_{eff} value for each model differently, and saves this value in the corresponding model section. The W_{eff} calculation is not the same as the W_{eff} value in the LEVEL 1, 2, 3, 6, 7 and 13 models.

$$W_{eff} = M \cdot (W_{scaled} \cdot WMLT + XW_{scaled})$$

The $2 \cdot WD_{scaled}$ factor is not subtracted.

CAPOP=0 — SPICE Meyer Gate Capacitances

Definition: $cap = COX_{scaled} \cdot W_{eff} \cdot L_{eff}$

Gate-Bulk Capacitance (cgb)

Accumulation, $v_{gs} \geq v_{th-PH1}$: $cgb = cap$

Depletion, $v_{gs} < v_{th}$: $cgb = cap \cdot \frac{v_{th} - v_{gs}}{PH1}$

Strong Inversion, $v_{gs} \geq v_{th}$: $cgb = 0$

Gate-Source Capacitance (c_{gs})

Accumulation: $v_{gs} \leq v_{th} - \frac{PHI}{2}$

$$c_{gs} = 0$$

Depletion, $v_{gs} \leq v_{th}$: $c_{gs} = CF5 \cdot cap + \frac{cap \cdot (v_{gs} - cth)}{0.75 \cdot PHI}$

Strong Inversion Saturation Region: $v_{gs} > v_{th}$ and $v_{ds} \geq v_{dsat}$

$$c_{gs} = CF5 \cdot cap$$

Strong Inversion Linear Region: $v_{gs} > v_{th}$ and $v_{ds} < v_{dsat}$

$$c_{gs} = CF5 \cdot cap \cdot \left\{ 1 - \left[\frac{v_{dsat} - v_{ds}}{2 \cdot (v_{dsat} + v_{sb}) - v_{ds} - v_{sb}} \right]^2 \right\}$$

Gate-Drain Capacitance (c_{gd})

The gate-drain capacitance has value only in the linear region.

Strong Inversion Linear Region: $v_{gs} > v_{th}$ and $v_{ds} < v_{dsat}$

$$c_{gd} = CF5 \cdot cap \cdot \left\{ 1 - \left[\frac{v_{dsat} + v_{sb}}{2 \cdot (v_{dsat} + v_{sb}) - v_{ds} - v_{sb}} \right]^2 \right\}$$

Example

This example is based on demonstration netlist capop0.sp, which is available in directory \$<installdir>/demo/hspice/mos:

Chapter 7: MOSFET Capacitance Models

CAPOP=0 — SPICE Meyer Gate Capacitances

```
*file capop0.sp---capop=0 capacitances
*
*this file is used to create spice meyer gate c-v plots
**
*(capop=0) for low vds and high vds
*
.options acct=2 post=2 dccap=1 nomod
.dc vg1 -1 4 .01
.print dc cgb_vdsp05=par('-lx21(m1)') cgd_vdsp05=par('-
lx19(m1)')
+ cgs_vdsp05=par('-lx20(m1)')
.print dc cgb_vdsp8=par('-lx21(m2)') cgd_vdsp8=par('-lx19(m2)')
+ cgs_vdsp8=par('-lx20(m2)')
*****
m1 d1 g1 0 0 mn l=5e-6 w=20e-6 $ create capacitances for vds=0.05
m2 d2 g1 0 0 mn l=5e-6 w=20e-6 $ create capacitances for vds=0.80
*****
vd1 d1 0 dc 0.05
vd2 d2 0 dc 0.80
vg1 g1 0 dc 0.0
*
*****
*
.model mn nmos ( level = 2
+ vto = 1.0 gamma = 1.40 nsub = 7.20e15
+ uo = 817 ucrit = 3.04e4 phi=.6
+ uexp = 0.102 neff = 1.74 vmax = 4.59e5
+ tox = 9.77e-8 cj = 0 cjsw = 0 js = 0
+ capop=0 )
.end
```

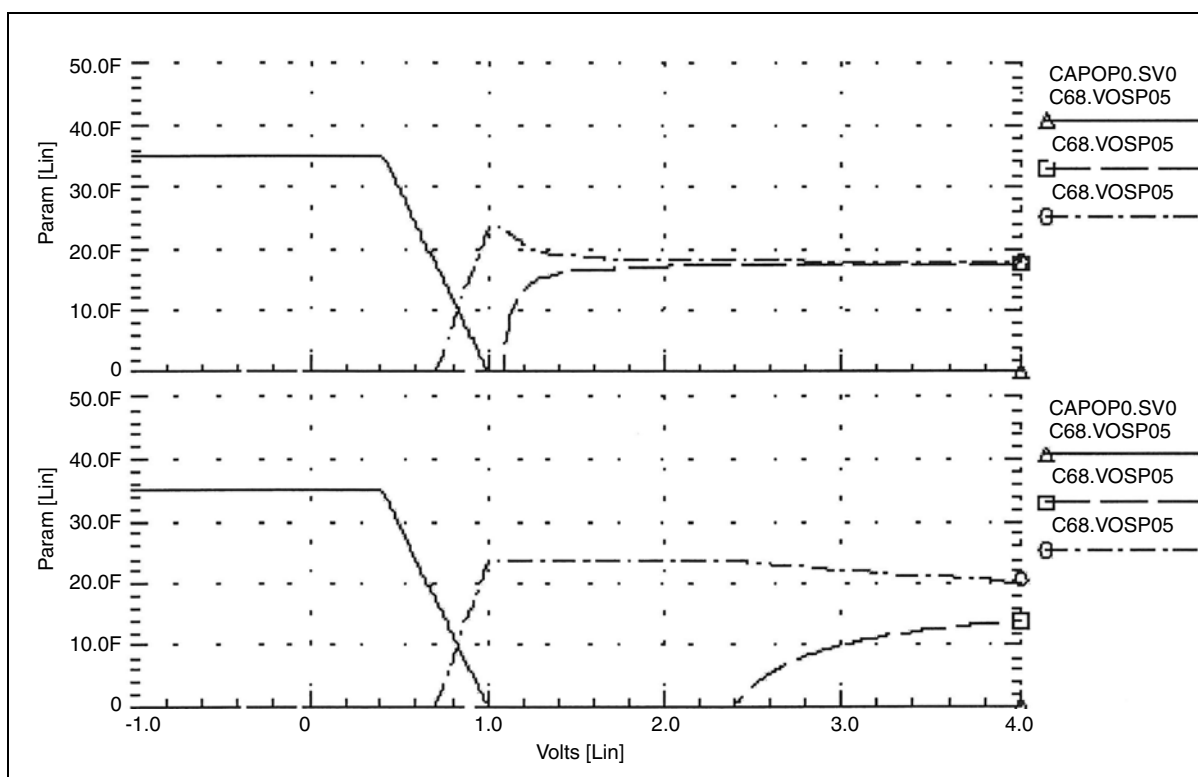



Figure 22 CAPOP=0 Capacitances

CAPOP=1 — Modified Meyer Gate Capacitances

Define: $cap = COXscaled \cdot Weff \cdot Leff$

In the following equations, G^- , G^+ , D^- , and D^+ are smooth factors. You cannot change the values of these parameters.

Gate-Bulk Capacitance (cgb)

Accumulation, $vgs \leq vfb - vsb$

$$cgb = cap$$

Depletion, $vgs \leq vth$

$$c_{gb} = \frac{cap}{\left[1 + 4 \cdot \frac{v_{gs} + v_{sb} - v_{fb}}{GAMMA^2} \right]^{CGBEX}}$$

Strong Inversion, $v_{gs} > v_{th}$

$$c_{gb} = \frac{G^+ \cdot cap}{\left[1 + 4 \cdot \frac{GAMMA \cdot (v_{sb} + PHI)^2 + v_{sb} + PHI}{GAMMA^2} \right]^{CGBEX}}$$

These equations replace GAMMA with effective γ for model levels higher than 4.

Gate-Source Capacitance (cgs)

Low vds ($v_{ds} < 0.1$)

Accumulation, $v_{gs} \leq v_{th}$ $c_{gs} = CF5 \cdot cap \cdot G^- \cdot D^-$

Weak Inversion, $v_{gs} < v_{th} + 0.1$

$$c_{gs} = CF5 \cdot cap \cdot \left\{ \frac{v_{gs} - v_{th}}{0.1} \cdot \left[1 - \left(\frac{0.1 - v_{ds}}{0.2 - v_{ds}} \right)^2 - D^- \right] + D^- \right\}$$

Strong Inversion, $v_{gs} \geq v_{th} + 0.1$

$$c_{gs} = CF5 \cdot cap \cdot \left\{ 1 - \left[\frac{v_{gs} - v_{th} - v_{ds}}{2 \cdot (v_{gs} - v_{th}) - v_{ds}} \right]^2 \right\}$$

High vds ($v_{ds} \geq 0.1$)

Accumulation, $v_{gs} \leq v_{th}$ $c_{gs} = CF5 \cdot cap \cdot G^-$

Saturation Region, $v_{gs} < v_{th} + v_{ds}$ $c_{gs} = CF5 \cdot cap$

Linear Region, $v_{gs} \geq v_{th} + v_{ds}$

$$c_{gs} = CF5 \cdot cap \cdot \left\{ 1 - \left[\frac{v_{gs} - v_{th} - v_{ds}}{2 \cdot (v_{gs} - v_{th}) - v_{ds}} \right]^2 \right\}$$

Gate-Drain Capacitance (c_{gd})

Low v_{ds} ($v_{ds} < 0.1$)

Accumulation, $v_{gs} \leq v_{th}$ $c_{gd} = CF5 \cdot cap \cdot G^- \cdot D^+$

Weak Inversion, $v_{gs} < v_{th} + 0.1$

$$c_{gd} = CF5 \cdot cap \cdot \left\{ D^+ + \frac{v_{gs} - v_{th}}{0.1} \cdot \max \left[0, 1 - \left(\frac{0.1}{0.2 - v_{ds}} \right)^2 - D^+ \right] \right\}$$

Strong Inversion, $v_{gs} \geq v_{th} + 0.1$

$$c_{gd} = CF5 \cdot cap \cdot \max \left\{ D^+, 1 - \left[\frac{v_{gs} - v_{th}}{2 \cdot (v_{gs} - v_{th}) - v_{ds}} \right]^2 \right\}$$

High v_{ds} ($v_{ds} > 0.1$)

Accumulation, $v_{gs} \leq v_{th}$: $c_{gd} = CF5 \cdot cap \cdot G^- \cdot D^+$

Saturation Region, $v_{gs} < v_{th} + v_{ds}$: $c_{gd} = CF5 \cdot cap \cdot D^+$

Strong Inversion, $v_{gs} \geq v_{th} + v_{ds}$:

$$c_{gd} = CF5 \cdot cap \cdot \max \left\{ D^+, 1 - \left[\frac{v_{gs} - v_{th}}{2 \cdot (v_{gs} - v_{th}) - v_{ds}} \right]^2 \right\}$$

Example

This example is based on demonstration netlist capop1.sp, which is available in directory \$<installdir>/demo/hspice/mos:

Chapter 7: MOSFET Capacitance Models

CAPOP=1 — Modified Meyer Gate Capacitances

```

*file capop1.sp---capop1 capacitances
*
*this file creates the modified meyer gate c-v plots
*(capop=1) for low vds and high vds.
*
.options acct=2 post=2 dccap=1 nomod
.dc vg1 -1 4 .01
.print dc cgb_vdsp05=par('-lx21(m1)') cgd_vdsp05=par('-
lx19(m1)')
+ cgs_vdsp05=par('-lx20(m1)')
.print dc cgb_vdsp8=par('-lx21(m2)') cgd_vdsp8=par('-lx19(m2)')
+ cgs_vdsp8=par('-lx20(m2)')
*****
m1 d1 g1 0 0 mn l=5e-6 w=20e-6 $creates capacitances for vds=0.05
m2 d2 g1 0 0 mn l=5e-6 w=20e-6 $creates capacitances for vds=0.80
*****
vd1 d1 0 dc 0.05
vd2 d2 0 dc 0.80
vg1 g1 0 dc 0.0
*
*****
*
.model mn nmos ( level = 2
+ vto = 1.0 gamma = 1.40 nsub = 7.20e15
+ tox = 9.77e-8 uo = 817 ucrit = 3.04e4
+ uexp = 0.102 neff = 1.74 vmax = 4.59e5
+ phi = 0.6 cj = 0 cjsw = 0 js = 0
+ capop=1 )
.end

```

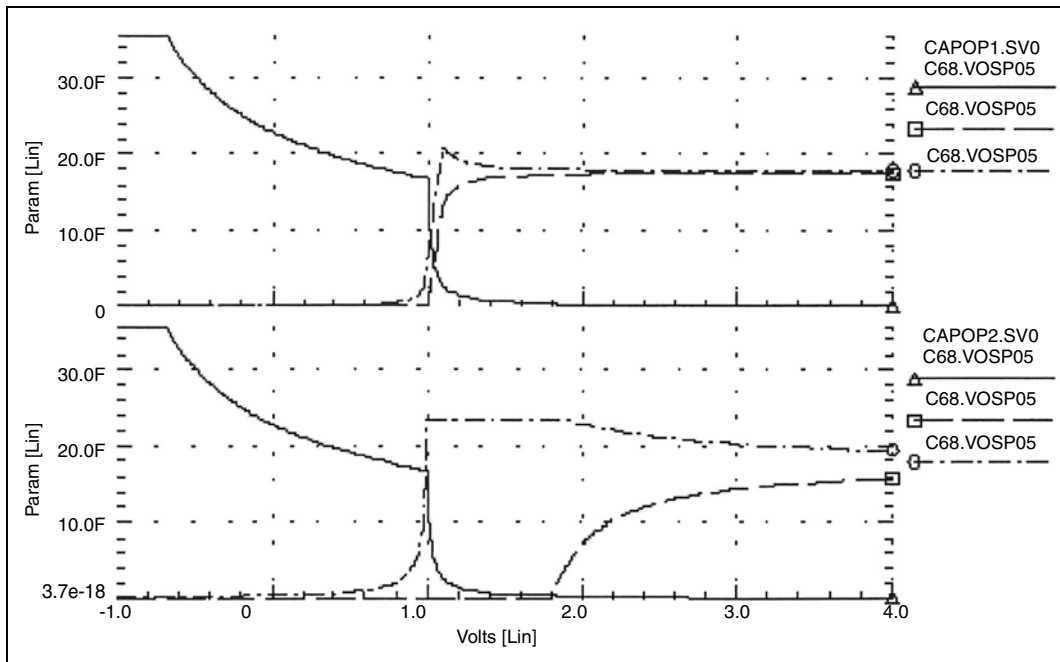


Figure 23 CAPOP=1 Capacitances

CAPOP=2—Parameterized Modified Meyer Capacitance

The CAPOP=2 Meyer capacitance model is the more general form of Meyer capacitance. The CAPOP=1 Meyer capacitance model is the special case of CAPOP=2 if CF1=0, CF2=0.1, and CF3=1.

In the following equations, G^- , G^+ , D^- , and D^+ are smooth factors. You cannot change the values of these parameters.

Definition: $cap = COX_{scaled} \cdot W_{eff} \cdot L_{eff}$

Gate-Bulk Capacitance (cgb)

Accumulation, $v_{gs} \leq v_{fb} - v_{sb}$: $cgb = cap$

Chapter 7: MOSFET Capacitance Models

CAPOP=2—Parameterized Modified Meyer Capacitance

$$\text{Depletion, } v_{gs} \leq v_{th}: c_{gb} = \frac{cap}{\left(1 + 4 \cdot \frac{v_{gs} + v_{sb} - v_{fb}}{GAMMA^2}\right)^{1/2}}$$

Inversion, $v_{gs} > v_{th}$:

$$c_{gb} = \frac{G^+ \cdot cap}{\left[1 + 4 \cdot \frac{GAMMA \cdot (PHI + v_{sb})^{1/2} + PHI + v_{sb}}{GAMMA^2}\right]^{1/2}}$$

These equations replace GAMMA with effective γ for model levels higher than 4.

Gate-Source Capacitance (cgs)

Low vds ($v_{ds} < 0.1$)

Accumulation, $v_{gs} < v_{th} - CF1$: $c_{gs} = CF5 \cdot cap \cdot G^- \cdot D^-$

Depletion, $v_{gs} \leq v_{th} + CF2 - CF1$:

$$c_{gs} = CF5 \cdot cap \cdot \left\{ \frac{v_{gs} - v_{th} + CF1}{CF2} \cdot \left[1 - \left(CF2 - \frac{v_{ds}}{2 \cdot CF2 - v_{ds}} \right)^2 - D^- \right] + D^- \right\}$$

Strong Inversion, $v_{gs} > v_{th} + \max(CF2 - CF1, CF3 \cdot v_{ds})$, UPDATE=0

Strong Inversion, $v_{gs} > v_{th} + CF2 - CF1$, UPDATE=1:

$$c_{gs} = CF5 \cdot cap \cdot \left\{ 1 - \left[\frac{v_{gs} - v_{th} + CF1 - v_{ds}}{2 \cdot (v_{gs} - v_{th} + CF1) - v_{ds}} \right]^2 \right\}$$

High vds

($v_{ds} \geq 0.1$)

Accumulation, $v_{gs} < v_{th} - CF1$: $c_{gs} = CF5 \cdot cap \cdot G^- \cdot D^+$, $CF1 \neq 0$

$c_{gs} = CF5 \cdot cap \cdot G^-$, $CF1 = 0$

Weak Inversion, $v_{gs} < v_{th} + CF2 - CF1$, $CF1 \neq 0$:

$$c_{gs} = CF5 \cdot cap \cdot \max\left(\frac{v_{gs} - v_{th} + CF1}{CF2}, D^+\right)$$

Saturation Region, $v_{gs} < v_{th} + CF3 \cdot v_{ds}$: $c_{gs} = CF5 \cdot cap$

Linear Region, $v_{gs} > v_{th} + CF3 \cdot v_{ds}$:

$$c_{gs} = CF5 \cdot cap \cdot \left\{ 1 - \left[\frac{v_{gs} - v_{th} - v_{ds}}{2 \cdot (v_{gs} - v_{th}) - v_{ds}} \right]^2 \right\}, \text{ UPDATE}=0, CF1=0$$

$$c_{gs} = CG5 \cdot cap \cdot \left\{ 1 - \left[\frac{v_{gs} - v_{th} - CF3 \Rightarrow v_{ds}}{2 \cdot (v_{gs} - v_{th}) - CF3 \Rightarrow v_{ds}} \right]^2 \right\}, \text{ UPDATE}=1$$

Gate-Drain Capacitance (c_{gd})

Low v_{ds}, (v_{ds} < 0.1)

Accumulation, $v_{gs} \leq v_{th} - CF1$: $c_{gd} = CF5 \cdot cap \cdot G^- \cdot D^-$

Weak Inversion, $v_{gs} < v_{th} + CF2 - CF1$:

$$c_{gd} = CF5 \cdot cap \cdot \left\{ D^- + \frac{v_{gs} - v_{th} + CF1}{CF2} \cdot \max \left[0, 1 - \left(\frac{CF2}{2 \cdot CF2 - v_{ds}} \right)^2 - D^- \right] \right\}$$

Strong Inversion, $v_{gs} \geq v_{th} + CF2 - CF1$:

$$c_{gd} = CF5 \cdot cap \cdot \max \left\{ D^-, 1 - \left[\frac{v_{gs} - v_{th} + CF1}{2 \cdot (v_{gs} - v_{th} + CF1) - v_{ds}} \right]^2 \right\}$$

High v_{ds} (v_{ds} > 0.1)

Accumulation, $v_{gs} \leq v_{th} - CF1$: $c_{gd} = CF5 \cdot cap \cdot G^- \cdot DD^+$

Saturation Region, $v_{gs} \leq v_{th} + CF3 \cdot v_{ds}$: $c_{gd} = CF5 \cdot cap \cdot DD^+$

DD^+ is a function of $CF3$, if $UPDATE=1$.

Linear Region, $v_{gs} > v_{th} + CF3 \cdot v_{ds}$:

$$c_{gd} = CF5 \cdot cap \cdot \max \left\{ DD^+, 1 - \left[\frac{v_{gs} - v_{th}}{2 \cdot (v_{gs} - v_{th}) - CF3 \Rightarrow v_{ds}} \right]^2 \right\}$$

Example

This example is based on demonstration netlist capop2.sp, which is available in directory `$installdir/demo/hspice/mos`:

Chapter 7: MOSFET Capacitance Models

CAPOP=2—Parameterized Modified Meyer Capacitance

```
*file capop2.sp capop=2 capacitances
*
*this file creates parameterized modified gate capacitances
*(capop=2) for low and high vds.
*
.options acct=2 post=2 dccap=1 nomod
.dc vgl -1 4 .01
.print dc cgb_vdsp05=par('-lx21(m1)') cgd_vdsp05=par('-
lx19(m1)')
+ cgs_vdsp05=par('-lx20(m1)')
.print dc cgb_vdsp8=par('-lx21(m2)') cgd_vdsp8=par('-lx19(m2)')
+ cgs_vdsp8=par('-lx20(m2)')
*****
m1 d1 g1 0 0 mn l=5e-6 w=20e-6 $creates capacitances for vds=0.05
m2 d2 g1 0 0 mn l=5e-6 w=20e-6 $creates capacitances for vds=0.80
*****
vd1 d1 0 dc 0.05
vd2 d2 0 dc 0.80
vgl g1 0 dc 0.0
*
*****
*
.model mn nmos ( level = 2
+ vto = 1.0 gamma = 1.40 nsub = 7.20e15
+ tox = 9.77e-8 uo = 817 ucrit = 3.04e4
+ uexp = 0.102 neff = 1.74 phi = 0.6
+ vmax = 4.59e5 cj = 0 cjsw = 0 js = 0
+ capop=2 cf1=0.15 cf2=.2 cf3=.8 cf5=.666)
.end
```

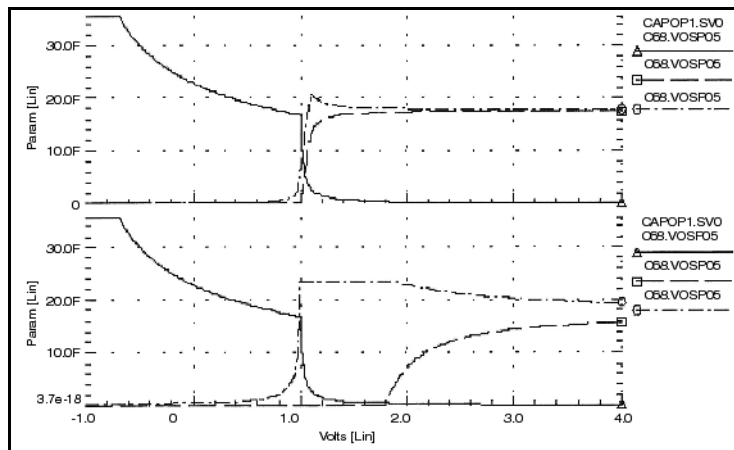


Figure 24 CAPOP=2 Capacitances

CAPOP=3 — Gate Capacitances (Simpson Integration)

The CAPOP=3 model uses the same set of equations and parameters as the CAPOP=2 model. Simulation obtains the charges using Simpson numeric integration instead of the box integration found in the CAPOP=1, 2, and 6 models.

Gate capacitances are not constant values with respect to voltages. The incremental capacitance best describes the capacitance values:

$$C(v) = \frac{dq(v)}{dv}$$

In the preceding equation, $q(v)$ is the charge on the capacitor, and v is the voltage across the capacitor.

The formula for calculating the differential is difficult to derive. Furthermore, the voltage is required as the accumulated capacitance over time. The timewise formula is:

$$i(t) = \frac{dq(v)}{dt} = C(v) \cdot \frac{dv(t)}{dt}$$

$$\text{The charge is: } q(v) = \int_0^v C(v)dv$$

$$\text{To calculate the current: } i(t) = \frac{dq(v)}{dt} = \left(\frac{d}{dt}\right) \int_0^v C(v)dv$$

$$\text{For small intervals: } I(n+1) = \frac{dq(v)}{dt} = \frac{1}{t(n+1) - t(n)} \int_{V(n)}^{V(n+1)} C(v)dv$$

In SPICE, the following equation approximates the integral:

$$I(n+1) = \left(\frac{V(n+1) - V(n)}{t(n+1) - t(n)}\right) \cdot \left(\frac{C[V(n+1)] + C[V(n)]}{2}\right)$$

This last formula is the trapezoidal rule for integration over two points. The charge is approximated as the average capacitance times the change in voltage. If the capacitance is nonlinear, this approximation can be in error. To

accurately estimate the charge, use Simpson's numerical integration rule. This method provides charge conservation control.

To use this model parameter:

- Set the `CAPOP` model parameter to 3 and use the existing `CAPOP=2` model parameters.
- Modify the `.OPTION RELV` (relative voltage tolerance), `.OPTION RELMOS` (relative current tolerance for MOSFETs), and `.OPTION CVTOL` (capacitor voltage tolerance) settings.

The default of 0.5 is a good nominal value for `CVTOL`. The `CVTOL` option uses the following equation to set the number of integration steps:

$$n = \frac{|V(n+1) - V(n)|}{CVTOL}$$

Use a large value for `CVTOL` to decrease the number of integration steps for the n to $n+1$ time interval; this yields slightly less accurate integration results. Using a small `CVTOL` value increases the computational load, sometimes severely.

CAPOP=4—Charge Conservation Capacitance Model

The charge conservation method (See “A Charge-Oriented Model for MOS Transistor,” Ward, Donald E. and Robert W. Dutton) is not implemented correctly into the SPICE2G.6 program. There are errors in the derivative of charges, especially in LEVEL 3 models. Also, the channel charge partition is not continuous from the linear region to the saturation region.

In the Synopsys MOSFET device models, these problems are corrected. If you specify the `CAPOP=4` model parameter, then simulation uses the level-dependent recommended charge conservation model. The `XQC` model parameter selects ratio of channel charge partitioning between drain/source.

For example, if you set `XQC= .4`, then in the saturation region, 40% of the channel charge is associated with the drain and the remaining 60% is associated with the source. In the linear region, the ratio is 50/50. Simulation uses an empirical equation to make a smooth transition from 50/50 (linear region) to 40/60 (saturation region).

The capacitance coefficients are the derivative of gate, bulk, drain, and source charges, and are continuous. LEVEL 2, 3, 4, 6, 7, and 13 models include a charge-conservation capacitance model. To invoke this model, set `CAPOP=4`.

The following example compares only the CAPOP=4 charge conservation capacitance and the CAPOP=9 improved charge conservation capacitance for the LEVEL 3 model. The CGS and CGD capacitances for CAPOP=4 model (SPICE2G.6) show discontinuity at the boundary between the saturation and linear regions. The CAPOP=9 model does not have discontinuity. The modified Meyer capacitances (CAPOP=2) are also provided for comparison. The shape of CGS and CGD capacitances resulting from CAPOP=9 are much closer to those of CAPOP=2.

Example

This example is based on demonstration netlist mcap3.sp, which is available in directory `$installdir/demo/hspice/mos`:

Chapter 7: MOSFET Capacitance Models

CAPOP=4—Charge Conservation Capacitance Model

```
FILE MCAP3.SP CHARGE CONSERVATION MOSFET CAPS., CAPOP=4,9 LEVEL=3
* CGGB = LX18 (M) DERIVATIVE OF QG WITH RESPECT TO VGB.
* CGDB = LX19 (M) DERIVATIVE OF QG WITH RESPECT TO VDB.
* CGSB = LX20 (M) DERIVATIVE OF QG WITH RESPECT TO VSB.
* CBGB = LX21 (M) DERIVATIVE OF QB WITH RESPECT TO VGB.
* CBDB = LX22 (M) DERIVATIVE OF QB WITH RESPECT TO VDB.
* CBSB = LX23 (M) DERIVATIVE OF QB WITH RESPECT TO VSB.
* CDGB = LX32 (M) DERIVATIVE OF QD WITH RESPECT TO VGB.
* CDDb = LX33 (M) DERIVATIVE OF QD WITH RESPECT TO VDB.
* CDSB = LX34 (M) DERIVATIVE OF QD WITH RESPECT TO VSB.
* SIX NONRECIPROCAL CAPACITANCES (CGB,CBG,CGS,CSG,CGD,AND CDG)
* ARE DERIVED FROM THE ABOVE CAPACITANCE FACTORS.
.OPTION DCCAP=1 POST NOMOD
.PARAM XQC=0.4 CAPOP=4
.DC VGG -2 5 .02
.print CGB=PAR('LX18 (M)+LX19 (M)+LX20 (M) ')
+ CBG=PAR(' -LX21 (M) ')
+ CGS=PAR(' -LX20 (M) ')
+ CSG=PAR('LX18 (M)+LX21 (M)+LX32 (M) ')
+ CGD=PAR(' -LX19 (M) ')
+ CDG=PAR(' -LX32 (M) ')
.print
+ CG =par('LX14 (M) ')
VDD D 0 2.5
VGG G 0 0
VBB B 0 -1
M D G 0 B MOS W=10U L=5U
.MODEL MOS NMOS LEVEL=3 COX=1E-4 VTO=.3 CAPOP=CAPOP
+ UO=1000 GAMMA=.5 PHI=.5 XQC=XQC
+ THETA=0.06 VMAX=1.9E5 ETA=0.3 DELTA=0.05 KAPPA=0.5 XJ=.3U
+ CGSO=0 CGDO=0 CGBO=0 CJ=0 JS=0 IS=0
*
.ALTER
.PARAM CAPOP=9
.END
```

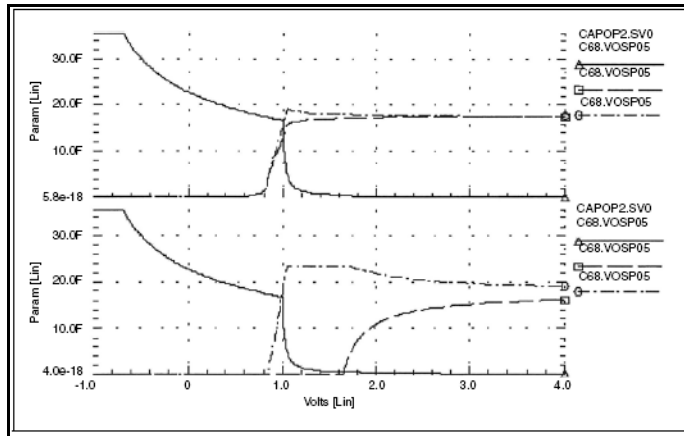


Figure 25 CAPOP=4, 9 Capacitances for LEVEL 3 Model

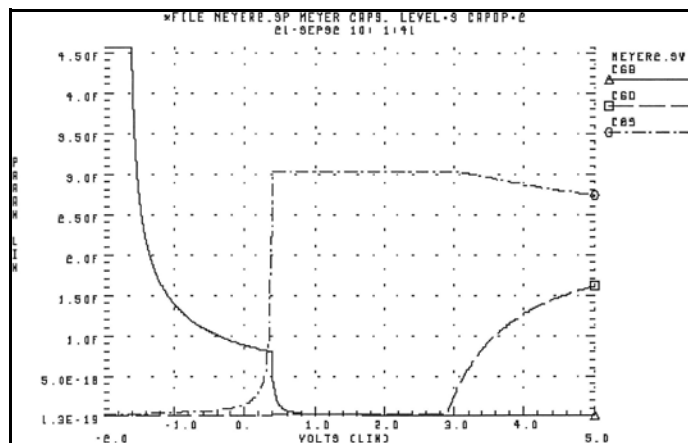


Figure 26 CAPOP=2 Capacitances for LEVEL 3 Model

The example below tests the charge conservation capacitance model (Yang, P., B.D. Epler, and P.K. Chatterjee 'An Investigation of the Charge Conservation Problem') and compares the Meyer and charge conservation models. As the graph in [Figure 28](#) shows, the charge conservation model returns more accurate results.

Example

This example is based on demonstration netlist chrgpump.sp, which is available in directory `$install_dir/demo/hspice/mos`:

Chapter 7: MOSFET Capacitance Models

CAPOP=4—Charge Conservation Capacitance Model

```

chrgpump.sp: charge conservation test for charge pump circuit
*test circuit of a mosfet capacitor and a linear capacitor
.options post acct list nomod $ method=gear
+ reltol=1e-3 abstol=1e-6 chgtol=1e-14 $ delmax=0.1ns
.param capop=2
.op
.tran 2ns 470ns sweep capop poi 2 2,9
.ic v(s)=1
*
vin g 0 pulse 0 5 15ns 5ns 5ns 50ns 100ns
vbb 0 b pulse 0 5 0ns 5ns 5ns 50ns 100ns
vdd d d- pulse 0 5 25ns 5ns 5ns 50ns 100ns
*
rc d- s 10k
c2 s 0 10p
m1 d g s b mm w=3.5u l=5.5u
+ad=100p as=100p pd=50u ps=50u nrd=1 nrs=1
*
.model mm nmos level=3 vto=0.7 kp=50e-6 gamma=0.96
+phi=0.5763 tox=50e-9 nsub=1.0e16 ld=0.5e-6
+vmax=268139 theta=0.05 eta=1 kappa=0.5 cj=1e-4
+cjsw=0.05e-9 rsh=20 js=1e-8 pb=0.7
+cgd=0 cgs=0 is=0 js=0
+capop=capop
*
.probe tran vout=v(s)
.probe tran vd=v(d) vg=v(g) vb=v(b)
.print tran v(s) v(d) v(g) v(b)
.end

```

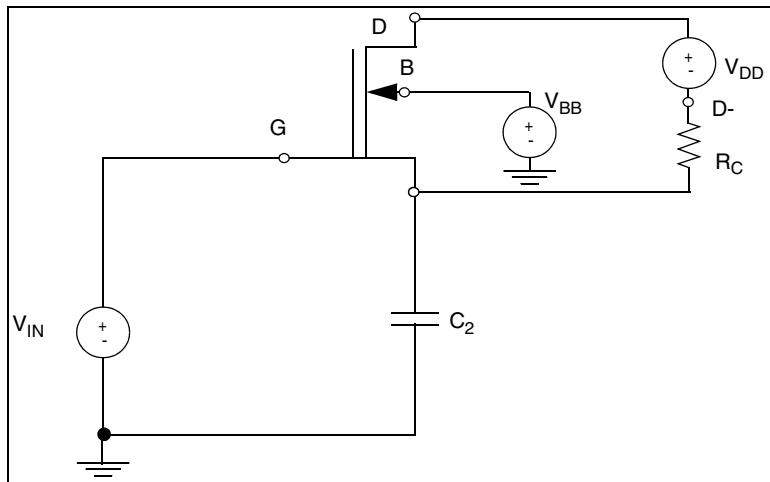


Figure 27 Charge Pump Circuit

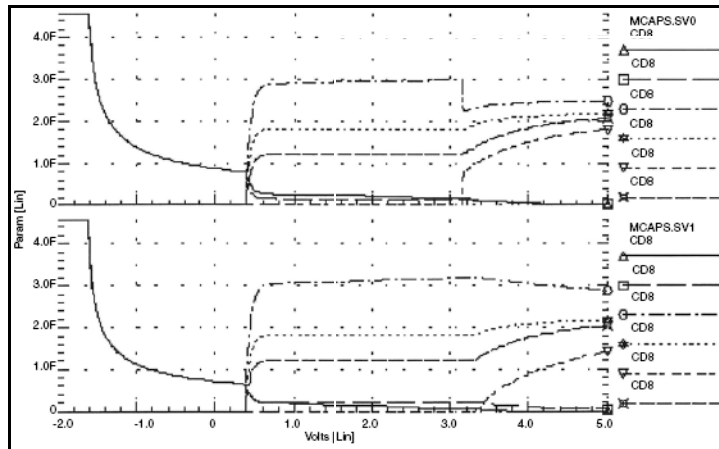


Figure 28 Charge Conservation Test: CAPOP=2 or 9

The following example applies a pulse through a constant capacitance to the gate of a MOS transistor. Ideally, if the model conserves charge, then the voltage at node 20 should become zero when the input pulse becomes zero. Consequently, the model that provides voltage closer to zero for node 20 conserves the charge better. The results of the CAPOP=4 model are better than the CAPOP=2 model.

This example compares charge conservation models in SPICE2G.6 and Synopsys device models. The results indicate that the Synopsys device models are more accurate.

Example

This example is based on demonstration netlist mcap2_a.sp, which is available in directory `$install_dir/demo/hspice/mos`:

Chapter 7: MOSFET Capacitance Models

CAPOP=5 — No Gate Capacitance

```
FILE MCAP2_A.SP
.OPTION SPICE NOMOD DELMAX=.25N POST=2
.PARAM CAPOP=4
.TRAN 1NS 40NS SWEEP CAPOP POI 2 4 2
.PRINT TRAN V(1) V(20)
VIN 1 0 PULSE (0V, 5V, 0NS, 5NS, 5NS, 5NS, 20NS)
CIN 1 20 1PF
RLEAK 20 0 1E+12
VDD 10 0 1.3
VBB 30 0 -1
M 10 20 0 30 MOS W=10U L=5U
.MODEL MOS NMOS LEVEL=2 TOX=250E-10 VTO=.3
+ UO=1000 LAMBDA=1E-3 GAMMA=.5 PHI=.5 XQC=.5
+ THETA=0.067 VMAX=1.956E5 XJ=.3U
+ CGSO=0 CGDO=0 CGBO=0
+ CJ=0 JS=0 IS=0
+ CAPOP=CAPOP
.END
```

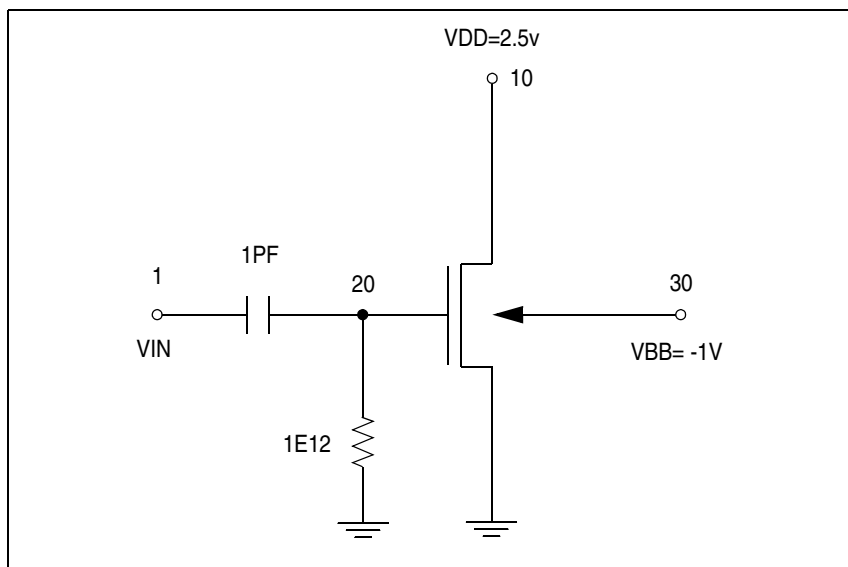


Figure 29 Charge Conservation Test Circuit

CAPOP=5 — No Gate Capacitance

If CAPOP=5 for no capacitors, then simulation does not calculate gate capacitance.

CAPOP=6 — AMI Gate Capacitance Model

Define: $vgst = vgs - \frac{(vth + vfb)}{2}$, $cox = \frac{\epsilon_{ox}}{TOX \cdot 1e-10} \cdot Weff \cdot Leff$

The following equations calculate the cgs gate capacitance in the different regions.

$0.5 \cdot (vth + vfb) > vgs$

$$cgs = 0$$

$0.5 \cdot (vth + vfb) < vgs < vth$

For $vgst < vds$: $cgs = \frac{4}{3} \cdot \frac{cox \cdot vgst}{vth - vfb}$

For $vgst > vds$: $cgs = arg \cdot \frac{4}{3} \cdot \frac{cox \cdot vgst}{vth - vfb}$

$vgs > vth$

For $vgst < vds$: $cgs = \frac{2}{3} \cdot cox$

For $vgst > vds$: $cgs = arg \cdot \frac{2}{3} \cdot cox$, $arg = vgst \cdot \frac{(3 \cdot vgst - 2 \Rightarrow vds)}{(2 \cdot vgst - vds)^2}$

The following equations calculate the cgd gate capacitance in the different regions.

$vgs < vth$

$$cgd = 0$$

$vgs > vth$ and $vgst < vds$

$$cgd = 0$$

$vgs > vth$ and $vgst > vds$

$$cgd = arg \cdot \frac{2}{3} \cdot cox, arg = (3 \cdot vgst - vds) \cdot \frac{(vgst - vds)}{(2 \cdot vgst - vds)^2}$$

The following equation combines the cgb gate capacitance with the calculation of both oxide capacitance and depletion capacitance:

$$cgb = \frac{cgbx \cdot cd}{cgbx + cd}$$

Chapter 7: MOSFET Capacitance Models

CAPOP=13 — BSIM1-based Charge-Conserving Gate Capacitance Model

Simulation calculates the oxide capacitance ($cgbx$) as:

$$cgbx = cox - cgs - cgd$$

Depletion capacitance (cd) is voltage-dependent:

$$cd = \frac{\epsilon_{si}}{wd} \cdot Weff \cdot Leff, wd = \left(\frac{2 \cdot \epsilon_{si} \cdot vc}{q \cdot NSUB} \right)^{1/2}$$

vc = The effective voltage from channel to substrate (bulk)

The following equations show vc under various conditions:

$vgs + vsb < vfb$

$$vc = 0$$

$vgs + vsb > vfb$

$$vc = vgs + vsb - vfb$$

$vgst > 0, vgs < vth, vgst < vds$

$$vc = \frac{1}{2} \cdot (vth - vfb) + \frac{3}{2} \cdot vgst + vsb$$

$vgst > 0, vgs < vth, vgst > vds$

$$vc = \frac{1}{2} \cdot (vth - vfb) + vgst + \frac{1}{2} \cdot vds + vsb$$

$vgs > vth, vgst < vds$

$$vc = vth - vfb + \frac{1}{2} \cdot vgst + vsb$$

$vgs > vth, vgst > vds$

$$vc = vth - vfb + \frac{1}{2} \cdot vds + vsb$$

CAPOP=13 — BSIM1-based Charge-Conserving Gate Capacitance Model

See [LEVEL 13 BSIM Model on page 345](#).

CAPOP=39 — BSIM2 Charge-Conserving Gate Capacitance Model

See [LEVEL 39 BSIM2 Model on page 380](#).

Calculating Effective Length and Width for AC Gate Capacitance

For some MOS processes and parameter extraction method, AC analysis might need different L_{eff} and W_{eff} values than for DC analysis. For AC gate capacitance calculations, substitute the `LDAC` and `WDAC` model parameters for `LD` and `WD` in the L_{eff} and W_{eff} calculations. You can use `LD` and `WD` in L_{eff} and W_{eff} calculations for DC current.

To use `LDAC` and `WDAC`, enter `XL`, `LD`, `LDAC`, `XW`, `WD`, and `WDAC` in the `.MODEL` statement. The model uses the following equations for DC current calculations.

$$L_{\text{eff}} = L + XL - 2 \cdot LD$$

$$W_{\text{eff}} = W + XW - 2 \cdot WD$$

The model parameters also use the following equations to calculate the AC gate capacitance:

$$L_{\text{eff}} = L + XL - 2 \cdot LDAC$$

$$W_{\text{eff}} = W + XW - 2 \cdot WDAC$$

The noise calculations use the DC W_{eff} and L_{eff} values.

Use `LDAC` and `WDAC` with the standard `XL`, `LD`, `XW`, and `WD` parameters. Do not use `LDAC` and `WDAC` with other parameters, such as `DL0` and `DW0`.

Chapter 7: MOSFET Capacitance Models

Calculating Effective Length and Width for AC Gate Capacitance

MOSFET Diode Models

This chapter discusses use of available MOSFET diode models.

HSPICE ships hundreds of examples for your use; see [Listing of Demonstration Input Files](#) for paths to demo files.

These topics are presented in the following sections:

- [Selecting MOSFET Diode Models](#)
- [Enhancing Convergence](#)
- [MOSFET Diode Model Parameters](#)
- [Using an ACM=0 MOS Diode](#)
- [Using an ACM=1 MOS Diode](#)
- [Using an ACM=2 MOS Diode](#)
- [Using an ACM=3 MOS Diode](#)
- [Using MOS Diode Capacitance Equations](#)

Selecting MOSFET Diode Models

You can use the Area Calculation Method (ACM) parameter to precisely control bulk-to-source and bulk-to-drain diodes within MOSFET models. Use the `ACM` model parameter to select one of three different modeling schemes for the MOSFET bulk diodes. This section discusses the model parameters and model equations used for the different MOSFET diode models.

To select a MOSFET diode model, set the `ACM` parameter within the MOSFET model statements.

- If $ACM=0$, the pn bulk junctions of the MOSFET are modeled in the SPICE style.
- The $ACM=1$ diode model is the original ASPEC model.
- The $ACM=2$ model parameter specifies the improved diode model, which is based on a model similar to the ASPEC MOSFET diode model.
- The $ACM=3$ diode model is a further improvement that deals with capacitances of shared sources and drains, and gate edge source/drain-to-bulk periphery capacitance.
- If you do not set the ACM model parameter, the diode model defaults to the $ACM=0$ model.
- If $ACM=0$ and $ACM=1$ models, you cannot specify $HDIF$. In the $ACM=0$ model, you cannot specify $LDIF$. The $ACM=1$ model does not use the AD , AS , PD , and PS geometric element parameters.

Enhancing Convergence

- The $GMIN$ option creates a parallel conductance across the bulk diodes and drain-source for transient analysis.
- The $GMINDC$ option creates a parallel conductance across the bulk diodes and drain-source for DC analysis.

These options enhance the convergence properties of the diode model, especially when the model has a high off resistance. Use the RSH , RS , and RD parameters to prevent over-driving the diode in either a DC or transient forward bias condition. These parameters also enhance the convergence properties of the diode model.

MOSFET Diode Model Parameters

Table 215 DC Model Parameters

Name (Alias)	Units	Default	Description
ACM		0	Area calculation method
JS	amp/m ²	0	Bulk junction saturation current: JSscaled=JS/SCALM2 – for ACM=1 unit is amp/m and JSscaled=JS/SCALM.
JSW	amp/m	0	Sidewall bulk junction saturation current: JSWscaled=JSW/SCALM.
IS	amp	1e-14	Bulk junction saturation current. For the ASPEC=1 option, default=0.
N		1	Emission coefficient.
NDS		1	Reverse bias slope coefficient.
VNDS	V	-1	Reverse diode current transition point.

Table 216 Capacitance Model Parameters

Name (Alias)	Units	Default	Description
CBD	F	0	Zero bias bulk-drain junction capacitance. Used only when CJ and CJSW are 0.
CBS	F	0	Zero bias bulk-source junction capacitance. Use only when CJ and CJSW are 0.

Table 216 Capacitance Model Parameters

Name (Alias)	Units	Default	Description
CJSW (CJP)	F/m	0	Zero-bias sidewall bulk junction capacitance. CJSWscaled = CJSW/SCALM. Default = 0.
CJ (CDB, CSB, CJA)	F/m ²	579.11 μF/m ²	Zero-bias bulk junction capacitance: <ul style="list-style-type: none"> ▪ CJscaled = CJ/SCALM2 —for ACM=1 the unit is F/m. ▪ CJscaled = CJ/SCALM. Default for the ASPEC=0 option is: $CJ = \left(\frac{\epsilon_{si} \cdot q \cdot NSUB}{2 \cdot PB} \right)^{1/2}$
CJGATE	F/m	CJSW	Zero-bias gate-edge sidewall bulk junction capacitance (ACM=3 only). CJGATEscaled=CJGATE/SCALM <ul style="list-style-type: none"> ▪ Default = CJSW for Hspice releases later than H9007D. ▪ Default = 0 for HSPICE releases H9007D and earlier, or if you do not specify CJSW.
FC		0.5	Forward-bias depletion capacitance coefficient (not used).
MJ (EXA, EXJ, EXS, EXD)		0.5	Bulk junction grading coefficient.
MJSW (EXP)		0.33	Bulk sidewall junction grading coefficient.
NSUB (DNB, NB)	1/cm ³	1.0e15	Substrate doping.
PB (PHA, PHS, PHD)	V	0.8	Bulk junction contact potential.
PHP	V	PB	Bulk sidewall junction contact potential.
TT	s	0	Transit time

Table 217 Drain and Source Resistance Model Parameters

Name (Alias)	Units	Default	Description
RD	ohm/sq	0.0	Drain ohmic resistance. This parameter is usually the sheet resistance of a lightly-doped region for $ACM \geq 1$.
RDC	ohm	0.0	Additional drain resistance due to contact resistance.
LRD	ohm/m	0	Drain resistance length sensitivity. Use this parameter with automatic model selection, WRD, and PRD to factor a model for the device size.
WRD	ohm/m	0	Drain resistance width sensitivity (used with LRD).
PRD	ohm/m ²	0	Drain resistance product (area) sensitivity (used with LRD).
RS	ohm/sq	0.0	Source ohmic resistance. This parameter is usually the sheet resistance of a lightly-doped region for $ACM \geq 1$.
LRS	ohm/m	0	Source resistance length sensitivity. Use this parameter with automatic model selection, WRS, and PRS to factor a model for the device size.
WRS	ohm/m	0	Source resistance width sensitivity (used with LRS).
PRS	ohm/m ²	0	Source resistance product (area) sensitivity (used with LRS).
RSC	ohm	0.0	Source resistance due to contact resistance.
RSH (RL)	ohm/sq	0.0	Drain and source diffusion sheet resistance.

Chapter 8: MOSFET Diode Models

Using an ACM=0 MOS Diode

Table 218 Using MOS Geometry Model Parameters

Name (Alias)	Units	Default	Description
HDIF	m	0	Length of heavily-doped diffusion, from contact to lightly-doped region (ACM=2, 3 only): $HDIF_{scaled} = HDIF \cdot SCALM$
LD (DLAT,LATD)	m		Lateral diffusion into the channel from the source and drain diffusion. <ul style="list-style-type: none">▪ If you do not specify LD and XJ, LD default=0.0.▪ If you specify LD, but you do not specify XJ, then simulation calculates LD from XJ. Default=$0.75 \cdot XJ$.▪ For LEVEL 4 only, lateral diffusion is derived from LD \cdot XJ. $LD_{scaled} = LD \cdot SCALM$
LDIF	m	0	Length of lightly-doped diffusion adjacent to the gate (ACM=1, 2): $LDIF_{scaled} = LDIF \cdot SCALM$
WMLT		1	Width diffusion layer shrink reduction factor.
XJ	m	0	Metallurgical junction depth: $XJ_{scaled} = XJ \cdot SCALM$
XW (WDEL, DW)	m	0	Accounts for masking and etching effects: $XW_{scaled} = XW \cdot SCALM$

Using an ACM=0 MOS Diode

Figure 30 shows the parameter value settings for a MOSFET diode, designed with a MOSFET that has a channel length of 3 μm and a channel width of 10 μm .

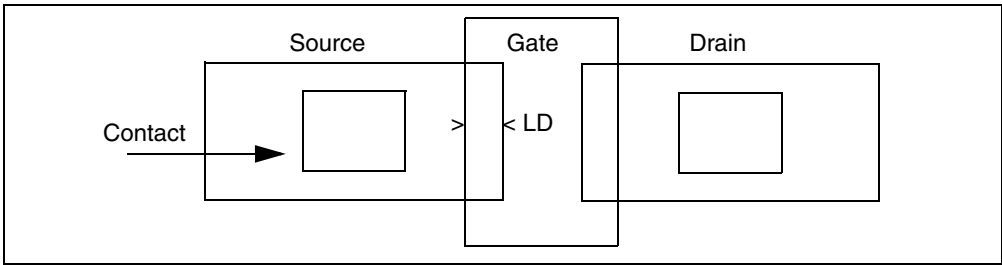


Figure 30 ACM=0 MOS Diode

Example

A transistor might include:

LD= .5mm W=10mm L=3mm

Parameter	Description
AD	area of drain (about 80 pm ²)
AS	area of source (about 80 pm ²)
CJ	4e-4 F/m ²
CJSW	1e-10 F/m
JS	1e-8 A/m ²
JSW	1e-13 A/m
NRD	number of squares for drain resistance
NRS	number of squares for source resistance
PD	sidewall of drain (about 36 μm)
PS	sidewall of source (about 36 μm)

Calculating Effective Areas and Peripheries

For ACM=0, simulation calculates the effective areas and peripheries as follows:

Chapter 8: MOSFET Diode Models

Using an ACM=0 MOS Diode

$$A_{Deff} = M \cdot AD \cdot WMLT^2 \cdot SCALE^2$$

$$A_{Seff} = M \cdot AS \cdot WMLT^2 \cdot SCALE^2$$

$$P_{Deff} = M \cdot PD \cdot WMLT \cdot SCALE$$

$$P_{Seff} = M \cdot PS \cdot WMLT \cdot SCALE$$

Calculating Effective Saturation Current

For $ACM=0$, simulation calculates the MOS diode effective saturation currents as follows:

Source Diode Saturation Current

Define: $val = JSscaled \cdot A_{Seff} + JSWscaled \cdot P_{Seff}$

If $val > 0$, then $isbs = val$

Otherwise, $isbd = M \cdot IS$

Drain Diode Saturation Current

Define: $val = JSscaled \cdot A_{Deff} + JSWscaled \cdot P_{Deff}$

If $val > 0$, then $isbd = val$

Otherwise, $isbd = M \cdot IS$

Calculating Effective Drain and Source Resistances

For $ACM=0$, simulation calculates the effective drain and source resistances as follows:

Source Resistance

Define: $val = NRS \cdot RSH$

If $val > 0$, then $R_{Seff} = \frac{val + RSC}{M}$

Otherwise, $R_{Seff} = \frac{RS + RSC}{M}$

Drain Resistance

Define: $val = NRD \cdot RSH$

If $val > 0$, then $RDeff = \frac{val + RDC}{M}$

Otherwise, $RDeff = \frac{RD + RDC}{M}$

Using an ACM=1 MOS Diode

If you specify the $ACM=1$ model parameter, simulation uses ASPEC-style diodes, and does not use the AD , PD , AS , and PS parameters. The JS and CJ units differ from SPICE-style diodes ($ACM=0$).

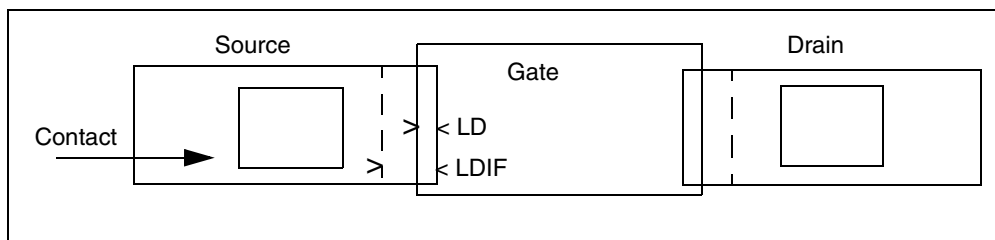


Figure 31 ACM=1 MOS Diode

Example

Table 30 lists parameter value settings for a transistor with the following parameter values:

- $LD=0.5 \mu m$
- $W=10 \mu m$

Chapter 8: MOSFET Diode Models

Using an ACM=1 MOS Diode

- $L=3\ \mu\text{m}$
- $LDIF=0.5\ \mu\text{m}$

Table 219 ACM=0 MOS Diode Parameters

Parameter	Description
CJ	1e-10 F/m of gate width Note the change from F/m ² (in ACM=0) to F/m.
CJSW	2e-10 F/m of gate width
JS	1e-14 A/m of gate width Note the change from A/m ² (in ACM=0) to A/m
JSW	1e-13 A/m of gate width
NRD	number of squares for drain resistance
NRS	number of squares for source resistance

Calculating Effective Areas and Peripheries

For ACM=1, simulation calculates the effective areas and peripheries as follows:

$$AD_{eff} = W_{eff} \cdot WMLT$$

$$AS_{eff} = W_{eff} \cdot WMLT$$

$$PD_{ff} = W_{eff}$$

$$PS_{eff} = W_{eff}$$

The following equation calculates the W_{eff} value used in the preceding equations:

$$W_{eff} = M \cdot (W_{scaled} \cdot WMLT + XW_{scaled})$$

Note: The W_{eff} value is not the same as the w_{eff} value in the LEVEL 1, 2, 3, 6, and 13 models. The $2 \cdot WD_{scaled}$ term is not subtracted.

Calculating Effective Saturation Current

For ACM=1, the MOS diode effective saturation currents are calculated as follows:

Source Diode Saturation Current

Define: $val = JSscaled \cdot ASeff + JSWscaled \cdot PSeff$

If $val > 0$, then $isbs = val$

Otherwise, $isbs = M \cdot IS$

Drain Diode Saturation Current

Define: $val = JSscaled \cdot ADeff + JSWscaled \cdot PDeff$

If $val > 0$, then $isbd = val$

Otherwise, $isbd = M \cdot IS$

Calculating Effective Drain and Source Resistances

For ACM=1, simulation calculates the effective drain and source resistances as follows.

Source Resistance

For UPDATE=0:

$$RSeff = \frac{LDscaled + LDIFscaled}{Weff} \cdot RS + \frac{NRS \cdot RSH + RSC}{M}$$

If UPDATE ≥ 1, LDIF=0, and you specify the ASPEC option, then:

$$RSeff = \frac{1}{M} \cdot (RS + NRS \cdot RSH + RSC)$$

Drain Resistance

For UPDATE=0:

$$RDeff = \frac{LDscaled + LDIFscaled}{Weff} \cdot RD + \frac{NRD \cdot RSH + RDC}{M}$$

If UPDATE ≥ 1, LDIF=0, and you specify the ASPEC option, then:

$$RDeff = \frac{1}{M} \cdot (RD + NRD \cdot RSH + RDC)$$

See [LEVEL 6/LEVEL 7 IDS: MOSFET Model on page 96](#) and [LEVEL 7 IDS Model on page 125](#) for more possibilities.

Using an ACM=2 MOS Diode

If you set the `ACM=2` model parameter, simulation uses HSPICE-style MOS diodes. You can use a fold-back calculation scheme similar to the ASPEC method, retaining full model-parameter compatibility with the SPICE procedure. This method also supports both lightly-doped and heavily-doped diffusions (the `LD`, `LDIF`, and `HDIF` parameters set the diffusion type). This model preserves the `JS`, `JSW`, `CJ`, and `CJSW` units (used in SPICE) for full compatibility.

`ACM=2` automatically generates more-reasonable diode parameter values than those for `ACM=1`. You can generate the `ACM=2` geometry in either of two ways:

- `AD`, `AS`, `PD`, and `PS` element parameters in the element statement generate parasitics. These parameters do not have default option values.
- To suppress the diode, set `IS=0`, `AD=0`, and `AS=0`.

If you set `AS=0` in the element and `IS=0` in the model, simulation suppresses the source diode. Use this setting for shared contacts.

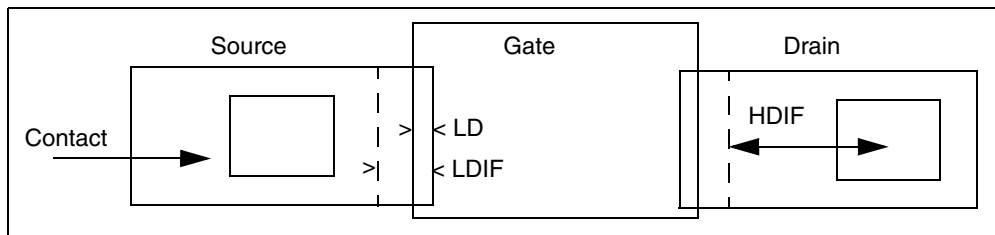


Figure 32 ACM=2 MOS Diode

Example

For a transistor with `LD=0.07μm`, `W=10μm`, `L=2μm`, `LDIF=1μm`, and `HDIF=4μm`. [Table 220](#) shows typical MOSFET diode parameter values.

Table 220 ACM=2 MOS Diode Parameters

Parameter	Description
<code>AD</code>	Area of drain. Default option value for <code>AD</code> is not applicable.

Table 220 ACM=2 MOS Diode Parameters

Parameter	Description
AS	Area of source. Default option value for AS is not applicable.
CJ	1e-4 F/m ²
CJSW	1e-10 F/m
JS	1e-4 A/m ²
JSW	1e-10 A/m
HDIF	Length of heavily-doped diffusion contact-to-gate (about 2 μm). HDIFeff=HDIF · WMLT · SCALM
LDIF+LD	Length of lightly-doped diffusion (about 0.4μm).
NRD	Number of squares drain resistance. Default value for NRD does not apply.
NRS	Number of squares source resistance. Default for NRS does not apply.
PD	Periphery of drain, including gate width for ACM=2. No default.
PS	Periphery of source, including gate width for ACM=2. No default.
RD	Resistance (ohm/square) of lightly-doped drain diffusion (about 2000).
RS	Resistance (ohm/square) of lightly-doped source diffusion (about 2000).
RSH	Diffusion sheet resistance (about 35).

Calculating Effective Areas and Peripheries

For ACM=2, simulation calculates the effective areas and peripheries as follows:

Chapter 8: MOSFET Diode Models

Using an ACM=2 MOS Diode

- If you do not specify AD , then $AD_{eff} = 2 \cdot HDIF_{eff} \cdot W_{eff}$
Otherwise, $AD_{eff} = M \cdot AD \cdot WMLT^2 \cdot SCALE^2$
- If you do not specify AS , then $AS_{eff} = 2 \cdot HDIF_{scaled} \cdot W_{eff}$
Otherwise, $AS_{eff} = M \cdot AS \cdot WMLT^2 \cdot SCALE^2$
- If you do not specify PD , then $PD_{eff} = M \cdot (4 \cdot HDIF_{eff} + 2 \cdot W_{eff})$
Otherwise, $PD_{eff} = M \cdot PD \cdot WMLT \cdot SCALE$
- If you do not specify PS , then $PS_{eff} = M \cdot (4 \cdot HDIF_{eff} + 2 \cdot W_{eff})$
Otherwise, $PS_{eff} = M \cdot PS \cdot WMLT \cdot SCALE$

The following equations calculate values used in the preceding equation:

$$W_{eff} = W_{scaled} \cdot WMLT + XW_{scaled}$$

$$HDIF_{eff} = HDIF_{scaled}$$

$$HDIF_{scaled} = HDIF \cdot SCALM \cdot WMLT$$

The W_{eff} value is not the same as the W_{eff} value in the LEVEL 1, 2, 3, and 6 models. The $2 \cdot WD_{scaled}$ term is not subtracted.

Calculating Effective Saturation Currents

For ACM=2, simulation calculates the MOS diode effective saturation currents as follows.

Source Diode Saturation Current

Define: $val = JS_{scaled} \cdot AS_{eff} + JSW_{scaled} \cdot PS_{eff}$

If $val > 0$, then $isbs = val$

Otherwise, $isbs = M \cdot IS$

Drain Diode Saturation Current

Define: $val = JS_{scaled} \cdot AD_{eff} + JSW_{scaled} \cdot PD_{eff}$

If $val > 0$, then $isbd = val$

Otherwise, $isbd = M \cdot IS$

Calculating Effective Drain and Source Resistances

For $ACM=2$, simulation calculates the effective drain and source resistances as follows.

Source Resistance

If you specify NRS , then:

$$R_{Seff} = \frac{LD_{scaled} + LDIF_{scaled}}{W_{eff}} \cdot RS + \left(\frac{NRS \cdot RSH + RSC}{M} \right)$$

Otherwise:

$$R_{Seff} = \frac{RSC}{M} + \frac{HDIF_{eff} \cdot RSH + (LD_{scaled} + LDIF_{scaled}) \cdot RS}{W_{eff}}$$

Drain Resistance

If you specify NRD , then:

$$R_{Deff} = \frac{LD_{scaled} + LDIF_{scaled}}{W_{eff}} \cdot RD + \left(\frac{NRD \cdot RSH + RDC}{M} \right)$$

Otherwise:

$$R_{Deff} = \frac{RDC}{M} + \frac{HDIF_{eff} \cdot RSH + (LD_{scaled} + LDIF_{scaled}) \cdot RD}{W_{eff}}$$

Using an ACM=3 MOS Diode

Use $ACM=3$ to properly model MOS diodes of stacked devices. You can also use the $CJGATE$ parameter to model the drain and source periphery capacitances separately, along the gate edge. Therefore, the PD and PS calculations do not include the gate periphery length. $CJGATE$ defaults to the $CJSW$ value, which in turn defaults to 0.

The AD , AS , PD , and PS calculations depend on the device layout as determined by the value of the GEO element parameter. You can specify the following GEO values in the MOS element description:

- $GEO=0$: other devices do not share the drain and source of the device (default).
- $GEO=1$: another device shares the drain.

Chapter 8: MOSFET Diode Models

Using an ACM=3 MOS Diode

- GEO=2: another device shares the source.
- GEO=3: another device shares the drain and source.

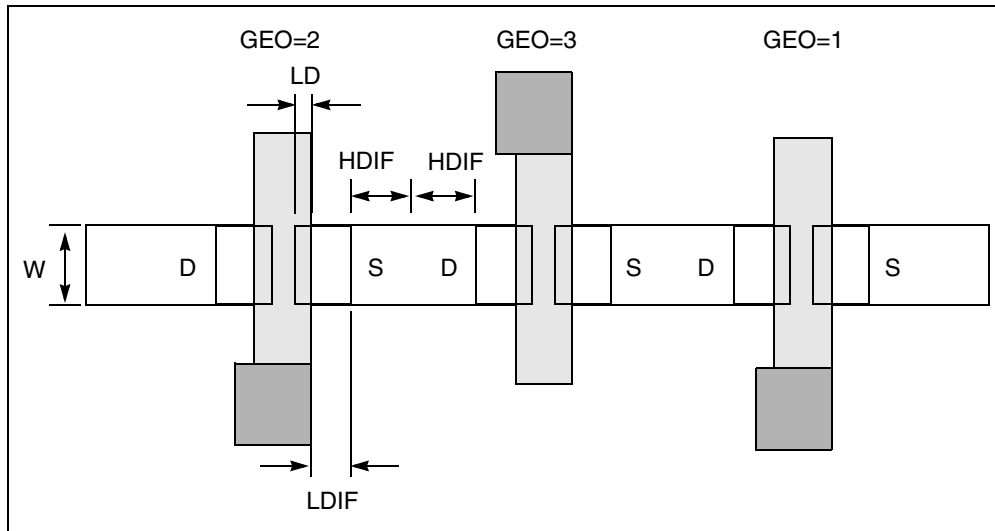


Figure 33 Stacked Devices and Corresponding GEO Values

Calculating Effective Areas and Peripheries

ACM=3 calculates the effective areas and peripheries based on the GEO value.

- If you do not specify AD, then:
 - For GEO=0 or 2, $AD_{eff} = 2 \cdot HDIF_{eff} \cdot W_{eff}$
 - For GEO=1 or 3, $AD_{eff} = HDIF_{eff} \cdot W_{eff}$
 - Otherwise, $AD_{eff} = M \cdot AD \cdot WMLT^2 \cdot SCALE^2$
- If you do not specify AS, then:
 - For GEO=0 or 1, $AS_{eff} = 2 \cdot HDIF_{eff} \cdot W_{eff}$
 - For GEO=2 or 3, $AS_{eff} = HDIF_{eff} \cdot W_{eff}$
 - Otherwise, $AS_{eff} = M \cdot AS \cdot WMLT^2 \cdot SCALE^2$
- If you do not specify PD, then:
 - For GEO=0 or 2, $PD_{eff} = 4 \cdot HDIF_{eff} + W_{eff}$

- For $GEO=1$ or 3 , $PD_{eff} = 2 \cdot HDIF_{eff}$
- Otherwise, $PD_{eff} = M \cdot PD \cdot WMLT \cdot SCALE$
- If you do not specify PS , then:
 - For $GEO=0$ or 1 , $PS_{eff} = 4 \cdot HDIF_{eff} + W_{eff}$
 - For $GEO=2$ or 3 , $PS_{eff} = 4 \cdot HDIF_{eff}$
 - Otherwise, $PS_{eff} = M \cdot PS \cdot WMLT \cdot SCALE$

Simulation calculates W_{eff} and $HDIF_{eff}$ as follows:

$$W_{eff} = M \cdot (W_{scaled} \cdot WMLT + XW_{scaled})$$

$$HDIF_{eff} = HDIF_{scaled} \cdot WMLT$$

Note: The W_{eff} value is not the same as the W_{eff} value in the LEVEL 1, 2, 3, and 6 models. The $2 \cdot WD_{scaled}$ term is not subtracted.

Effective Saturation Current Calculations

The $ACM=3$ model calculates the MOS diode effective saturation currents the same as $ACM=2$.

Effective Drain and Source Resistances

The $ACM=3$ model calculates the effective drain and source resistances the same as $ACM=2$.

MOS Diode Equations

This section describes MOS diode equations.

DC Current

- Simulation parallels the drain and source MOS diodes with G_{MINDC} conductance in the DC analysis.
- Simulation parallels the drain and source MOS diodes with G_{MIN} conductance in the transient analysis.

The total DC current is the sum of the diode current and the conductance current. The diode current is calculated as follows.

Drain and Source Diodes Forward Biased

- $v_{bs} > 0$: $i_{bs} = i_{sbs} \cdot (e^{v_{bs}/(N \cdot v_t)} - 1)$
- $v_{bd} > 0$: $i_{bd} = i_{sbd} \cdot (e^{v_{bd}/(N \cdot v_t)} - 1)$

Drain and Source Diodes Reverse Biased

- For $0 > v_{bs} > V_{NDS}$: $i_{bs} = g_{sbs} \cdot v_{bs}$
- For $v_{bs} < V_{NDS}$: $i_{bs} = g_{sbs} \cdot V_{NDS} + \left(\frac{g_{sbs}}{NDS}\right) \cdot (v_{bs} - V_{NDS})$
- For $0 > v_{bd} > V_{NDS}$: $i_{bd} = g_{sbd} \cdot v_{bd}$
- For $v_{bd} < V_{NDS}$: $i_{bd} = g_{sbd} \cdot V_{NDS} + \left(\frac{g_{sbd}}{NDS}\right) \cdot (v_{bd} - V_{NDS})$

The following equations calculate values used in the preceding equations:

$$|g_{sbs}| = |i_{sbs}| \text{ and } |g_{sbd}| = |i_{sbd}|$$

Using MOS Diode Capacitance Equations

Each MOS diode capacitance is the sum of diffusion and depletion capacitance. Simulation evaluates the diffusion capacitance in terms of the small signal conductance of the diode and a τ_T model parameter, representing the transit time of the diode. The depletion capacitance depends on which ACM you choose.

To calculate bias-dependent depletion capacitance, define C_{0BS} , C_{0BD} , C_{0BS_SW} , and C_{0BD_SW} intermediate quantities. These depend on geometric parameters, such as AS_{eff} and PS_{eff} , calculated under various ACM specifications.

For $ACM=3$, the $C0BS_SW$ and $C0BD_SW$ intermediate quantities include an extra term to account for $CJGATE$.

$ACM=2$ includes the $CJGATE$ parameter for backward compatibility. Therefore, the default behavior of $CJGATE$ makes the $C0BS_SW$ and $C0BD_SW$ intermediate quantities the same as for previous versions. The default patterns are:

- If you do not specify $CJSW$ or $CJGATE$, both default to zero.
- If you do not specify $CJGATE$, it defaults to $CJSW$, which defaults to zero.
- If you specify $CJGATE$, but you do not specify $CJSW$, then $CJSW$ defaults to zero.

Simulation calculates the $C0BS$, $C0BS_SW$, $C0BD$, and $C0BD_SW$ intermediate quantities as follows.

```
C0BS = CJscaled*ASeff
C0BD = CJscaled*ADeff
```

- If ($ACM=0$ or 1), then:

```
C0BS_SW = CJSWscaled*PSeff
C0BD_SW = CJSWscaled*PDeff
```

- If ($ACM=2$) and ($PS_{eff} < W_{eff}$), then:

```
C0BS_SW = CJGATEscaled*PSeff
```

- If ($ACM=2$) and ($PS_{eff} > W_{eff}$), then:

```
C0BS_SW = CJSWscaled*(PSeff-Weff) + CJGATEscaled*Weff
```

- If ($ACM=2$) and ($PD_{eff} < W_{eff}$), then:

```
C0BD_SW = CJGATEscaled*PDeff
```

- If ($ACM=2$) and ($PD_{eff} > W_{eff}$), then:

```
C0BD_SW = CJSWscaled*(PDeff-Weff) + CJGATEscaled*Weff
```

- If ($ACM=3$), then:

```
C0BS_SW = CJSWscaled*PSeff + CJGATEscaled*Weff
C0BD_SW = CJSWscaled*PDeff + CJGATEscaled*Weff
```

Source Diode Capacitance

- If $(C0BS + C0BS_SW) > 0$ and $vbs < 0$, then:

$$capbs = TT \cdot \frac{\partial ibs}{\partial vbs} + C0BS \cdot \left(1 - \frac{vbs}{PB}\right)^{-MJ} \\ + C0BS_SW \cdot \left(1 - \frac{vbs}{PHP}\right)^{-MJSW}$$

If $(C0BS + C0BS_SW) > 0$ and $vbs > 0$, then:

$$capbs = TT \cdot \frac{\partial ibs}{\partial vbs} + C0BS \cdot \left(1 + MJ \cdot \frac{vbs}{PB}\right) \\ + C0BS_SW \cdot \left(1 + MJSW \cdot \frac{vbs}{PHP}\right)$$

Otherwise, if $(C0BS + C0BS_SW) \leq 0$, then:

For $vbs < 0$: $capbs = TT \cdot \frac{\partial ibs}{\partial vbs} + M \cdot CBS \cdot \left(1 - \frac{vbs}{PB}\right)^{-MJ}$

For $vbs > 0$: $capbs = TT \cdot \frac{\partial ibs}{\partial vbs} + M \cdot CBS \cdot \left(1 + MJ \cdot \frac{vbs}{PB}\right)$

Drain Diode Capacitance

If $(C0BD + C0BD_SW) > 0$, then:

$$capbd = TT \cdot \frac{\partial ibd}{\partial vbd} + C0BD \cdot \left(1 - \frac{vbd}{PB}\right)^{-MJ} \\ + PDeff \cdot C0BD_SW \cdot \left(1 - \frac{vbd}{PHP}\right)^{-MJSW}$$

For $vbd < 0$:

$$capbd = TT \cdot \frac{\partial ibd}{\partial vbd} + C0BD \cdot \left(1 + MJ \cdot \frac{vbd}{PB}\right) \\ + C0BD_SW \cdot \left(1 + MJSW \cdot \frac{vbd}{PHP}\right)$$

For $vbd > 0$:

Otherwise, if $(AD_{eff} \cdot CJ_{scaled} + PD_{eff} \cdot CJSW_{scaled}) \leq 0$, then:

$$\text{For } v_{bd} < 0: c_{apbd} = TT \cdot \frac{\partial i_{bd}}{\partial v_{bd}} + M \cdot CBD \cdot \left(1 - \frac{v_{bd}}{PB}\right)^{-MJ}$$

$$\text{For } v_{bd} > 0: c_{apbd} = TT \cdot \frac{\partial i_{bd}}{\partial v_{bd}} + M \cdot CBD \cdot \left(1 + MJ \cdot \frac{v_{bd}}{PB}\right)$$

Chapter 8: MOSFET Diode Models

MOS Diode Equations

CMC MOS Varactor Model (Level 7)

This chapter discusses use of CMC MOSFET resistor varactor models.

HSPICE ships hundreds of examples for your use; see [Listing of Demonstration Input Files](#) for paths to demo files.

These topics are presented in the following sections:

- [Overview: CMC Varactor Model \(Level 7\)](#)
- [Model Parameters: CMC Varactor Model \(Level 7\)](#)

Overview: CMC Varactor Model (Level 7)

The MOS varactor compact model is based in part on the PSP MOSFET model and is intended for analog and RF-design. It includes dynamic inversion, finite poly doping, quantum mechanics, tunneling currents, and parasitics to model advanced MOS technologies.

The CMC MOS varactor model is Level 7 in the Synopsys models. To use this model, specify:

```
cXXX g [bi] b cmname w=1u l=1u
.MODEL cmname c LEVEL=7
```

General Syntax for CMC MOS varactor Model, Version 1.1, Version 1.0, Revision 0.8

The general syntax for a CMC MOS varactor Model element in a netlist is:

```
cXXX g [bi] b cname [L=val] [W=val]
+ [M=val] [M_SEG=val] [NGCON=val>] [DTA=val]
```

Model Parameters: CMC Varactor Model (Level 7)

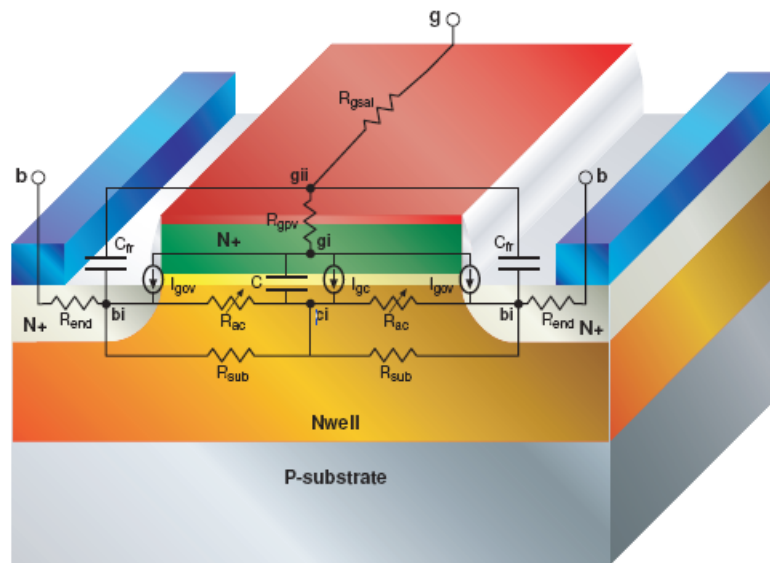


Figure 34 Cross-section of MOS varactor with equivalent circuit model overlapped

In Figure 34, **g**, **bi** and **b** are the external terminals while **gii**, **gi** and **ci** are the internal nodes

The following section describes the PSP-based varactor model parameter set.

Model Parameters: CMC Varactor Model (Level 7)

Table 221 and Table 223 describe instance and model parameters, respectively.

Table 221 Instance Parameters

Name	Units	Default	Min.	Max.	Description
L	m	10^{-6}	0	-	Design length of a varactor
W	m	10^{-6}	0	-	Design width of a varactor
m		1	0	-	Multiplicity factor
M_SEG		1	1	-	Number of gate segments

Table 221 Instance Parameters (Continued)

Name	Units	Default	Min.	Max.	Description
NGCON		1	1	2	Number of gate contacts
DTA	°C	0	-	-	Local temperature offset with respect to ambient circuit temperature

Table 222 Special Model Parameters

Name	Units	Default	Min.	Max.	Description
version		1	N/A	N/A	Model version
TMIN	°C	-100	-250	27	Minimum ambient temperature
TMAX	°C	500	27	1000	Maximum ambient temperature

Table 223 Model Parameters

Name	Units	Default	Min.	Max.	Description
TR	°C	21	-250	1000	Nominal (reference) temperature
LMIN	m	10^{-8}	0	-	Minimum allowed drawn length
LMAX	m	$9.9 \cdot 10^{-8}$	0	-	Maximum allowed drawn length
WMIN	m	10^{-8}	0	-	Minimum allowed drawn width
WMAX	m	$9.9 \cdot 10^{-8}$	0	-	Maximum allowed drawn width
TOXO	m	$2 \cdot 10^{-9}$	$5 \cdot 10^{-10}$	$2 \cdot 10^{-8}$	Oxide thickness
VFBO	V	-1	-	-	Flat-band voltage ¹
NSUBO	m ⁻³	$3 \cdot 10^{23}$	10^{22}	10^{25}	Substrate doping level
MNSUBO		1	1	10	Maximum change in absolute doping, limited to 1 order of magnitude up

Chapter 9: CMC MOS Varactor Model (Level 7)

Model Parameters: CMC Varactor Model (Level 7)

Table 223 Model Parameters (Continued)

Name	Units	Default	Min.	Max.	Description
DNSUBO		0	0	100	Doping profile slope parameter
VNSUBO		0	-5	5	Doping profile corner voltage parameter
NSLPO		0.1	0.1	1	Doping profile smoothing parameter
DLQ	m	0	-	-	Length delta for capacitor size
DWQ	m	0	-	-	Width delta for capacitor size
DWR	m	0	-	-	Width delta for substrate resistance calculation
CFRL	F/m	0	0	-	Fringing capacitance in length direction
CFRW	F/m	0	0-		Fringing capacitance in width direction
RSHG	Ω/sq	1	0	-	Gate sheet resistance
RPV	$\Omega \cdot m^2$	0	0	-	Vertical resistance down through gate
REND	$\Omega \cdot m$	10^{-4}	0	-	End resistance (extrinsic well resistance plus vertical contact resistance to well) per width
RSHS	Ω/sq	1000	0	-	Substrate sheet resistance
UAC	$m^2/\text{V} \cdot s$	$5 \cdot 10^{-2}$	0	-	Accumulation layer zero-bias mobility
UACRED	V^{-1}	0	0	-	Accumulation layer mobility degradation factor
STVFB	V/K	0	-	-	Temperature dependence of V_{fb}
STRSHG		0	-	-	Temperature dependence of R_{shg}
STRPV		0	-	-	Temperature dependence of R_{pv}
STREND		0	-	-	Temperature dependence of R_{end}
STRSHS		0	-	-	Temperature dependence of R_{shs}

Table 223 Model Parameters (Continued)

Name	Units	Default	Min.	Max.	Description
STUAC		0	-	-	Temperature dependence of U_{ac}
FETA		1.0	0	-	Effective field parameter
Switch or switch-like parameters					
SWRES		1	0	1	Switch to control series resistance: 0: exclude 1: include
TYPE		-1	-1	1	Substrate doping type: -1: n-type +1: p-type
TYPEP		-1	-1	1	Polysilicon doping type: -1: ntype +1! p-type
TAU	s	0.1	0	10	Time constant for inversion charge recombination/generation
NPO	m^{-3}	10^{27}	10^{24}	10^{27}	Polysilicon doping level
QMC		1	0	-	Quantum mechanical correction factor
SWIGATE		0	0	1	Flag for gate current: 0: turn off 1: turn on
Additional model parameters for modeling gate tunneling currents					
CHIBO	V	3.1	1.0	-	Tunneling barrier height for electrons
CHIBPO	V	4.5	1.0	-	Tunneling barrier height for holes
LOV	m	0	0	-	Overlap length
NOVO	m^{-3}	$5 \cdot 10^{25}$	10^{22}	10^{26}	Effective doping level of overlap regions
IGINVLW	A	0	0	-	ECB gate channel current prefactor for $1\mu m^2$ channel area
IGOVW	A	0	0	-	ECB gate overlap current pre-factor for $1\mu m$ wide gate overlap region
IGMAX	A	10^{-5}	0	-	Maximum gate current
GCOO		0	-10	10	ECB gate tunneling energy adjustment

Chapter 9: CMC MOS Varactor Model (Level 7)

Model Parameters: CMC Varactor Model (Level 7)

Table 223 Model Parameters (Continued)

Name	Units	Default	Min.	Max.	Description
GC2O		0.375	0	0	ECB gate current slope factor
GC3O		0.063	-10	10	ECB gate current curvature factor
IGCHVLW	A	0	0	-	HVB gate channel current prefactor for $1\mu m^2$ channel area
IGOVHVV	A	0	0	-	HVB gate overlap current prefactor for $1\mu m$ wide gate overlap region
GCOHVO		0	-10	10	HVB gate tunneling energy adjustment
GC2HVO		0.375	0	0	HVB gate current slope factor
GC3HVO		0.063	-10	10	HVB gate current curvature factor
IGCEVLW	A	0	0	-	EVB gate channel current prefactor for $1\mu m^2$ channel area
IGOVEVV	A	0	0	-	EVB gate overlap current pre-factor for $1\mu m$ wide gate overlap region
GCOEVO		0	-10	10	EVB gate tunneling energy adjustment
GC2EVO		0.375	0	0	EVB gate current slope factor
GC3EVO		0.063	-10	10	EVB gate current curvature factor

1. In PSP, VFBO corresponds to NMOS and is negative of the actual value for PMOS. For varactor, you specify the actual value.

MOSFET Noise Models

This chapter discusses use of available MOSFET noise model parameters.

HSPICE ships hundreds of examples for your use; see [Listing of Demonstration Input Files](#) for paths to demo files.

These topics are presented in the following sections:

- [Noise Model Parameters](#)
- [MOSFET Model Noise Equations](#)

Noise Model Parameters

This section describes noise model parameters.

Table 224 Noise Parameters

Name (Alias)	Units	Default	Description
AF		1.0	Flicker noise exponent.
KF		0.0	Flicker noise coefficient. Reasonable values for KF are in the range 1e-19 to 1e-25 V ² F.
NLEV		2.0	Noise equation selector. Values are 1, 2, or 3.
RD	V ² /Hz		Output thermal noise due to drain resistor.
RS	V ² /Hz		Output thermal noise due to source resistor.

Table 224 Noise Parameters

Name (Alias)	Units	Default	Description
RX			<p>Transfers the function of thermal noise to the output. This is not noise, but is a transfer coefficient, which reflects the contribution of thermal noise to the output. For example:</p> $V(\text{output}) = I(\text{local}) * rx(\text{from local to output})$ <p>Where $V(\text{output})$ is the noise voltage at the output port, $I(\text{local})$ is the local noise current in the specific noise element.</p> <p>It is clear that rx should have an unit of impedance, therefore we call it transimpedance. By summarizing all the contributions (power) from each independent noisy element, we can get the total noise contribution(power) at the output port.</p>
ID	V^2/Hz		Output channel thermal noise: $ID = RX^2P$ (channel thermal noise) ² .
FN	V^2/Hz		Output flicker noise: $FN = RX^2P$ (flicker noise) ² .
IFEX			Noise due to floating body
LGS			Shot noise due to I_{gs}
LGD			Shot noise due to I_{gd}
LGF			Shot noise due to I_{gf}
TOT	V^2/Hz		<p>Total output noise:</p> $TOT = RD + RS + ID + FN + IFEX + RG + IGS + IGD + IGF.$

For different MOS models, the total noise equation maybe different; it always equals the sum of the noise types listed. RD , RS , ID , FN are the basic noise types (all MOSFET models contain these).

MOSFET Model Noise Equations

The MOSFET model noise equations have a selector parameter, `NLEV`, that selects either the original SPICE flicker noise or an equation proposed by Gray and Meyer.

You can model thermal noise generation in the drain and source resistors as two sources, `inrd` and `inrs` (units $\text{amp}/(\text{Hz})^{1/2}$) as shown in [Example 35 on page 723](#).

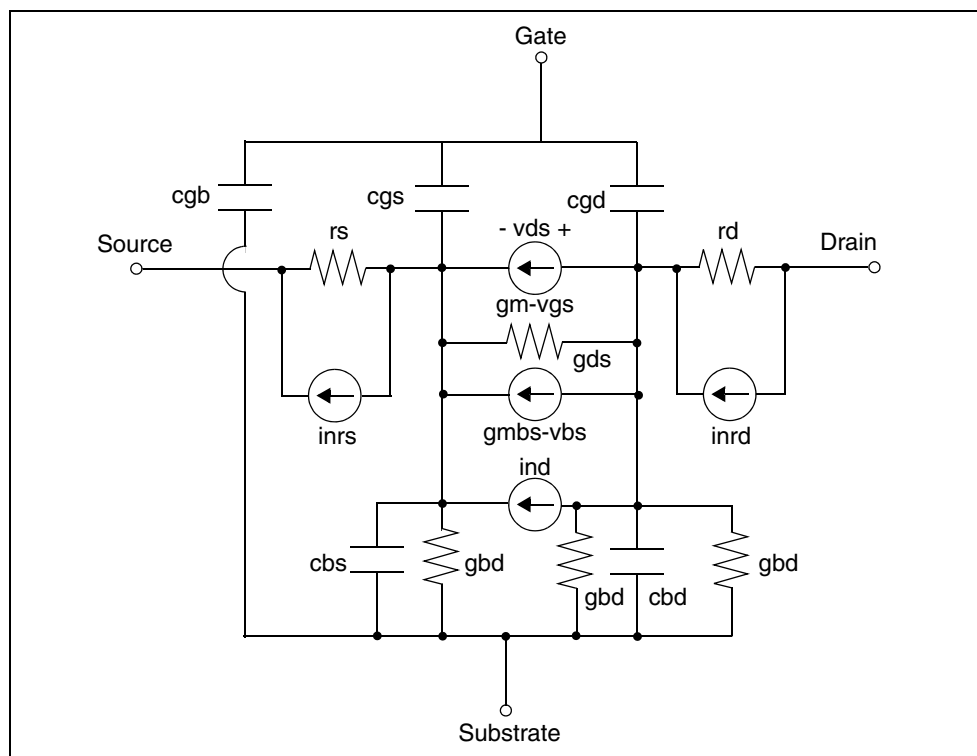


Figure 35 Equivalent Circuit, MOSFET AC Noise Analysis

The following equations calculate the values of these sources:

$$inrs = \left(\frac{4kt}{rs} \right)^{1/2}, \quad inrd = \left(\frac{4kt}{rd} \right)^{1/2}$$

You can model the channel thermal noise and the flicker noise as the `ind` current source, which the following equation defines:

Chapter 10: MOSFET Noise Models

MOSFET Model Noise Equations

$$ind^2 = (channel\ thermal\ noise)^2 + (flicker\ noise)^2$$

If the NLEV model parameter is less than 3, then:

$$channel\ thermal\ noise = \left(\frac{8kT \cdot gm}{3} \right)^{1/2}$$

The preceding formula, used in both saturation and linear regions, can lead to wrong results in the linear region. For example, at VDS=0, channel thermal noise becomes zero because gm=0. This calculation is physically impossible. If you set the NLEV model parameter to 3, simulation uses a different equation, which is valid in both linear and saturation regions. (See *Operation and Modeling of the MOS Transistor* by Yanis P. Tsividis, published by McGraw-Hill, 1987, p. 340.)

For NLEV=3

$$channel\ thermal\ noise = \left(\frac{8kt}{3} \cdot \beta \cdot (vgs - vth) \cdot \frac{1 + a + a^2}{1 + a} \cdot GDSNOI \right)^{1/2}$$

The following equations calculate the a value used in the preceding equation:

$$a = 1 - \frac{vds}{vdsat} \quad \text{Linear region}$$

$$a = 0 \quad \text{Saturation region}$$

Use the AF and KF parameters in the small-signal AC noise analysis to determine the equivalent flicker noise current generator, which connects the drain to the source.

NLEV=0 (SPICE):

$$flicker\ noise = \left(\frac{KF \cdot Ids^{AF}}{COX \cdot Leff^2 \cdot f} \right)^{1/2}$$

For NLEV=1

$Leff^2$ in the above equation is replaced by $Weff \cdot Leff$.

For NLEV=2, 3

$$flicker\ noise = \left(\frac{KF \cdot gm^2}{COX \cdot Weff \cdot Leff \cdot f^{AF}} \right)^{1/2}$$

Finding Device Libraries

Describes how to use the HSPICE automatic model selector to find the proper model for each transistor size.

HSPICE ships hundreds of examples for your use; see [Listing of Demonstration Input Files](#) for paths to demo files.

The HSPICE Automatic Model Selector

For libraries with multiple models of a specific element, you can use an automatic model selector in HSPICE to automatically find the proper model for each transistor size.

The automatic model selector uses the following criteria:

$$L_{MIN} + XLREF \leq L + XL < L_{MAX} + XLREF$$

$$W_{MIN} + XWREF \leq W + XW < W_{MAX} + XWREF$$

If you do not specify `XLREF`, simulation sets it to `XL`. If you do not specify `XWREF`, simulation sets it to `XW`.

The model selector syntax is based on a common model root name, with a unique extension for each model.

The following is an example of HSPICE syntax for MOSFET models:

```
M1 drain gate source bulk NJ W=2u L=1u
.MODEL NJ4 NJF WMIN=1.5u WMAX=3u LMIN=.8u LMAX=2u
.MODEL NJ5 NJF WMIN=1.5u WMAX=3u LMIN=2u LMAX=6u
```

[Figure 36 on page 726](#) illustrates the MOSFET model selection method.

Appendix A: Finding Device Libraries

The HSPICE Automatic Model Selector

This example illustrates several pch.x models, with varying drawn channel lengths and widths, in the model library. The model root name is “pch”, and the extensions are 1, 2, ..., 6. The NJ4 instance of the NJ Element ($W=2\ \mu$, $L=1\ \mu$) requires a model for which $1.5\ \mu \leq \text{channel width} \leq 3\ \mu$, and $0.8\ \mu \leq \text{channel length} \leq 2\ \mu$.

The automatic model selector chooses the pch.4 model because that model satisfies these requirements. Similarly, the NJ5 transistor requires a model with $1.5\ \mu \leq \text{channel width} \leq 3\ \mu$, and $2\ \mu \leq \text{channel length} \leq 6\ \mu$. The pch.5 model satisfies these requirements. If a device size is out of range for all models, the automatic model selector issues an error message.

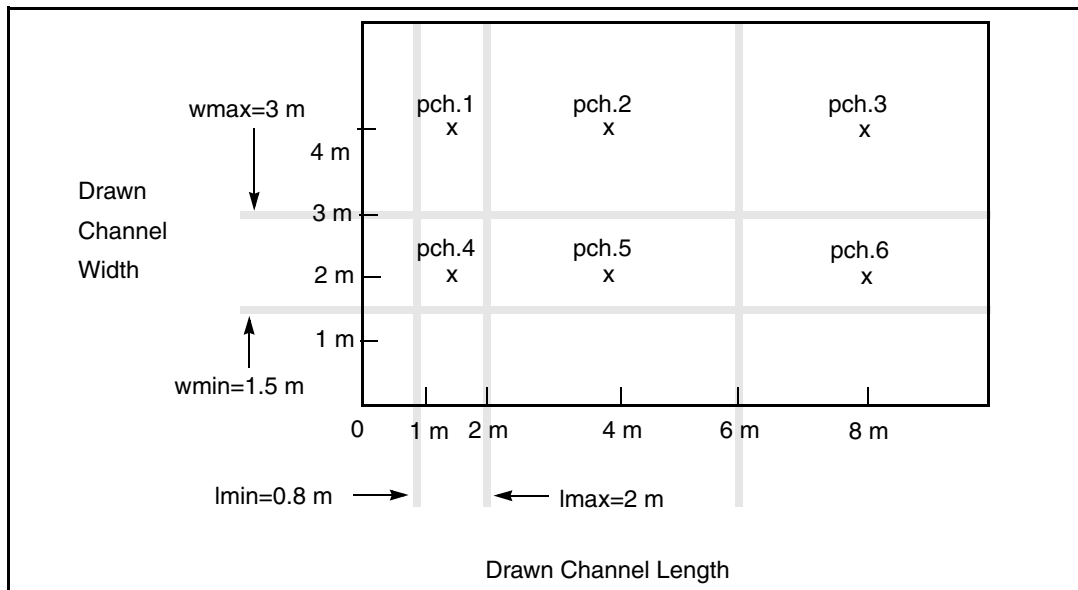


Figure 36 Automatic Model Selector Method

If the automatic model selector cannot find a model within a subcircuit, the automatic model selector searches the top level. If the automatic model selector fails to find a model, simulation terminates.

The following combination of conditions causes the automatic model selector to fail and terminates the simulation:

- The element statement uses a model name that contains a period (.).
- The model library was not designed for use with the automatic model selector.
- The simulation input includes either a multisweep specification or a .TEMP temperature analysis statement.

The following example illustrates how a period in a model name can cause problems in automatic model selection.

Example 1

```
M1 d g s b N.CHN W=10u L=5u          * Element statement
.MODEL N.CHN LMIN=1u LMAX=4u WMIN=2u WMAX=100u
* .MODEL statement
```

Example 2

```
.TEMP 25
.M1 d g s b N.CHN W=10u L=5u          * Element statement
.MODEL N.CHN LMIN=1u LMAX=4u WMIN=2u WMAX=100u
* .MODEL statement
```

Because Example 1 does not specify multisweep or temperature analysis, simulation does not invoke the model selector feature, so simulation uses the N.CHN model with no problems.

In Example 2, however, the .TEMP statement invokes the model selector feature. The model selector tries to find a model named “N.nnn” that fits within the length and width ranges specified in the element statement.

Because the length in the element statement (5 μm) is not within the 1 to 4 μm range specified in the .MODEL statement, the model selector cannot find a model that matches the element statement, and simulation issues a “device ‘N’ not found” error message.

Appendix A: Finding Device Libraries

The HSPICE Automatic Model Selector

Technology Summary for HSPICE MOSFET Models

Describes the technology used in all HSPICE MOSFET models.

These topics are covered in the following sections:

- [Nonplanar and Planar Technologies](#)
- [Field Effect Transistors](#)
- [MOSFET Equivalent Circuits](#)
- [MOSFET Diode Models](#)
- [Common Threshold Voltage Equations](#)
- [MOSFET Impact Ionization](#)
- [MOS Gate Capacitance Models](#)
- [Noise Models](#)
- [Temperature Parameters and Equations](#)

Nonplanar and Planar Technologies

Two MOSFET fabrication technologies have dominated integrated circuit design: nonplanar and planar technologies.

Nonplanar Technology

Nonplanar technology uses metal gates. The simplicity of the process generally provides acceptable yields.

The primary problem with metal gates is metal breakage across the field oxide steps. Field oxide grows when oxidizing the silicon surface. When the surface is cut, it forms a sharp edge. Because metal is affixed to these edges to contact the diffusion or make a gate, thicker metal must be applied to compensate for the sharp edges. This metal tends to gather in the cuts, making etching difficult. The inability to accurately control the metal width necessitates very conservative design rules and results in low transistor gains.

Planar Technology:

In planar technology, the oxide edges are smooth with a minimal variance in metal thickness. Shifting to nitride is accomplished using polysilicon gates.

Adding a chemical reactor to the MOS fabrication process enables depositing silicon nitride, silicon oxide, and polysilicon. The ion implanter is the key element in this processing by using implanters with beam currents greater than 10 milliamperes.

Because implanters define threshold voltages, diffusions, and field thresholds, processes require a minimum number of high temperature oven steps. This enables low temperature processing and maskless pattern generation. The new wave processes are more similar to the older nonplanar metal gate technologies.

Field Effect Transistors

The metal gate MOSFET is nonisoplanar as shown in [Figure 37](#) and [Figure 38](#) on page 731.

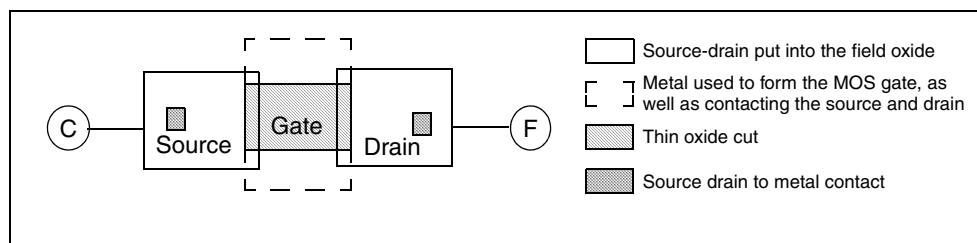


Figure 37 Field Effect Transistor

Looking at the actual geometry, from source-to-drain, [Figure 38](#) shows a perspective of the nonisoplanar MOSFET.

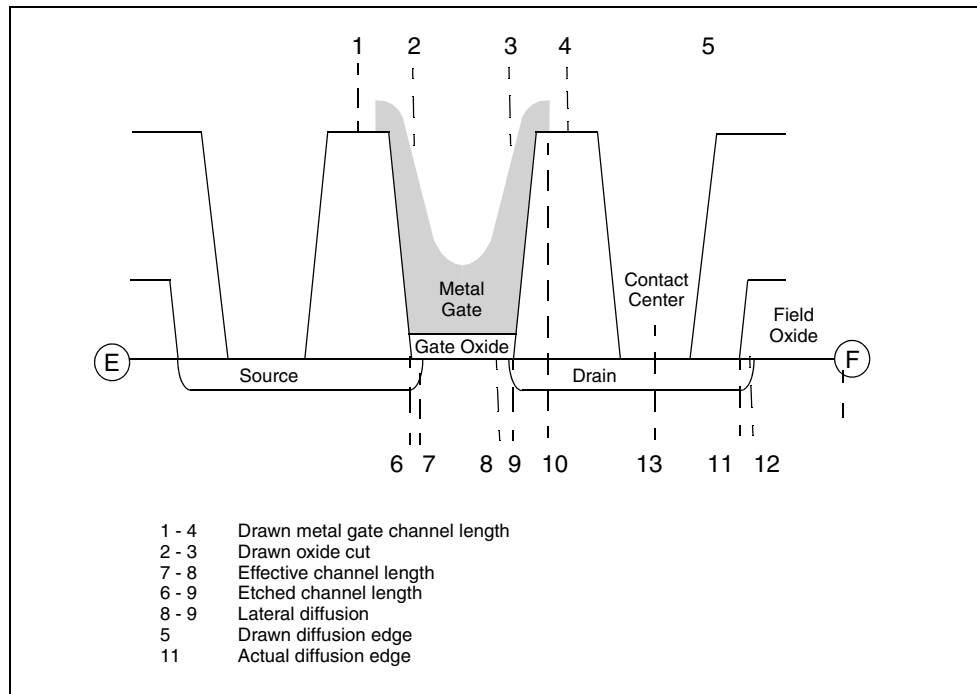


Figure 38 Field Effect Transistor Geometry

To visualize the construction of a silicon gate MOSFET, observe how a source or drain to field cuts ([Figure 39](#).) Cut A-B shows a drain contact ([Figure 40](#)).

Appendix B: Technology Summary for HSPICE MOSFET Models

Field Effect Transistors

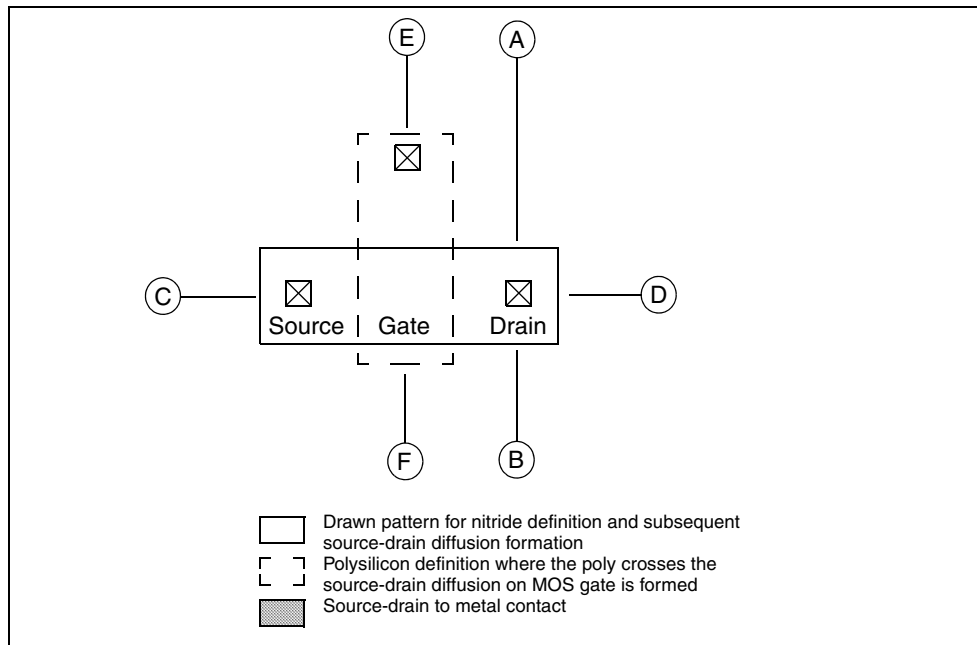


Figure 39 Isoplanar Silicon Gate Transistor

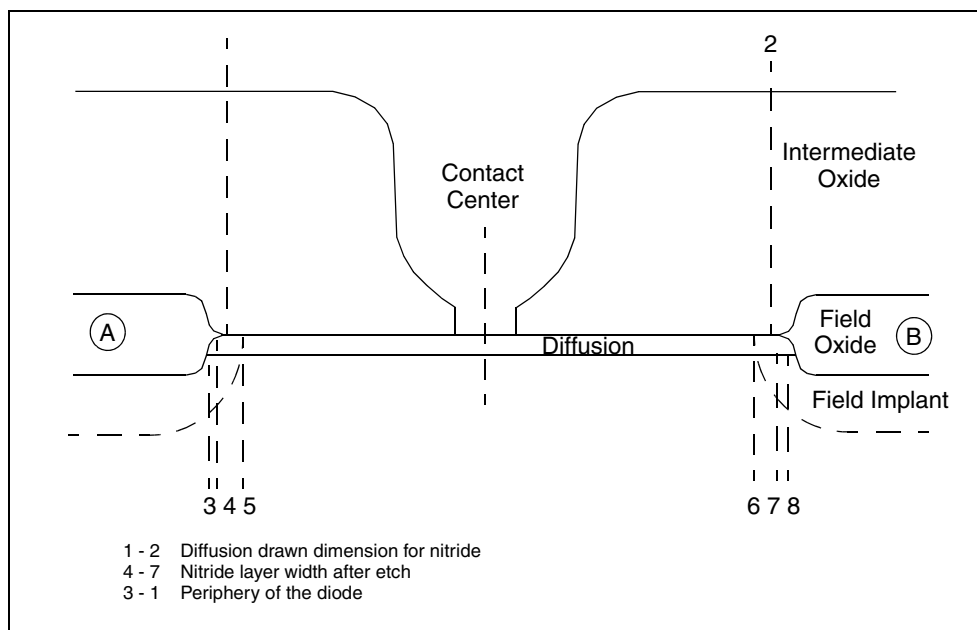


Figure 40 Isoplanar MOSFET Construction, Part A

CD represents the cut from the source to the drain (Figure 41 on page 733), and includes the contacts.

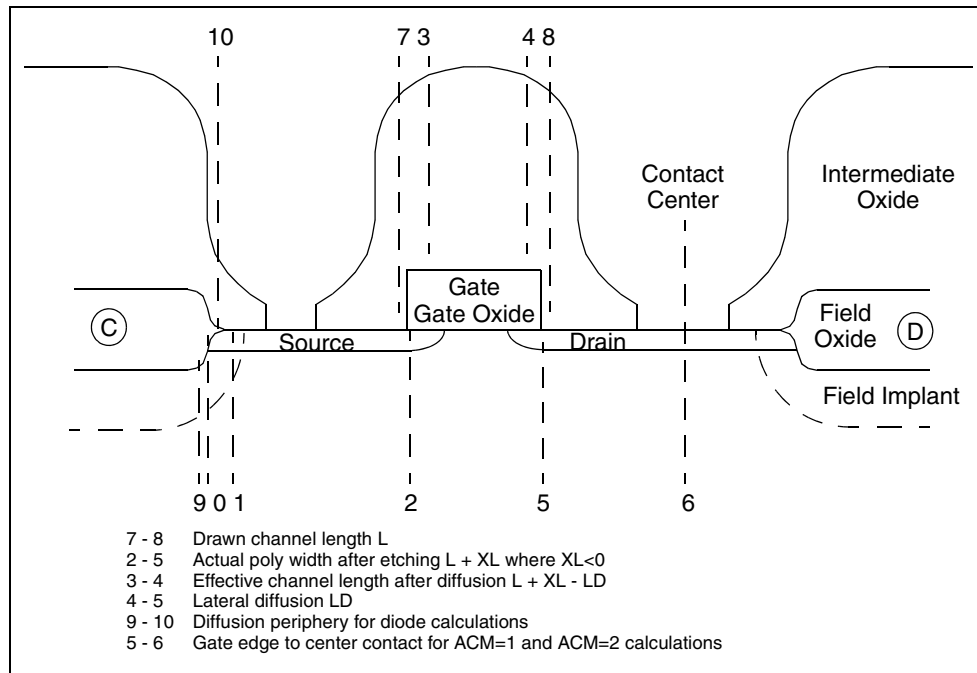


Figure 41 Isoplanar MOSFET Construction, Part B

The planar process produces parasitic capacitances at the poly to field edges of the device. The cut along the width of the device demonstrates the importance of these parasitics (Figure 42 on page 734).

The encroachment of the field implant into the channel narrows the channel width, and increases the gate to bulk parasitic capacitance.

Appendix B: Technology Summary for HSPICE MOSFET Models

MOSFET Equivalent Circuits

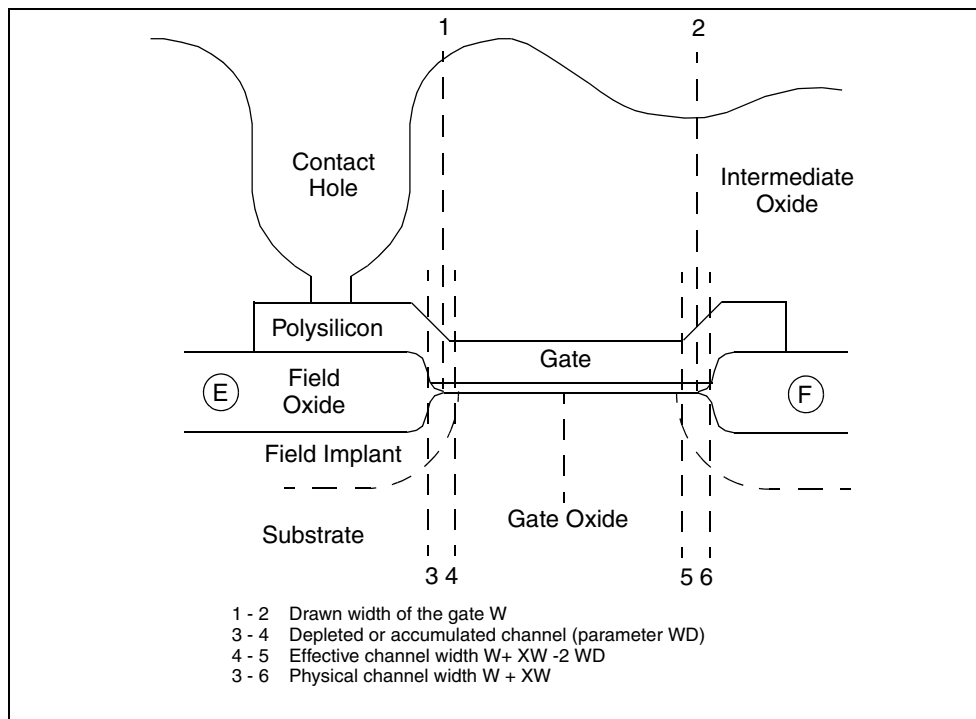


Figure 42 Isoplanar MOSFET, Width Cut

MOSFET Equivalent Circuits

The following sections describe MOSFET equation variables, current convention, and equivalent circuits.

Equation Variables

This section lists the equation variables and constants.

Table 225 Equation variables and Constants

Variable/ Quantity	Definition
cbd	Bulk-to-drain capacitance

Table 225 Equation variables and Constants

Variable/ Quantity	Definition
cbs	Bulk-to-source capacitance
cbg	Gate-to-bulk capacitance
cgd	Gate-to-drain capacitance
cgs	Gate-to-source capacitance
f	Frequency
gbd	Bulk-to-drain dynamic conductance
gbs	Bulk-to-source dynamic conductance
gds	Drain-to-source dynamic conductance (controlled by vds)
gdb	Drain-to-bulk impact ionization conductance
gm	Drain-to-source dynamic transconductance (controlled by vgs)
gmbs	Drain-to-source dynamic bulk transconductance (controlled by vsb)
ibd	Bulk-to-drain DC current
ibs	Bulk-to-source DC current
ids	Drain-to-source DC current
idb	Drain-to-bulk impact ionization current
ind	Drain-to-source equivalent noise circuit
inrd	Drain resistor equivalent noise circuit
inrs	Source resistor equivalent noise circuit
rd	Drain resistance
rs	Source resistance
vsb	Source-to-bulk voltage

Appendix B: Technology Summary for HSPICE MOSFET Models

MOSFET Equivalent Circuits

Table 225 Equation variables and Constants

Variable/ Quantity	Definition
vds	Drain-to-source voltage
vgs	Gate-to-source voltage
Δt	t-tnom
ϵ_{si}	1.0359e-10F/m dielectric constant of silicon
k	1.38062e-23 (Boltzmann's constant)
q	1.60212e-19 (electron charge)
t	New temperature of model or element in °K
tnom	tnom = TNOM + 273.15. This variable represents the nominal temperature of parameter measurements in °K (user input in °C).
vt	$k \cdot t/q$
vt(tnom)	$k \cdot tnom/q$

Using MOSFET Current Convention

Figure 43 shows the assumed direction of current flow through a MOS transistor. To print the drain current, use either I(M1) or I1(M1) syntax.

- I2 produces the gate current.
- I3 produces the source current.
- I4 produces the substrate current.

References to bulk are the same as references to the substrate.

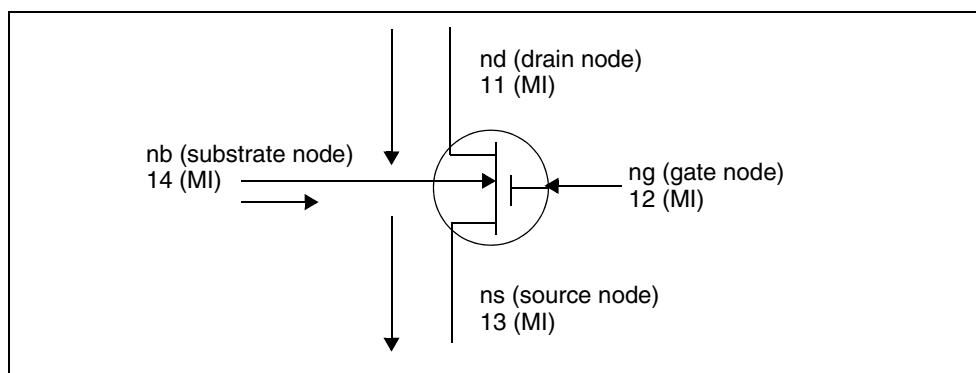


Figure 43 MOSFET Current Convention, N-channel

Using MOSFET Equivalent Circuits

Simulators use three equivalent circuits to analyze MOSFETs:

- DC
- Transient
- AC and noise-equivalent circuits

The components of these circuits form the basis for all element and model equations. The equivalent circuit for DC sweep is the same as the one used for transient analysis, but excludes capacitances. [Figure 44](#) through [Figure 46](#) display the MOSFET equivalent circuits.

The fundamental component in the equivalent circuit is the DC drain-to-source current (i_{ds}). Noise and AC analyses do not use the actual i_{ds} current. Instead, the model uses the partial derivatives of i_{ds} with respect to the v_{gs} , v_{ds} , and v_{bs} terminal voltages.

The names for these partial derivatives are as follows.

$$\text{Transconductance: } g_m = \frac{\partial(i_{ds})}{\partial(v_{gs})}$$

$$\text{Conductance: } g_{ds} = \frac{\partial(i_{ds})}{\partial(v_{ds})}$$

$$\text{Bulk Transconductance: } g_{mbs} = \frac{\partial(i_{ds})}{\partial(v_{bs})}$$

Appendix B: Technology Summary for HSPICE MOSFET Models

MOSFET Equivalent Circuits

The i_{ds} equation describes the basic DC effects of the MOSFET. Simulation considers the effects of gate capacitance, and of source and drain diodes, separately from the DC i_{ds} equations. Simulation also evaluates the impact ionization equations separately from the DC i_{ds} equation, even though the ionization effects are added to i_{ds} .

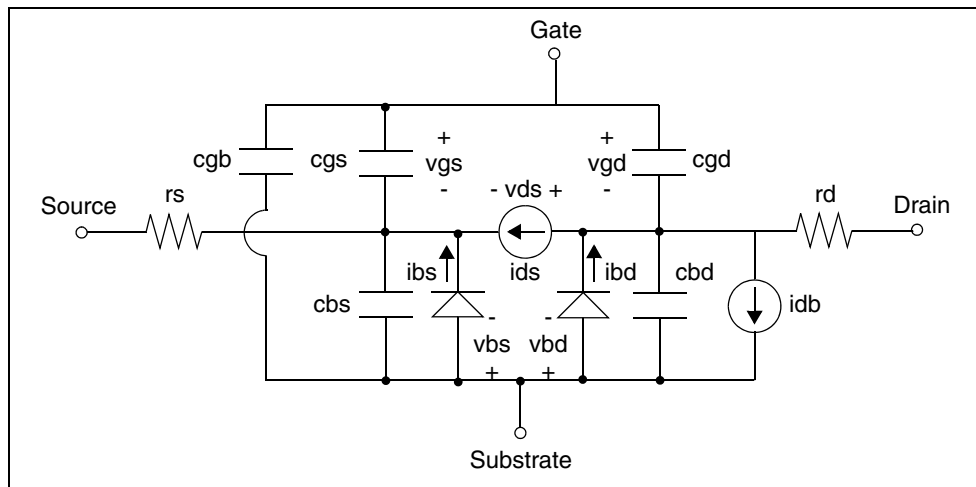


Figure 44 Equivalent Circuit, MOSFET Transient Analysis

Appendix B: Technology Summary for HSPICE MOSFET Models

MOSFET Equivalent Circuits

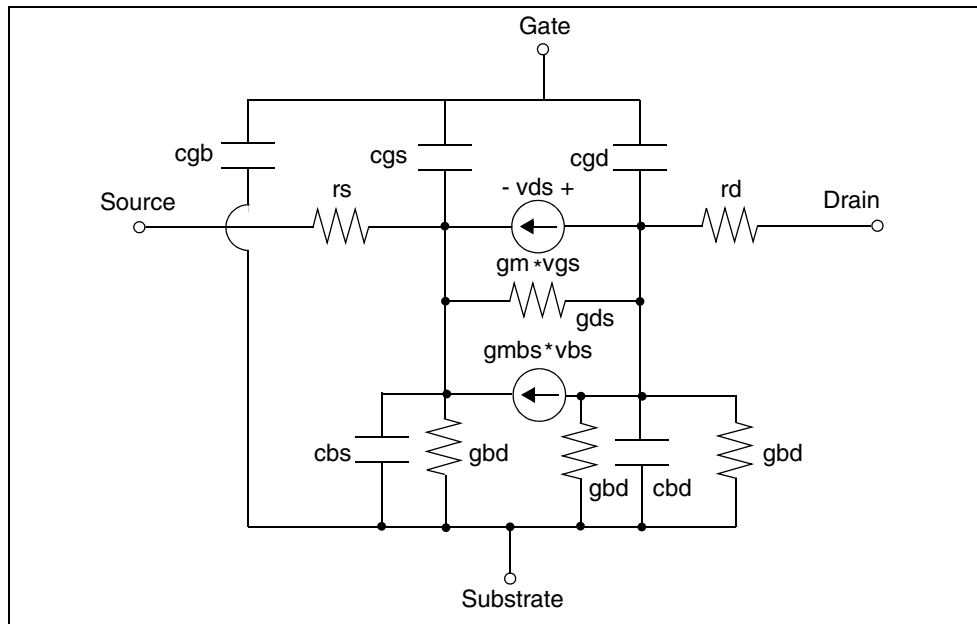


Figure 45 Equivalent Circuit, MOSFET AC Analysis

Appendix B: Technology Summary for HSPICE MOSFET Models

MOSFET Equivalent Circuits

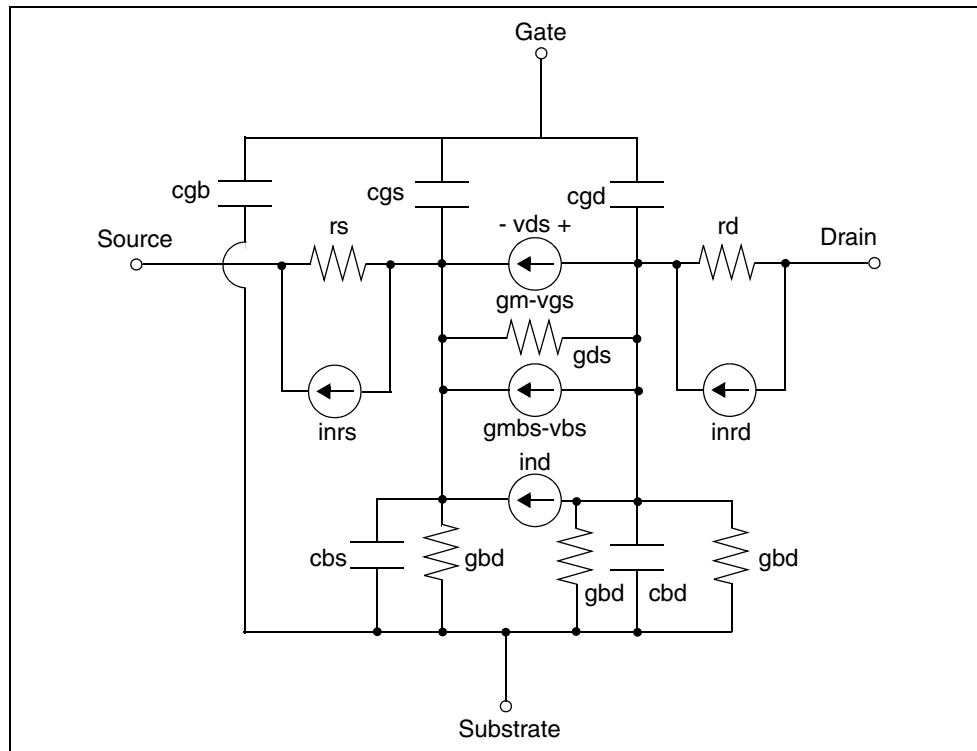


Figure 46 Equivalent Circuit, MOSFET AC Noise Analysis

Table 226 MOSFET DC Operating Point Output

Quantities	Definitions
id	drain current
ibs	B-S bulk-to-source current
ibd	B-D bulk-to-drain current
vgs	G-S gate-source voltage
vds	D-S drain-source voltage
vbs	B-S bulk-source voltage
vth	threshold voltage
vdsat	saturation voltage

Table 226 MOSFET DC Operating Point Output

Quantities	Definitions
beta	beta value
gam eff	gamma effective
gm	DC gate transconductance
gds	D-S drain-source conductance
gmb	B-S bulk-source conductance
cdtot	total drain capacitance
cgtot	total gate capacitance
cstot	total source capacitance
cbtot	total bulk capacitance (total floating body capacitance for SOI MOSFET)
cgs	total gat- to-source capacitance
cgd	total gat- to-drain capacitance

MOSFET Diode Models

See [Chapter 8, MOSFET Diode Models](#) for full discussion of available MOSFET diode models and parameters.

Common Threshold Voltage Equations

Common Threshold Voltage Parameters

The parameters described in this section apply to all MOSFET models except Levels 5 and 13.

Table 227 MOSFET Common Threshold Voltage Parameters

Name (Alias)	Units	Default	Description
DELVTO	V	0.0	Zero-bias threshold voltage shift.
GAMMA	$\sqrt{V}^{1/2}$	0.527625	Body effect factor. If you do not set GAMMA, simulation calculates it from NSUB.
NGATE	$1/\text{cm}^3$	-	Polysilicon gate doping, used for analytical models only. Undoped polysilicon is represented by a small value. If NGATE ≤ 0.0 , it is set to $1\text{e}+18$.
NSS	$1/\text{cm}^2$	1.0	Surface state density.
NSUB (DNB, NB)	$1/\text{cm}^3$	$1\text{e}15$	Substrate doping.
PHI	V	0.576036	Surface potential. NSUB default= $1\text{e}15$.
TPG (TPS)	-	1.0	Type of gate material for analytical models. LEVEL 4 TPG default=0. The TPG value can be: <ul style="list-style-type: none"> TPG = 0 al-gate. TPG = 1 same as source-drain diffusion. TPG = -1 gate type opposite to source-drain diffusion.
VTO (VT)	V	-	Zero-bias threshold voltage.

Calculating PHI, GAMMA, and VTO

Use the PHI, GAMMA, and VTO model parameters to calculate threshold voltages. If you do not specify these parameters, simulation calculates them as follows, except for the LEVEL 5 model.

If you do not specify PHI, then: $PHI = 2 \cdot v_t \cdot \ln\left(\frac{NSUB}{ni}\right)$

If you do not specify GAMMA, then: $GAMMA = \frac{(2 \cdot q \cdot \epsilon_{si} \cdot NSUB)^{1/2}}{COX}$

The following equations determines the energy gap (eg) and intrinsic carrier concentration used in the above equations:

$$eg = 1.16 - 7.02e-4 \cdot \frac{tnom^2}{tnom + 1108}$$

$$ni = 1.45e+10 \cdot \left(\frac{tnom}{300}\right)^{3/2} \cdot e^{\left[\frac{q \cdot eg}{2 \cdot k} \cdot \left(\frac{1}{300} - \frac{1}{tnom}\right)\right]} (1/\text{cm}^3)$$

In the preceding equation, $tnom = TNOM + 273.15$.

If you do not specify VTO, then for Al-Gate (TPG=0), the following equation determines the Φ_{ms} work function: $\Phi_{ms} = -\frac{eg}{2} - \text{type} \cdot \frac{PHI}{2} - 0.05$

In the preceding equation, *type* is +1 for n-channel or -1 for p-channel.

For Poly-Gate (TPG=±1), the following equations determine the work function.

If you do not specify the NGATE model parameter, then:

$$\Phi_{ms} = \text{type} \cdot \left(-TPG \cdot \frac{eg}{2} - \frac{PHI}{2}\right)$$

If you specify NGATE, then: $\Phi_{ms} = \text{type} \cdot \left[-TPG \cdot v_t \cdot \ln\left(\frac{NGATE}{ni}\right) - \frac{PHI}{2}\right]$

If you do not specify the VTO model parameter, then the following equation determines the VTO voltage: $VTO = v_{fb} + \text{type} \cdot (GAMMA \cdot PHI^{1/2} + PHI)$

In the preceding equation, $v_{fb} = \Phi_{ms} - \frac{q \cdot NSS}{COX} + DELVTO$.

If you specify V_{TO} , then: $V_{TO} = V_{TO} + DELV_{TO}$.

MOSFET Impact Ionization

Impact ionization current is available for all MOSFET levels. ALPHA, VCR, and IIRAT are the controlling parameters. IIRAT sets the fraction of the impact ionization current sent to the source.

$$I_{ds} = I_{ds_normal} + IIRAT \cdot I_{impact}$$

$$I_{db} = I_{db_diode} + (1 - IIRAT) \cdot I_{impact}$$

IIRAT defaults to zero, which sends all impact ionization current to bulk. Leave IIRAT at its default value unless data is available for both drain and bulk current.

Table 228 Impact Ionization Model Parameters

Name (Alias)	Units	Default	Description
ALPHA	1/V	0.0	Impact ionization current coefficient
LALPHA	$\mu\text{m}/\text{V}$	0.0	ALPHA length sensitivity
WALPHA	$\mu\text{m}/\text{V}$	0.0	ALPHA width sensitivity
VCR	V	0.0	Critical voltage
LVCR	$\mu\text{m} \cdot \text{V}$	0.0	VCR length sensitivity
WVCR	$\mu\text{m} \cdot \text{V}$	0.0	VCR width sensitivity
IIRAT		0.0	Portion of impact ionization current sent to the source

Calculating the Impact Ionization Equations

The following equations calculates the I_{impact} current due to the impact

ionization effect:
$$I_{impact} = I_{ds} \cdot ALPHA_{eff} \cdot (v_{ds} - v_{dsat}) \cdot e^{\frac{-VCR_{eff}}{v_{ds} - v_{dsat}}}$$

The following equations calculate values used in the preceding equation:

$$ALPHA_{eff} = ALPHA + LALPHA \cdot 1e-6 \cdot \left(\frac{1}{Leff} - \frac{1}{LREF_{eff}} \right)$$

$$WALPHA \cdot 1e-6 \cdot \left(\frac{1}{Weff} - \frac{1}{WREF_{eff}} \right)$$

$$VCR_{eff} = VCR + LVCR \cdot 1e-6 \cdot \left(\frac{1}{Leff} - \frac{1}{LREF_{eff}} \right)$$

$$WVCR \cdot 1e-6 \cdot \left(\frac{1}{Weff} - \frac{1}{WREF_{eff}} \right)$$

The following equations calculate the $LREF_{eff}$ and $WREF_{eff}$ values used in the preceding equations:

$$LREF_{eff} = LREF + XLREF - 2 \cdot LD$$

$$WREF_{eff} = WREF + XWREF - 2 \cdot WD$$

Calculating Effective Output Conductance

You can use the element template to directly output gds. For example:

```
.PRINT I (M1) gds=LX8 (M1)
```

If you use impact ionization current, gds is the derivative of I_{ds} only, rather than the total drain current, which is $I_{ds} + I_{db}$.

The complete drain output conductance is:

$$g_{dd} = \frac{\partial I_d}{\partial V_d} = \frac{\partial I_{ds}}{\partial V_{ds}} + \frac{\partial I_{db}}{\partial V_{db}} = \frac{\partial I_{ds}}{\partial V_{ds}} + \frac{\partial I_{bd}}{\partial V_{bd}} = g_{ds} + g_{bd}$$

$$G_{dd} = LX8 + LX10$$

For example, to print the drain output resistance of the M1 device:

```
.PRINT rout=PAR('1.0/(LX8 (M1) + LX10 (M1))')
```

Appendix B: Technology Summary for HSPICE MOSFET Models

MOSFET Impact Ionization

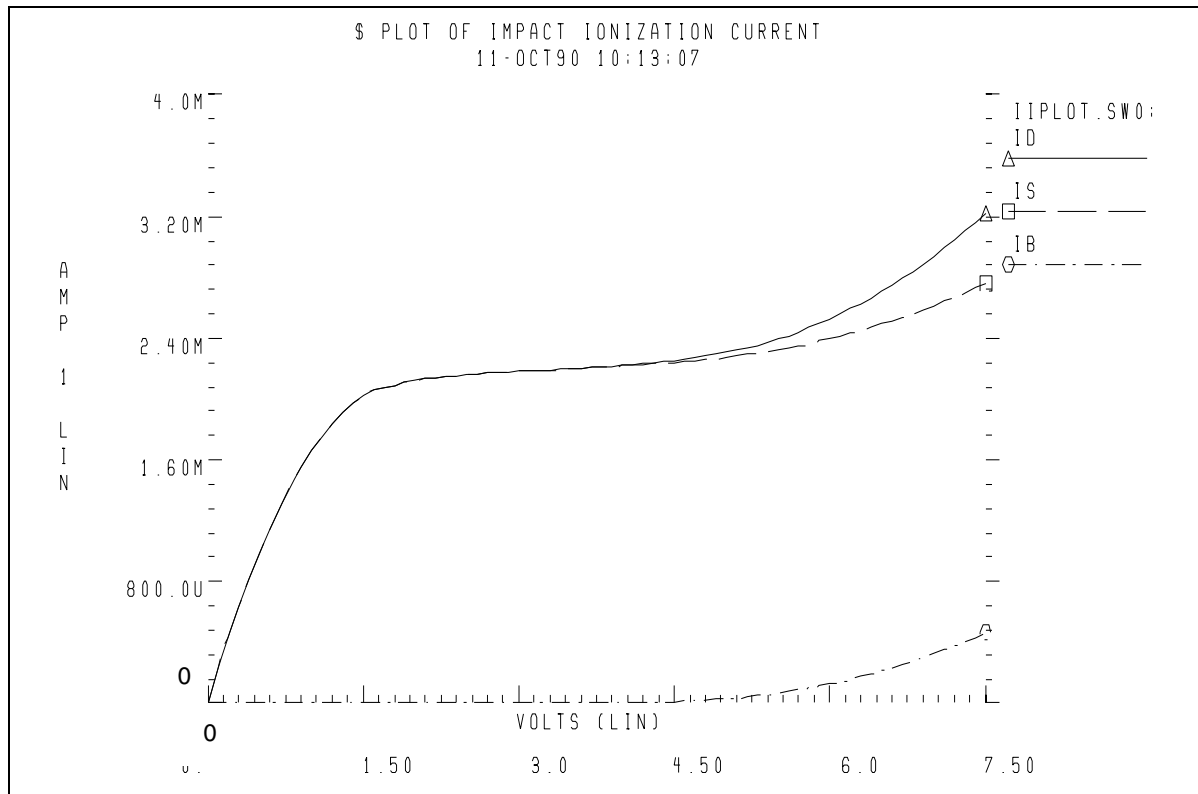


Figure 47 Drain, Source, and Bulk Currents for $v_{gs}=3$ with $IIRAT=0.5$

Cascoding Example

Drain-to-bulk impact ionization current limits the use of cascoding to increase output impedance. The following cascode example shows the effect of changing $IIRAT$. If $IIRAT$ is less than 1.0, the drain-to-bulk current lowers the output impedance of the cascode stage.

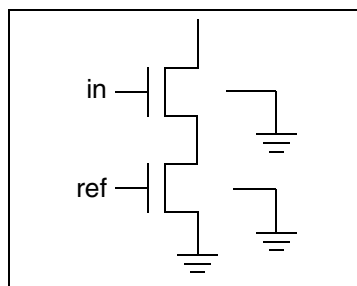


Figure 48 Low-frequency AC Analysis Measuring Output Impedance

Cascode Circuit

Example

iirat	gout_ac	rout
0.0	8.86E-6	113 K
0.5	4.30E-6	233 K
1.0	5.31E-8	18.8 Meg

This example is based on demonstration netlist cascode.sp, which is available in directory \$<installdir>/demo/hspice/mos:

```
$ cascode test
.option post
.param pvds=5.0 pvref=1.4 pvin=3.0
vdd dd 0 pvds ac 1
$ current monitor vd
vd dd d 0
vin in 0 pvin
vref ref 0 pvref
x1 d in ref cascode
.macro cascode out in ref
m1 out in 1 0 n L=1u W=10u
mref 1 ref 0 0 n L=1u W=10u
.eom
.param xiirat=0
.ac dec 2 100k 1x sweep xiirat poi 3 0, 0.5, 1.0
.print ir(vd)
.measure gout_ac avg ir(vd)
.model n nmos level=3
+ tox=200 vto=0.8 gamma=0.7 uo=600 kappa=0.05
+ alpha=1 vcr=15 iirat=xiirat
.end
```

MOS Gate Capacitance Models

See [Chapter 7, MOSFET Capacitance Models](#) for full discussion of these models and their parameters.

Noise Models

See [MOSFET Noise Models](#) for discussion of parameters and noise model equations.

Temperature Parameters and Equations

Temperature Parameters

The following temperature parameters apply to all MOSFET model levels and the associated bulk-to-drain and bulk-to-source MOSFET diode within the MOSFET model. The **TLEV** and **TLEVC** parameters select the temperature equations used to calculate the temperature effects on the model parameters.

Table 229 Temperature Effects Parameters

Name (Alias)	Units	Default	Description
BEX		-1.5	Low field mobility, UO , temperature exponent.
CTA	$1/^{\circ}\text{K}$	0.0	Junction capacitance (CJ) temperature coefficient. If TLEVC =1, CTA overrides the default temperature compensation.
CTP	$1/^{\circ}\text{K}$	0.0	Junction sidewall capacitance ($CJSW$) temperature coefficient. If TLEVC =1, CTP overrides the default temperature compensation.
EG	eV		Energy gap for pn junction diode for TLEV =0 or 1, default=1.11; for TLEV =2, default=1.16 1.17 – silicon 0.69 – Schottky barrier diode 0.67 – germanium 1.52 – gallium arsenide
F1EX		0	Bulk junction bottom grading coefficient

Appendix B: Technology Summary for HSPICE MOSFET Models

Temperature Parameters and Equations

Table 229 Temperature Effects Parameters

Name (Alias)	Units	Default	Description
GAP1	eV/° K	7.02e-4	First bandgap correction factor (from Sze, alpha term). 7.02e-4 – silicon 4.73e-4 – silicon 4.56e-4 – germanium 5.41e-4 – gallium arsenide
GAP2	° K	1108	Second bandgap correction factor (from Sze, beta term). 1108 – silicon 636 – silicon 210 – germanium 204 – gallium arsenide
LAMEX	1/° K	0	LAMBDA temperature coefficient.
N		1.0	Emission coefficient.
MJ		0.5	Bulk junction bottom grading coefficient.
MJSW		0.33	Bulk junction sidewall grading coefficient.
PTA	V/° K	0.0	Junction potential (PB) temperature coefficient. If you set TLEVVC to 1 or 2, PTA overrides the default temperature compensation.
PTC	V/° K	0.0	Fermi potential (PHI) temperature coefficient. If you set TLEVVC to 1 or 2, PTC overrides the default temperature compensation.
PTP	V/° K	0.0	Junction potential (PHP) temperature coefficient. If TLEVVC=1 or 2, PTP overrides the default temperature compensation.
TCV	V/° K	0.0	Threshold voltage temperature coefficient. Typical values are +1mV for n-channel and -1mV for p-channel.

Appendix B: Technology Summary for HSPICE MOSFET Models

Temperature Parameters and Equations

Table 229 Temperature Effects Parameters

Name (Alias)	Units	Default	Description
TLEV		0.0	Temperature equation level selector. Set TLEV=1 for ASPEC style. Default is SPICE style. If you invoke the ASPEC option, the program sets TLEV for ASPEC.
TLEVC		0.0	Temperature equation level selector for junction capacitances and potentials. Interacts with TLEV. Set TLEVC=1 for ASPEC style. Default is SPICE style. If you invoke the ASPEC option, the program sets TLEVC for ASPEC.
TRD	1/° K	0.0	Temperature coefficient for drain resistor.
TRS	1/° K	0.0	Temperature coefficient for source resistor.
XTI		0.0	Saturation current temperature exponent. Use XTI=3 for silicon diffused junction. Set XTI=2 for Schottky barrier diode.

MOS Temperature Coefficient Sensitivity Parameters

Model levels 13 (BSIM1), 39 (BSIM2), and 28 (METAMOS) include length and width sensitivity parameters as shown in [Table 230](#). Use these parameters with the Automatic Model Selector to enable more accurate modeling for various device sizes. The default value of each sensitivity parameter is zero to ensure backward compatibility.

Table 230 MOS Temperature Coefficient Sensitivity Parameters

Parameter	Description	Sensitivity Parameters		
		Length	Width	Product
BEX	Low field mobility, UO, temperature exponent	LBEX	WBEX	PBEX
FEX	Velocity saturation temperature exponent	LFEX	WFEX	PFEX
TCV	Threshold voltage temperature coefficient	LTCV	WTCV	PTCV

Table 230 MOS Temperature Coefficient Sensitivity Parameters

Parameter	Description	Sensitivity Parameters		
		Length	Width	Product
TRS	Temperature coefficient for source resistor	LTRS	WTRS	PTRS
TRD	Temperature coefficient for drain resistor	LTRD	WTRD	PTRD

Temperature Equations

This section describes how to use temperature equations.

Energy Gap Temperature Equations

These equations set the energy gap for temperature compensation:

For $TLEV = 0$ or 1

$$egnom = 1.16 - 7.02e-4 \cdot \frac{tnom^2}{tnom + 1108.0}$$

$$eg(t) = 1.16 - 7.02e-4 \cdot \frac{t^2}{t + 1108.0}$$

For $TLEV = 2$

$$egnom = EG - GAP1 \cdot \frac{tnom^2}{tnom + GAP2}$$

$$eg(t) = EG - GAP1 \cdot \frac{t^2}{t + GAP2}$$

Saturation Current Temperature Equations

$$isbd(t) = isbd(tnom) \cdot e^{\text{fac1n}/N}, isbs(t) = isbs(tnom) \cdot e^{\text{fac1n}/N}$$

The following equation calculates the `fac1n` value used in the preceding equations:

$$facln = \frac{egnom}{vt(tnom)} - \frac{eg(t)}{vt(t)} + XTI \cdot \ln\left(\frac{t}{tnom}\right)$$

[MOSFET Diode Models on page 741](#) defines the `isbd` and `isbs` values.

MOS Diode Capacitance Temperature Equations

`TLEVC` selects the temperature equation level for MOS diode capacitance.

For `TLEVC=0`

$$PB(t) = PB \cdot \left(\frac{t}{tnom}\right)^{-vt(t)} \Rightarrow \left[3 \cdot \ln\left(\frac{t}{tnom}\right) + \frac{egnom}{vt(tnom)} - \frac{eg(t)}{vt(t)}\right]$$

$$PHP(t) = PHP \cdot \left(\frac{t}{tnom}\right)^{-vt(t)} \Rightarrow \left[3 \cdot \ln\left(\frac{t}{tnom}\right) + \frac{egnom}{vt(tnom)} - \frac{eg(t)}{vt(t)}\right]$$

$$CBD(t) = CBD \cdot \left[1 + MJ \cdot \left(400u \cdot \Delta t - \frac{PB(t)}{PB} + 1\right)\right]$$

$$CBS(t) = CBS \cdot \left[1 + MJ \cdot \left(400u \cdot \Delta t - \frac{PB(t)}{PB} + 1\right)\right]$$

$$CJ(t) = CJ \cdot \left[1 + MJ \cdot \left(400u \cdot \Delta t - \frac{PB(t)}{PB} + 1\right)\right]$$

$$CJSW(t) = CJSW \cdot \left[1 + MJSW \cdot \left(400u \cdot \Delta t - \frac{PHP(t)}{PHP} + 1\right)\right]$$

For `TLEVC=1`

$$PB(t) = PB - PTA \Rightarrow \Delta t, PHP(t) = PHP - PTP \Rightarrow \Delta t$$

$$CBD(t) = CBD \cdot (1 + CTA \cdot \Delta t), CBS(t) = CBS \cdot (1 + CTA \cdot \Delta t)$$

$$CJ = CJ \cdot (1 + CTA \cdot \Delta t), CJSW = CJSW \cdot (1 + CTP \cdot \Delta t)$$

For `TLEVC=2`

$$PB(t) = PB - PTA \Rightarrow \Delta t, PHP(t) = PHP - PTP \Rightarrow \Delta t$$

$$CBD(t) = CBD \cdot \left(\frac{PB}{PB(t)}\right)^{MJ}, CBS(t) = CBS \cdot \left(\frac{PB}{PB(t)}\right)^{MJ}$$

$$CJ(t) = CJ \cdot \left(\frac{PB}{PB(t)}\right)^{MJ}, CJSW(t) = CJSW \cdot \left(\frac{PHP}{PHP(t)}\right)^{MJSW}$$

For TLEVC=3

$$PB(t) = PB + dpbdt \cdot \Delta t, \quad PHP(t) = PHP + dphpdt \cdot \Delta t$$

$$CBD(t) = CBD \cdot \left(1 - 0.5 \cdot \frac{dpbdt}{PB} \cdot \Delta t\right)$$

$$CBS(t) = CBS \cdot \left(1 - 0.5 \cdot \frac{dphpdt}{PHP} \cdot \Delta t\right)$$

$$CJ(t) = CJ \cdot \left(1 - 0.5 \cdot \frac{dpbdt}{PB} \cdot \Delta t\right)$$

$$CJSW(t) = CJSW \cdot \left(1 - 0.5 \cdot \frac{dphpdt}{PHP} \cdot \Delta t\right)$$

If TLEVC=3 and TLEV=0 or 1, then:

$$dpbdt = -\frac{\left[egnom + 3 \cdot vt(tnom) + (1.16 - egnom) \cdot \left(2 - \frac{tnom}{tnom + 1108}\right) - PB\right]}{tnom}$$

$$dphpdt = -\frac{\left[egnom + 3 \cdot vt(tnom) + (1.16 - egnom) \cdot \left(2 - \frac{tnom}{tnom + 1108}\right) - PHP\right]}{tnom}$$

For TLEV=2

$$dpbdt = -\frac{\left[egnom + 3 \cdot vt(tnom) + (EG - egnom) \cdot \left(2 - \frac{tnom}{tnom + GAP2}\right) - PB\right]}{tnom}$$

$$dphpdt = -\frac{\left[egnom + 3 \cdot vt(tnom) + (EG - egnom) \cdot \left(2 - \frac{tnom}{tnom + GAP2}\right) - PHP\right]}{tnom}$$

Surface Potential Temperature Equations

For TLEVC=0

$$PHI(t) = PHI \cdot \left(\frac{t}{tnom}\right) - vt(t) = \left[3 \cdot \ln\left(\frac{t}{tnom}\right) + \frac{egnom}{vt(tnom)} - \frac{eg(t)}{vt(t)}\right]$$

Appendix B: Technology Summary for HSPICE MOSFET Models

Temperature Parameters and Equations

For $TLEV=1$

$$PHI(t) = PHI - PTC \cdot \Delta t$$

If you do not specify the PHI parameter, simulation calculates it as:

$$PHI(t) = 2 \cdot vt(t) \cdot \ln\left(\frac{NSUB}{ni}\right)$$

The intrinsic carrier concentration, ni , must be temperature updated, and it is calculated from the silicon bandgap at room temperature.

$$ni = 145e16 \cdot \left(\frac{t}{tnom}\right)^{3/2} \cdot \exp\left[EG \cdot \left(\frac{t}{tnom} - 1\right) \cdot \left(\frac{1}{2 \cdot vt(t)}\right)\right]$$

For $TLEV=2$

$$PHI(t) = PHI - PTC \cdot \Delta t$$

For $TLEV=3$

$$PHI(t) = PHI + dphidt \cdot \Delta t$$

If $TLEV=3$ and $TLEV=0$ or 1 , then:

$$dphidt = -\frac{\left[egnom + 3 \cdot vt(tnom) + (1.16 - egnom) \cdot \left(2 - \frac{tnom}{tnom + 1108}\right) - PHI\right]}{tnom}$$

For $TLEV=2$

$$dphidt = -\frac{\left[egnom + 3 \cdot vt(tnom) + (EG - egnom) \cdot \left(2 - \frac{tnom}{tnom + GAP2}\right) - PHI\right]}{tnom}$$

Threshold Voltage Temperature Equations

The threshold temperature equations are:

For $TLEV=0$

$$vbi(t) = vbi(tnom) + \frac{PHI(t) - PHI}{2} + \frac{egnom - eg(t)}{2}$$

$$VTO(t) = vbi(t) + GAMMA \cdot (PHI(t))^{1/2}$$

For $TLEV=1$

$$VTO(t) = VTO - TCV \cdot \Delta t$$

$$vbi(t) = VTO(t) - GAMMA \cdot \ln(PHI(t))^{1/2}$$

For TLEV=2

$$VTO(t) = VTO + \left(1 + \frac{GAMMA}{2 \cdot PHI^{1/2}}\right) \cdot dphidt \cdot \Delta t$$

$$vbi(t) = VTO(t) - GAMMA \cdot \ln(PHI(t))^{1/2}$$

Mobility Temperature Equations

The MOS mobility temperature equations are:

$$UO(t) = UO \cdot \left(\frac{t}{tnom}\right)^{BEX}$$

$$KP(t) = KP \cdot \left(\frac{t}{tnom}\right)^{BEX}$$

$$F1(t) = F1 \cdot \left(\frac{t}{tnom}\right)^{F1EX}$$

Channel Length Modulation Temperature Equation

If you specify the LAMEX model parameter, then the temperature modifies the LAMBDA value.

$$LAMBDA(t) = LAMBDA \cdot (1 + LAMEX \cdot \Delta t)$$

Calculating Diode Resistance Temperature Equations

The following equations are examples of the effective drain and source resistance:

$$RD(t) = RS \cdot (1 + TRD \cdot \Delta t), RS(t) = RS \cdot (1 + TRS \cdot \Delta t)$$

Appendix B: Technology Summary for HSPICE MOSFET Models

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