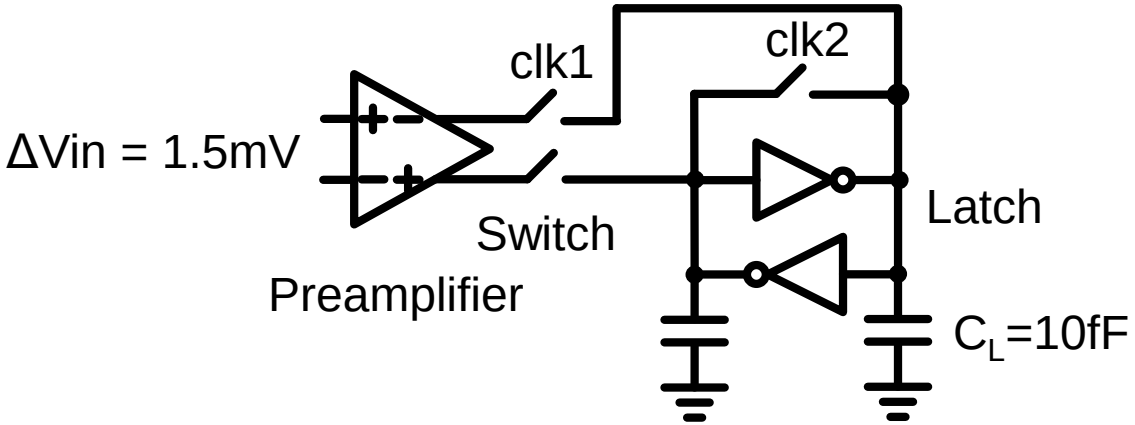
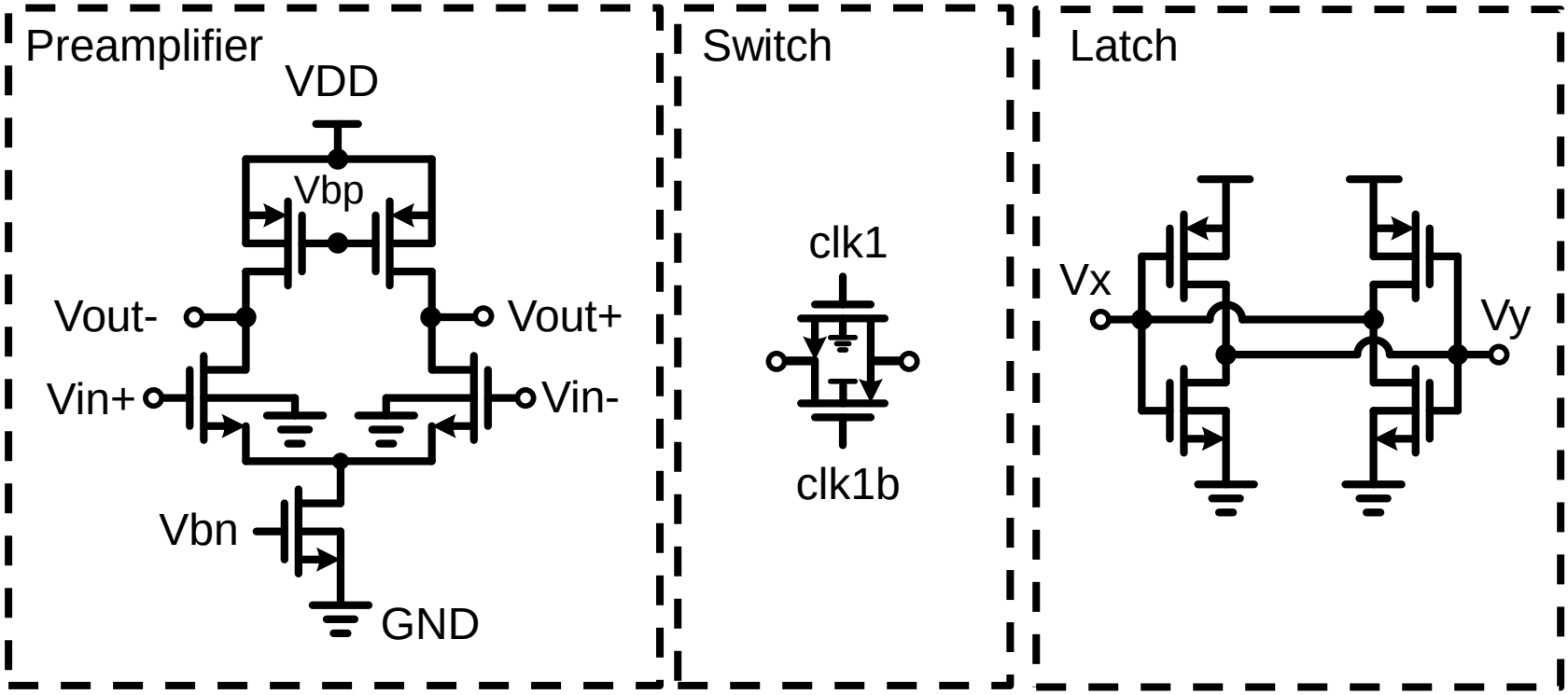
Analog IC Design Homework 4 (1/6)

- 1. Using CIC 0.18μm 1.8V SPICE Model (cic018.l).
- 2. Please optimize the comparator shown in P.2 by calculation with ΔVin = 1.5mV. Preamplifier can be referenced from the attachment or designed by yourself. Circuit operation is shown in P.3 (t_1+t_2 is the enlarge time of preamplifier), the specifications are as follows:
  - Preamplifier
    - DC gain = 8~12 V/V / 3-dB frequency ≧ 1.6GHz / Power supply VDD = 1.8V
  - Total compare time (Tc) ≦ 0.38 ns
    - Tc: Period between preamplifier get started and the output voltage of latch either is more than 1.7V of less than 0.1V.
  - Load of Latch (C_L) = 10 fF (Load is included in testbench file.)
- 3. Please use HSPICE to verify the comparator with ideal switch (turn on:1mΩ, turn off:100MΩ) (Include preamplifier, switches and latch circuit), t_2=5ps. Please use the attached testbench.
- 4. Please use HSPICE to verify the comparator with real switch (Include preamplifier, switches and latch circuit).Please set t_2 yourself. Please use the attached testbench.
- 5. Compare and analyze the results between calculation and HSPICE verification.

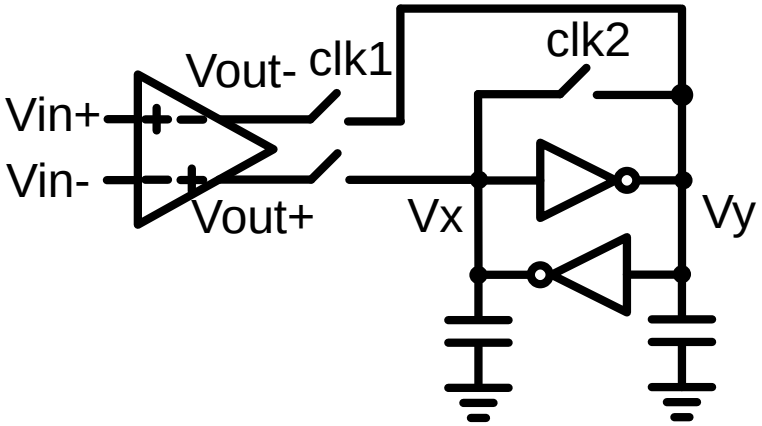
- Note
  - Follow design rules of maximum and minimum transistor width and length.
  - You can use external voltage sources instead of bias circuit, but the voltage should be limited between 0V to 1.8V.
  - All transistor's body should connect to VDD or GND.
  - Please use Cadence Virtuoso to build schematic and export the .cir file for verification.

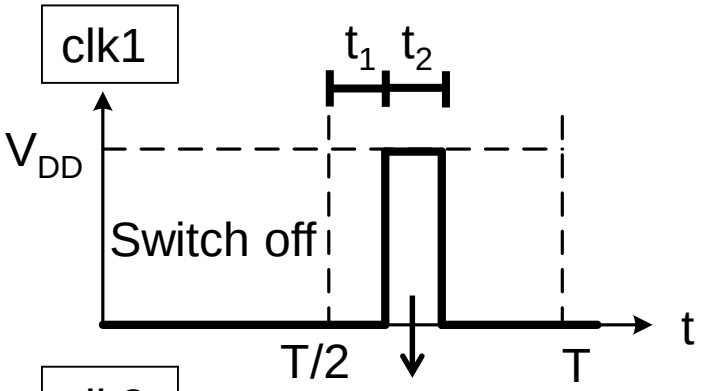
Analog IC Design Homework 4 (2/6)

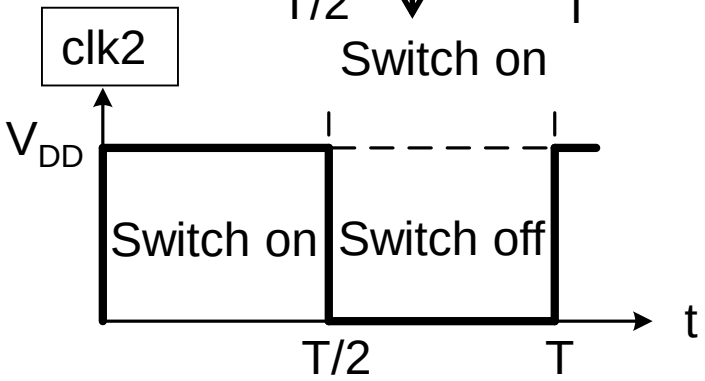


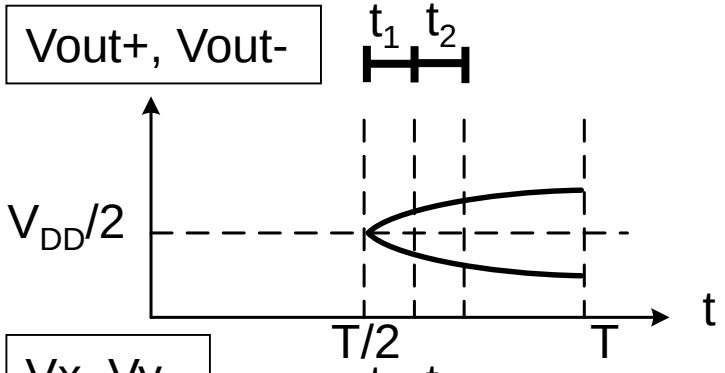


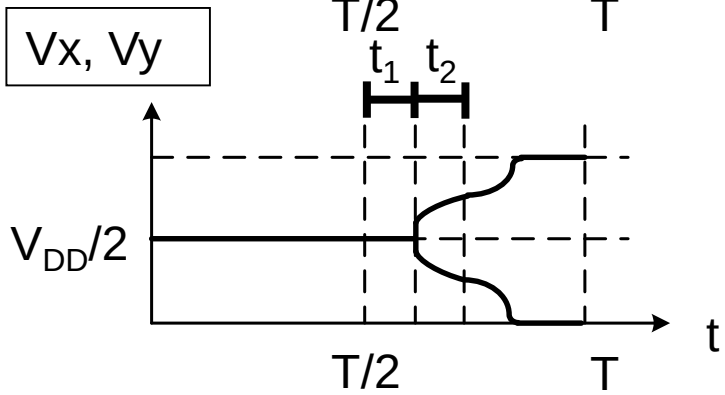
Analog IC Design Homework 4 (3/6)











Analog IC Design Homework 4 (4/6)

- Your report should include
  - Design flow
  - HSPICE verification results
    - Please show the waveform and mark the Total compare time,Tc.
  - Virtuoso schematic
    - Include the .cir file and circuit diagram
  - Area
    - MOSFET：Please calculate the sum of the W*L for all the MOS used in the designed circuit $A_{MOS} = \sum W_i \times L_i$
    - Capacitor：Just show the capacitance (if used)
    - Resistor：Just show the resistance (if used)
  - Total current and power consumption
  - Table of specifications (shown in P.6)

- Note: The total current, power consumption and area should include preamplifier, switches and latch circuit

Analog IC Design Homework 4 (5/6)

- Grading
  - Please name all nodes and transistors as shown in P.2 and P.3
  - Under the condition of all circuits are composed of MOS, R and C and meet the test conditions, the smaller Tc, area, and power consumption will receive higher scores. (According to the circuit design of TT corner, please upload the subckt.sp)
  - Extra points: Design this circuit to meet specifications in TT, SS, FF corner. (You can design anther circuit not only to satisfy at TT corner and upload the subckts_bonus.sp)
  - Please clearly describe the design flow in your report and attach your calculation process. (Do not copy)
  - Report with simulation results only but no design flow will get deducted points according to the situation.
  - Report with advanced discussion and analysis will receive higher scores.
- Precautions
  - Deadline: 10/29/2023(Sun.) 23:59:59 pm (不接受作業補交)
  - Personal work, please upload Word and HSPICE code (.sp file and .cir file) to moodle
  - Please compress files into a .zip file and name it as HW#_student ID,
    ex: HW2_E24086535 Font size: 12pt (Chinese: 標楷體, English: Times New Roman)
  - Refer to the IEEE submission regulations, set the picture resolution to 300dpi.
  - Upload file size is recommended to be 2MB

Analog IC Design Homework 4 (6/6)

- Please attach the following table to the last page of your HW4 report to help TA scoring

(Use real switches)

		Basic	Bonus (Optional)		
		TT	TT	SS	FF
Pre-amplifier	DC gain (V/V)				
	3-dB frequency (GHz)				
Whole Comparator	Tc (ps)				
	Area (μm^2)				
	Current (μA)				