Analog IC Design Homework 5 (1/6)

- 1. Using CIC 0.18μm 1.8V SPICE Model (cic018.l)
- 2. Please optimize the Comparator shown in P.2 by calculation with ΔVin = -0.5mV
    - Circuit operation is shown in P.2, the specifications are as follows:
        - Power supply V_{DD} = 1.8V
        - Total compare time (Tc) ≦ 1.2ns
            - Tc: Period between preamplifier get started and the output voltage of latch either is more than 1.7V of less than 0.1V
        - Load of Latch (C_L) = 10 fF (Load is included in testbench file.)
- 3. Please use HSPICE to verify the comparator with t_{on}=100ns
    - Please use the attached testbench to test your circuit
- 4. Please design the offset cancellation circuit to cancel input offset voltage. Please use the size you have designed in 2., and increase/decrease the width of positive/negative input by 0.1 μm. You can design the circuit by yourself or refer to circuit in P.3
- 5. Please use HSPICE to verify comparator with offset cancellation
- 6. Compare and analyze the results between calculation and HSPICE verification
- Note
    - Follow design rules of maximum and minimum transistor width and length
    - For 4., you can use ideal switch(turn on:1mΩ, turn off:100MΩ) and the external clk source to achieve offset cancellation circuit
    - All transistor's body should connect to VDD or GND
    - Please use Cadence Virtuoso to build schematic and export the .cir file for verification

- Circuit diagram
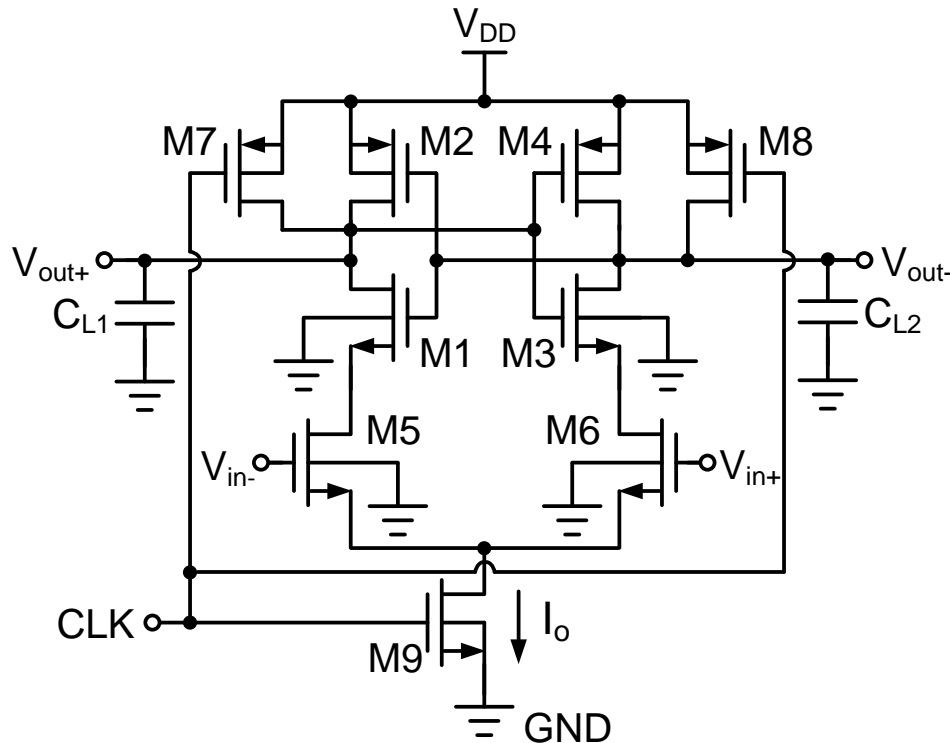
- Waveforms
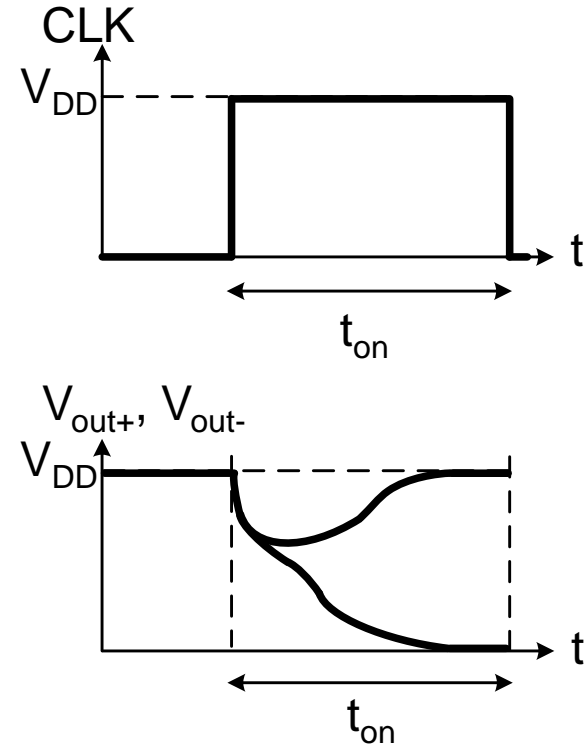
- Operation
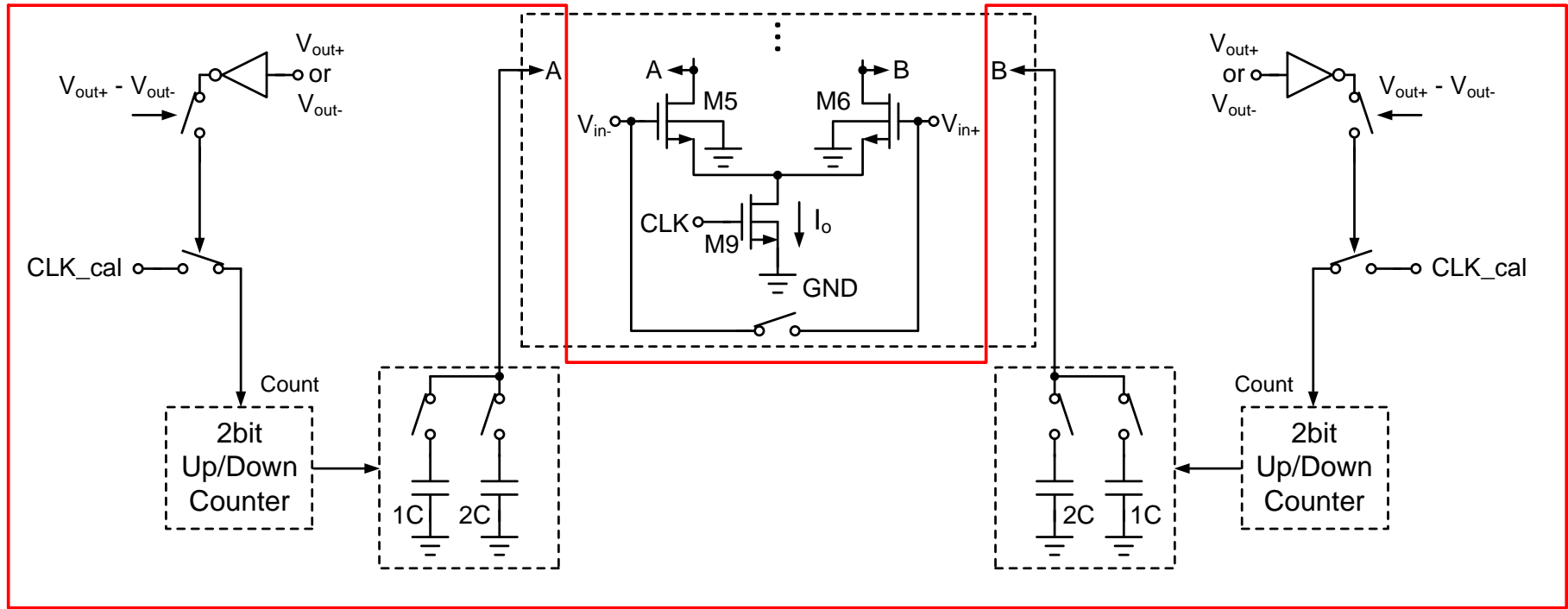 - ◆ CLK off → Reset V_{out+} and V_{out-} to V_{DD}
  - ◆ CLK on → ΔVin makes I_{M5} and I_{M6} different
    → different discharging speed of C_L → $ΔV_{out}$
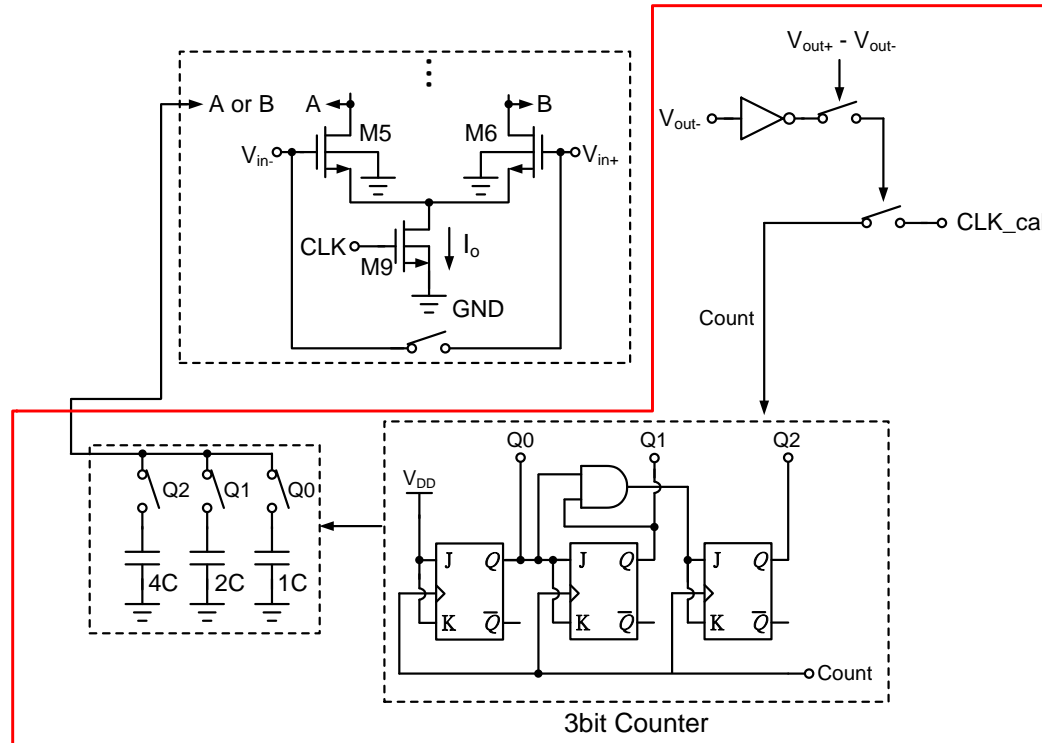   → latch positive feedback

- Reference

- Note
  - ◆ You can design the circuit in red frame by yourself
  - ◆ Please finish the offset cancellation before CLK on in P.2. CLK signal in testbench can be modified (But the timing, period, t_{on} of original turn on state is not changed)
  - ◆ Please descript the circuit operation principle in detail

Analog IC Design Homework 5 (4/6)

- Reference

- Note
  - ◆ You can design the circuit in red frame by yourself
    - ➤ You have to design the Up/Down counter in this example
  - ◆ Please finish the offset cancellation before CLK on in P.2. CLK signal in testbench can be modified (But the timing, period, t_{on} of original turn on state is not changed)
  - ◆ Please descript the circuit operation principle in detail

Analog IC Design Homework 5 (5/6)

- Your report should include
  - ◆ Design flow
  - ◆ HSPICE verification results
    - ➢ Please show the waveform and mark the Total compare time,Tc.
  - ◆ Virtuoso schematic (Include the .cir file and circuit diagram)
  - ◆ Area
    - ➢ MOSFET：Please calculate the sum of the W*L for all the MOS used in the designed circuit
    $$A_{MOS} = \sum W_i \times L_i$$
    - ➢ Capacitor：Just show the capacitance (if used)
    - ➢ Resistor：Just show the resistance (if used)
  - ◆ Total current and power consumption (M9 turn on) (including waveform)
  - ◆ Table of specifications

AIC HW5_Name		
Comparator	w/o Offset cancellation circuit	w/ Offset cancellation circuit
Tc (ps)		
Area (µm^2)		
Current (nA)		

Analog IC Design Homework 5 (6/6)

- Grading
  - Customization of the .sp file will not be accepted
  - Please name all nodes and transistors as shown in P.2 and P.3
  - Under the condition of all circuits are composed of MOS, R and C and meet the test conditions, the smaller Tc, area, and power consumption will receive higher scores. (According to the circuit design of TT corner, please upload the subckt.sp)
  - Extra points: Design the offset cancellation circuit in P.3 by yourself.
  - Please clearly describe the design flow in your report and attach your calculation process (Do not copy)
  - Report with simulation results only but no design flow will get deducted points according to the situation.
  - Report with advanced discussion and analysis will receive higher scores.

- Precautions
  - Deadline: 11/19/2023 (Sun.) 23:59:59 pm (不接受作業補交)
  - Personal work, please upload Word and HSPICE code (.sp file and .cir file) to moodle
  - Please compress files into a .zip file and name it as HW#_student ID, ex: HW5_E24064088 Font size: 12pt (Chinese: 標楷體, English: Times New Roman)
  - Refer to the IEEE submission regulations, set the picture resolution to 300dpi.
  - Upload file size is recommended to be 2MB

IEET問卷調查

- 請修課的同學，上網填寫工程認證問卷，網址如下：http://ieet.ee.ncku.edu.tw/ieet/student/ (IEET問卷調查系統)
- 進入系統後，請點選"忘記密碼"，之後到學校信箱收信，於信件中取得密碼後，並點選連結啟動新密碼，即可填寫問卷。