Final Exam Analog IC Design NCKUEE

1. For the system in Fig. P1(a), the sampling frequency f_s of the ideal ADC is 150 kHz and the spectrum of $x_a(t)$ is shown in Fig. P1(b).
   (a) Please design the cut off frequency ω_c of the ideal low pass filter shown in Fig. P1(c) to avoid the aliasing effect when the down-sampling factor is 3. (5%)
   (b) Please plot the spectra of, $x_d[n]$, $x_{LPF}[n]$ and $x_{out}[n]$, respectively (You need to mark the magnitude and corresponding frequency on each spectrum). (15%)

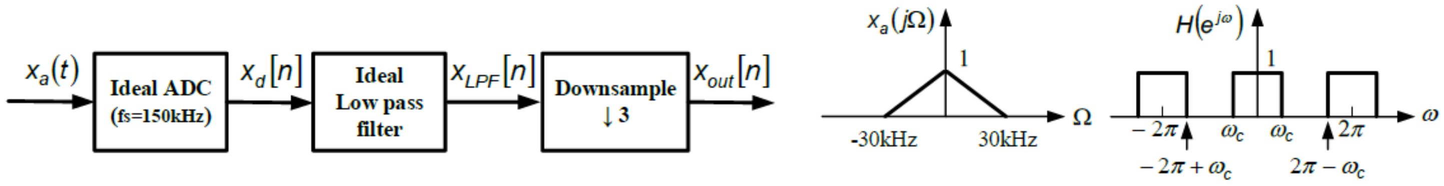

Fig. P1(a) Fig. P1(b) Fig. P1(c)

2. Briefly describe the following questions.
   (a) Draw a latched comparator circuit. Explain why its input hysteresis, i.e., memory effect, exists. (5%)
   (b) Please draw the circuit diagram of a 3-bit flash A/D converter. Explain what problems should be noticed in designing this type of ADC (List at least 2 problem). (10%)
   (c) Please draw the circuit diagrams of a 3-bit binary-weighted DAC and a thermometer-code current-steering DAC. Please evaluate the maximum DNL and gain-error for these two DACs' in (a), respectively. Assume the maximum mismatch error of 1:1 current mirror is ±1%. (20%)
   (d) List and briefly explain a S/H circuit design with signal-independent switch errors. Please give 2 methods to minimize signal-dependent switch error, and explain how they work. (10%)
   (e) Please explain the pre-filtering and post-filtering strategies for conventional high-resolution signal-processing systems utilizing Nyquist-rate ADCs and DACs, respectively. (20%)
   (f) Please explain the pre-filtering strategies for conventional Nyquist-rate A/D converters (5%) and oversampling A/D converters. Explain the bandwidths chosen for the filters used. (5%)
   (g) Draw the cross section of the parasitic PNP and the circuit diagram of CMOS N-well bandgap voltage reference operating in weak inversion. Derive an equation to express the reference voltage V_{ref}. Channel length modulation effect can be ignored. Please explain why a bandgap voltage reference is temperature independent. (10%)
   (h) Briefly explain the absolute accuracy of data converter and list three main errors included in it. (5%)
   (i) Please draw the circuit diagram of a 3-bit successive approximation (SA) A/D converter and briefly explain its operation (3 phases). (10%)
3. What is the SNR of an ideal 12-bit unipolar ADC with V_{REF}=0.8V when a sinusoidal input of 0.15V~0.65V is applied? (5%) What size input (V_{pp}) would result in an SNR of 35dB? (5%)
4. A sinusoidal input of 0.8V_{pp} is applied to an ideal N-bit unipolar ADC with V_{ref}=1V. If the requirement of SNR is at least 70dB, please calculate the minimum bit number N and find SNR when the amplitude of sinusoidal input is changed to 60mV_{pp}.

5. A Multiplying DAC (MDAC) and the waveform of its non-overlapped clock is shown in Fig. P5 (a) and Fig. P5 (b), respectively. In an ideal case, the MDAC output can be expressed as $V_{out}=2V_{in}$. However, in an actual case, the opamp finite DC gain, A, parasitic capacitor of opamp input node, C_p, and capacitor mismatch, $C_s \neq C_f$, would degrade the accuracy of the MDAC output.
   (a) Please express the MDAC output in term of A, C_s, C_f, C_p and V_{in}. (10%)
   (b) Assuming $C_f=C_s=C$ and $C_p=1/20C$, please calculate the minimum opamp DC gain A such that |2Vin-Vout| is less than 0.001Vin? (5%)

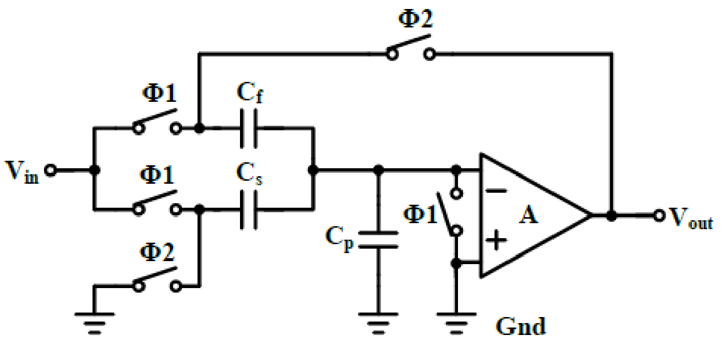

Fig. P5(a)

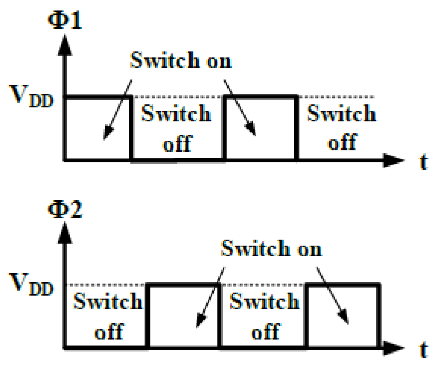

Fig. P5(b)

6. Fig. P6 shows a 3-bit R-2R-based DAC. Due to mismatch effect, the resistance of R_A and R_B are 0.9R and 1.1R respectively. Assume that the opamp is ideal, V_{REF}=1.8V and R_f=R. (Hint: Compared with ideal R-2R-based DAC)
   (a) Find the offset and gain errors in unit of LSB. (6%)
   (b) Find the INL (endpoint) errors in unit of LSB. (12%)
   (c) Find the DNL errors in unit of LSB. (12%)
   (d) Is this DAC monotonic? Why? (5%)

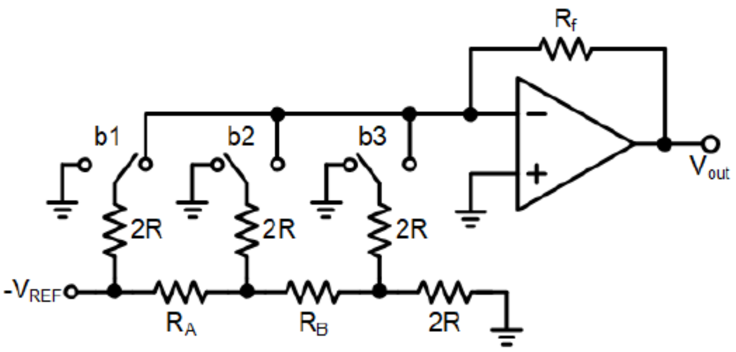

Fig. P6

7. Consider a 3-bit D/A converter in which V_{REF} = 1.2V (that is, 000 refers to 0V and 111 refers to 1.05V), with the following measured voltage values: { 0.031 : 0.204 : 0.312 : 0.467 : 0.619 : 0.814 : 0.802 : 1.124}
   (a) Find the offset and gain errors in unit of LSB. (10%)
   (b) Find the INL (endpoint) errors in unit of LSB. (10%)
   (c) Find the DNL errors in unit of LSB. (10%)
   (d) Is the input/output transfer curve of the D/A converter monotonic? Why? (5%)

8. Fig. P8(a)~(c) shows a 5-bit modified successive approximation A/D converter which operates in different mode.
   (a) According to Fig. P8(a)~(c), please describe the operation. (6%)
   (b) According to Fig. P8(a)~(c), please calculate the V_x value in terms of V_{in}, V_{ref} where parasitic capacitance (C_p) at node V_x can be ignored. (9%)
   (c) Assume parasitic capacitance (C_p) at node V_x can be ignored. Please derive the digital output (b_1~b_5) where V_{in} = 1.15V and V_{ref} = 2V. (5%)
   (d) Assume parasitic capacitance (C_p) of 3C exists at node V_x. Please calculate the V_x value where b_1~b_5 is switch to the digital output calculated in (b). (5%)

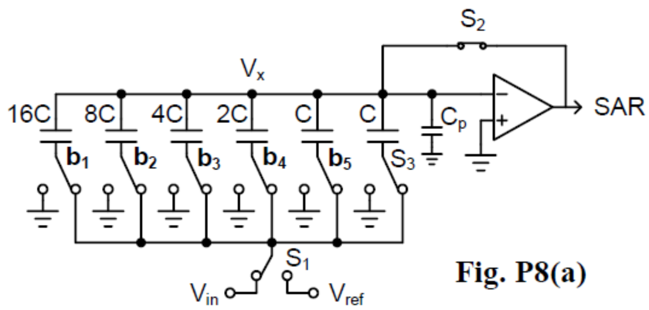

Fig. P8(a)

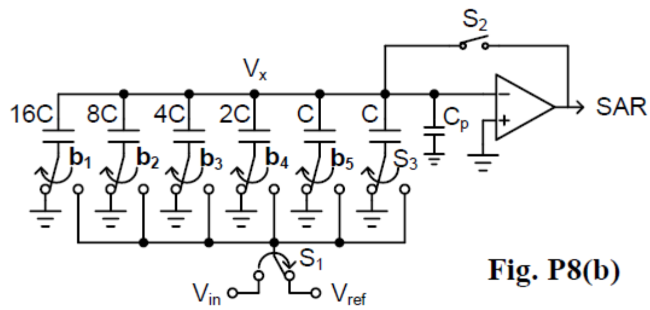

Fig. P8(b)

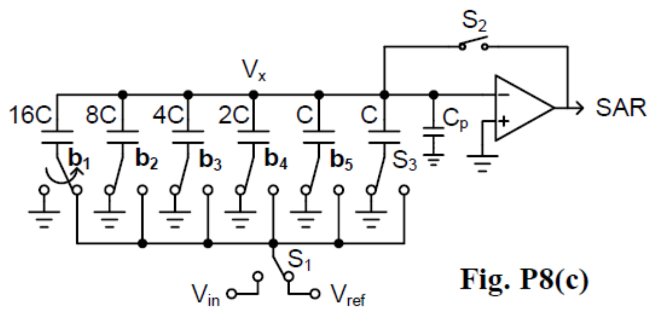

Fig. P8(c)

9. The deterministic approach for calculation of ADC quantization noise is shown in Fig. P9(a). A ramp input signal ($V_{in}(t)$) is injected into the ADC and the staircase output signal ($V_{out}(t)$) is the output of an ideal DAC converting the ADC digital output (B_{out}). Quantization error ($V_Q(t)$) can be given as $V_{out}(t) - V_{in}(t)$. Both $V_{in}(t)$ and $V_{out}(t)$ for the ideal 2-bit ADC is shown in Fig. P9(b). (No overloading is assumed.)
   (a) Please plot $V_Q(t)$ for the ideal 2-bit ADC and mark upper bound, lower bound, and timing. (10%)
   (b) Please derive root mean squared quantization error $V_Q(rms) = V_{LSB}/\sqrt{12}$. (10%)
   (c) Please derive SNR of N-bit ideal ADC under sine input signal with a peak-to-peak amplitude V_{ref}, where SNR (N-bit) = 6.02*N+1.76 (dB). (10%)

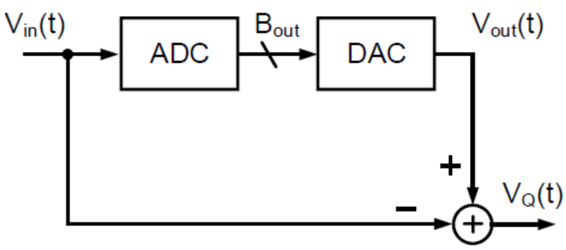

Fig. P9(a)

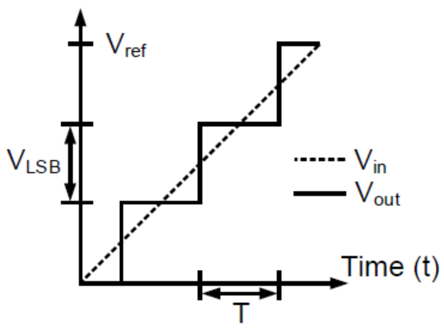

Fig. P9(b)

10. For a 4-bit R-2R-ladder DAC converter shown in Fig. P10, what is the output error (in LSBs) when input digital word is {b1 b2 b3 b4}={1 1 0 0} and R_A is 1.98R instead of ideal 2R?

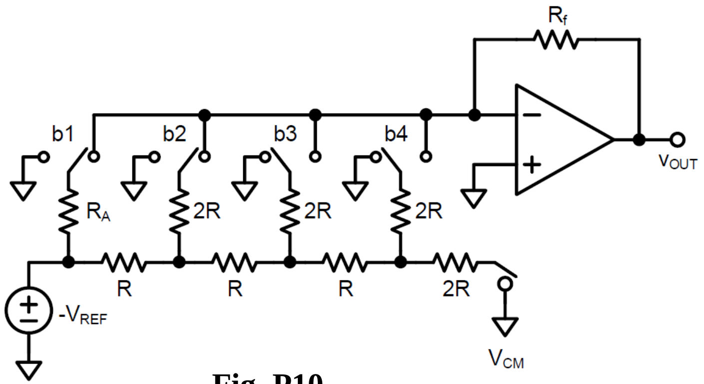

Fig. P10

11. Consider the multiply-by-two gain circuitry shown in Fig. P11.

(a) For C_1 is twice the capacitance of C_2, and assuming the opamp has an input offset designated as V_{off}, find the values of V_{C1}, V_{C2} and V_{out} at the end of each of the phases shown. (8%)

(b) What is the value of V_{out} when C_2 is twice the capacitance of C_1 at the end of the Phase4 ? (2%)

(c) How to obtain $V_{out} = 3\ V_{in}$ with this circuit ? (5%)

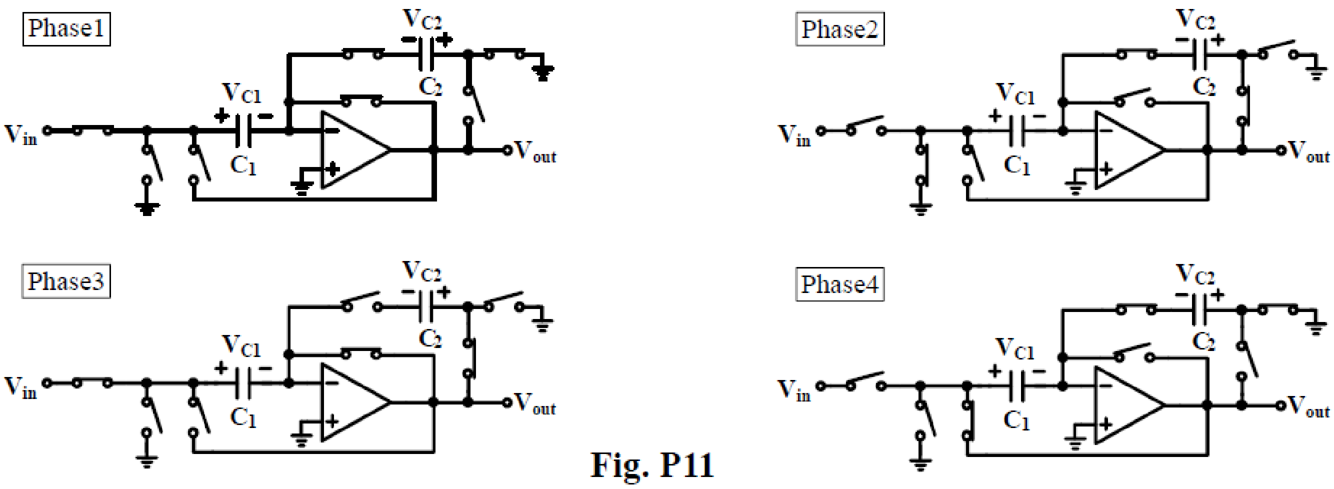

Fig. P11

12. Use C_H, $\mu_n C_{OX}$, (W/L), V_{DD} and NMOS threshold voltage (V_T) to answer question (a) and (b).

(a) In Fig P12 (a), please explain why an NMOS sampler passes a weak "1" and find the typical maximum output level of it. (5%)

(b) For the sampling circuit in Fig. P12 (b), please derive the output voltage v_O as a function of time (t), C_H, $\mu_n C_{OX}$, (W/L), V_{DD} and NMOS threshold voltage (V_T), where the initial output voltage is assumed to be v_O (t=0)=V_{DD}. (Neglect early effect and body effect.) (15%) Hint: MOS current in triode region: $I_D = \frac{1}{2}\mu_n C_{OX}\left(\frac{W}{L}\right)\{V_{DS}[2(V_{GS}-V_T)-V_{DS}]\}$

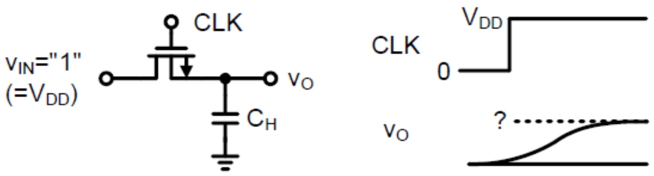

Fig. P12(a)

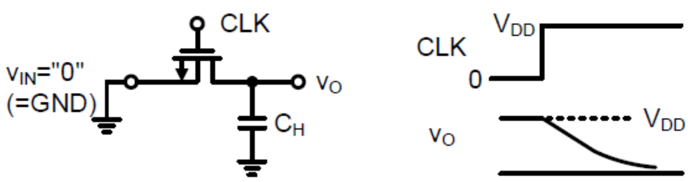

Fig. P12(b)

13. Two switched-capacitor integrators are shown in Fig. P13(a) and Fig. P13(b), where the non-overlapping clocks, Φ_1 and Φ_2, for both of them are depicted in Fig. P13(c). An extra switch near the output is shown to indicate that output signal is valid at the end of Φ_1. If the offset voltage V_{OFF} modelled at the non-inverting input are taken into consideration and the OPAMPs are assumed to be ideal, please
   (a) Derive the z-domain transfer function of V_{in} to V_{out} for Fig. P13(a) (7%)
   (b) Derive the z-domain transfer function of V_{in} to V_{out} for Fig. P13(b) (8%)
   (c) List 2 advantages of the integrator in Fig. P13(b) compared with the one in Fig. P13(a) (5%)

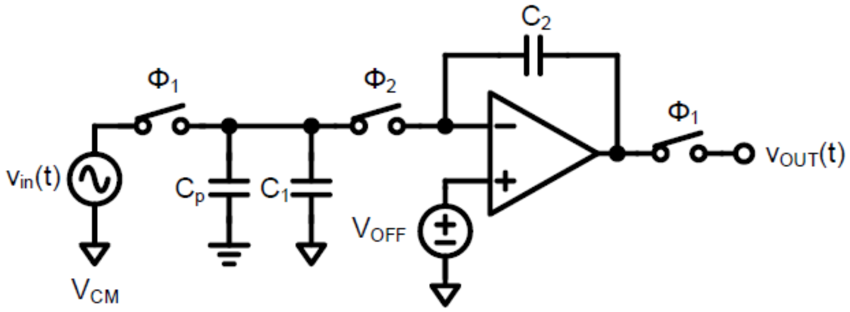

Fig. P13(a)

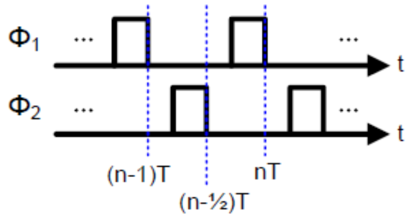

Fig. P13(c)

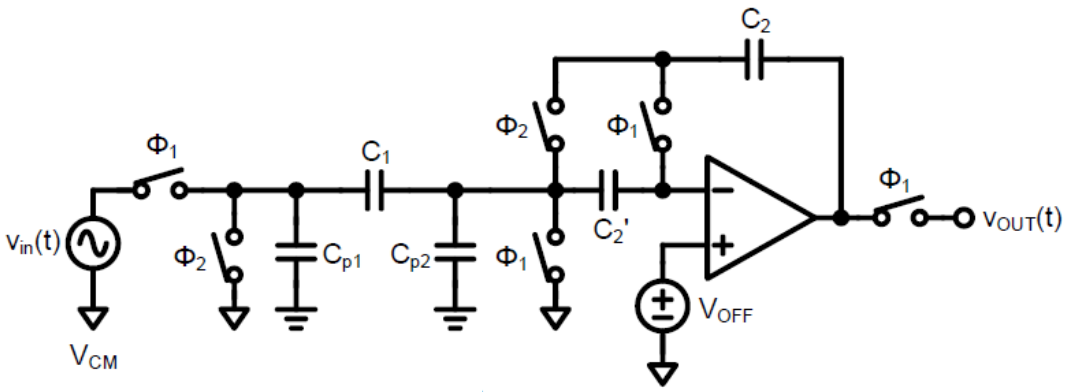

Fig. P13(b)

14. As shown in Fig. P14, the comparator is operated with offset cancellation, where C_{in} is the input capacitance of the OPAMP and A_o is the OPAMP gain. Assume that the three switches are ideal.
   (a) Briefly describe how this circuit operates. (5%)
   (b) Please derive V_{out} in terms of V_{in}, C_{main}, $C_{parasitic}$, C_{in} and A_o. (5%)
   (c) If the two terminals of C are interchanged, derive V_{out} in terms of V_{in}, C_{main}, $C_{parasitic}$, C_{in} and A_o. (5%)
   (d) Based on the derivations in (b) and (c), which placement of C is the better choice? (5%)

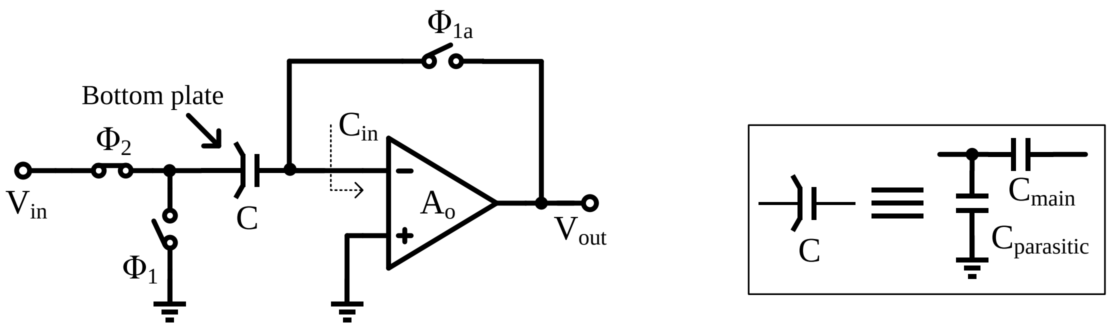

Fig. P14

15. A multiplying DAC (MDAC) of pipelined ADCs is shown in Fig. P15(a), where $C_s=3C_f$. Fig. P15(b) shows the corresponding non-overlapped waveforms. Neglect the effects of finite slew rate of OPAMP.

(a) Assume the OPAMP has a finite dc gain of 60dB and an infinite unity-gain bandwidth, please calculate the gain of MDAC. (10%) If the gain error, $|4V_{in}-V_{out}|$, is less than $0.002V_{in}$, please find the minimum required OPAMP dc gain. (5%)

(b) Assume the OPAMP has an infinite dc gain and a finite unity-gain bandwidth ω_u, where the OPAMP transfer function $A(s)=\frac{\omega_u}{s}$. Please calculate the minimum required ω_u such that 0.1% settling error in a time of 10ns can be achieved. (10%)

Hint : $\mathcal{L}^{-1}\left[1\Big/s\left(1+\dfrac{s}{\alpha}\right)\right]=\left(1-e^{-\alpha t}\right)\cdot u(t)$, where u(t) is a unit step function.

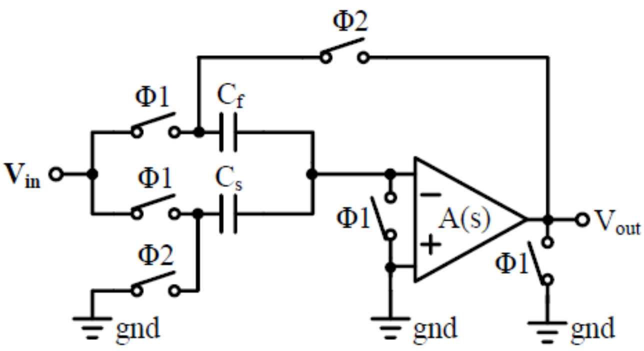

Fig. P15(a)

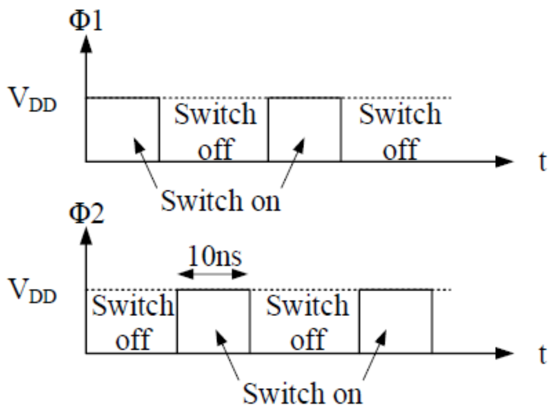

Fig. P15(b)

16. As shown in Fig. P16, there is a multiplying-by-four gain amplifier. The accuracy of the amplifier is influenced by OPAMP's offset voltage V_{offset}, OPAMP's noise $V_{n\_op}(t)$ and reference voltage's noise $V_{n\_vcm}(t)$. Assuming the gain of the OPAMP is infinite.

(a) Only considering the offset voltage V_{offset}, briefly describe how the circuit reduces the offset voltage V_{offset}. (5%)

(b) Only considering the OPAMP's noise $V_{n\_op}(t)$, please derive the z-domain transfer function of V_{n_op} to V_{out} and plot the gain v.s. frequency. (5%)

(c) Only considering the reference voltage's noise $V_{n\_vcm}(t)$, please derive the z-domain transfer function of V_{n_vcm} to V_{out} and plot the gain v.s. frequency. (5%)

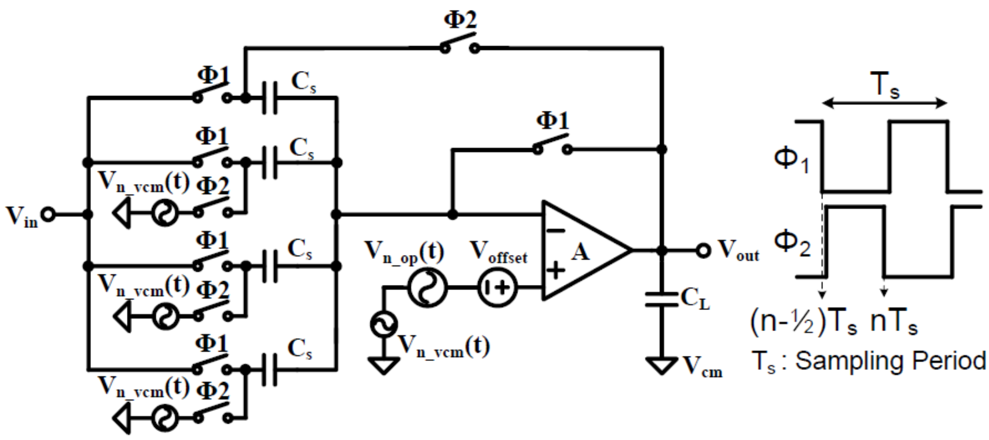

Fig. P16

17. For the circuit diagram shown in Fig. P17, please draw its ideal input/output characteristic, i.e., transfer curve and explain how the gain-error and offset-error are generated.

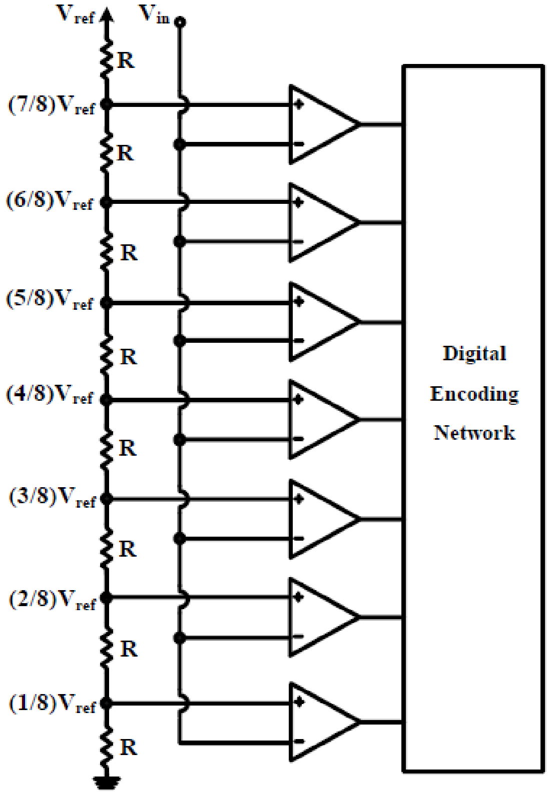

Fig. P17

18. Fig. P18(a) is a signal processing system including a switch-capacitor filter (SCF), an A/D converter, an ideal digital low pass filter (LPF), and a down-sampler. The ADC sampling rate f_S is 50kHz. The circuit of SCF is shown in Fig. P18(b), where $f_C=1/T_C=500$kHz and the ideal OPAMP has infinite dc gain and infinite unity-gain bandwidth. The frequency spectrum of the LPF response is shown is Fig. P18(c), where ω_u is LPF cut-off frequency.

(a) Derive the s-domain transfer function of V_{in} to V_{out} and its unity-gain frequency by using ω, C_1, C_2, and T_C in Fig. P18(b). Assume $\omega T_C \ll 1$.

(b) Derive the minimum C_2/C_1 ratio for SCF to prevent A/D converter from aliasing.

(c) Derive the maximum output frequency (unit: Hz) of Y_{out} to reconstruct signal without aliasing.

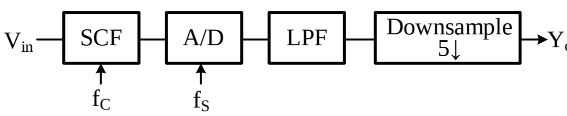

Fig. P18(a)

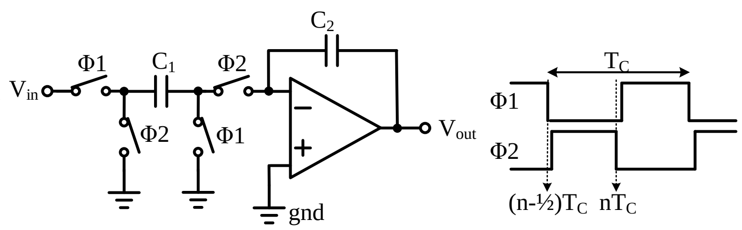

Fig. P18(b)

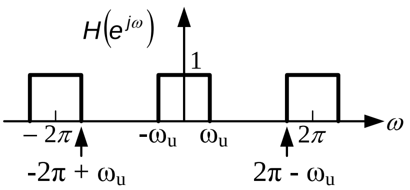

Fig. P18(c)

19. (a) Consider an 6-bit binary-weighted resistor D/A converter composed of R_1, R_2, … R_6 , where all resistor tolerances are $\pm$ 5%. Please derive the worst-case differential nonlinearity in units of LSBs and if the D/A converter can be guaranteed to be monotonic? Why?

(b) A 12-bit binary-weighted resistor D/A converter composed of R_1, R_2, … R_{12} produce a glitch voltage of -0.5V when digital code changes from 100...00 to 011…11 because MSB switch turns off early. Please derive the glitch voltage when MSB switching if a thermometer-code approach is used for the top 7 bits, whereas binary-weighting is used for the remaining 5 bits.