

Electronics (3) Homework2

Use level-1 SPICE model for MOSFET in **0.5μm** CMOS process (sedra_lib.lib)

- (1) Please design a two-stage CMOS OPAMP by **hand calculation**.

The circuit schematic is shown below. All process parameters are listed on p. B-9 of Appendix B in Sedra's CD. The specifications are listed below:

- ◆ DC gain ≥ 72 dB
- ◆ Unity-gain bandwidth $\geq (90-Y)$ MHz
- ◆ Phase margin ϕ_m : $60^\circ \leq \phi_m \leq 66^\circ$
- ◆ Slew rate (rise and fall) $\geq (60+X)$ V/ μ s
- ◆ Power supply voltage $V_{DD} = 3.3V$
- ◆ Load capacitance $C_L = 2.0\text{pF}$

<Note> X = 學號最後一碼

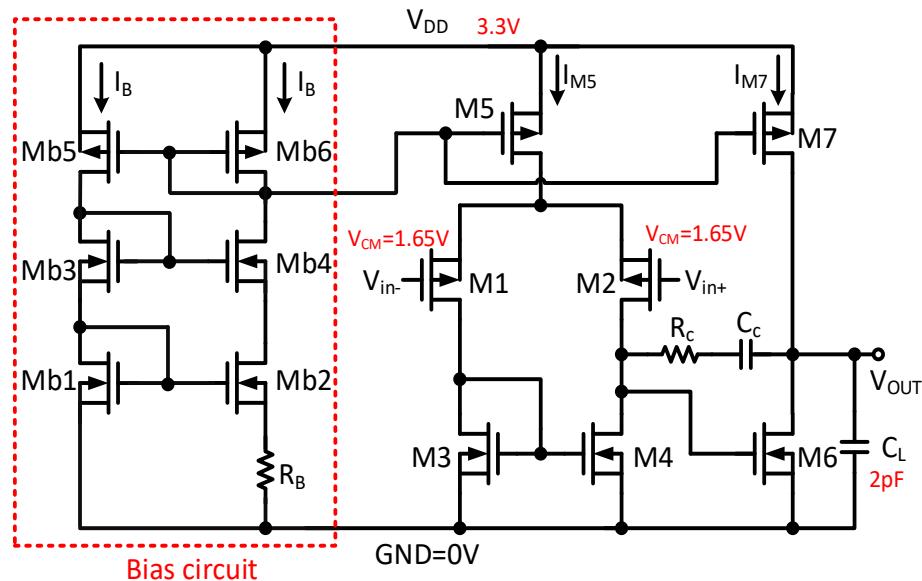
$$Y = 10 - X$$

<Example> E24036254

$$\rightarrow X = 4 \text{ and } Y = 6$$

\rightarrow Unity-Gain Bandwidth ≥ 84 MHz

\rightarrow Slew Rate ≥ 64 V/ μ s



Electronics (3) Homework2 (Cont.)

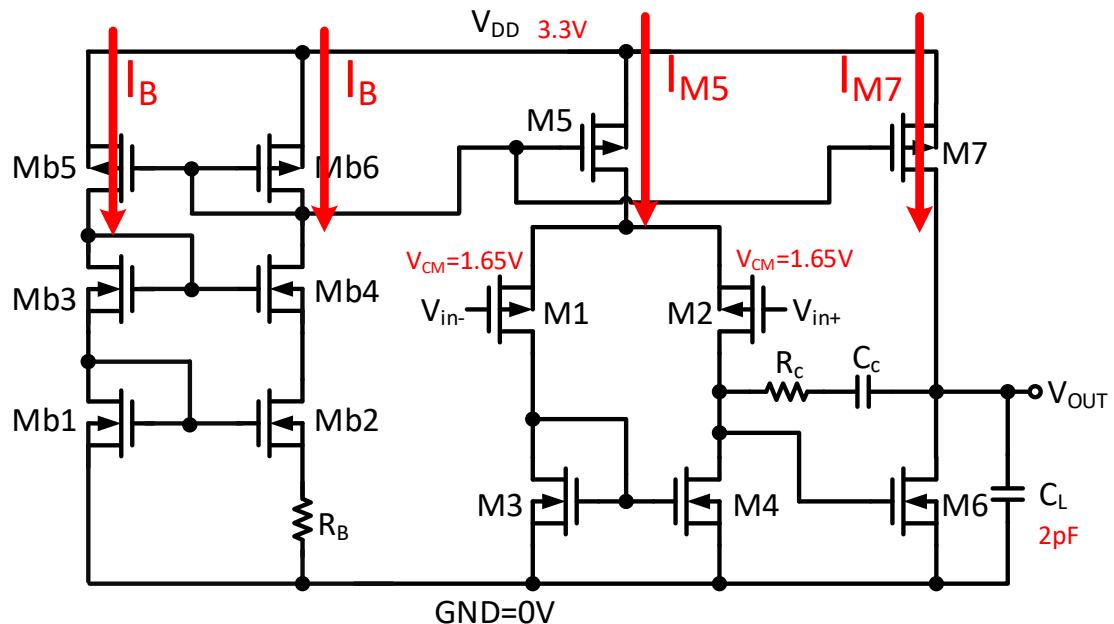
(2) Use PSpice to verify your design in (1)

(3) Please calculate

a. The total MOSFETs area : $A_{\text{total}} = \sum_{i=1}^7 (W_i \times L_i) + \sum_{i=1}^6 (W_{bi} \times L_{bi})$

b. The total power consumption : $P_{\text{total}} = V_{DD} \times (I_B + I_B + I_{M5} + I_{M7})$

c. $A_{\text{total}} \times P_{\text{total}}$



P.S: Smaller “ $A_{\text{total}} \times P_{\text{total}}$ ” designs will get better grades if they are verified to meet **all** the specifications

Notes

- Design examples for reference
 - ◆ Bias circuit on pp. 627 – 629 in the textbook (6th edition)
 - ◆ Example 10.1 on pp. 888 – 891 in the textbook (6th edition)
 - ◆ Example PS. 12.1 on pp. B-55 – B-60 of Appendix B in Sedra's CD
- Your report should include
 - ◆ Hand-calculation progress
 - ◆ PSpice circuit schematics
 - ◆ PSpice verification results with all specifications **clearly marked**
 - ◆ Verification results of **BOTH** positive and negative slew rates should meet the specification



- Upload your report to **MOODLE** in **Word** format
 - ◆ **Deadline: 23:59:59 on 2023/10/02 (Mon.) ;**
(2023/10/06 (Fri.) 前遲交一天原則上扣5分)
 - ◆ Filename example: HW2_鄭聿程_E2408XXXX_v1.doc (如更新請用v2, v3, ...)

Notes (Cont.)

- When verifying your hand calculation by PSpice
 - ◆ 軟體安裝與使用說明請參考Homework1的PSpice Tutorial
 - ◆ Correct the value of LAMBDA for NMOS0P5 to **0.1**
 - ◆ Use 4-terminal MOSFET models (NMOS0P5_BODY and PMOS0P5_BODY)
- Others
 - ◆ 請勿抄襲，抄襲等同考試作弊，將依校規處理
 - ◆ 此次作業佔學期總成績之5%
 - ◆ 作業若遇到問題，可於下列時段至奇美樓95302室與助教討論
 - 原定office hours：每週一17:00~18:00 and 每週五16:00~17:00
 - 新增時段：**每週四14:00~15:00**
 - ◆ 請注意手算過程之掃描圖檔務必清晰並轉正以利助教判讀
 - ◆ Word format
 - 字體12pt、單行間距、中英文字體分別為標楷體與Times New Roman
 - 頁碼置中於頁尾、各邊界2.54公分(上下邊界可依內容量縮減，但不得小於1.28公分)
 - 分別在每個繪圖下方與表格上方依序編號，並輔以caption描述
 - 圖表中的字體不小於10pt，尤其注意驗證波形圖的座標值
 - 驗證波形圖以白色為底，且重要驗證結果應清楚標記

Slew Rate Analysis of Two-Stage OPAMPs in General Cases

- Positive slew rate
- Negative slew rate

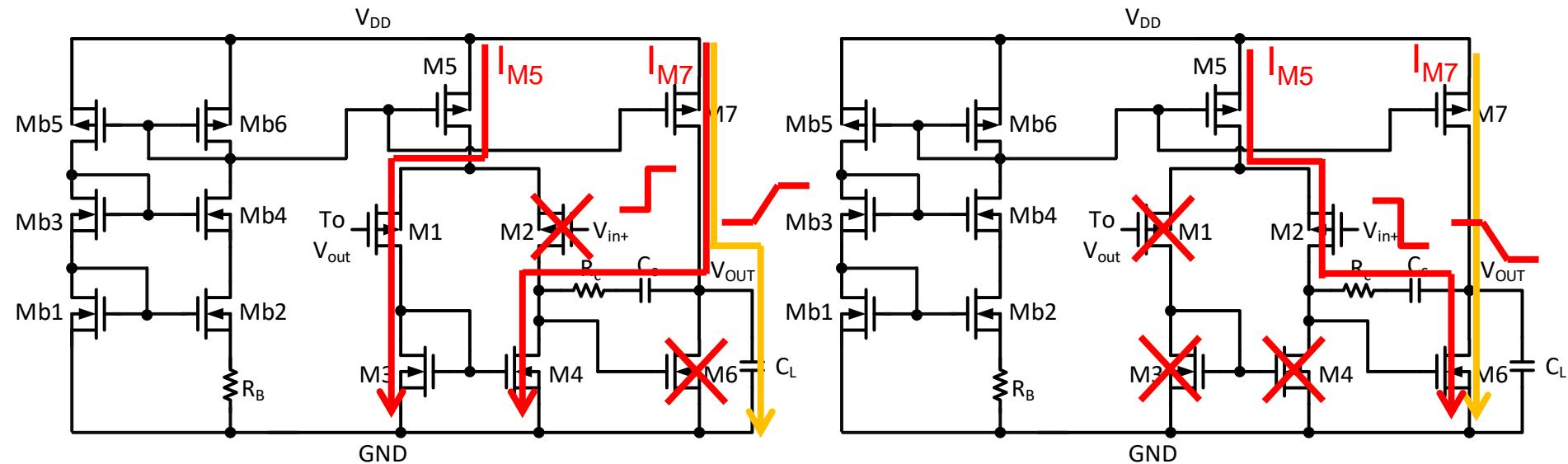
- ◆ If I_{M7} is large enough :

$$SR^+ \approx \frac{I_{M5}}{C_c}$$

- ◆ If I_{M7} is NOT large enough :

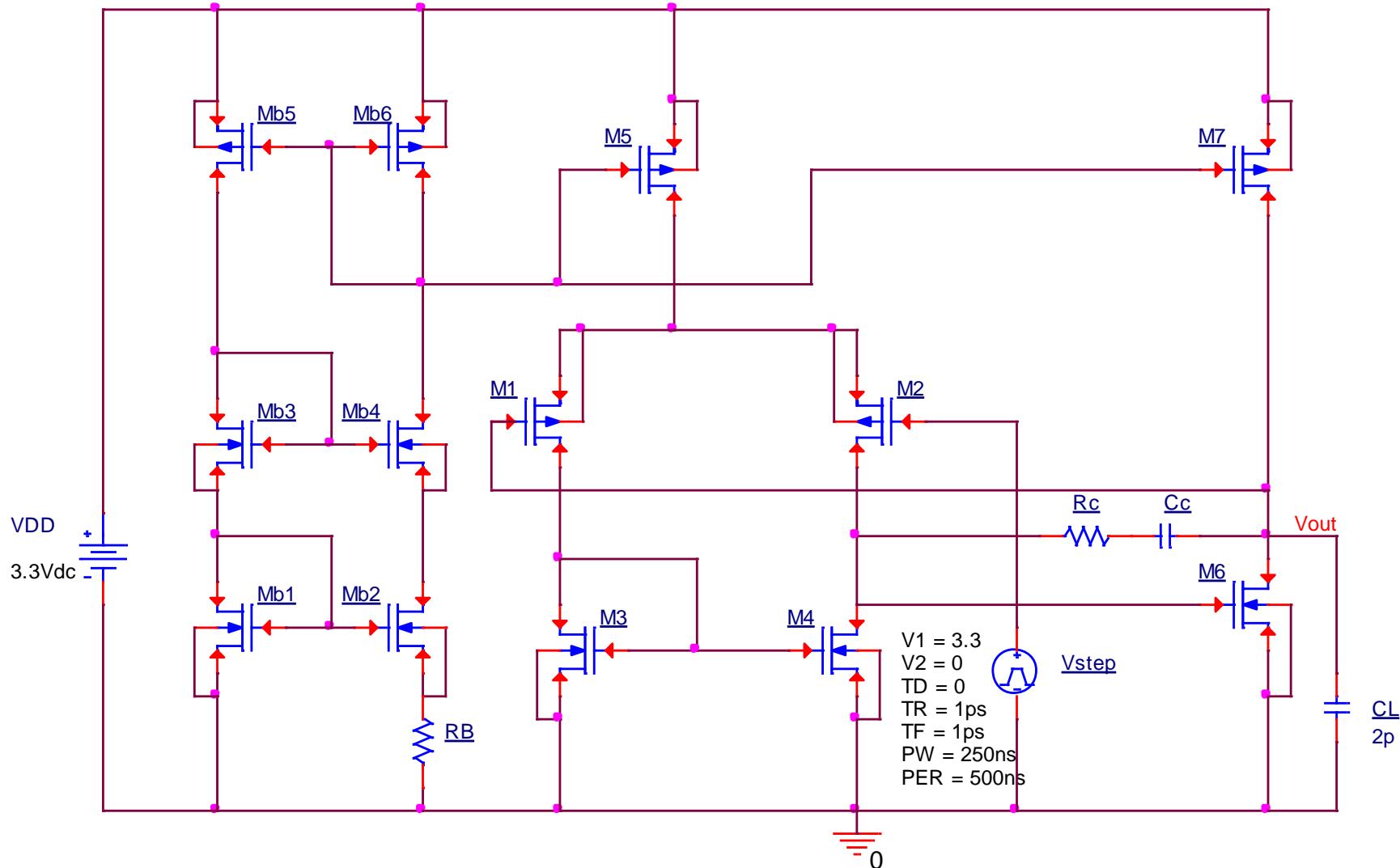
$$SR^+ \approx \frac{I_{M7}}{C_c + C_L}$$

$$SR^- \approx \frac{I_{M5}}{C_c}$$



PSpice Verification Example of Slew Rate

- Schematic



PSpice Verification Example of Slew Rate (Cont.)

- Waveforms

