Electronics (3) Homework3

1. Fig.1 shows a filter, where R_1=2MΩ, R_2=2MΩ, C_1=1nF, C_2=10pF, C_L=2pF. Assume that the OP_1 has an infinite DC gain and an infinite bandwidth, please
   (a) Derive the transfer function of the filter.
   (b) Draw the magnitude/phase Bode plots of the filter by hand.

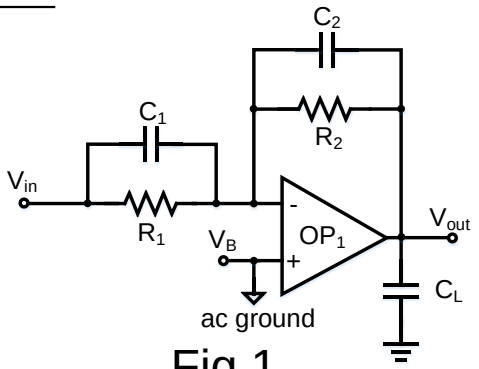


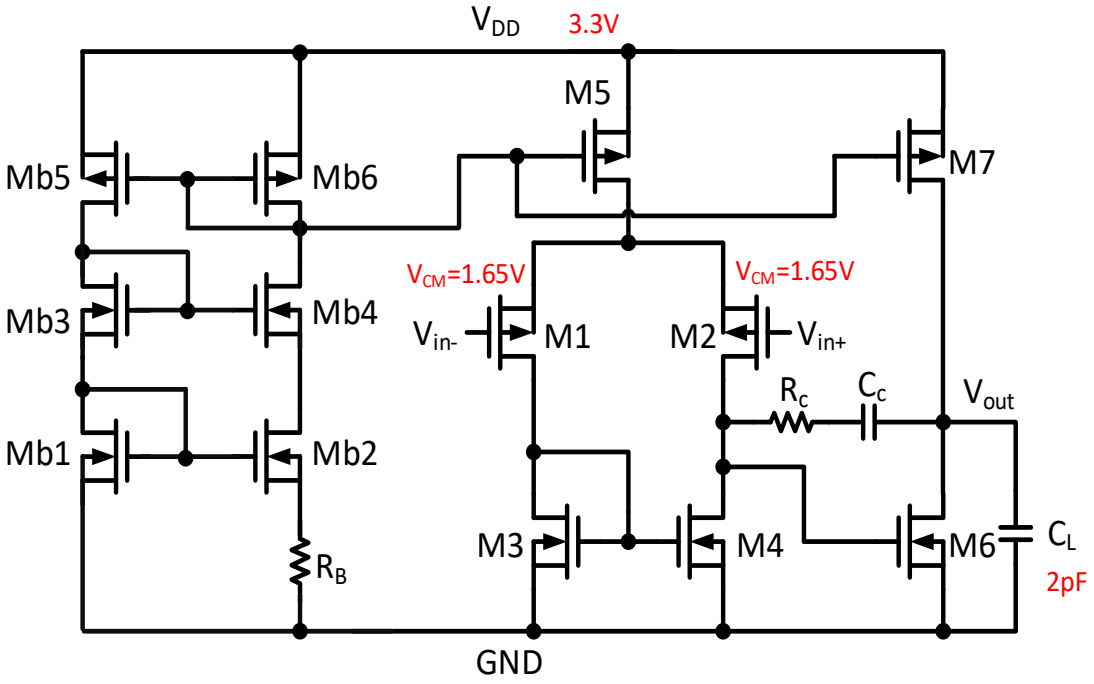
Fig.1

2. In Fig.1, assume that V_{DD}=3.3V, V_B is biased at 1.65V, and the common-mode voltage of V_{in} is V_{CM}=1.65V. Please replace the OP_1 with the transistor-level circuit of the two-stage op amp designed by yourself in HW2.
   (a) List the DC gain (A_0), unity-gain bandwidth (f_t), phase margin (PM), and slew rates (SR^+ and SR^-) of the op amp you used.
   (b) Draw the magnitude/phase Bode plots of the filter by PSpice AC-sweep simulation.
   (c) Discuss the difference of the plots in 1(b) and 2(b).

3. To verify 2(b), assume that $V_{in}(t) = V_{CM}+V_P \times \sin(2\pi f_{in} t)$, where V_{CM}=1.65V.
   (a) Let V_P=0.01V, please use PSpice time-domain simulation to measure the swing of $V_{out}(t)$ when f_{in}= 10Hz, 1KHz, 100KHz and 100MHz, respectively. Check if the results match the magnitude Bode plots in 2(b).
   (b) If V_P is changed to 0.02V, repeat 3(a) and discuss the difference.

Notes

- When verifying the filter circuit by PSpice, you MUST use an op amp which meets ALL specifications listed in HW2.
- If your original op amp in HW2 doesn't meet ALL of the specifications, you can re-design a two-stage op amp. Or, you can use the following op amp to finish HW3.



$$\left(\frac{W}{L}\right)_{M1,2}=\frac{5.5\mu m}{0.5\mu m},\ \left(\frac{W}{L}\right)_{M3,4}=\frac{1.4\mu m}{0.5\mu m},$$

$$\left(\frac{W}{L}\right)_{M5}=\frac{11\mu m}{0.5\mu m},\ \left(\frac{W}{L}\right)_{M6}=\frac{27\mu m}{0.5\mu m},$$

$$\left(\frac{W}{L}\right)_{M7}=\frac{105\mu m}{0.5\mu m},\ \left(\frac{W}{L}\right)_{Mb1,3\sim6}=\frac{1.25\mu m}{0.5\mu m},$$

$$\left(\frac{W}{L}\right)_{Mb2}=\frac{5\mu m}{0.5\mu m},\ R_B=18k\Omega,$$

$$C_C=0.15pF,\ R_C=685\Omega.$$

- Finishing HW3 with an op amp designed by yourself will get a better grade.

Notes (Cont.)

- Hints
  - According to page 38 of ch13's lecture slides, non-idealities of OP_1 might affect the frequency response of the filter.
  - Maximum slope of a signal $V_P \times \sin(2\pi f_{in} t)$ is $2\pi f_{in} \times V_P$.
- Your report should include
  - Hand-calculation progress
    - Derivation procedure in 1(a)
    - Brief drawing of magnitude/phase Bode plots in 1(b)
  - PSpice circuit schematics
    - Schematic of AC-sweep simulation in 2(b)
    - Schematic of time-domain simulation in 3(a)
  - PSpice verification results
    - Magnitude/phase Bode plots of filter in 2(b)
    - Time-domain waveforms of V_{out} in 3(a) and 3(b)
  - Discussion in 2(c) and 3(b)
- If you have re-designed a new op amp, your report should also include
  - Hand-calculation design procedure of the new op amp
  - Diagrams for verifying A_0, f_t, PM, SR^+, and SR^- of the new op amp

Notes (Cont.)

- When verifying your hand calculation by PSpice
  - 軟體安裝方式與使用介紹請參考Homework1的PSpice Tutorial
  - Correct the value of LAMBDA for NMOS0P5 to 0.1 (the same as on pp. B-9 of Appendix B in Sedra's CD)
  - Use 4-terminal MOSFET models (NMOS0P5_BODY and PMOS0P5_BODY)
- **Upload** your report **to MOODLE** in **Word** format
  - Deadline: 23:59:59 on 2023/11/20 (Mon.) (不接受作業補交)
  - Filename example: HW3_鄭聿程_E2408XXXX_v1.doc (如更新請用v2, v3, …)
  - Word format請參考Homework1, Homework2的Notes

- Others
  - 請勿抄襲，抄襲等同考試作弊，將依校規處理
  - 完成此次作業加學期總成績之1% (bonus)
  - 作業若遇到問題，可於下列時段至奇美樓95304室與助教討論
    - 原定office hours : 每週一17:00~18:00 and 每週五16:00~17:00
    - 新增時段：2023/11/09(Thu.) and 2023/11/16(Thu.) 14:00~15:00
  - 請注意手算過程之掃描圖檔務必清晰並轉正以利助教判讀