Electronics (3) Homework4

Use level-1 SPICE model for MOSFET in **0.5μm** CMOS process (sedra_lib.lib)

All process parameters are listed on p. B-9 of Appendix B in Sedra's CD.

(a) Please calculate the output swing of unity-gain buffer(Fig.3) with the two-stage class-A CMOS OPAMP shown in Fig.1, and then verify your results by PSpice with 0.5μm CMOS model in sedra_lib.lib (set L of all MOSFETs to 0.5μm)

Mb1	W=0.6μm	M6	W=60μm M=2
Mb2	W=2.4μm		
Mb3	W=1.25μm	M7	W=78μm M=2
Mb4	W=1.25μm		
Mb5	W=2.6μm	C_C	0.2pF
Mb6	W=2.6μm	R_C	2.1kΩ
M1	W=9.0μm	C_L	1pF
M2	W=9.0μm	C_O	1mF
M3	W=2.0μm	R_L	6kΩ
M4	W=2.0μm	R_B	25kΩ
M5	W=5.2μm		

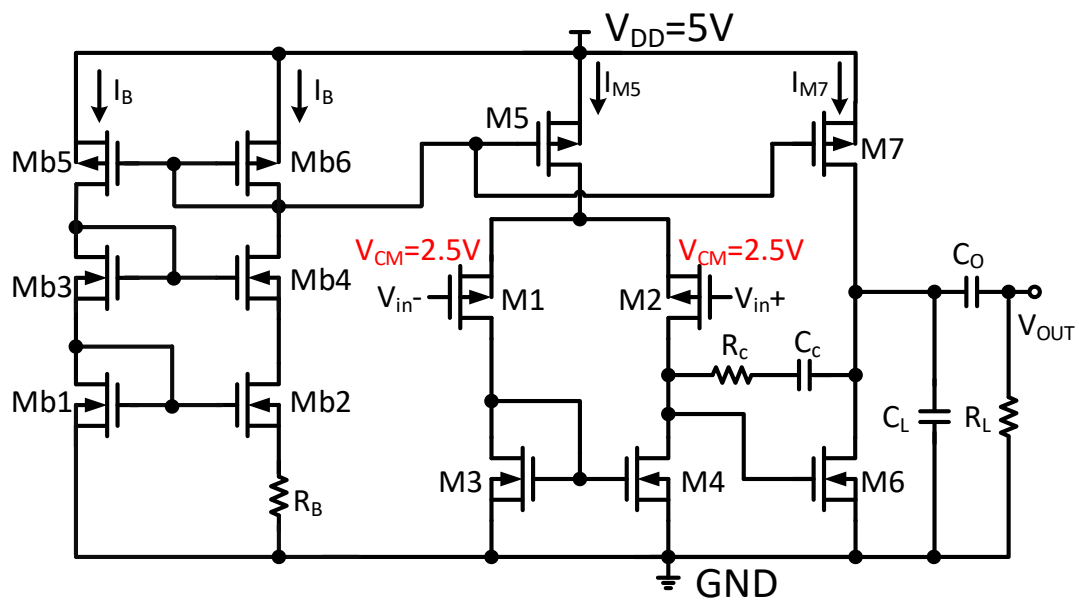


Fig.1

Note : set initial voltage across C_O to $V_{DD}/2$ to prevent long settling time

Electronics (3) Homework4 (Cont.)

(b) Please calculate the output swing of unity-gain buffer (Fig.3) with two-stage class-AB CMOS OPAMP shown in Fig.2, and then verify your results by PSpice with 0.5μm CMOS model in sedra_lib.lib (set L of all MOSFETs to 0.5μm)

Mb1	W=0.6μm	M7	W=10.4μm
Mb2	W=2.4μm	M8	W=4.5μm
Mb3	W=1.25μm	M9	W=15μm
Mb4	W=1.25μm	M10	W=9μm
Mb5	W=2.6μm	M11	W=30μm
Mb6	W=2.6μm	C_C	0.2pF
M1	W=9.0μm	R_C	2.3kΩ
M2	W=9.0μm	C_L	1pF
M3	W=2.0μm	C_O	1mF
M4	W=2.0μm	R_L	6kΩ
M5	W=5.2μm	R_B	25kΩ
M6	W=8.0μm		

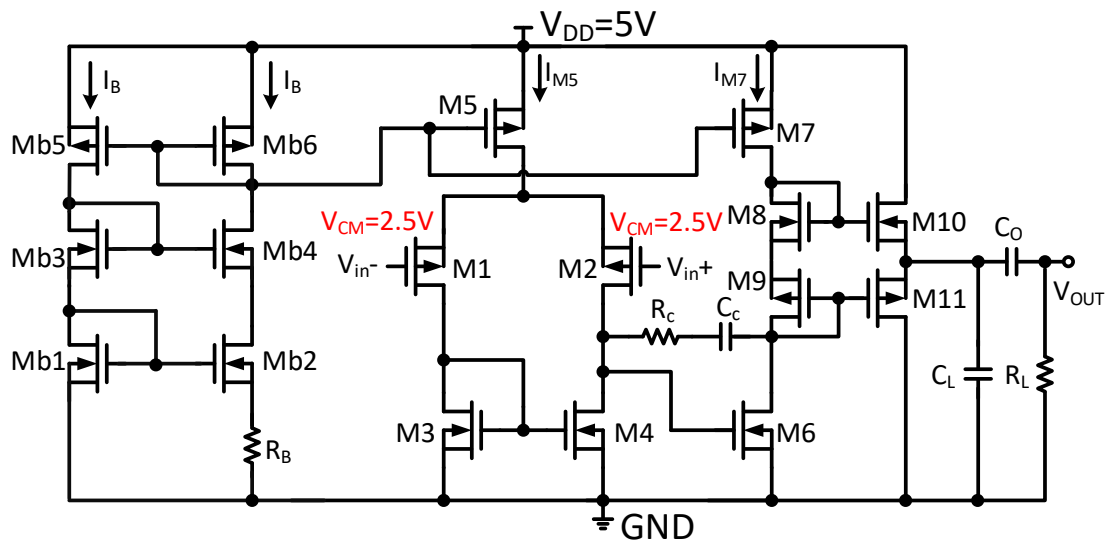


Fig.2

Note : set initial voltage across C_O to $V_{DD}/2$ to prevent long settling time

Electronics (3) Homework4 (Cont.)

(c) Please plot the conversion efficiency(η) vs. output power(P_{out}) figure of the unity-gain buffer shown in Fig. 3 with (i) the class-A OPAMP in Fig. 1 and (ii) the class-AB OPAMP in Fig. 2.

(As shown in Fig. 4, please use V_{in} = 1kHz sine wave, biased at a DC level of $V_{DD}/2$, with its amplitude of 0.1V, 0.4V, 0.7V, 1.0V, 1.3V, 1.6V, 1.9V, 2.2V, 2.5V)

(d)With the results in (c), please compare the maximal output power and efficiency of the class-A and the class-AB OPAMPs

$$\text{Conversion efficiency}(\eta) = \frac{\text{signal power deliver to load}}{\text{DC power supply to output circuit}} \times 100\%$$

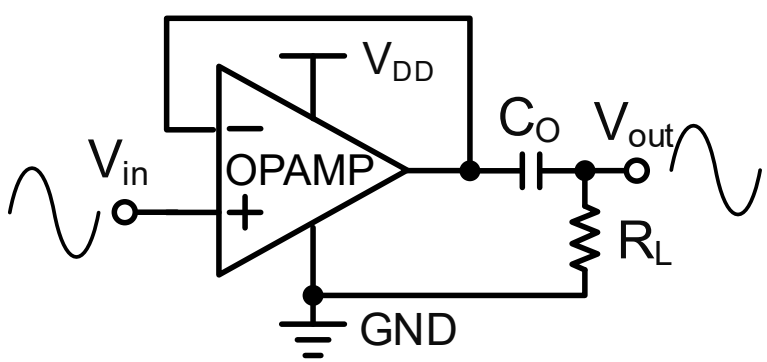


Fig.3

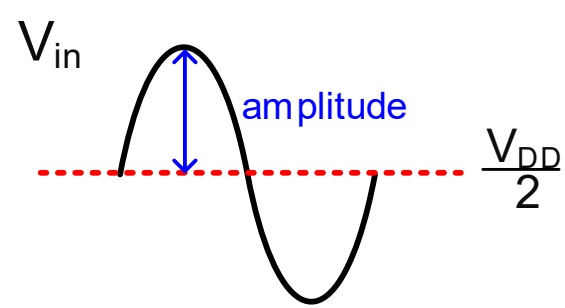
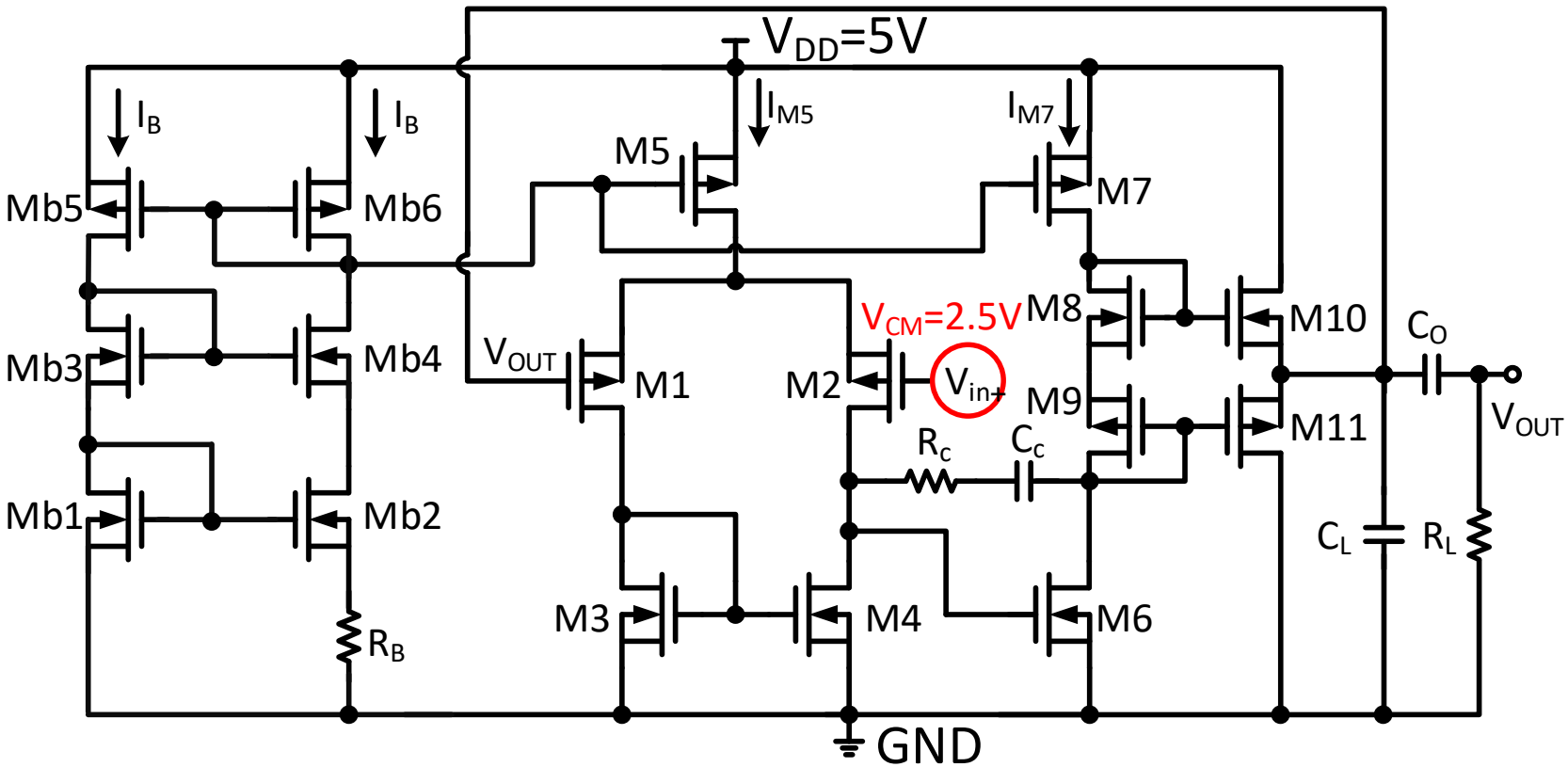


Fig.4

Note : set initial voltage across C_O to $V_{DD}/2$ to prevent long settling time

PSpice Verification Example of (a) and (b)

- Pspice simulation of maximal output swing (Class-AB as example)



- Set V_{in}+ = 1kHz sine wave, biased at a DC level of $V_{DD}/2$, with an amplitude of 2.5V (full swing)

PSpice Verification Example of (a) and (b) (Cont.)

- Setup of capacitor initial value
  - Double click on C_O and modify IC to $V_{DD}/2$

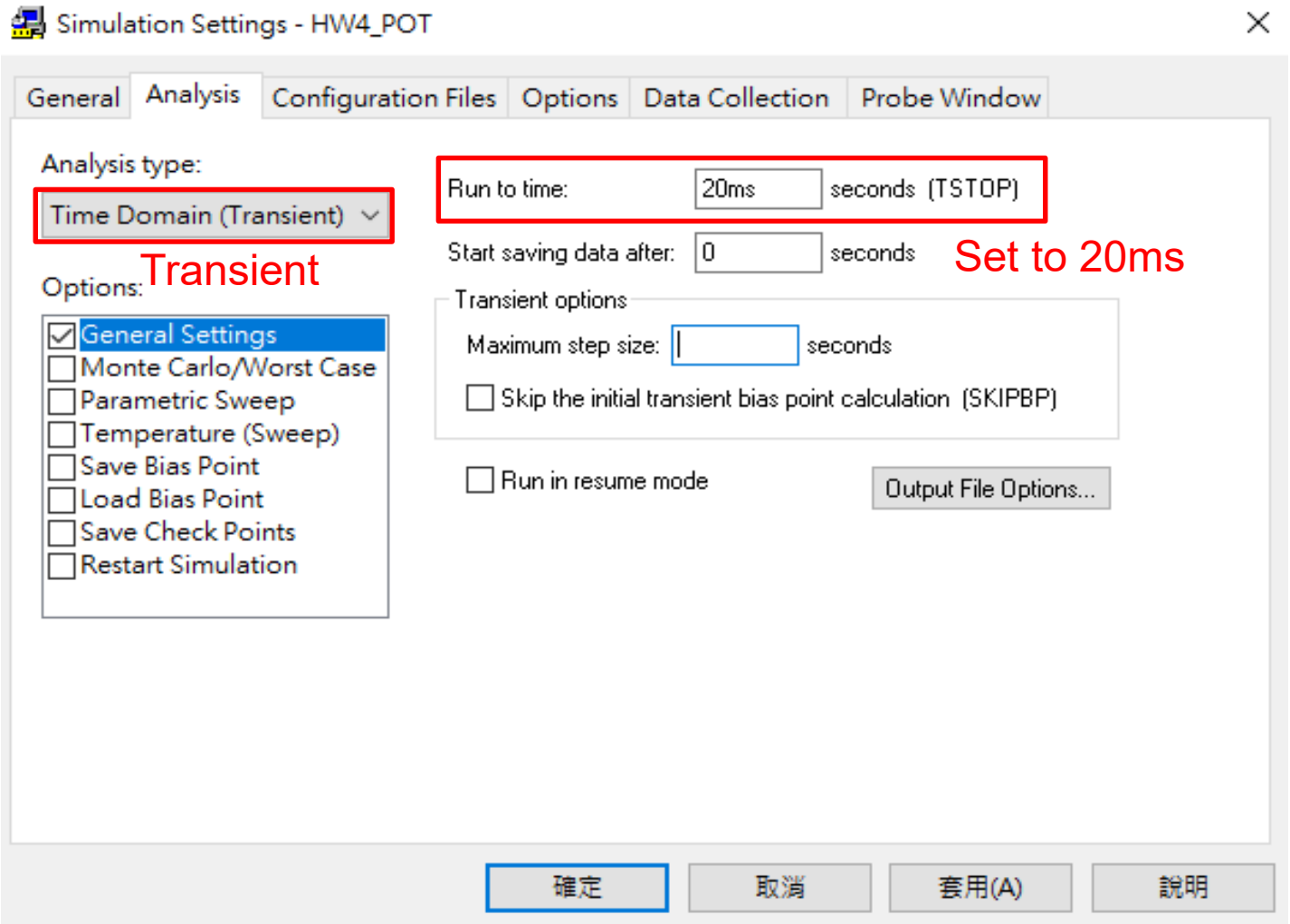
	A
	SCHEMATIC1 : PAGE1
Color	Default
CURRENT	CIMAX
Designator	
DIST	FLAT
Graphic	C.Normal
IC	2.5
ID	
Implementation	
Implementation Path	
Implementation Type	<none>
KNEE	CBMAX
Location X-Coordinate	800
Location Y-Coordinate	160
MAX_TEMP	CTMAX
Name	INS52685
Part Reference	CO
PCB Footprint	RAD/CK05
Power Pins Visible	
Primitive	DEFAULT
PSpiceTemplate	C^@REFDES %1 %2 ?TOL
Reference	CO
SLOPE	CSMAX
Source Library	C:\ORCAD\ORCAD_16
Source Package	C
Source Part	C.Normal
TC1	0
TC2	0
TOLERANCE	
Value	1m
VC1	0
VC2	0
VOLTAGE	CMAX

$V_{DD}/2$

C_O

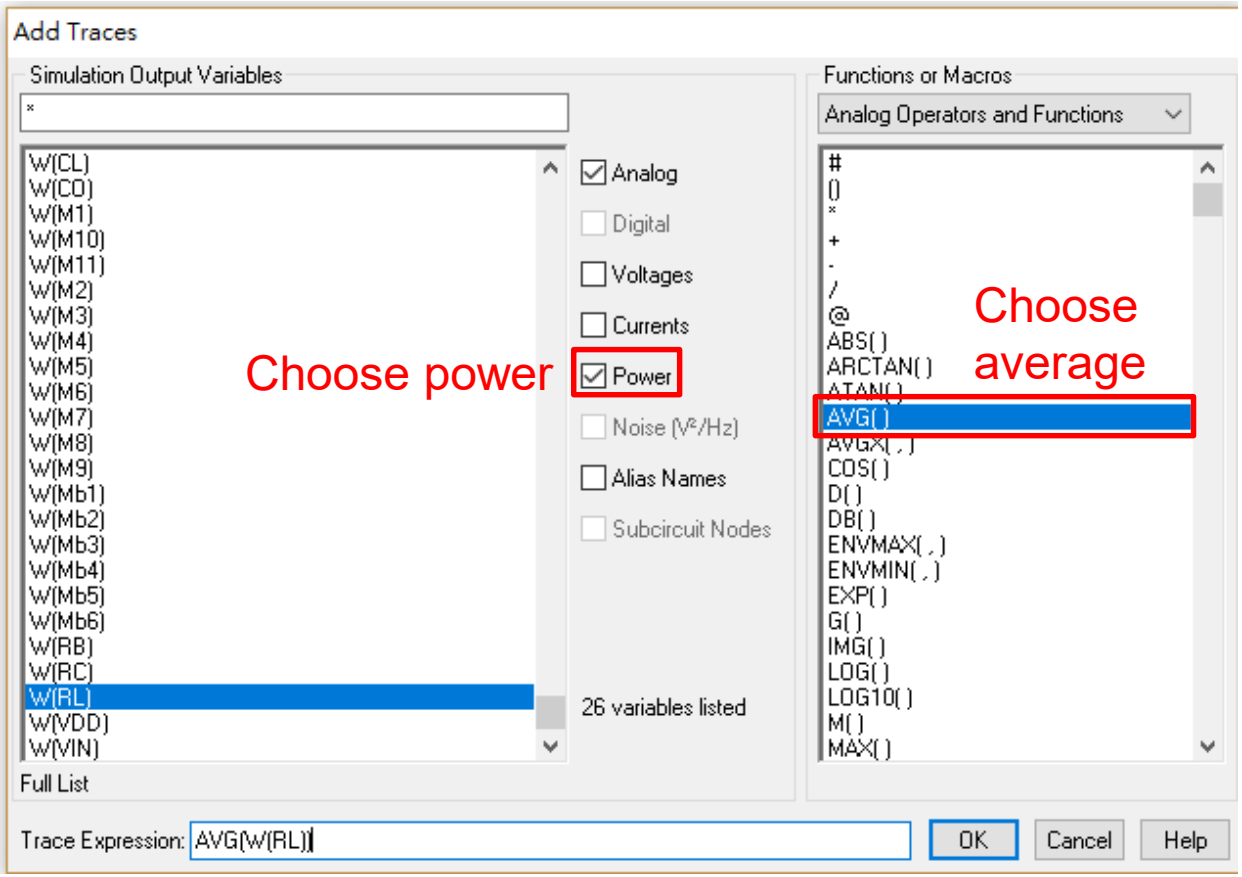
PSpice Verification Example of (c)

- Pspice simulation setting:



PSpice Verification Example of (c) (Cont.)

- Pspice simulation result:

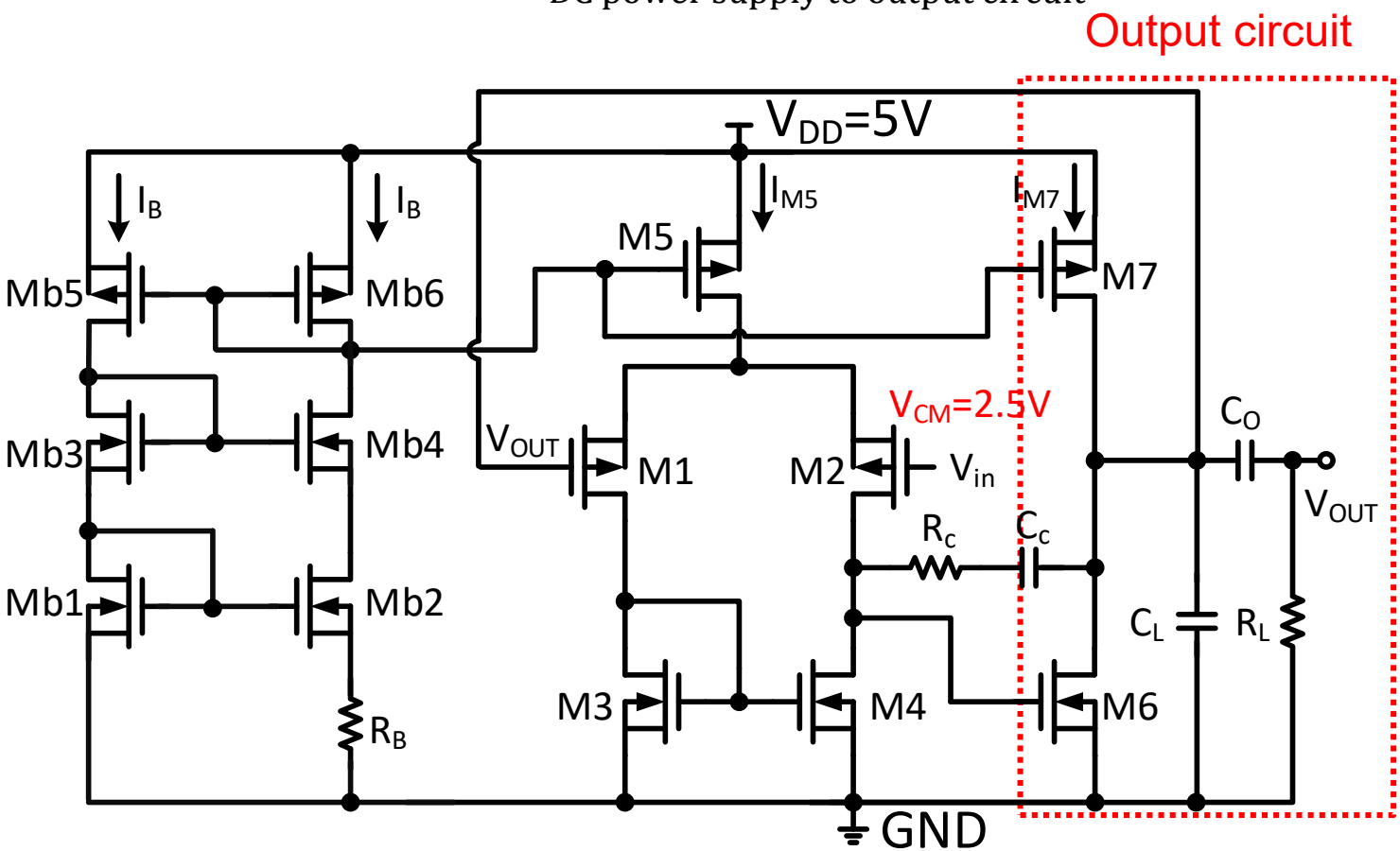


add traces : output average power = AVG(W(RL))

PSpice Verification Example of (c) (Cont.)

- Conversion efficiency for class-A CMOS OPAMP

$$\text{Conversion efficiency}(\eta) = \frac{\text{signal power deliver to load}}{\text{DC power supply to output circuit}} \times 100\%$$

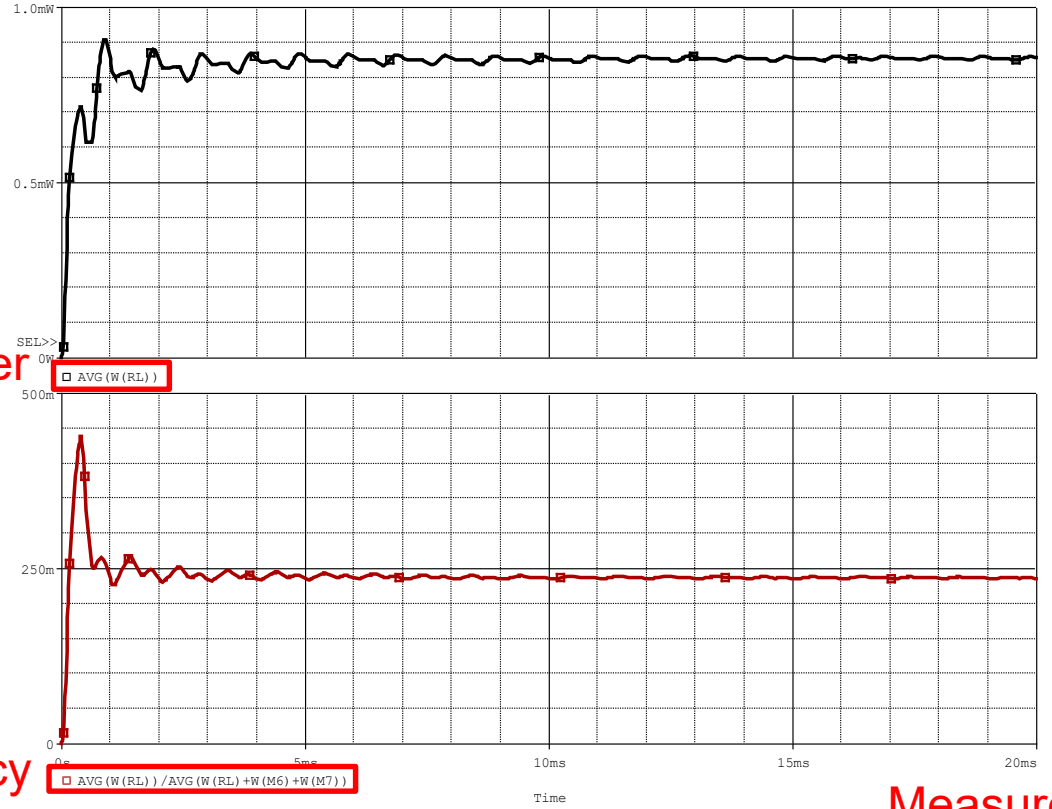


→ efficiency : add trace AVG(W(RL))/AVG(W(RL)+W(M6)+W(M7))

PSpice Verification Example of (c) (Cont.)

- Simulation results of class-A CMOS OPAMP

Output power



Efficiency

Measure at 20ms

Trace Color	Trace Name	Y1	Y2	Y1 - Y2
	X Values	19.986m	0	
	AVG(W(RL))/AVG(W(RL)+W(M6)+W(M7))	235.339m	1	
	AVG(W(RL))	856.383u	2	

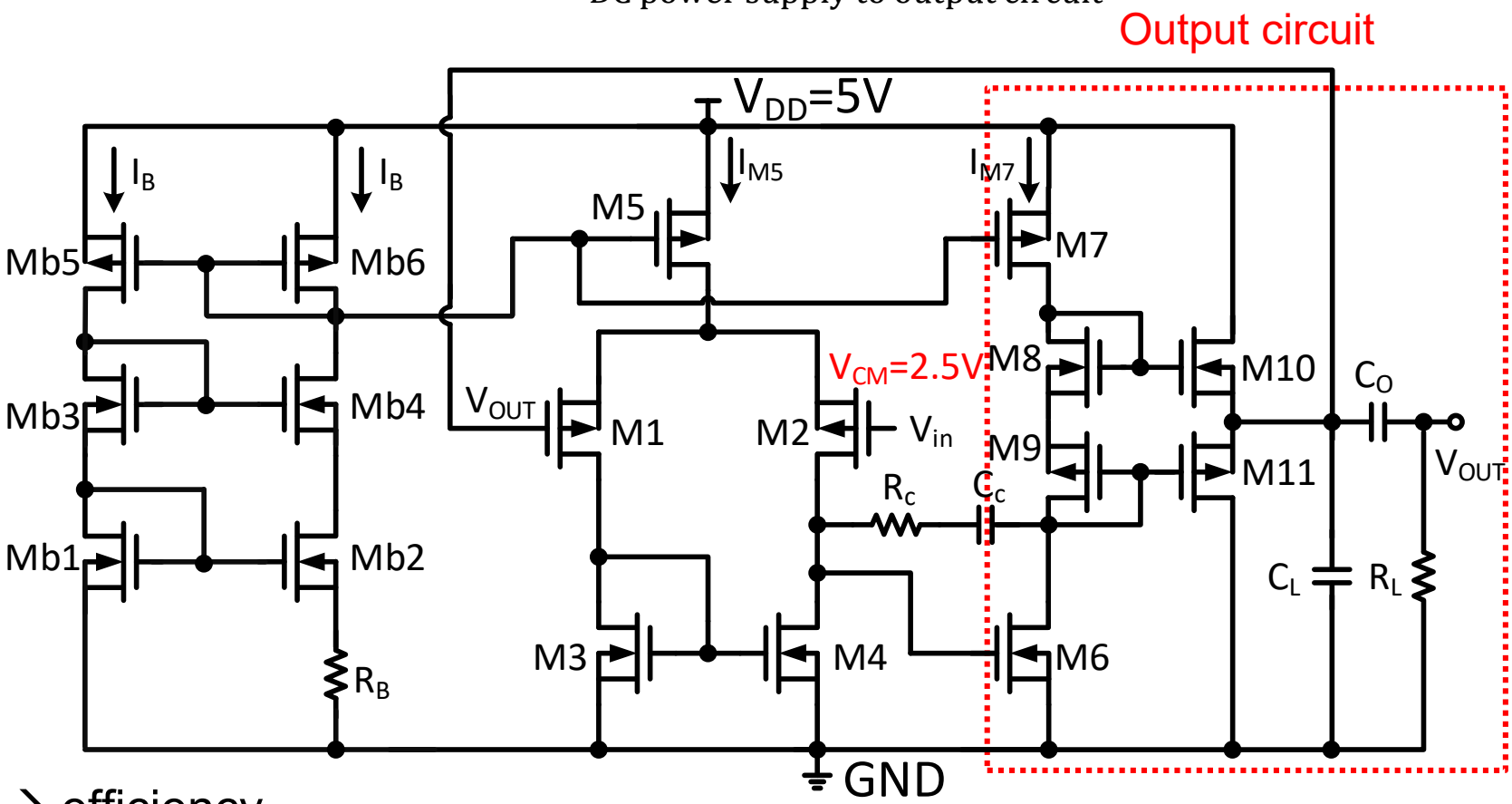
Efficiency = 23.5%

Output power = 856uW

PSpice Verification Example of (c) (Cont.)

- Conversion efficiency for class-AB CMOS OPAMP

$$\text{Conversion efficiency}(\eta) = \frac{\text{signal power deliver to load}}{\text{DC power supply to output circuit}} \times 100\%$$



→ efficiency

add trace: AVG(W(RL))/AVG(W(RL)+W(M7)+W(M8)+W(M9)+W(M10)+W(M11))

PSpice Verification Example of (c) (Cont.)

- Simulation results of class-AB CMOS OPAMP

Measure at 20ms

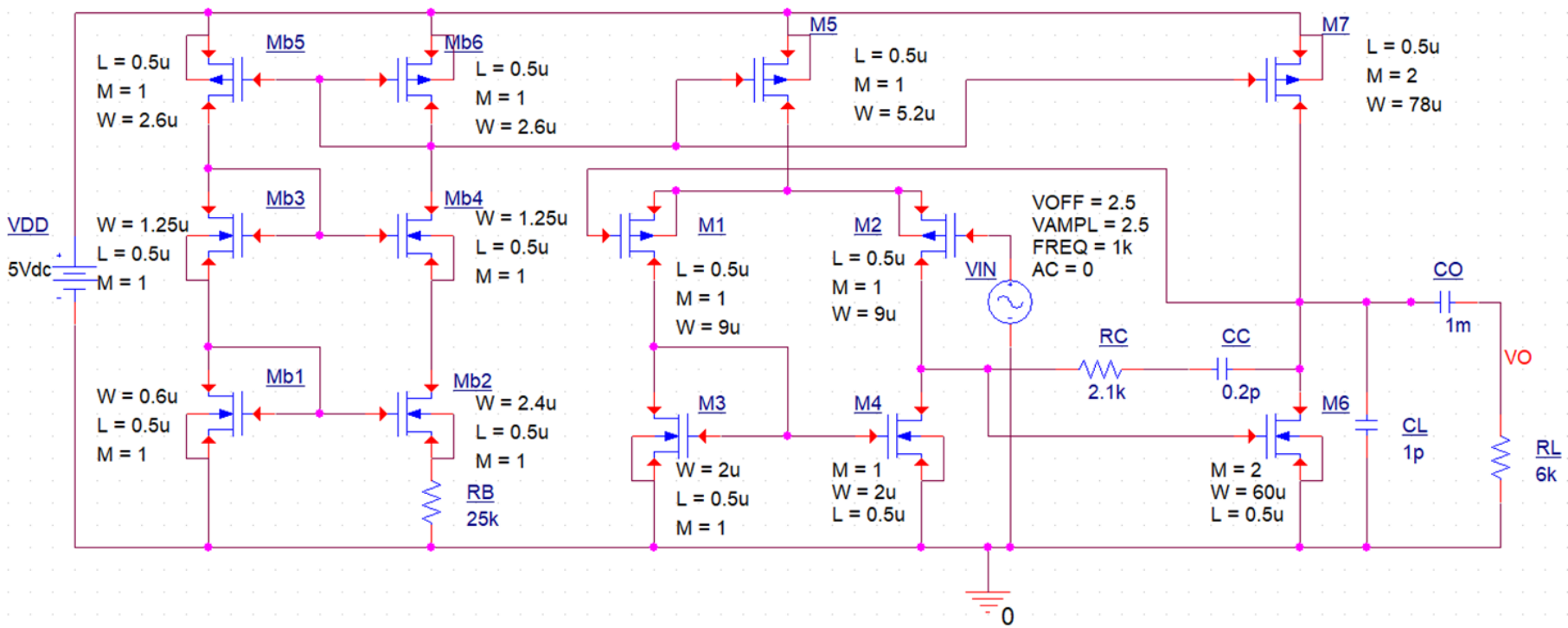
Trace Color	Trace Name	Y1	Y2	Y1 - Y2
	X Values	20.000m	0	
CURSOR 1,2	AVG(W(RL))/AVG(W(RL)+W(M7)+W(M8)+W(M9)+W(M10)+W(M11))	477.233m	[illegible]	[illegible]
	AVG(W(RL))	523.071u	63.903n	523.007u

Efficiency = 47.7%

Output power = 523uW

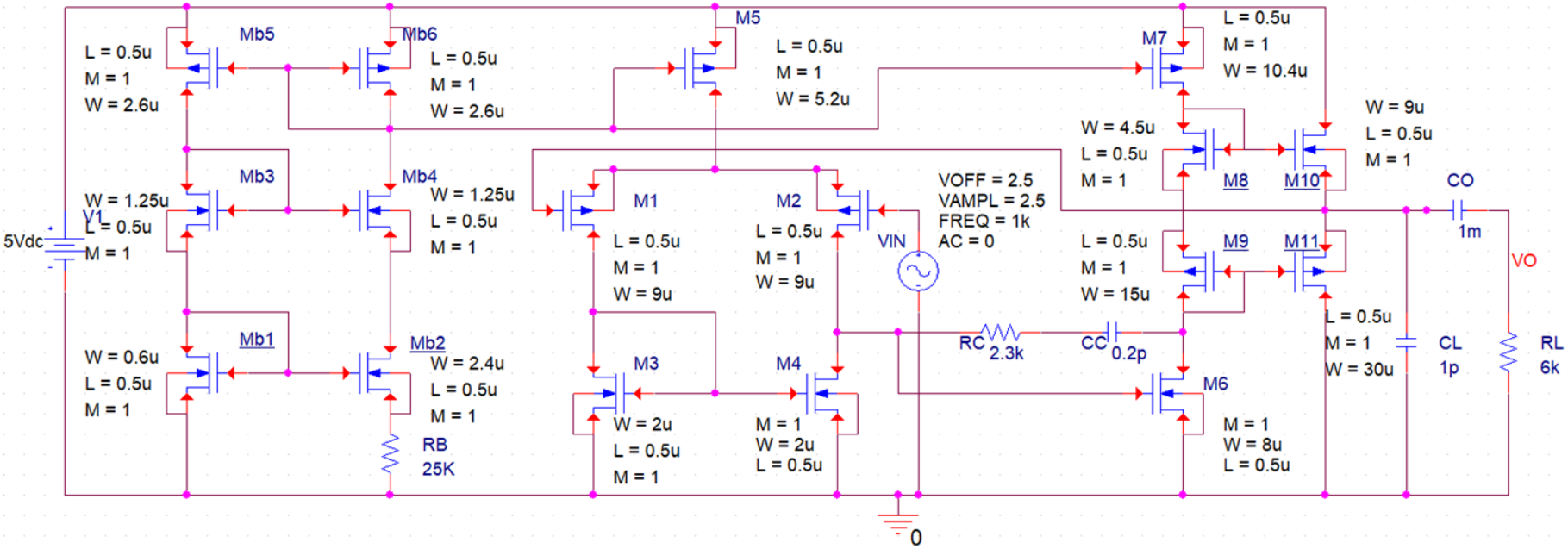
PSpice Verification Schematic

- Class A



PSpice Verification Schematic (Cont.)

- Class-AB



Notes

- Your report should include
  - Hand-calculation progress
  - PSpice circuit schematics
  - PSpice verification results with all specifications **clearly marked**

- Upload your report to **MOODLE** in **Word** format
  - Deadline: 23:59:59 on 2023/12/25 (Mon.)；(不接受遲交、補交)
  - Filename example: HW4_鄭聿程_E2408XXXX_v1.doc (如更新請用v2, v3, …)

- When verifying your hand calculation by PSpice
  - 軟體安裝與使用說明請參考Homework1的PSpice Tutorial
  - Correct the value of LAMBDA for NMOS0P5 to **0.1**
  - Use 4-terminal MOSFET models (NMOS0P5_BODY and PMOS0P5_BODY)

Notes (Cont.)

- Others
  - 請勿抄襲，抄襲等同考試作弊，將依校規處理
  - 此次作業佔學期總成績之1%
  - 作業若遇到問題，可於下列時段至奇美樓95304室與助教討論
    - 原定office hours：每週一17:00~18:00 and 每週五16:00~17:00
    - 新增時段： 2023/12/14(Thu.) and 2023/12/21(Thu.) 14:00~15:00
  - 請注意手算過程之掃描圖檔務必**清晰並轉正**以利助教判讀
  - Word format
    - 字體12pt、單行間距、中英文字體分別為標楷體與Times New Roman
    - 頁碼置中於頁尾、各邊界2.54公分 (上下邊界可依內容量縮減，但不得小於1.28公分)
    - 分別在每個繪圖下方與表格上方依序編號，並輔以caption描述
    - 圖表中的字體不小於10pt，尤其注意驗證波形圖的座標值
    - 驗證波形圖以**白色**為底，且重要驗證結果應清楚標記