Mid-Term Exam I Electronics (III) NCKUEE

1. Fig. 1 shows a bias circuit, where the current I_{bias} = 25μA. Assume that V_{DD}=3.3V, $(W/L)_{M5,M6}$ =4μm/1μm, $(W/L)_{M3,M4}$ = 2.5μm/1μm, $(W/L)_{M2} = 4(W/L)_{M1}$ = 8μm/1μm, $\mu_n C_{ox}$=300μA/V^2, $\mu_p C_{ox}$ = 150μA/V^2, V_{tn} = 0.7 V, $|V_{tp}|$ = 0.7 V. Note that channel-length modulation and the parasitic gate, drain, and body capacitance of MOS are neglected.

(a) Please derive $\mathbf{g_m}$ of M_1 in terms of $(W/L)_{M1}$, $(W/L)_{M2}$, and R_B.

(b) Please calculate the value of $\mathbf{g_m}$.

(c) Please calculate the value of R_B.

(d) Please explain why start-up circuit is needed.

(e) Please list at least two benefits of the bias circuit.

(f) Please explain what is the benefit of cascoding M3 and M4.

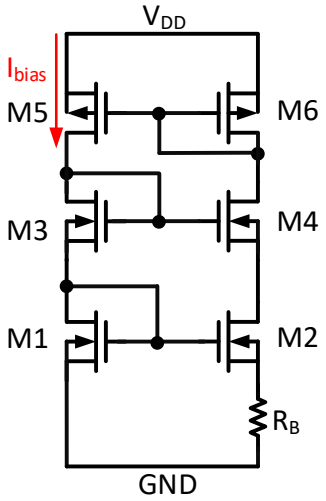


Fig. 1

2. Fig. 2(a) and Fig. 2(b) are two bias circuits. Assume V_{DD}=3.3V, $\mu_n C_{ox}$=200μA/V^2, V_{tn}=0.7V, $(W/L)_{Mn}=(W/L)_{M1\sim5}$=(20μm/1μm), $(W/L)_{M6}$=(80μm/1μm), R_S=100kΩ, and R_B=2256Ω. Without considering the channel-length modulation,

(a) Please calculate $\mathbf{g_m}$ and $\mathbf{I_D}$ of M_n in Fig. P2(a).

(b) Please derive $\mathbf{g_m}$ of M_1 in Fig. P2(b) in terms of $(W/L)_{M1}$, $(W/L)_{M6}$, and R_B.

(c) Please calculate $\mathbf{g_m}$ and $\mathbf{I_D}$ of M_1 in Fig. P2(b).

(d) Please repeat (a) and (c) if V_{DD} is changed to 3V.

(e) Please explain the benefits of the bias circuit in Fig. P2(b) compared with the one in Fig. P2(a).

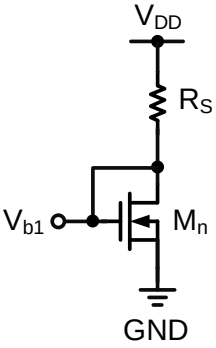


Fig. 2(a)

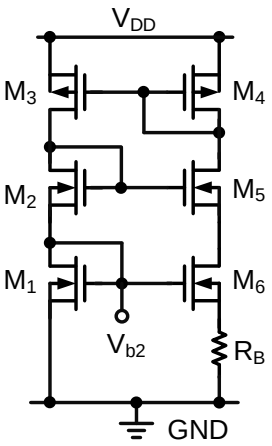


Fig. 2(b)

3. Fig. 3 shows the Bode plot of an open-loop gain A(s). It is a three-pole system with pole locations at 10^6, 10^8 and 10^9 Hz. Assume that the β-circuit is independent of frequency.

(a) If the phase margin of 45° is required, what is the value of β and the corresponding DC gain of the closed-loop gain?

(b) If the phase margin of 63° is required, what is the value of β and the corresponding DC gain of the closed-loop gain?

(c) To obtain a loop gain with its DC gain > 45dB and phase margin ≥ 0°, what is the acceptable range of β?

(d) To prevent the system from unstable operation, what is the maximum value of β?

(e) Find the unit-gain bandwidth of A(s).

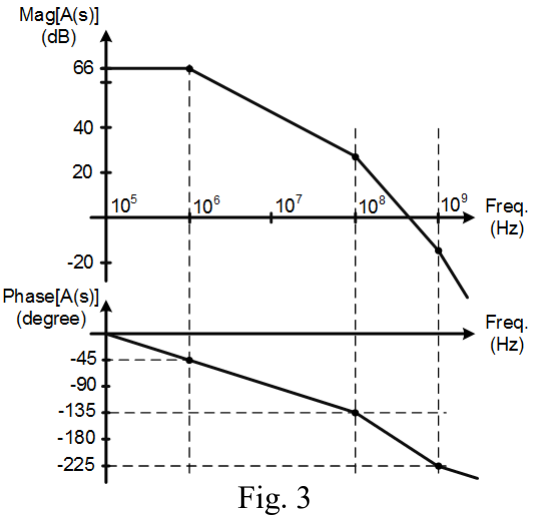


Fig. 3

4. A transfer function $T_{PL}(s) = \frac{1}{1+s/\omega_{PL}}$ contains a left plane pole, and its magnitude and phase bode plot are drawn in Fig. 4.

(a) Please express the transfer functions and draw the bode plots of another system which respectively contains a right plane pole (ω_{PR}), a left plane zero (ω_{ZL}) and a right plane zero (ω_{ZR}).

(b) Draw the bode plot for the transfer function $T(s) = \frac{(1+s/\omega_{Z1})}{(1+s/\omega_{P1})(1+s/\omega_{P2})}$ where ω_{z1} =10^5 rad/s, ω_{p2} = 10^3 rad/s and ω_{p1} = 10 rad/s.

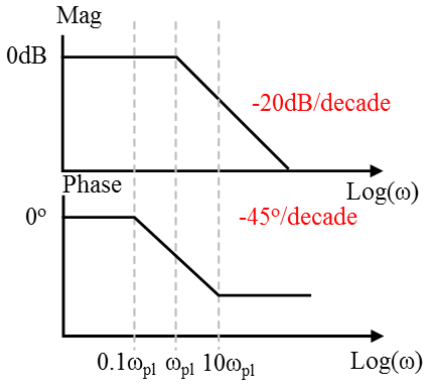


Fig. 4

5. Fig. 5(a) and Fig. 5(b) show a conventional and a wide-swing cascode current mirror, respectively. All MOSFETs are identical. The $|V_{OV}|$ is 0.25V, and the $|V_t|$ is 0.7V. In order to maximize the allowable V_O swing, please calculate

(a) V_{B1}, V_{B2} and the minimum V_O in Fig. P5(a).

(b) V_{B3}, V_{B4} and the minimum V_O in Fig. P5(b).

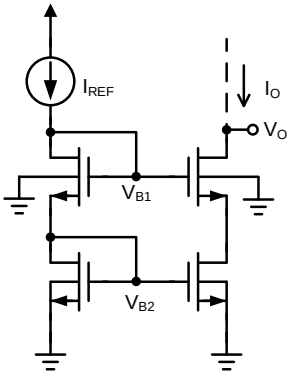


Fig. 5(a)

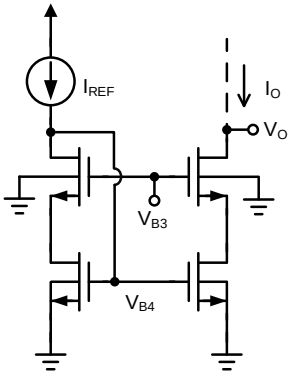


Fig. 5(b)

6. Fig. 6 shows a cascode current mirror. Assume that $(W/L)_{M1}=(W/L)_{M2}=(W/L)_{M3}=n_1\cdot(W/L)_{M4}$, I_{REF}=20μA. V_{tn}=0.7V for all transistors and $|V_{OV}|$=0.2V for all transistors except M4.

(a) To design $I_{OUT}=I_{REF}$ without considering channel-length modulation, please calculate n_1 to minimize the allowable output voltage V_{OUT} while all transistors work in saturation region.

(b) Find the minimum allowable V_{OUT} as mentioned in (a).

(c) If the channel-length modulation(λ_n=0.05V^{-1}) is considered, please calculate the I_{OUT} when V_{OUT} is biased at its minimum value.

(d) Draw a modified circuit to cancel the error due to channel length modulation. Explain your reason.

(Hint: the wide-swing current mirror shown in the textbook is one solution.)

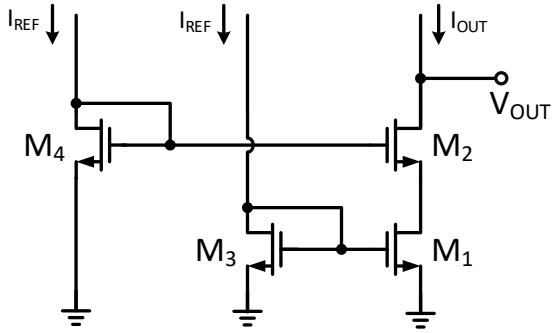


Fig. 6

7. A wide-swing current mirror is shown in Fig. 7. Assume V_{tn}=0.7V for all transistors, and $I_{bias}=I_{in}=I_{out}$. The V_{OV} of M_1, M_2, M_3, M_4 are 0.3V. In order to minimize the allowable output voltage,

(a) find **V_{OV} of M_5**.

(b) if $(W/L)_{M1}=(W/L)_{M2}=n_1\cdot(W/L)_{M3}=n_1\cdot(W/L)_{M4}=n_2\cdot(W/L)_{M5}$, what are the values of **n_1** and **n_2** should be designed?

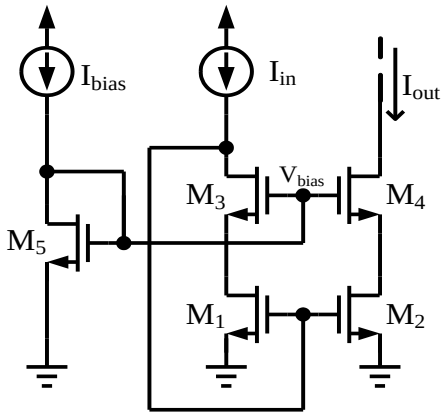


Fig. 7

8. (a) With less than 25 words, please list the name of the **four feedback amplifiers** (e.g. Trans… amplifier) and their **corresponding topologies** (e.g. series-shunt).

(b) As shown in Fig.8(a), please specify which type of feedback amplifier it is. Explain your reason.

(c) As shown in Fig.8(b), please specify which type of feedback amplifier it is. Explain your reason.

(d) Show how to derive A circuit and β circuit for a voltage amplifier. Please give detailed procedure from two-port feedback network to A circuit and β circuit.

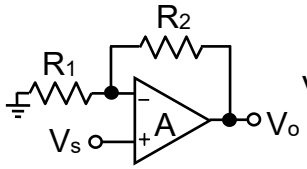


Fig. 8(a)

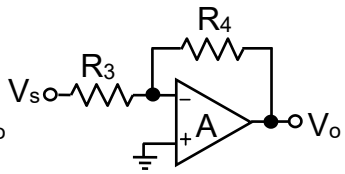


Fig. 8(b)

9. Fig. 9(a) shows an inverting closed-loop amplifier. To derive the loop gain by breaking the loop at X in Fig. P9(a), the equivalent small-signal circuit of the loop gain is shown in Fig. 9(b).

(a) Please derive the feedback gain β.

(b) Assume that output impedance of M_3 is r_{ds3}, please derive Z_t.

(c) Please derive the loop gain (βA).

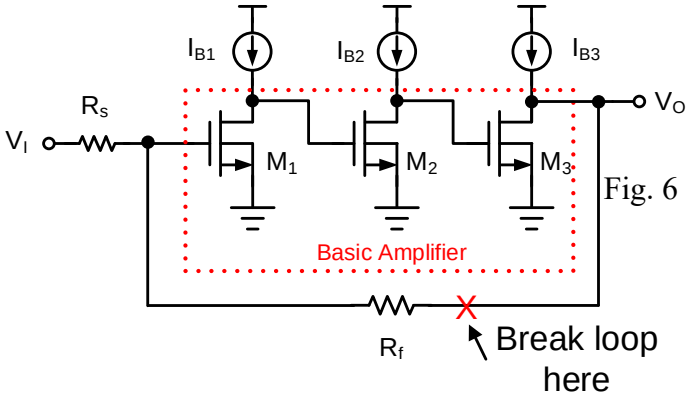


Fig. 6

Fig. 9(a)

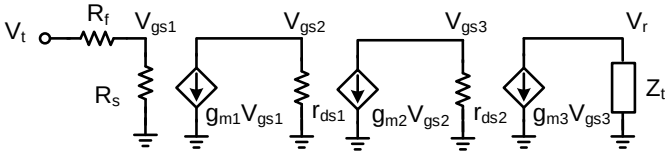


Fig. 9(b)

10. Consider a closed-loop circuit shown in Fig. 10. Assume the input impedance of the basic amplifier is infinite and the output impedance of the basic amplifier is r_o.

(a) Please find the **DC-gain** of loop gain by breaking the loop **at *X***.

(b) Please find the **DC-gain** of loop gain by breaking the loop **at *Y***.

(c) Draw its A circuit and β circuit.

(d) Assume $\mu = 10^3$ V/V, $r_o = R_L = 100k\ \Omega$, $R_1 = R_2 = 50k\ \Omega$, $C_L = 1p$ F, please calculate the **DC-gain** of the loop gain, and the **dominant pole location** of the loop gain.

(e) Based on (c), if A decreases by 20%, what is the corresponding decrease in A_f?

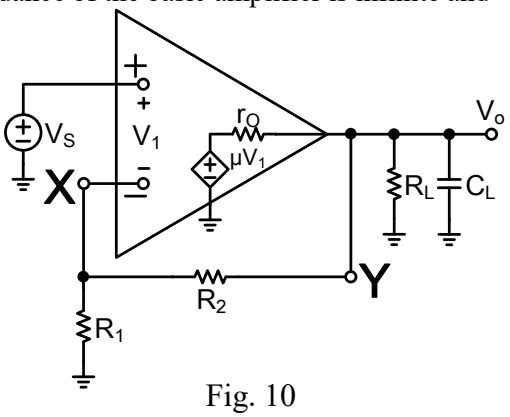


Fig. 10

(Note: To explain your answers for both (a) and (b), you have to draw the circuits after breaking the loop.)

11. Fig. 11 shows the noninverting closed-loop configuration. Assume that the op amp has infinite input resistance and zero output resistance, open-loop voltage gain A=1000, $R_1=R_2=R_L=100k\Omega$, $C_L=2pF$,

(a) Find an expression for the feedback factor β.

(b) If the open-loop voltage gain $A = 10^3$, find R_2/R_1 to obtain a close-loop voltage gain A_f of 10.

(c) Please calculate the closed-loop gain A_f if open-loop voltage gain A=1000, $R_1=R_2=R_L=100k\Omega$, $C_L=2pf$.

(d) Based on (c), if A decreases by 20%, what is the corresponding decrease in A_f?

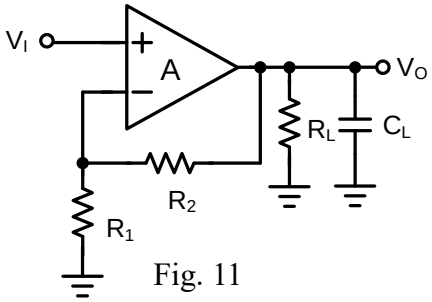


Fig. 11

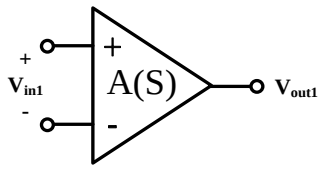
12. A single-pole amplifier as shown in Fig.12(a) is designed to have a low-frequency gain of 100 and a pole at 10^6 Hz (i.e. $2\pi\times10^6$rad/sec). The single-pole amplifier (transfer function=A(S)) is used to design a feedback amplifier (transfer function=A_F(S) as shown in Fig.12(b).

(a) Derive A(S) and draw its Bode plot.

(b) What's the feedback type of the internal stage of the feedback amplifier? β for the internal stage=?

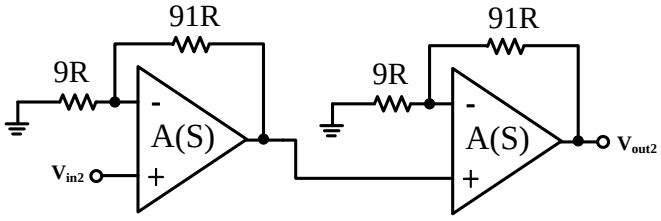
(c) Derive A_F(S) and draw its Bode plot.

(d) If the gain of the single-pole amplifier is decreased by 20%, what is the corresponding gain decrease in the feedback amplifier?



$$A(S) = \frac{V_{out1}(S)}{V_{in1}(S)}$$

Fig. 12(a)



$$A_F(S) = \frac{V_{out2}(S)}{V_{in2}(S)}$$

Fig. 12(b)

13. Please explain or give definitions of the following terms.

(a) MOSFET transconductance (g_m).

(b) CMRR

(c) PSRR

(d) Slew rate

(e) Rail-to-rail input operation

(f) -3dB bandwidth

(g) Unity-gain bandwidth

(h) Pole-splitting by Miller capacitor.

14. Fig. 14(a) shows the simplified small-signal circuit of a two-stage op amp before frequency compensation. Assume G_{m1}=1mA/V, G_{m2}=2mA/V, R_1=R_2=200kΩ, C_1=0.5pF and C_2=1pF.

(a) Please calculate the pole locations of the system.

(b) C_A is added as shown in Fig. P3(b). To obtain a dominant pole located on 10kHz, please find C_A.

(c) C_C is added as shown in Fig. P3(c). To obtain a dominant pole located on 10kHz, please find C_C.

(d) Please explain the benefit of adding C_C compared with adding C_A.

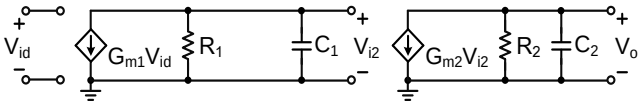


Fig. 14(a)

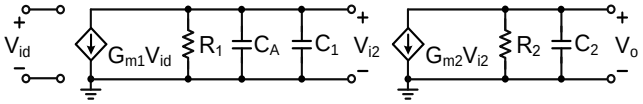


Fig. 14(b)

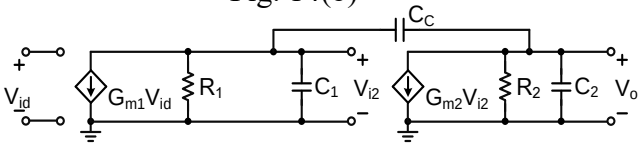


Fig. 14(c)

15. Fig. 15 shows a two-stage op amp with a simple bias circuit. Assume that $\mu_n C_{ox}$=300μA/V^2, $\mu_p C_{ox}$=150μA/V^2, R_B =150kΩ, C_L=2pF, C_C=1pF, V_{tn} = 0.7V, $|V_{tp}|$ = 0.7V, $|V_{OV}|_{M1\sim M4}$=0.15V, W_B=1.25μm, W_5=12.5μm, and the lengh (L) of all transistors are 1.25μm. Phase margin is designed to be 63°, and right-plane zero is eliminated by adding R_C. Note that the parasitic gate, drain, and body capacitance of MOS are neglected.

(a) Please calculate the value of I_B, I_{D5} and I_{D7}.

(b) Please calculate DC-gain in first stage and second stage respectively.

(c) Please calculate the unity-gain bandwidth.

(d) Please calculate the second pole location.

(e) Please calculate R_C such that the right-plane zero is eliminated.

(f) Please re-design C_C such that phase margin is 45°. (Assume that right-plane zero is eliminated)

(g) List at least two methods to increase its DC gain. Explain your answers.

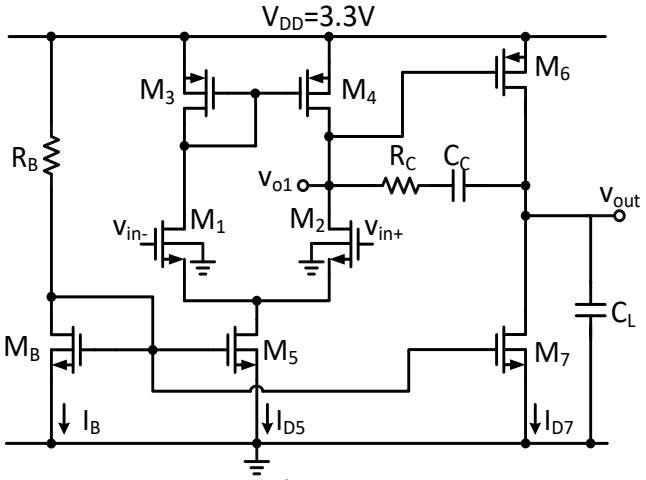


Fig. 15

(h) Assume that phase margin = 70° is needed, and the right-half plane zero is canceled by adding R_C. Show the value of I_2, W_2, W_4, W_6, W_7, R_C . (Don't need to consider parasitic effect)

16. A single-stage opamp with a constant-gm bias circuit is shown in Fig. 2. Assume that $\mu_n C_{ox}=3\mu_p C_{ox}$ and $I_{M7}=10I_{M5}$. The W/L of transistors M_i is denoted as $(W/L)_i$, where i=1,2,3…11. Please derive gm_5 and gm_8 in terms of R_B and $(W/L)_i$.

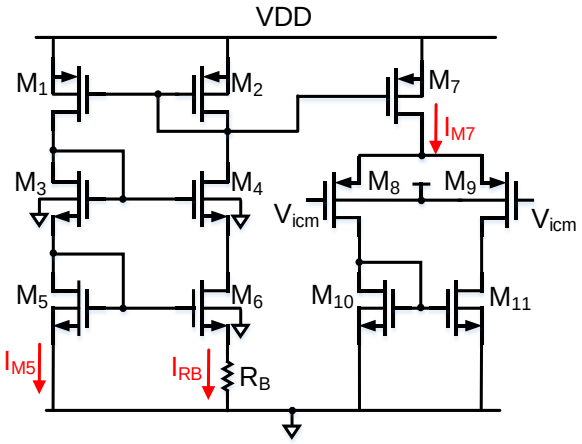


Fig. 16

17. Fig. 17 shows a two-stage op amp with a simple bias circuit. Assume that $\mu_n C_{ox}=300\mu A/V^2$, $\mu_p C_{ox}=120\mu A/V^2$, $I_{D5}=0.2mA$, $C_L=2pF$, $(W/L)_{M10}=0.1(W/L)_{M5}=0.05(W/L)_{M9}=1.25\mu m/1\mu m$. For all transistors, $|V_t|=0.7V$ and $|V_{OV}|$ are all the same. $\lambda_n= 0.05\ V^{-1}$ and $\lambda_p=0.1\ V^{-1}$. Please neglect channel-length modulation.

(a) Please calculate the value of R_B.

(b) Open loop gain $A=\frac{v_{out}}{v_{id}}$, where vid=vin+-vin-.

(c) Briefly explain how to design the value of R_C, and how the R_C and Cc influence two-stage op amp.

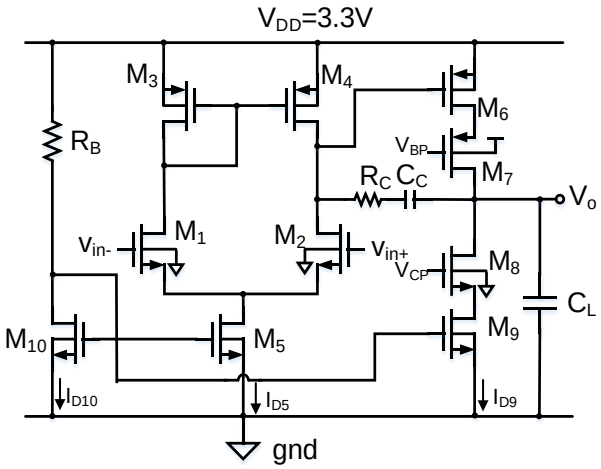


Fig. 17

18. Fig. 18(a) shows a two-stage op-amp, and its input-to-output Bode plot is shown in Fig. 18(b). Assume that all the MOSFETs' sizes are fixed, and V_{ov1} = 0.2V, I_{M5} = 200μA. If we redesign the value of C_c to make this system have only one pole before the unity-gain frequency, please answer the following questions. (Note: All the parasitic capacitance of MOSFETs can be neglected.)

(a) If the unity-gain frequency is designed to be 100MHz, please calculate the dominant pole location and the corresponding value of C_c.

(b) Briefly explain how to design the R_c value, and how the R_c affect the pole/zero location of the system.

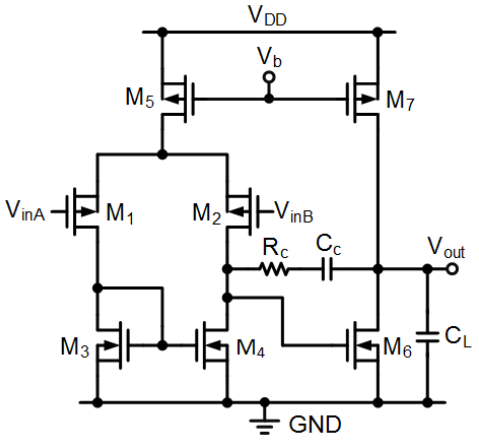


Fig. 18(a)

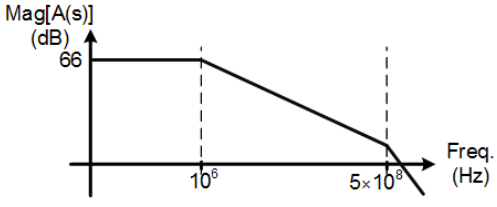


Fig. 18(b)

19. Fig. 19 shows a two-stage op amp. Assume $(W/L)_{M3,4}$=(10μm/1μm), $(W/L)_{M5}$=(20μm/1μm), I_{D5}=100μA, I_{D7}=200μA, C_C=0.5pF and C_L=2pF. Without considering the channel-length modulation, please

(a) design **$(W/L)_{M6}$** to minimize the input systematic offset if the input stage is perfectly balanced.

(b) specify which node is the **positive input terminal** (V_{inA} or V_{inB}) and explain your answer.

(c) calculate the **negative slew rate** and explain your answer.

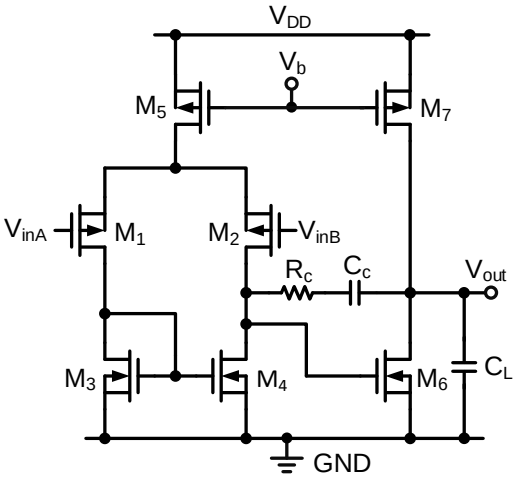


Fig. 19

20. A folded-cascode op amp is shown in Fig. 20, where I_{M11} = 200μA, I_{M9} = I_{M10} = 250μA, and $|V_{OV}|$ = 0.15V for all transistors. Assume that $\mu_n C_{ox}$ = 300μA/V^2, $\mu_p C_{ox}$ = 150μA/V^2, λ_n = 0.05V^{-1}, λ_p = 0.1V^{-1},VDD = 3.3V, V_{tn} = 0.7V, $|V_{tp}|$ = 0.7V, and C_L=3pF. Note that the parasitic gate, drain, and body capacitance of MOS are neglected.

(a) Please specify which node is the **negative** input terminal (V_{ina} or V_{inb}), and explain your answer.

(b) Please calculate the input common-mode range and the output voltage swing, output resistor, DC-gain and unit-gain bandwidth.

(c) Please calculate both the positive and negative slew rates, and explain your reason.

(d) DC-gain and unity-gain bandwidth.

(e) Please revise the connection of M3~8 to increase output voltage swing and calculate the value of output voltage swing of the modified opamp. (Note: Additional bias voltage is needed)

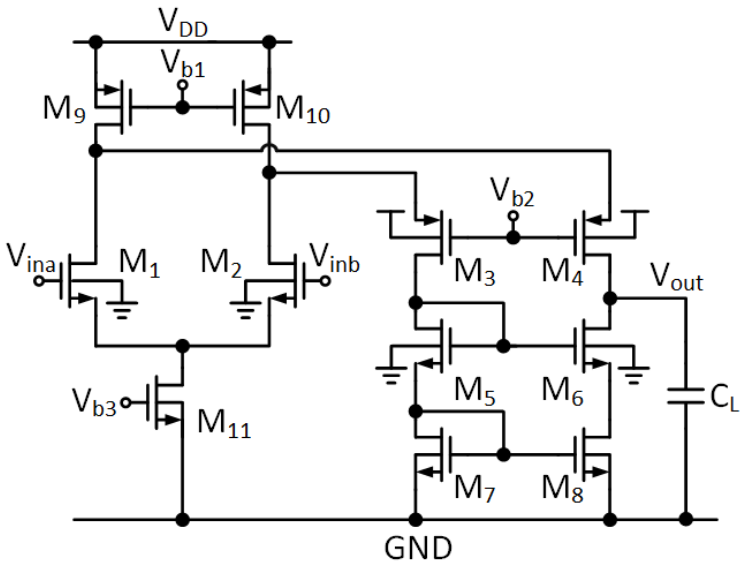


Fig. 20

21. Fig. 21 shows a telescopic-cascode op amp. Assume that $|V_{ov}|$ of all transistor is 0.3V, threshold voltages V_{tn}=0.7V, $|V_{tp}|$=0.8V and V_{DD}=3.3V.

(a) Find the **input common-mode ranges**.

(b) Assume that all inputs are biased at 1.65V, please find the **output swings**.

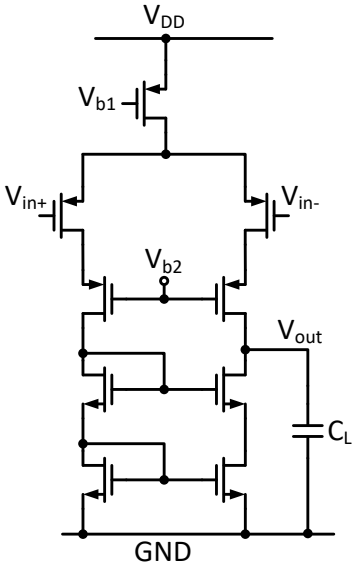


Fig. 21

22. Fig. P22 shows a current-mirror op amp. Assume that $(W/L)_{M5}=(W/L)_{M6}=3\cdot(W/L)_{M3}=3\cdot(W/L)_{M4}$, $(W/L)_{M7}=(W/L)_{M8}$, IB=100μA, C_L=1pF. Please

(a) specify which node is the **negative input terminal** (V_{inA} or V_{inB}).

(b) calculate the **negative slew rate**. Explain your answer.

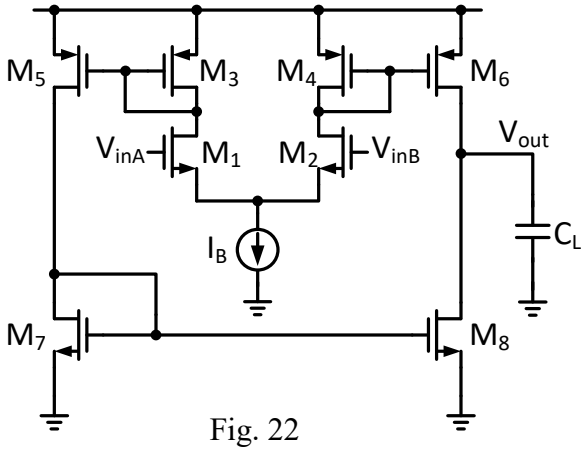


Fig. 22

23. V_-, V_+, and V_O are the inverting input voltage, noninverting input voltage, and output voltage of the OPAMP, respectively 0 V<output swing of V_O<3.3 V.

(a) Calculate V_- and V_O of the circuit shown in Fig. 23(a) where the OPAMP gain A_a = 10.

(b) Calculate V_+ and V_O of the circuit shown in Fig. 23(b) where the OPAMP gain A_b = 10.

(c) Calculate V_+ and V_O of the circuit shown in Fig. 23(c) where the OPAMP gain A_c = 1.

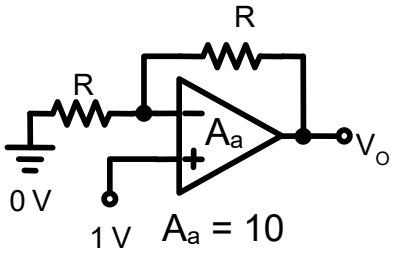


Fig. 23(a)

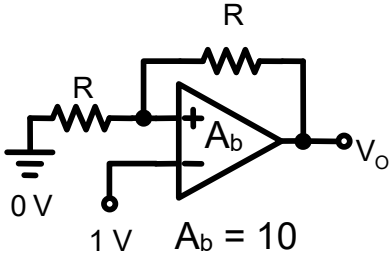


Fig. 23(b)

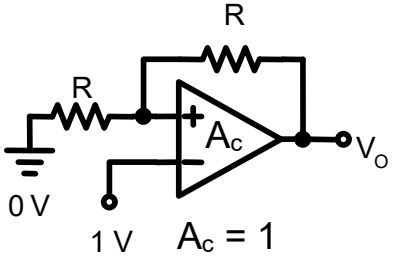


Fig. 23(c)

24. Fig. 24 shows a magnitude bode plot of a two left-hand-plane poles system. Please answer the following questions.

(a) If $\omega_t \gg \omega_{p1}$, please calculate the value of ω_{p2}/ω_t to satisfy phase margin = 63°.

(b) If $\omega_t = 5\omega_{p1}$, please calculate the value of ω_{p2}/ω_t to satisfy phase margin = 63°.

(c) Following (b). Suppose that a left-hand-plane zero, $\omega_z = 2\omega_t$, is added to the system, please calculate the value of ω_{p2}/ω_t to satisfy phase margin = 63°.

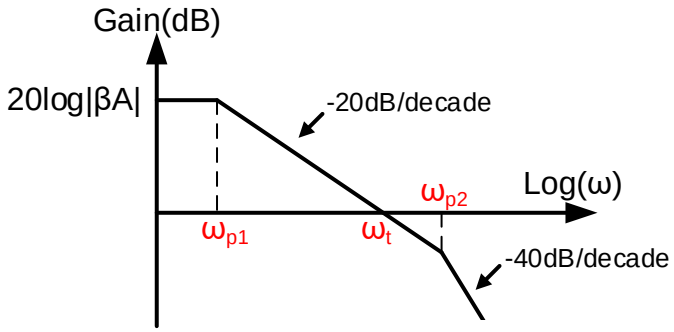


Fig. 24

25. A fully-differential folded-cascode op amp is shown in Fig. 25

(a) Please list at least two benefits of fully-differential op amp compared to single-ended design.

(b) Why CMFB circuit is required in fully-differential op amp?

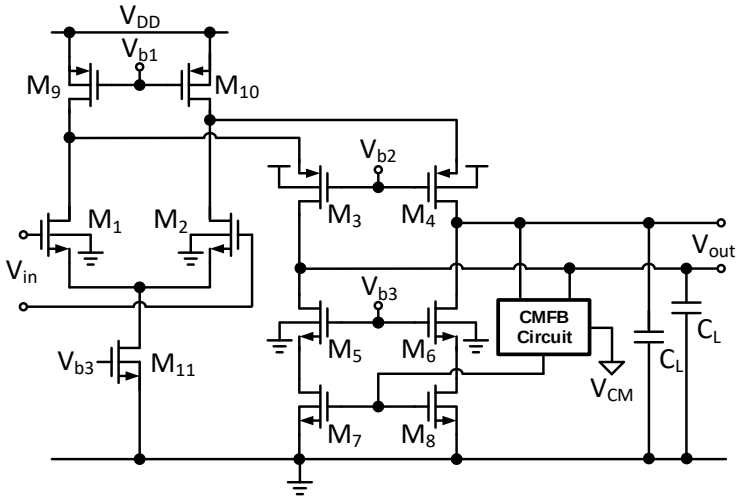


Fig. 25