Mid-Term Exam II Electronics (III) NCKUEE

1. Consider an N[th]-order Butterworth low-pass filter $T(j\omega)$ whose passband edge ω_p=200krad/s, stopband edge ω_s=2Mrad/s, maximum allowed variation in passband A_{max}=2.7dB, minimun required stopband attenuation A_{min}=60dB, and magnitude function $|T(j\omega)| = \frac{1}{\sqrt{1+\varepsilon^2(\frac{\omega}{\omega_p})^{2N}}}$.

(a) Please find how many poles and zeros does this filter have.

(b) Find ε.

(c) Find the minimum required order N of the filter.

(d) If ω_s is changed to 20Mrad/s, please repeat (b).

(e) If N = 2 and ε=0.5, Please re-calculate the maximum allowed variation in passband A_{max} and the minimun required stopband attenuation A_{min}. (Your answers should be expressed in dB.)

(f) Please derive the normalized polynominal T(s) of a 2[nd]-order Butterworth filter with ε = 1.

2. Fig. 2 shows an active-RC integrator, and assume that R=10kΩ, C=10pF.

(a) Assume that the op amp is ideal, please find the unity-gain bandwidth of the integrator.

(b) If the op amp has a finite DC gain A_0=80dB and an infinite bandwidth, please find the dominant pole location of the integrator.

(c) If the op amp has a finite DC gain A_0 and a -3dB bandwidth ω_p, please explain the influence on the transfer function of the integrator.

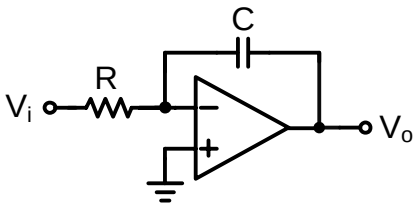


Fig. 2

3. Fig. 3 shows a switched-capacitor (SC) integrator and its two-phase clock Φ_1 and Φ_2.

(a) Explain why a SC-circuit can behave as a resistor?

(b) Derive the equivalent time constant for the SC integrator in terms of C_1, C_2 and T_c.

(c) Compared with an active-RC integrator, please explain two **benefits** of a SC integrator for on-chip implementation.

(d) Explain how stray capacitances affect the circuit.

(e) Sketch two kinds of stray-insensitive switched-capacitor integrators (both inverting and non-inverting) and explain why it is stray-insensitive.

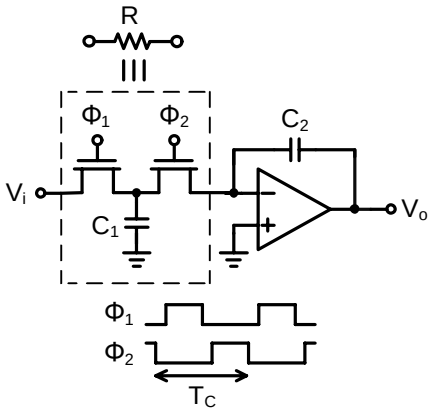


Fig. 3

4. Fig. 4 shows a tuned amplifier, assuming that the transconductance and the output resistance of M_1 are g_m and r_o, respectively.

(a) Sketch the small-signal equivalent circuit of the tuned amplifier.

(b) Assume that R=40kΩ, L=20nH, C=20pF, g_m=4mA/V, r_o=40kΩ, please derive $\frac{v_o}{v_i}(s)$

(c) Find its center frequency ω_0.

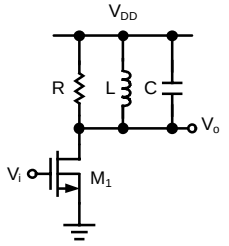


Fig. 4

5. Fig. 5(a) and 5(b) show two 4-bit DACs, where R = R_F = 5kΩ, V_{REF} = 1.8V and I = 1.5mA.

(a) Describe the operational principle of a 2-bit R-2R D/A converter. (Show figures if necessary)

(b) In Fig. 5(a), please derive $\frac{V_o}{V_{ref}}$ in terms of B_0, B_1, B_2, B_3, R and R_F.

(c) In Fig. 5(a), If bits $B_0B_1B_2B_3 = (1010)_2$, please find the V_o value.

(d) In Fig. 5(b), if B_3 switches to **d**, and B_0 ~ B_2 switch to ground, please find the V_o value.

(e) In Fig. 5(b), please derive $\frac{V_o}{I}$ in terms of B_0, B_1, B_2, B_3, R and R_F.

(f) Please list pros and cons of the structure in Fig. 5(a) compared with that in Fig. 5(b).

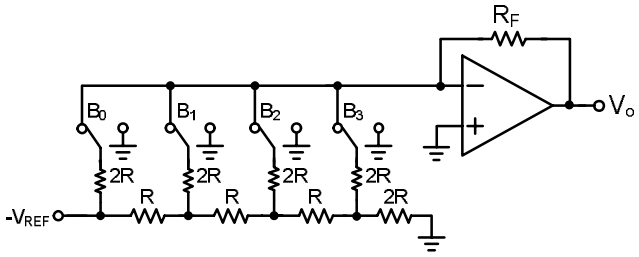


Fig. 5(a)

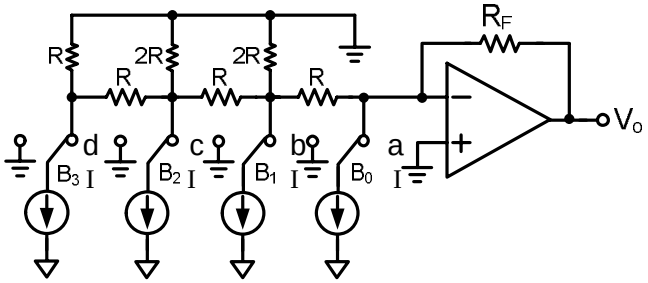


Fig. 5(b)

6. Fig. 6 shows a 5-bit charge-redistribution ADC.

(a) Please determine and explain where the switches (S_1, S_2 and S_3) should be connected when the ADC is in sample, hold, and charge-redistribution mode, **respectively**.

(b) Assume parasitic capacitance (C_p) at node V_X can be ignored. Please find the digital output (b_1~b_5) and intermediate node voltage (V_X) when V_{in} = 1.23 V and V_{ref} = 5 V.

(c) Assume parasitic capacitance (C_p) at node V_X is 8C. Please find the digital output (b_1~b_5) and intermediate node voltage (V_X) when V_{in} = 1.23 V and V_{ref} = 5 V.

(d) If the ADC is redesigned and the specification that a V_{LSB} less than 0.01V is required, how many number of bits are needed for the new ADC.

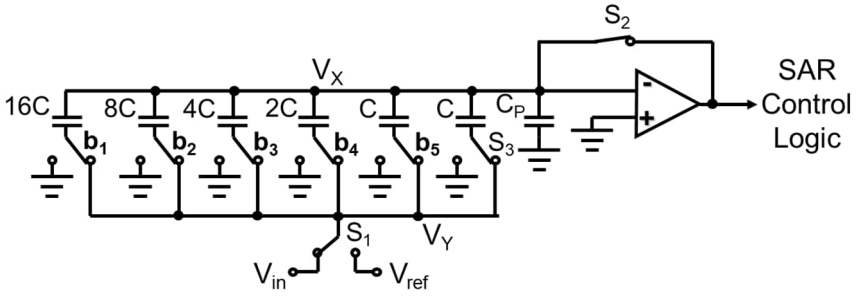
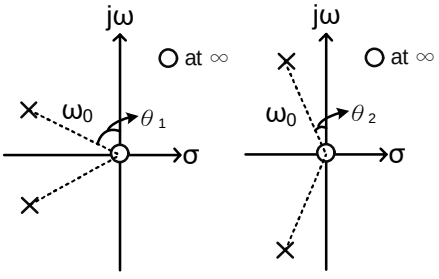


Fig. 6

7. Fig. 7 shows the pole-zero patterns of two filters. Both filters have one zero at the origin and the other zero at infinite. The distance from the origin to each pole is ω_0, while $\boldsymbol{\theta_1 > \theta_2}$.

(a) For Fig. 7, please specify which type of filters it is and its order. Explain your reason. (low-pass/ high-pass/ band-pass/ band-reject/ all-pass)

(b) Compare both filters in Fig. 7 by roughly drawing their Bode magnitude plots. Explain your reason. (**Mark ω_0 in your plot**.)



(a) (b)

Fig. 7

8. Fig. 8 is an active RC filter, assuming that the opamp has infinite input resistance, zero output resistance, and infinite bandwidth. Please answer the following questions.

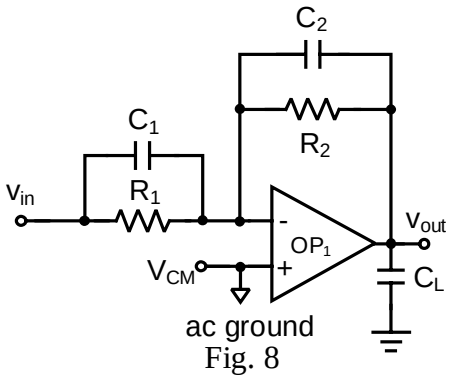


Fig. 8

(a) Please derive the transfer function $\frac{v_{out}}{v_{in}}(s)$.

(b) Assume that $R_1 = R_2 = 100k\Omega$, $C_1 = 10pF$, $C_2 = 0.2pF$. When $v_{in} = V_{CM}+V_{in}\times\sin(\omega t)$, where V_{in} =0.25V and ω = 10Mrad/s, please calculate the amplitude of v_{out}.

(c) According to (b), if the opamp with limited slew rate=15V/us, please calculate the maximum operation frequency without slew rate limitation of this filter.

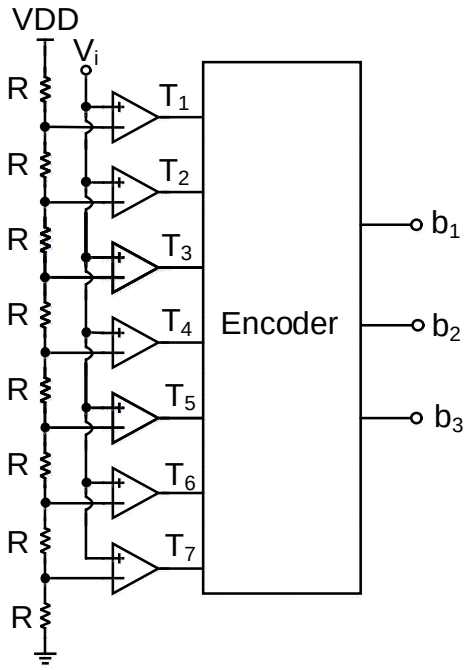
9. Please draw inverting and non-inverting type of stray insensitive SC integrators and explain why they are stray insensitive.

10. Fig. 10 shows a 3-bit flash ADC and its truth table of encoder. If V_{DD}=12V, V_i=8V, please

(a) find $b_1b_2b_3$.

(b) calculate the number of comparators needed for a 6-bit flash ADC.

(c) explain the benefits and the drawbacks of the flash ADC compared with a 3-bit charge-redistribution ADC.



Inputs							Outputs		
T_1	T_2	T_3	T_4	T_5	T_6	T_7	b_1	b_2	b_3
0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	0	0	1
0	0	0	0	0	1	1	0	1	0
0	0	0	0	1	1	1	0	1	1
0	0	0	1	1	1	1	1	0	0
0	0	1	1	1	1	1	1	0	1
0	1	1	1	1	1	1	1	1	0
1	1	1	1	1	1	1	1	1	1

Fig. 10

11. Fig. 11 is a cascade ADC and its encoder table. The opearation process is that Vin1 is quantized by a first-stage ADC, then the encoder changes the thermalmeter code $T_{1\sim3}$ to the binary code $b_{1\sim2}$. The value of V_{in2} is the difference between V_{in1} and V_{out1}, and then is quantized by the second-stage ADC to generate $b_{3\sim5}$.

(a) Please answer what type the first-stage ADC is?

(b) Please answer what type the second-stage ADC is?

(c) If V_{in1} = 3V, please find the result of $T_{1\sim3}$ and $b_{1\sim2}$.

(d) If V_{in2} = 1V, please find the result of $b_{3\sim5}$.

(e) Please calcuate the resolution, in terms of bit number, of this cascade ADC.

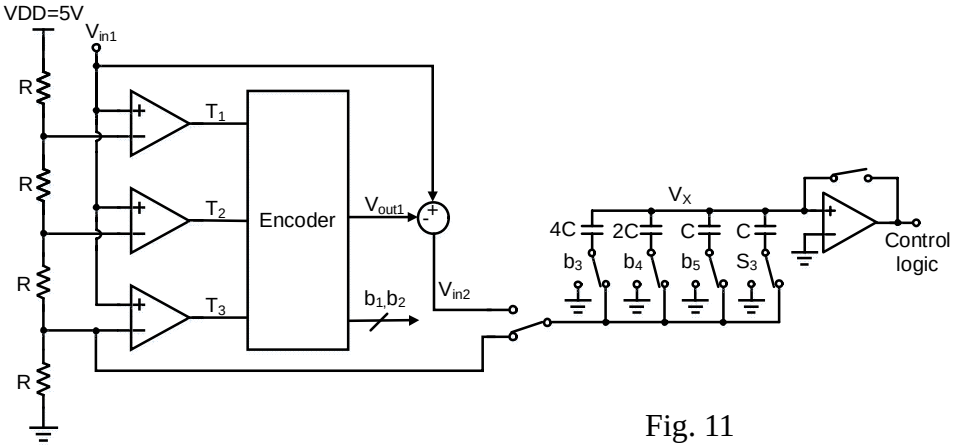


Fig. 11

Encoder Table

Thermometer code			Binary code		V_{out1}
T_1	T_2	T_3	b_1	b_2	
0	0	0	0	0	0V
0	0	1	0	1	1.25V
0	1	1	1	0	2.5V
1	1	1	1	1	3.75V

12. Fig. 12 shows an active-RC filter circuit, where R_1 = 100kΩ, R_2 = 1MΩ and C = 2pF.

(a) Assume the op-amp is ideal, please derive the transfer function $T(s) = \frac{V_o}{V_i}$ in terms of R_1, R_2 and C.

(b) According to (a), V_i is a sine wave with a frequency of 10Hz and a peak amplitude of 0.1V, please find the peak amplitude of V_o.

(c) Assume that the op-amp has a finite gain and a finite bandwidth, please derive T(s) and explain how the filter will be affected by these two non-idealities.

(d) Please calculate the pole of this filter. (unit: Hz)

(e) To avoid affecting the passband of the filter, please specify the required unity-gain bandwidth of the opamp. Explain your reason.

(f) If a 0.5-V_{peak}, 50MHz sine wave is inputted at V_i, please specify the required slew rate of the opamp. Explain your reason.

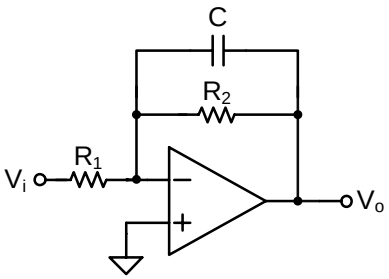


Fig. 12

13. Figs. 13(a) and 13(b) show a SC integrator and an active inductor circuit, respectively.

(a) In Fig. 13(a), please derive the SC integrator's time constant in terms of C_1, C_2 and T_C.

(b) In Fig. 13(a), explain why the circuit is insensitive to stray capacitances at node a, b and c.

(c) Please explain the pros and cons of a SC integrator compared with an active-RC one.

(d) In Fig. 13(b), assume that all G_m blocks have infinite input impedance, please derive the equivalent inductance L_{eq} in terms of C_L and G_m.

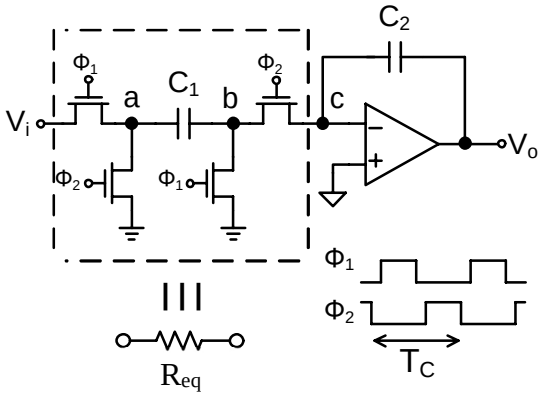


Fig. 13(a)

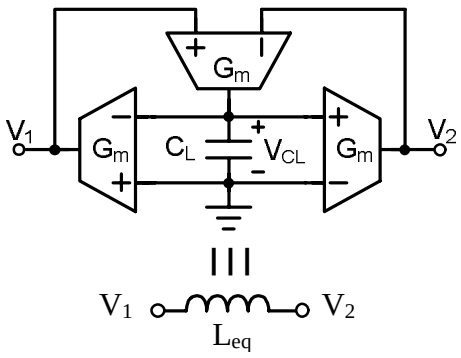


Fig. 13(b)

14. Please explain or give definitions of the following terms.

(a) Stagger-tuned amplifier

(b) Synchronous-tuned amplifier

(c) Total harmonic distortion (THD)

(d) Antoniou inductance-simulation circuit

(e) Slew rate

(f) Inter-modulation distortion

(g) Full-power bandwidth

(h) Stray capacitor

(i) Universal filter

(j) Nyquist theorem

15. Fig. 15 shows the block diagram of a universal filter, where $\frac{V_x(s)}{V_i(s)} = \frac{Ks^2}{s^2 + s(\omega_0/Q) + \omega_0^2}$.

(a) Please specify which type of filter $\frac{V_x(s)}{V_i(s)}$ is. Explain your reason.

[Hint: low-pass/ high-pass/ band-pass/ band-reject/ all-pass]

(b) Please derive the transfer function $\frac{V_z(s)}{V_i(s)}$. Specify and explain which type of filter it is.

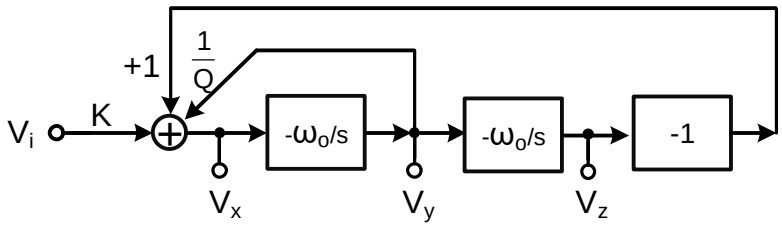


Fig. 15

16. Figs. 16(a) and 16(b) show an inductor-simulation circuit and its equivalent model, respectively.

(a) Assume that the op amp is ideal, please express $V_x(s)$ in terms of $V_i(s)$, R_2, and C.

(b) Please prove that the equivalent inductance $L_{eq} = R_1R_2C$, assume that $R_2 >> R_1$ and $sL_{eq} << 1/(sC)$. [Hint: Fig. 16(c)].

(c) Compared with real on-chip inductor, please explain the pros and cons of the circuit in Fig. 16(a).

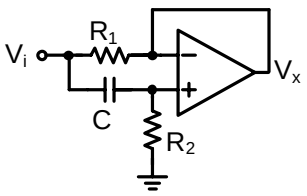


Fig. 16(a)

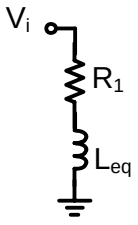


Fig. 16(b)

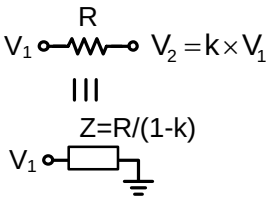


Fig. 16(c)

17. Fig. 17(a) shows an inductor-simulation circuit, and Fig. 17(b) shows its equivalent model. Assume that the four transconductors is ideal, and ideal transconductors are defined in Fig. 17(c).

(a) In Fig. 17(b), please express the current I in terms of V_1, V_2, and the impedance sL_{eq}.

(b) Assume $g_{m2}=g_{m3}$, please prove that $I_1=I_2$.

(c) Assume $g_{m1}=g_{m2}=g_{m3}=g_{m4}=g_m$, please derive the equivalent inductance (L_{eq}) in terms of g_m and C.

(d) Compared with a real inductor, please explain the benefits and drawbacks of the circuit in Fig. 17(a).

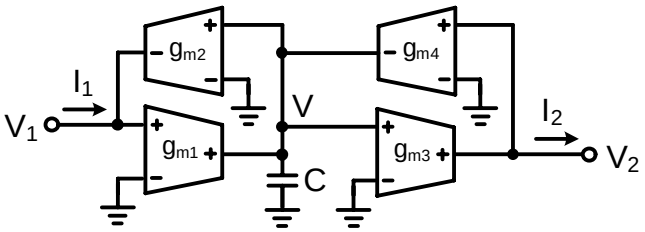


Fig. 17(a)

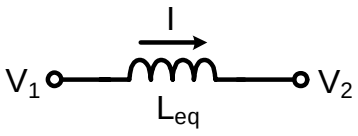


Fig. 17(b)

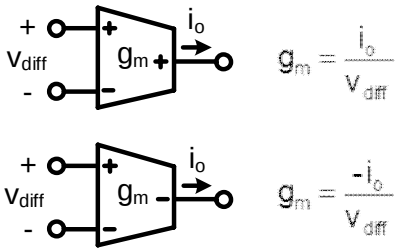


Fig. 17(c)

18. Fig. 18 shows the block diagram of a two-integrator-loop biquad. Please

(a) Express $V_t(s)$ in terms of $V_x(s)$, ω_o and Q.

(b) Derive the transfer function of $\dfrac{V_x(s)}{V_i(s)}$.

(c) Specify which types of filters $\dfrac{V_y(s)}{V_i(s)}$ and $\dfrac{V_z(s)}{V_i(s)}$ are. Explain your reason.

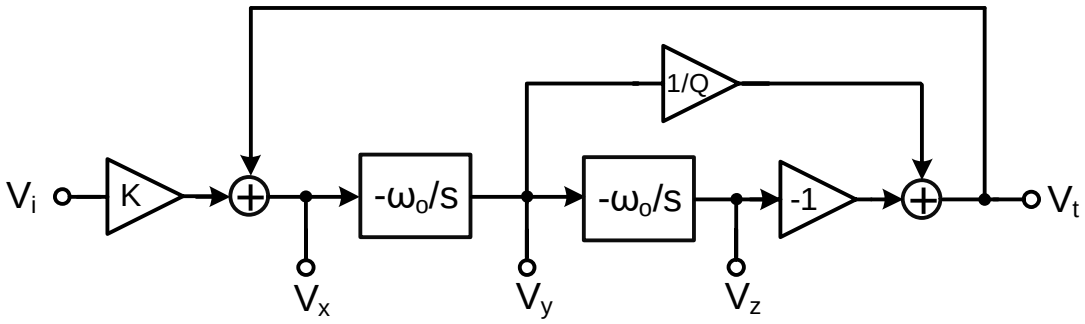


Fig. 18

19. Fig. 19 shows two implementation methods of noninverting integrator.

(a) Derive the transfer function of $\dfrac{V_{o1}(s)}{V_{i1}(s)}$ in Fig. 19(a).

(b) In Fig. 19(b), assume that R_2 is equivalent to a negative resistor, where $R_2=-R_1<0$. Please derive the transfer function of $\dfrac{V_{o2}(s)}{V_{i2}(s)}$.

(c) Draw the switched-capacitor version of the circuit in Fig. 19(b) by replacing R_1 and R_2 with stray-insensitive switched-capacitor circuit.

(d) Compared with Fig. 19(a), please list the benefits of switched-capacitor version in (c).

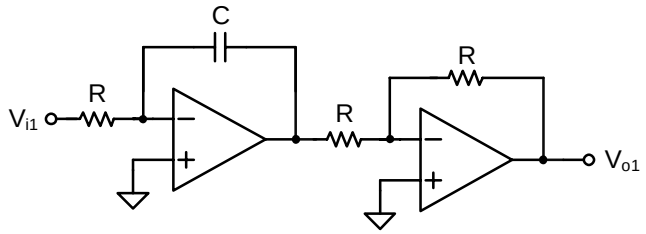


Fig. 19(a)

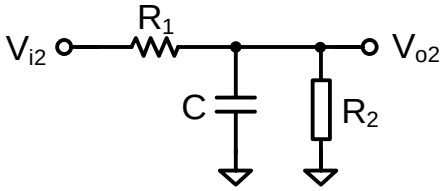


Fig. 19(b)

20. (a) Please sketch both **inverting and non-inverting** stray-insensitive switched-capacitor (SC) integrator respectively.

(b) Fig. 20 shows an active-RC biquad, please sketch its SC equivalent circuit with **only two** op amps.

(c) Compared with active-RC filters, please list the **benefits** of SC filters.

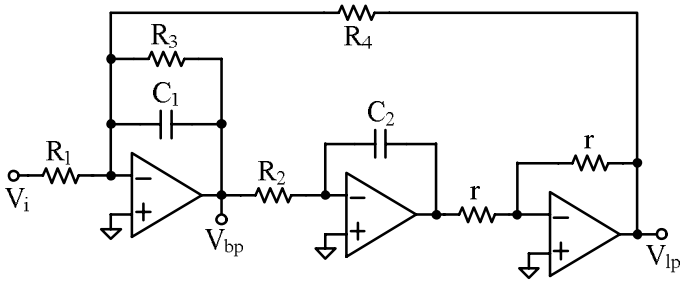


Fig. 20

21. Fig. 21 shows a filter, where R=100kΩ and C=1.6pF.

(a) Assume that V_i is a sine wave with a frequency of 100kHz and a peak amplitude of 1V. If the op amp is ideal, please find the peak amplitude of V_o.

(b) If the op amp has a finite bandwidth and a finite slew rate, please explain how the filter's function will be influenced by the two non-idealities **respectively**.

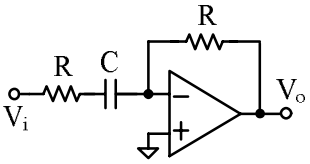


Fig. 21

22. Fig. 22 shows a 14-bit dual-slope ADC. Assume C = 100pF, V_{REF} = -1.8V, and v_{IN} is in the range of 0V and 1.8V. If the maximum conversion time T is 1ms, find the value of R and the required clock frequency f_{clk}. ($f_{clk} = 1 / T_{clk}$)

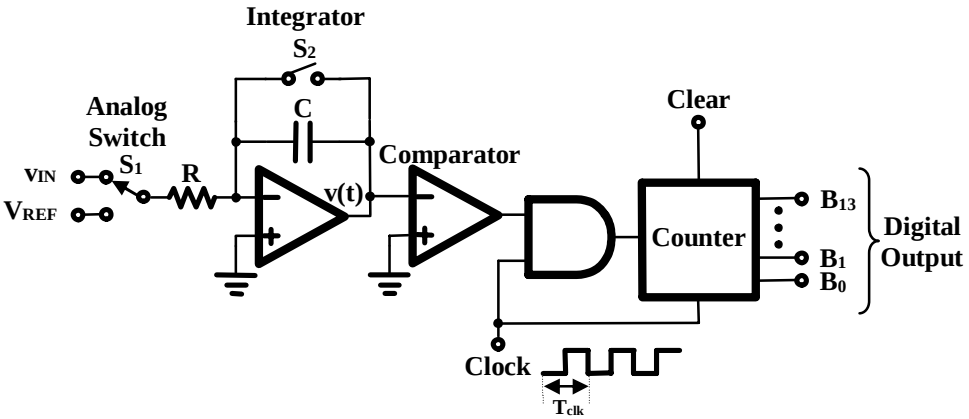


Fig. 22

23. Draw a basic circuit of a 3-bit DAC utilizing an R-2R ladder network, and describe its operation.

24. (a) A charge-redistribution circuit is initially connected as in Fig. 34a and then the circuit is connected as in Fig.

24b. Find the node voltage V_x in Fig. 34b where V_{in}=1V and V_{ref}=5V.

(b) Describe the operational principle of a 2-bit R-2R D/A converter. (Illustration is needed.)

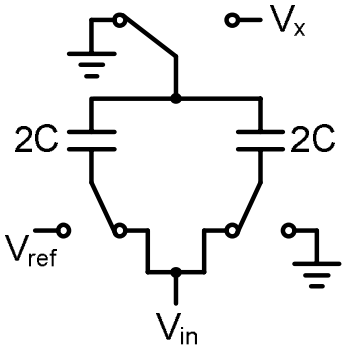


Fig. 24a

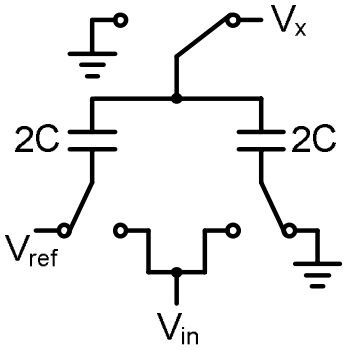


Fig. 24b

25. (a) For a KHN circuit shown in Fig. 25, please describe the functions of V_a, V_b, V_c nodes and briefly explain the operational principle of the KHN circuit.

(b) Draw a Tow-Thomas circuit and explain its operational principle.

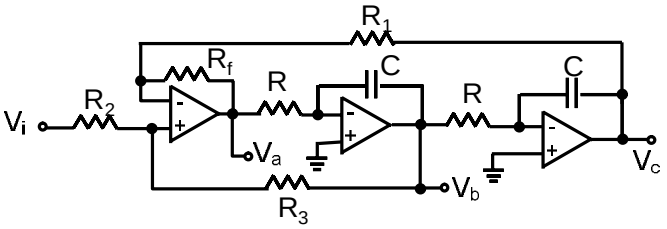


Fig. 25

26. As shown in Fig. 26, a low-pass filter is specified to have passband edge f_p = 5 kHz and a selectivity factor (f_s/f_p) of 10. The specifications are met by a first-order transfer function $T(s) = \frac{2\pi\times10^4}{s+2\pi\times10^4}$. Please answer the following questions.

(a) Find the value of stopband edge (f_s).

(b) Find the value of passband ripple (A_{max}).

(c) Find the value of stopband attenuation (A_{min}).

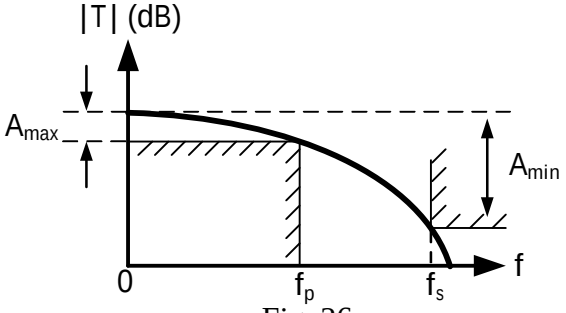


Fig. 26

27. Fig. 27 shows one of successive-approximation ADC's implementation operating in sample mode. Assume that V_i = 0.6V, V_{ref} = 1.0V.

(a) When entering the hold mode, B_0 ~ B_2 and S_3 switch from V_i to ground, and S_2 switches off, please find the value of V_X.

(b) According to (a), when entering the redistribution mode, only B_2 switches to V_{ref}, please find the value of V_X.

(c) Please give one benefit and one drawback of the successive-approximation ADC compared with a 3-bit flash ADC.

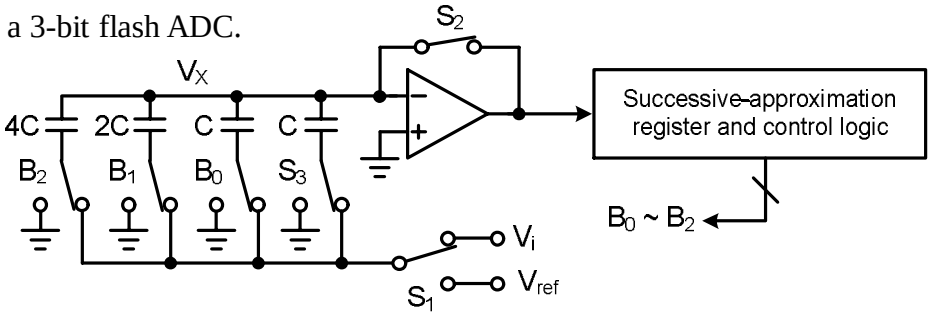


Fig. 27

28. Fig. 28 shows an active-RC integrator.

(a) Assume that the opamp is ideal with A(s) = ∞, please derive the transfer function $\frac{V_o}{V_i}(s)$.

(b) Assume that the opamp is real with $A(s) = \frac{A_o}{1+s/s_1}(s)$, pleases derive transfer function $\frac{V_o}{V_i}(s)$.

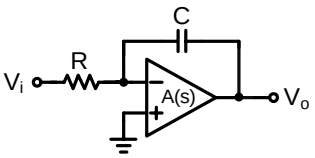


Fig. 28

(c) Please explain how the integrator will be affected by the finite gain and finite bandwidth of the real opamp, **respectively**.

29. Fig. 29 shows a binary-weighted 3-bit DAC, where V_{ref} = 0.5V, R_F=2kΩ and R=1kΩ. Please

(a) find V_{out} when the input binary bits $B_2B_1B_0 = (110)_2$.

(b) sketch an R-2R ladder-type 3-bit DAC.

(c) explain the benefit of the R-2R ladder-type compared with the binary-weighted DAC.

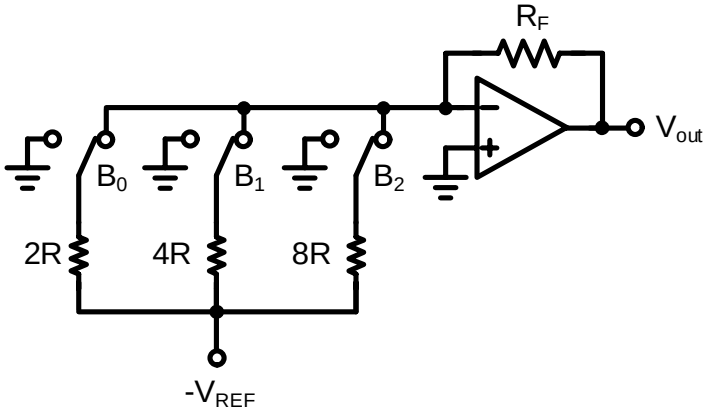


Fig. 29