Operational Amplifier (OPAMP)

- Analog ICs include
  - Operational amplifier
  - Filters
  - Analog-to-digital converter (ADC)
  - Digital-to-analog converter (DAC)
  - Analog modulator
  - Phase-locked loop
  - Power management
  - Others
- Basic building blocks of analog ICs
  - Single-stage amplifier
  - Differential pairs
  - Current mirrors
  - MOS switches
  - Others

Operational Amplifier (Cont.)

- OPAMP design
  - CMOS OPAMPs are adequate for VLSI implementation.
    - Main stream
    - Two-stage and folded-cascode OPAMPs will be introduced.
  - Bipolar OPAMPs
    - Can achieve better performance than CMOS OPAMPs.
    - Less popular
    - 741 OPAMP will be introduced.
  - BiCMOS OPAMPs
    - Combine the advantages of bipolar and CMOS devices.
    - Less popular
    - First published by H. C. Lin in 1960's.

CMOS Operational Amplifier (OPAMP)

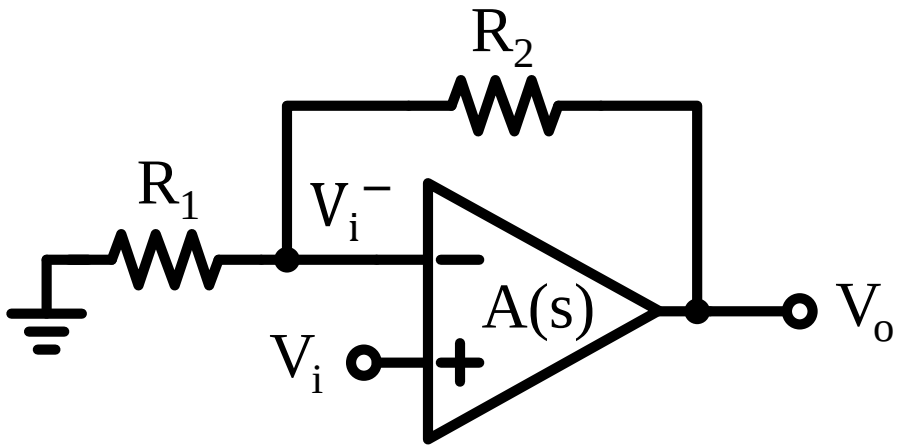
- Two-stage

  I guess, it is for 70% applications.
- Folded-cascode

  I guess, it is for 20% applications.
- Others

Stability and Compensation of OPAMP

- Operational amplifier with negative feedback



$$\beta = \frac{R_1}{R_1 + R_2}$$

$$V_i^-(s) = \beta V_o(s)$$

$$V_o(s) = A(s)(V_i(s) - V_i^-(s))$$

$$A_f(s) = \frac{V_o(s)}{V_i(s)} = \frac{A(s)}{1 + \beta A\,(s)}$$

for
- A_f is closed-loop gain
- A is open-loop gain
- βA is loop gain

Open-loop : always stable (no internal feedback)

Closed-loop : stability depends on βA(s)

Stability and Compensation of OPAMP (Cont.)

- For stable system, the real part of all poles must be negative.
  - Gain margin = $20\log|\beta A(j\omega_{180})|$
  - Unity-gain frequency ω_t
  - Phase Margin = $\measuredangle\beta A(j\omega_t) + 180°$

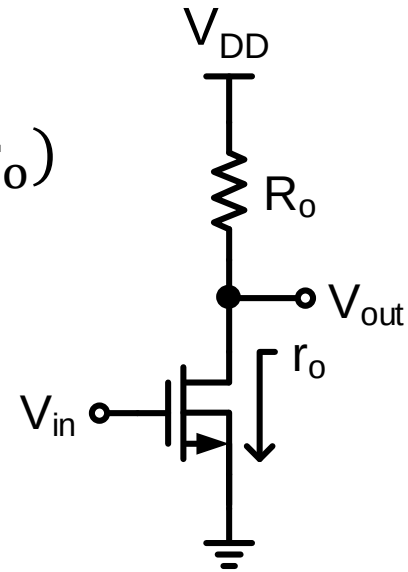
    At least 45° ~ 60° (or larger) margin is preferred.

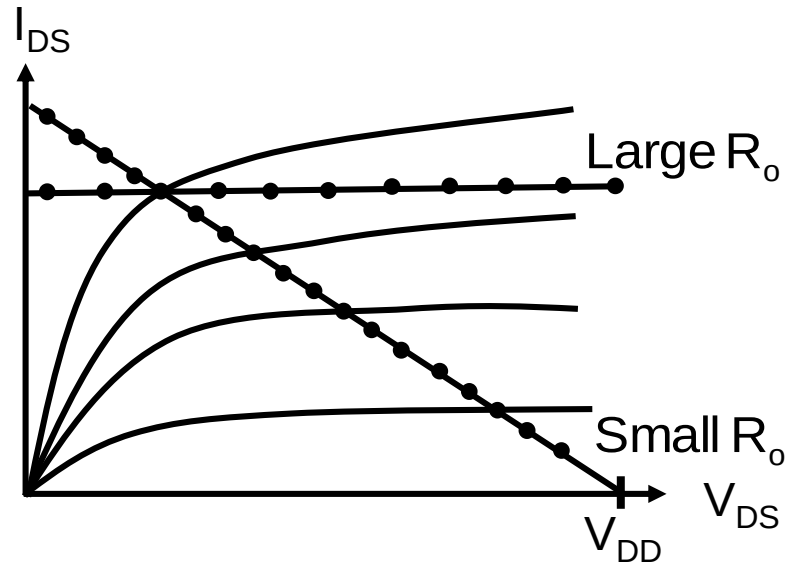
    This will also give a desirable (i.e., small or no ringing) step response for the closed-loop amplifier.

CMOS Amplifier with Resistive Load

- Resistor Load

$$A = -g_m(R_o//r_o)$$
$$\approx -g_m R_o$$
$$\propto \frac{-I_D R_o}{V_{ov}}$$

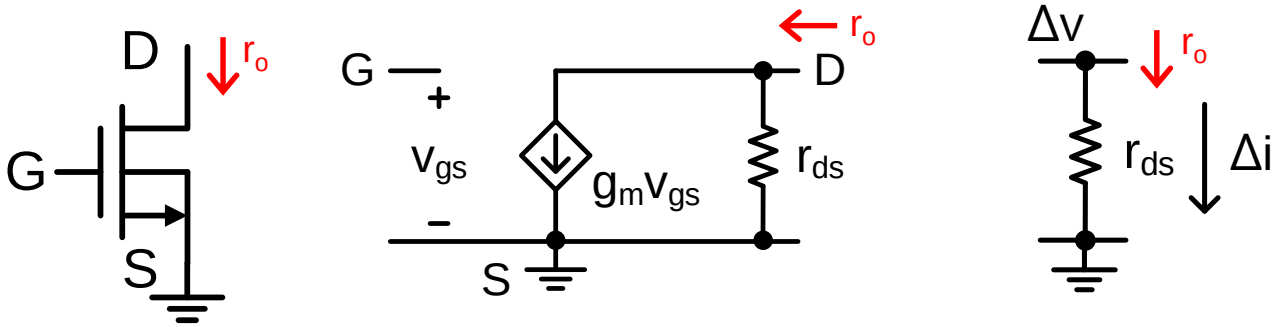




- For high gain
  - High $I_D R_o$
    - High $I_D R_o$ means large voltage drop on R_o
    - Large power supply
  - High R_o reduces speed
  - Use active loads to overcome the above problems.

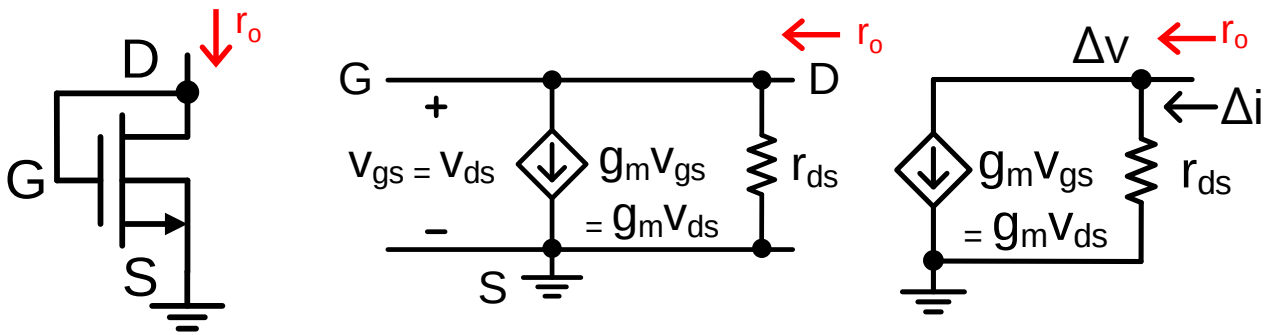
Resistance of Active Load

- Small signal model of NMOS



$$r_o = \frac{\Delta v}{\Delta i} = r_{ds}$$

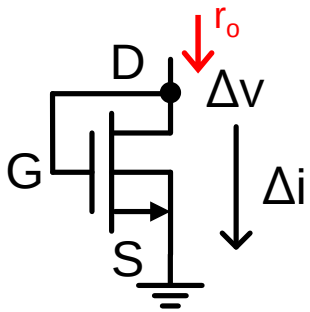
- Small signal model of diode-connected NMOS



$$\Delta i = g_m \Delta v + \frac{\Delta v}{r_{ds}}$$

$$r_o = \frac{\Delta v}{\Delta i} = r_{ds} || \frac{1}{g_m}$$

- Same analysis method



$$r_o = \frac{\Delta v}{\Delta i} = r_{ds} || \frac{1}{g_m}$$

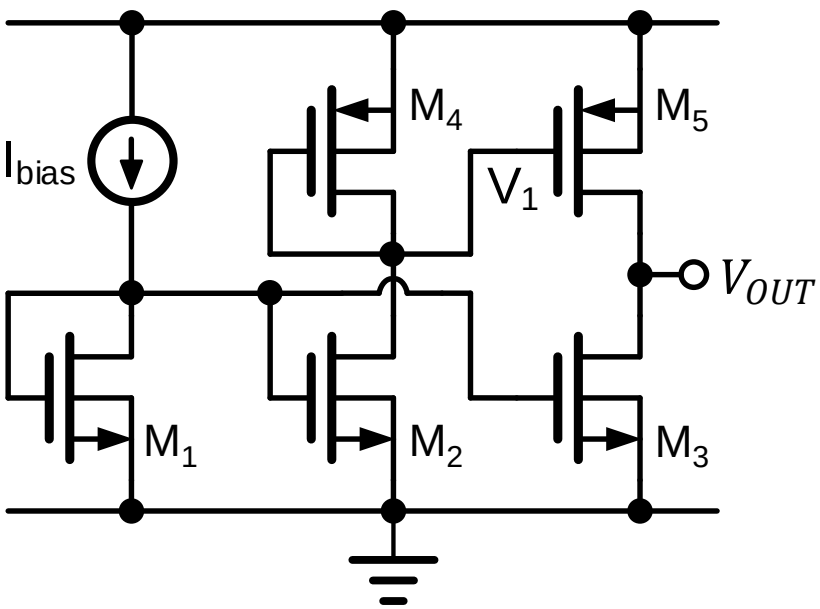
CMOS Amplifier with Active Load

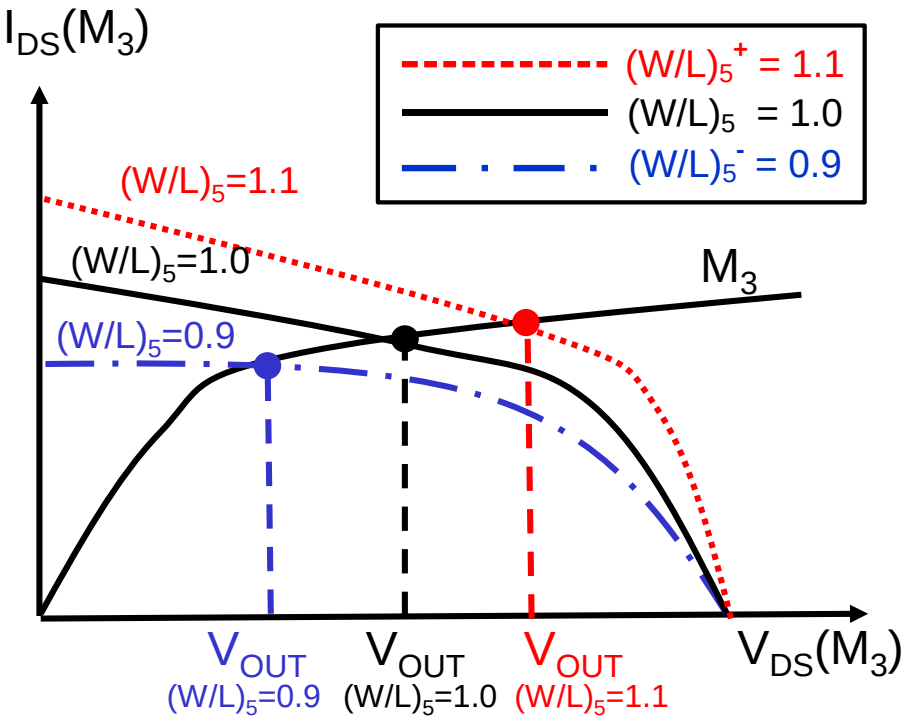
- The effect of process variations on quiescent point V_{OUT}

Nominal design: $\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = \left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_4 = \left(\frac{W}{L}\right)_5 = 1$

Assumption: $\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = \left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_4 = 1$, $\boxed{\left(\frac{W}{L}\right)_5 = 1 \pm 10\%}$ Due to process variations

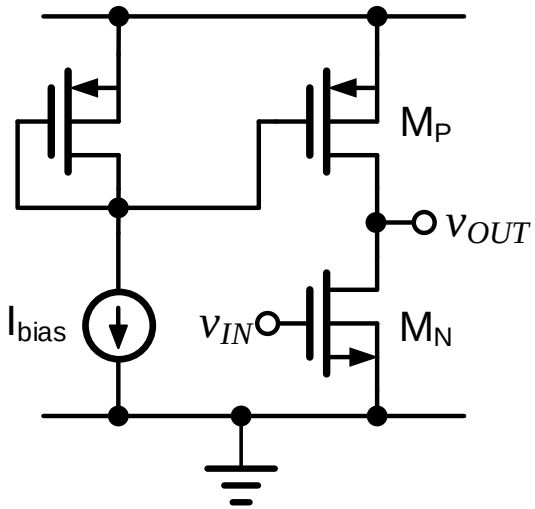
→ V_{OUT} is determined by the actual values of M_1 ~ M_5

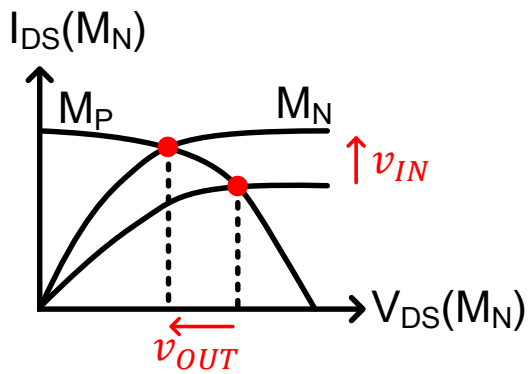




Single-Ended Amplifier with Active Load

- N-input common-source amplifier



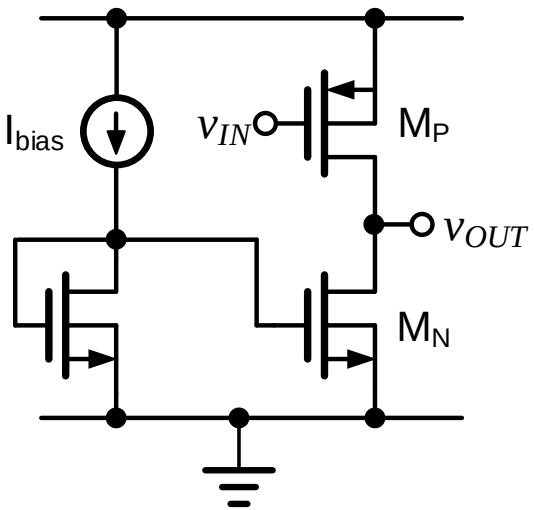


$$v_{IN} = V_{IN} + C\sin\omega t$$

$$v_{OUT} = V_{OUT} + AC\sin\omega t$$

where $A = \frac{v_{out}}{v_{in}} = -g_{mn}\left(r_{dsp} \parallel r_{dsn}\right)$

- P-input common-source amplifier



$$v_{IN} = V_{IN} + C\sin\omega t$$

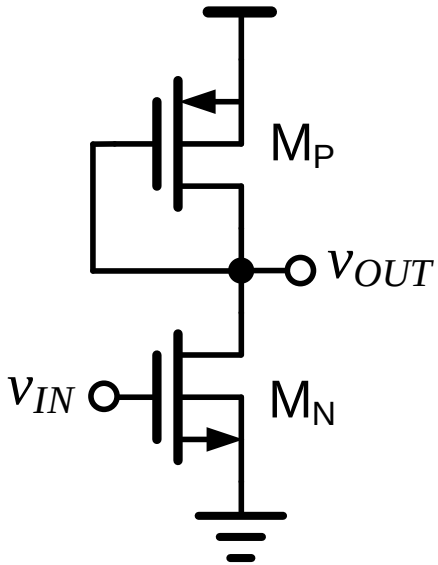
$$v_{OUT} = V_{OUT} + AC\sin\omega t$$

where $A = \frac{v_{out}}{v_{in}} = -g_{mp}\left(r_{dsp} \parallel r_{dsn}\right)$

→ Quiescent point V_{OUT} is hard to be determined with active load

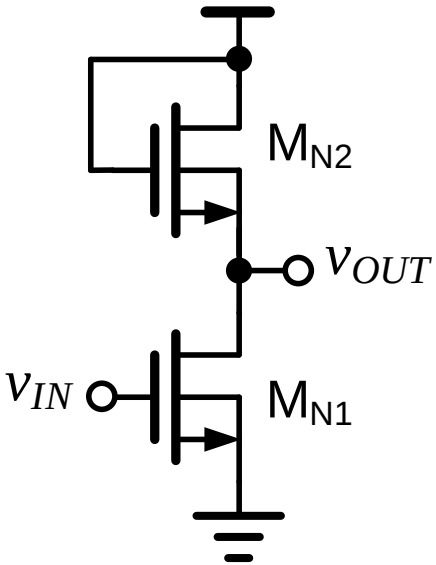
Single-Ended Amplifier with Diode-Connected Load

- Input and load transistor types
  - Different type



$$v_{IN} = V_{IN} + C\sin\omega t$$
$$v_{OUT} = V_{OUT} + AC\sin\omega t$$
$$A = \frac{v_{out}}{v_{in}} = -g_{mn}\left(r_{dsp} \parallel r_{dsn} \parallel \frac{1}{g_{mp}}\right)$$
$$= -\frac{g_{mn}}{g_{mp}} \text{ (gain with small } \sqrt{\frac{\mu_n}{\mu_p}} \text{ variation)}$$

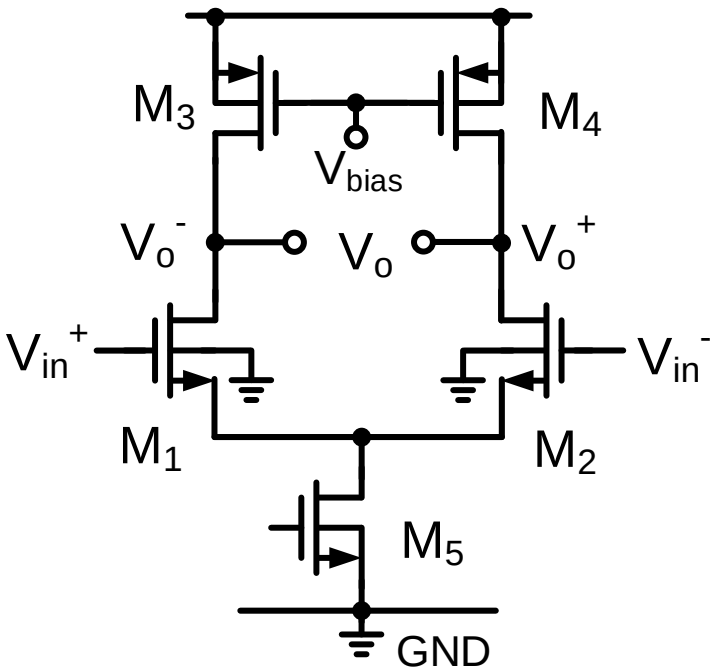
  - Same type

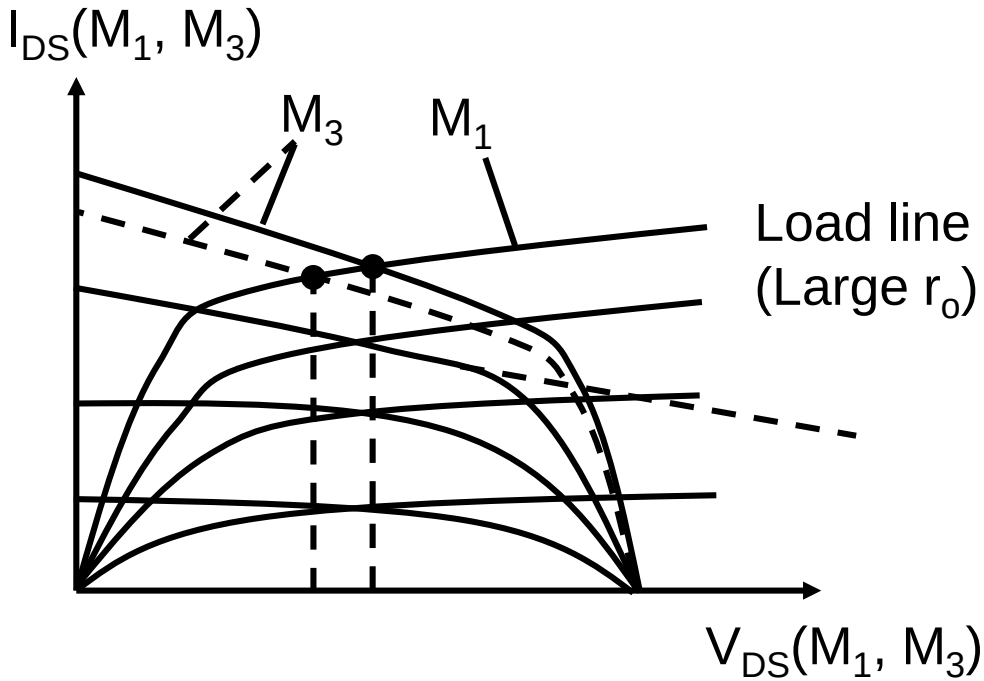


$$v_{IN} = V_{IN} + C\sin\omega t$$
$$v_{OUT} = V_{OUT} + AC\sin\omega t$$
$$A = \frac{v_{out}}{v_{in}} = -g_{mn1}\left(r_{dsn1} \parallel r_{dsn2} \parallel \frac{1}{g_{mn2}}\right)$$
$$= -\frac{g_{mn1}}{g_{mn2}} \approx \sqrt{\frac{(W/L)_{MN1}}{(W/L)_{MN2}}} \text{ (accurate gain)}$$

CMOS Amplifier with Active Load

- With external bias





- Why not?

→ Quiescent point of V_o^+ & V_o^- can't be determined due to process variations

CMOS Amplifier with Active Load (Cont.)

- Self-biased active load: quiescent V_o less sensitive to M_1 ~ M_4 variations
- Performs differential gain and differential to single-ended
  $g_{m,M1}, g_{m,M2}, g_{m,M3}, g_{m,M4} \gg \frac{1}{r_{ds}}$; $r_{out} \approx r_{ds2} \parallel r_{ds4}$
- Differential gain A_{dm} $(v_{i1} = -v_{i2} = \frac{1}{2} v_{in})$
  $A_{dm} \approx g_{m1}(r_{ds2} \parallel r_{ds4})$ at node B = A_{dmB}
  Node A: $A_{dmA} \approx -\frac{1}{2} g_{m1} \cdot \frac{1}{g_{m3}}$
  Node B: $A_{dmB} \approx (-\frac{1}{2} g_{m2} - A_{dmA} \cdot g_{m4}) \cdot (r_{ds2} \parallel r_{ds4})$
- Common-mode gain A_{cm} $(v_{i1} = v_{i2} = v_1)$

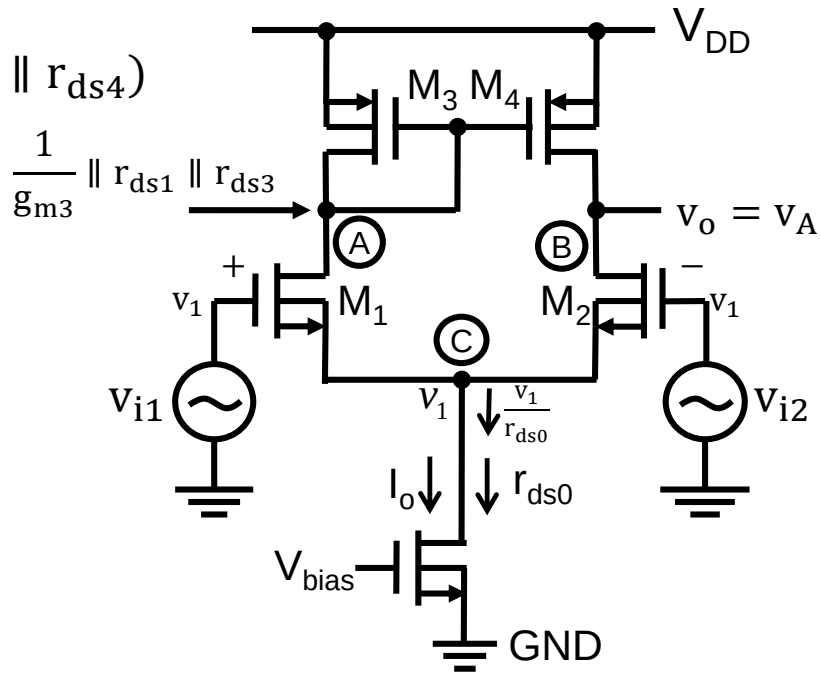
$$v_A = \frac{1}{2} \frac{v_1}{r_{ds0}} \left(\frac{1}{g_{m3}} \parallel r_{ds1} \parallel r_{ds3} \right)$$

$$A_{cm} \approx \frac{1}{2} \frac{1}{r_{ds0}} \left(\frac{1}{g_{m3}} \parallel r_{ds1} \parallel r_{ds3} \right) \approx \frac{1}{2 g_{m3} r_{ds0}}$$

- CMRR(Common-Mode Rejection Ratio)

$$\mathrm{CMRR} = \frac{A_{dm}}{A_{cm}} \approx 2 g_{m1} (r_{ds2} \parallel r_{ds4}) g_{m3} r_{ds0}$$

- Model of A_{dm}/A_{cm}

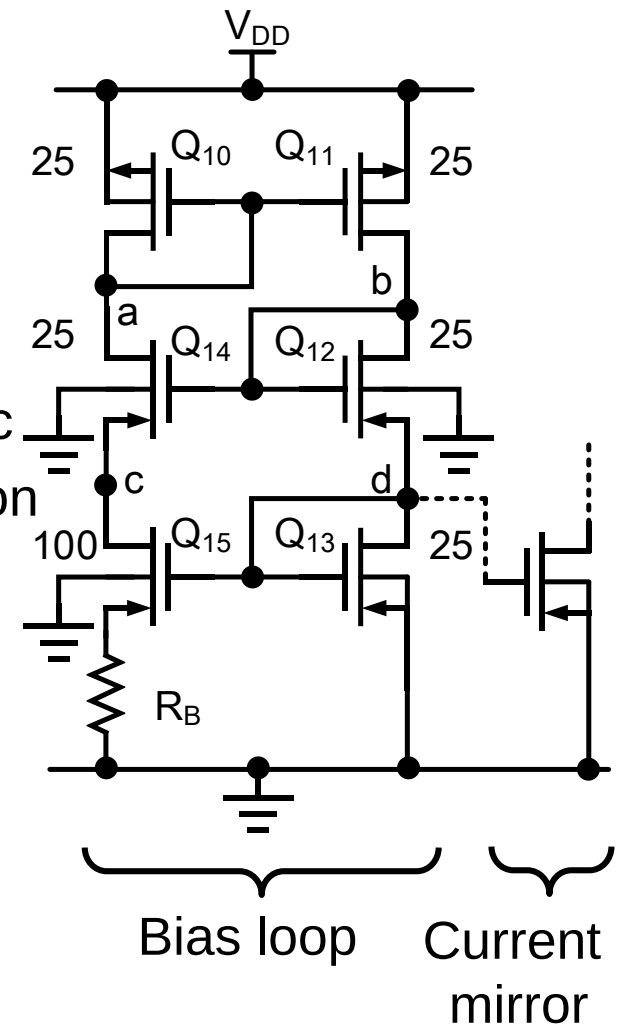


Constant Transconductance Bias Circuit

- Biasing circuits that provide stable transconductances
  - Transistor transconductances are matched to the conductance of a resistor.
    To a first-order effect, the transistor transconductances are independent of process as well as power-supply voltage and temperature variations (PVT variations).
  - Q_{14} (Q_{12}) causes voltage drop between a and c (b and d) to minimize channel length modulation
  - Q_{12} is diode-connected to provide a bias voltage to Q_{14}
  - Example

$$\left(\frac{W}{L}\right)_{10} = \left(\frac{W}{L}\right)_{11} = \left(\frac{W}{L}\right)_{12} = \left(\frac{W}{L}\right)_{13} = \left(\frac{W}{L}\right)_{14}$$

Unity current mirror



Constant Transconductance Bias Circuit (Cont.)

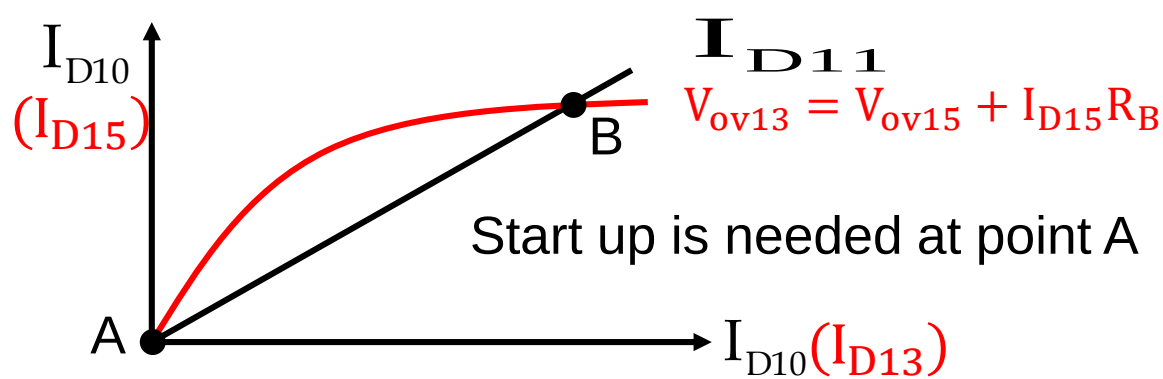
$$\begin{cases} V_{ov13} = V_{ov15} + I_{D15}R_B & \text{bottom current mirror (widlar)} \\ I_{D10} = I_{D11} \text{ i.e. } I_{D13} = I_{D15} & \text{top current mirror (linear)} \\ g_{m13} = \dfrac{2I_D}{V_{ov13}} \end{cases}$$

- Simple derivation

$$\rightarrow \quad g_{m13} = 2\left(\frac{V_{ov13} - V_{ov15}}{R_B}\right) \times \frac{1}{V_{ov13}} = \frac{2\left[1 - \sqrt{\dfrac{(W/L)_{13}}{(W/L)_{15}}}\right]}{R_B}$$

- g_{m13} is determined by geometric ratios only, independent of process parameters, temperature (PVT), or any other parameters with large variability.
- At point A, loop gain

$$= \frac{(W/L)_{11}}{(W/L)_{10}} \times \frac{(W/L)_{15}}{(W/L)_{13}}$$



Constant Transconductance Bias Circuit (Cont.)

- For a special case, $\left(\frac{W}{L}\right)_{15} = 4\left(\frac{W}{L}\right)_{13} \rightarrow \quad g_{m13} = \frac{1}{R_B}$
- Thus, not only is g_{m13} stabilized, but all other transistors transconductances are also stabilized since the ratios of transistor currents are mainly dependent on geometry.
- For all n-channel transistors

$$g_{mi} = \sqrt{\frac{(W/L)_i I_{Di}}{(W/L)_{13} I_{D13}}} \times g_{m13}$$

- For all p-channel transistors

$$\begin{cases} I_{D10} = I_{D13} \\ g_{m10} = \sqrt{2\mu_p C_{ox}(W/L)_{10} I_{D10}} \\ g_{m13} = \sqrt{2\mu_n C_{ox}(W/L)_{13} I_{D13}} \end{cases} \Rightarrow g_{m10} = \sqrt{\frac{\mu_p}{\mu_n}\frac{(W/L)_{10}}{(W/L)_{13}}} \times g_{m13}$$

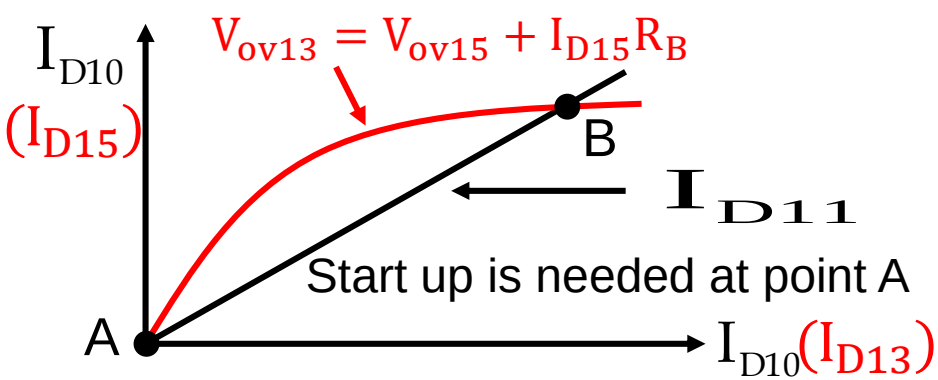
Similarly, $g_{mi} = \sqrt{\frac{\mu_p (W/L)_i I_{Di}}{\mu_n (W/L)_{13} I_{D13}}} \times g_{m13}$

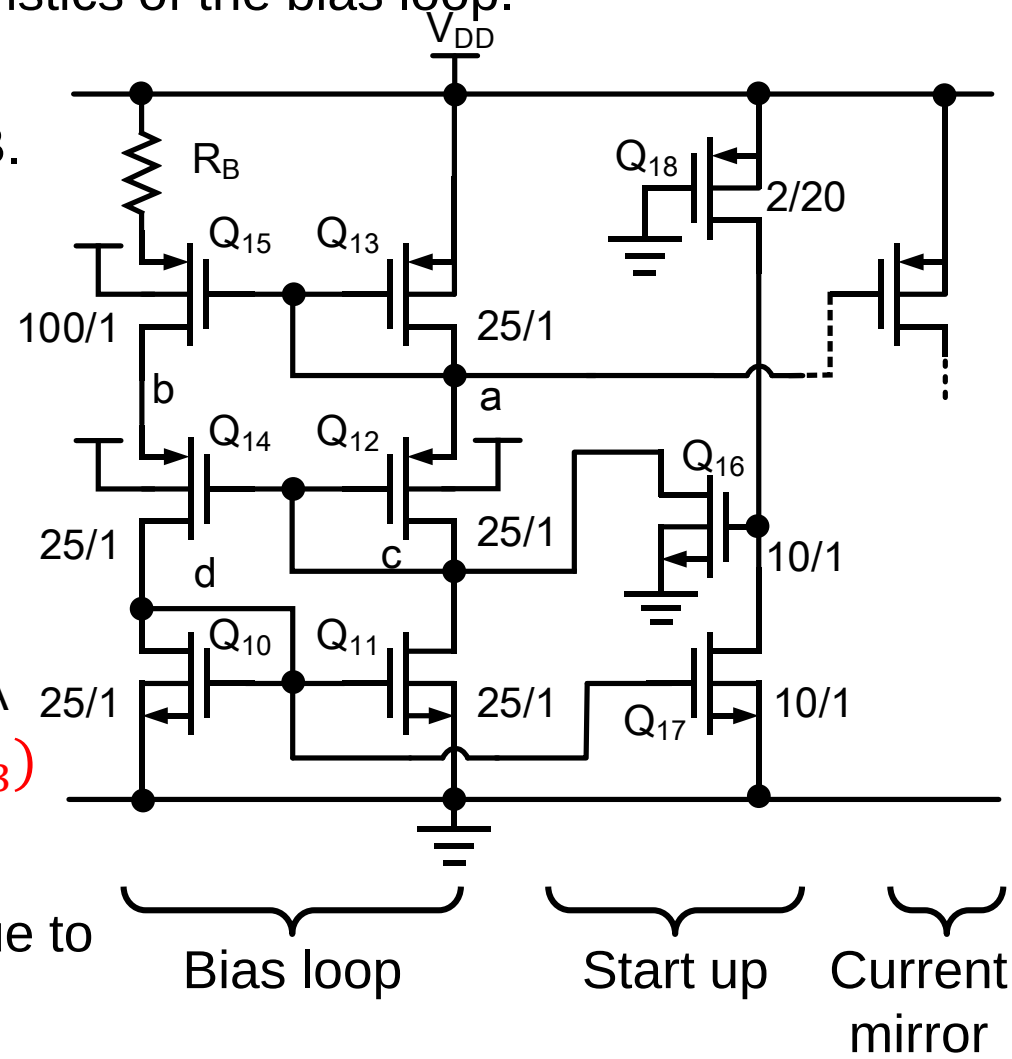
(Larger variation due to extra $\sqrt{\mu_p/\mu_n}$ variation)

Constant Transconductance Bias Circuit (Cont.)

- P-type constant transconductance bias circuit with start-up circuit
  - Approximate current characteristics of the bias loop.
  - Positive feedback bias loop:
    - Two stable points, A and B.
    - At point A, loop gain

$$\approx \frac{(W/L)_{11}}{(W/L)_{10}} \times \frac{(W/L)_{15}}{(W/L)_{13}} = 4$$





  - For all n-channel transistors
    - g_{mi} has larger variation due to extra $\sqrt{\mu_n/\mu_p}$ variation

Constant Transconductance Bias Circuit (Cont.)

- Start-up circuit
  - Operational principle of start-up circuit
    - All currents in the bias loop are zero, Q_{17} will be off.
    - Q_{18} is always on, the gates of Q_{16} will be pulled high.
    - Q_{16} will inject currents into the bias loop, which will start up the circuit.
    - Once the loop starts up, Q_{17} will be on, pulling the gate of Q_{16} low, and thereby turning it off so it no longer affects the bias loop.
    - This circuit is only one example of a start-up loop, and there are many other variations.
    - For example, sometimes Q_{18}, is replaced by an actual resistor.

Widlar Current Sources

- For large current mirror ratio
- Bipolar

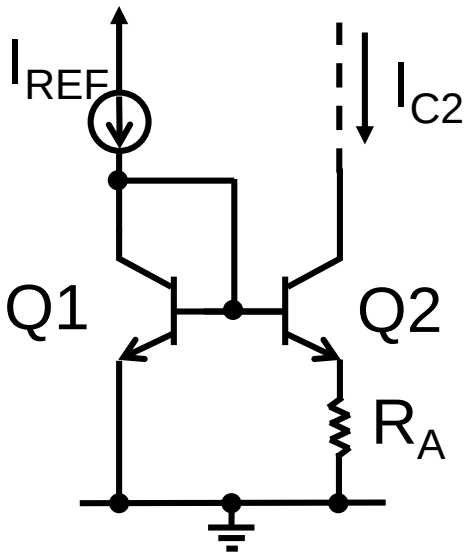
$I_{REF} = 0.73mA, R_A = 5k\Omega$

$V_{BE1} - V_{BE2} = I_{C2}R_A$

$\Rightarrow V_T \ln \frac{I_{REF}}{I_{C2}} = I_{C2}R_A$

$\Rightarrow$ Trial and error to determine I_{C2}

$\Rightarrow I_{C2} = 19\mu A$



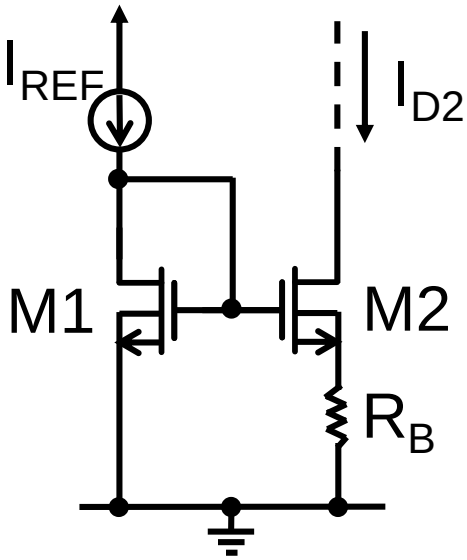
- MOSFET

$V_{OV1} = V_{OV2} + I_{D2} \times R_B$

Assume $I_D = K \cdot V_{OV}^2 \Rightarrow \sqrt{\frac{I_{REF}}{K}} = \sqrt{\frac{I_{D2}}{K}} + \left(\sqrt{I_{D2}}\right)^2 \times R_B$

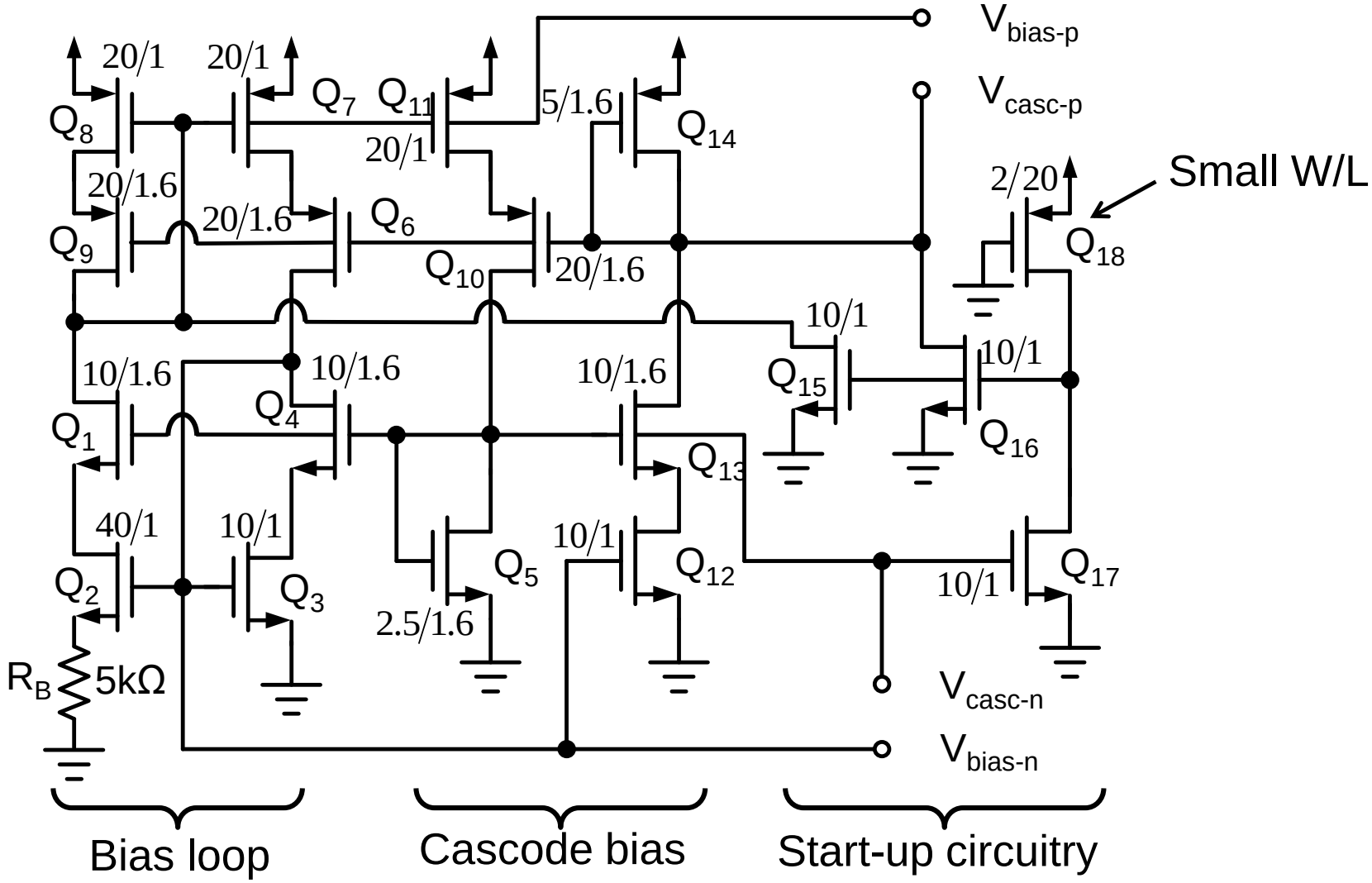
$$\sqrt{I_{D2}} = \frac{-\sqrt{\frac{1}{K}} \pm \sqrt{\frac{1}{K} + 4R_B\sqrt{\frac{I_{REF}}{K}}}}{2R_B} > 0$$

$$\Rightarrow I_{D2} = \frac{1 + 2R_B\sqrt{KI_{REF}} - \sqrt{1 + 4R_B\sqrt{KI_{REF}}}}{2K(R_B)^2}$$



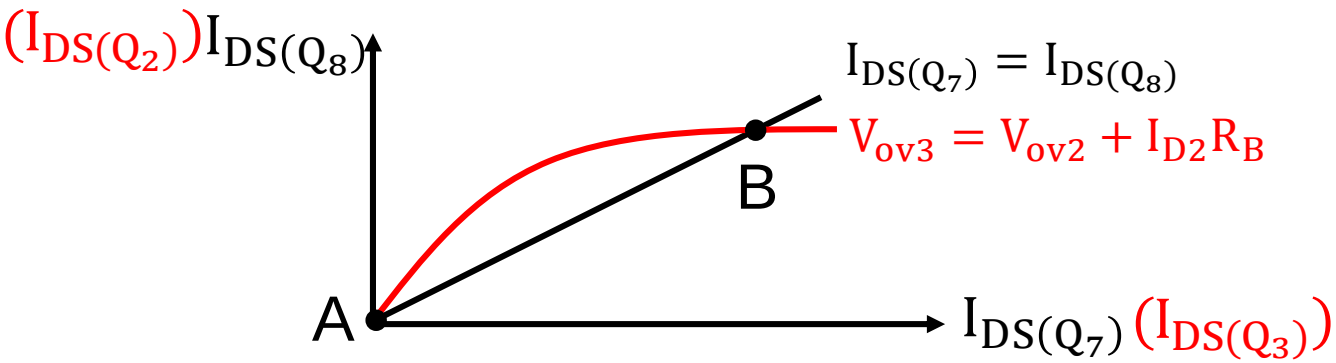
Wide-Swing Constant Transconductance Bias Circuit

- Wide-swing current mirrors + constant g_m bias circuit



Wide-Swing Constant Transconductance Bias Circuit (Cont.)

- Wide-swing :
  - Minimize V_{DS} of bias transistors to V_{ov}
- Constant g_m : $g_m = 1/R_B$
- Minimization of finite output impedance effect :
  - Use cascode bias
- Start-up
  - Approximate current characteristics of the bias loop
  - At point A, loop gain $\approx \frac{(W/L)_7}{(W/L)_8} \bullet \frac{(W/L)_2}{(W/L)_3} = 4$



Uncompensated Two-Stage CMOS OPAMP

$$A(s) = \frac{A_0}{(1+s/\omega_{P1})(1+s/\omega_{P2})}$$

$$A_0 = g_{m1}R_{01}g_{m6}R_{02}$$

$$g_{m1} = \sqrt{2\mu_p C_{OX}(W/L)_{M_1} I_1}$$

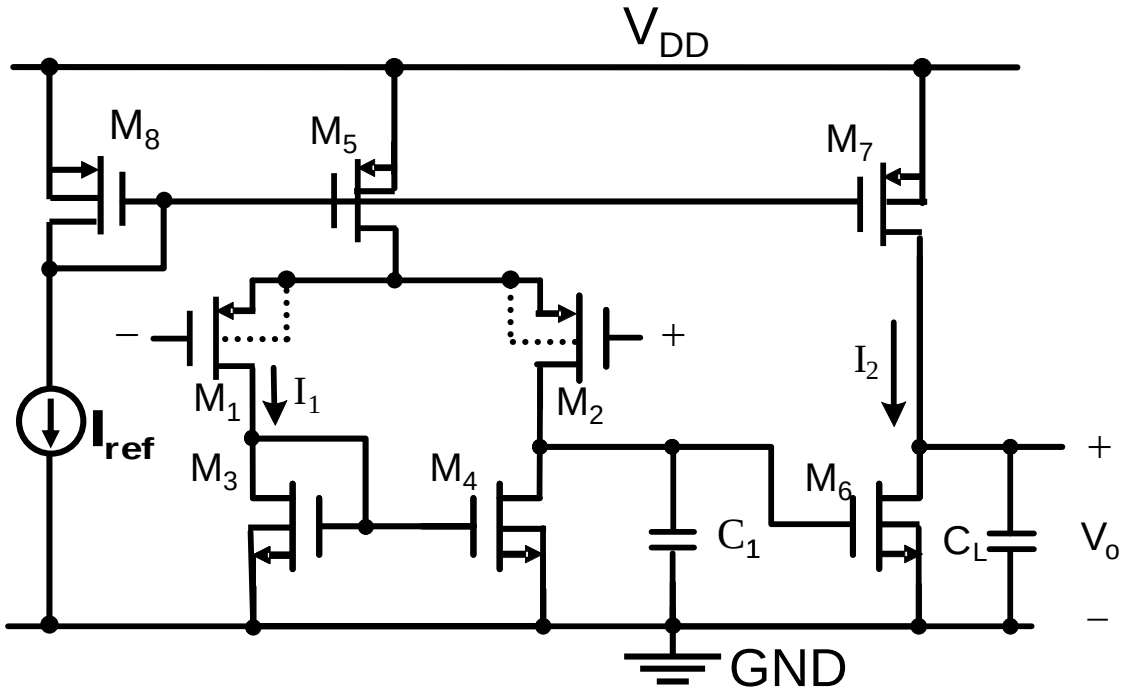
$$g_{m6} = \sqrt{2\mu_n C_{OX}(W/L)_{M_6} I_6}$$

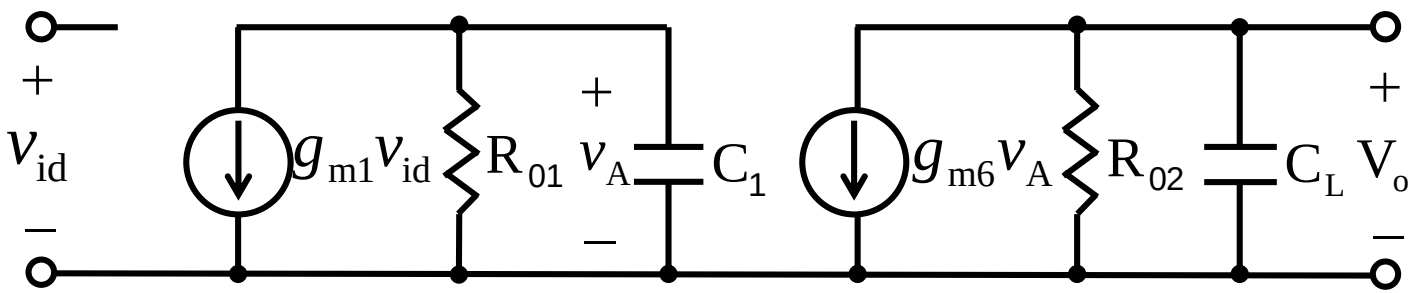
$$R_{01} = r_{ds2}//r_{ds4}$$

$$R_{02} = r_{ds6}//r_{ds7}$$

$$\omega_{P1} = -1/R_{01}C_1$$

$$\omega_{P2} = -1/R_{02}C_L$$





- P_1 & P_2 are dominant poles since R_{01} and R_{02} are normally large. The effects of other poles are usually negligible.

Uncompensated Two-Stage CMOS OPAMP (Cont.)

- For low frequency, $A(j\omega) = A(0) \approx A_0$

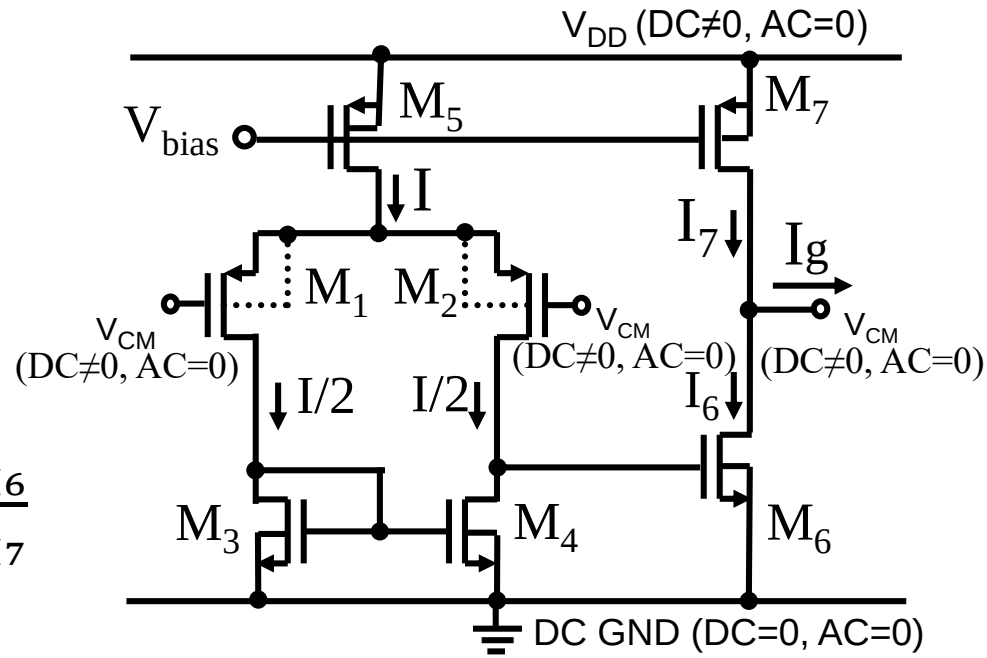
  For high frequency, $A(j\omega) \approx -\dfrac{g_{m1}g_{m6}}{\omega^2 C_1 C_L}$

  Hence, for high frequency, the amplifier inverts the input voltage. If feedback is used, then positive feedback occurs.

- Two dominant poles
  - ◆ Phase margin is not large enough
  - ◆ Use pole-splitting technique to solve this problem

Offset Voltage of Two-Stage CMOS OPAMPs

- Input voltage needs to restore the output to zero (ideal DC level)
- Two components
  - Systematic offset
  - Random offset



- To avoid systematic offset, design must follow the rule

$$\frac{(W/L)_{M3}}{(W/L)_{M5}} = \frac{(W/L)_{M4}}{(W/L)_{M5}} = \frac{1}{2}\frac{(W/L)_{M6}}{(W/L)_{M7}}$$

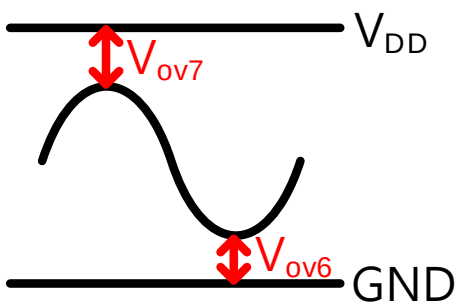
- To minimize random offset
  - $L_1=L_2$, $W_1=W_2$, $L_3=L_4$, $W_3=W_4$, $L_3=L_6$ and $L_5=L_7$ to minimize the offsets of channel length and channel width mismatch
  - Large L and W such that $\Delta L/L$ and $\Delta W/W$ can be ignored

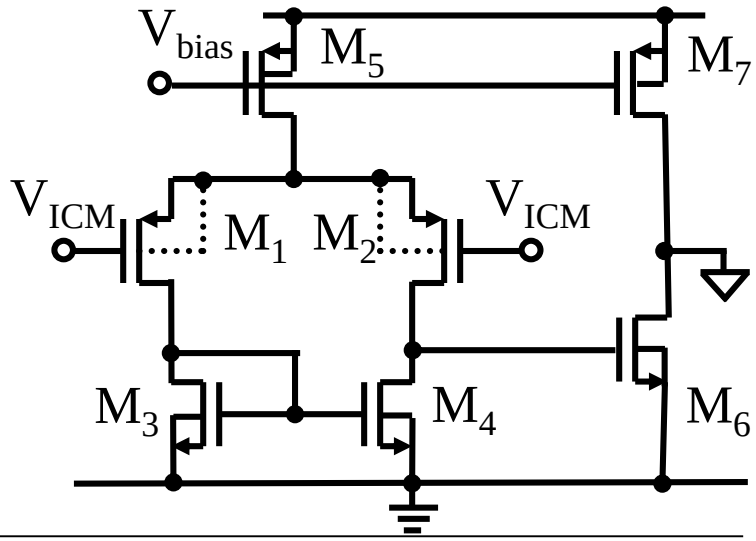
Input Common-Mode Range and Output Swing of Two-Stage CMOS OPAMP

- Input common-mode range, V_{ICM}
  - Minimum V_{ICM}
    - Keep M_1 and M_2 in saturation → $V_{dg1,2} < |V_{tp}|$
    - Hence, $V_{ICM} \geq V_{tn} + V_{OV3} - |V_{tp}|$, where V_{ov} is overdrive voltage
  - Maximum V_{ICM}
    - Keep M_5 in saturation, $V_{ds5} > V_{ov5}$
    - Hence, $V_{ICM} \leq V_{DD} - |V_{OV5}| - |V_{tp}| - |V_{OV1}|$

  → $V_{OV3} + V_{tn} - |V_{tp}| \leq V_{ICM} \leq V_{DD} - |V_{tp}| - |V_{OV1}| - |V_{OV5}|$
- Output swing, V_O
  - Keep M_6 and M_7 in saturation

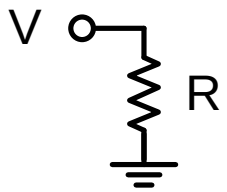
  $V_{OV6} \leq V_o \leq V_{DD} - |V_{OV7}|$





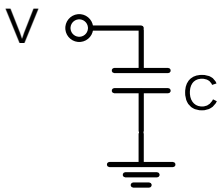
Miller Effect

- Resistor



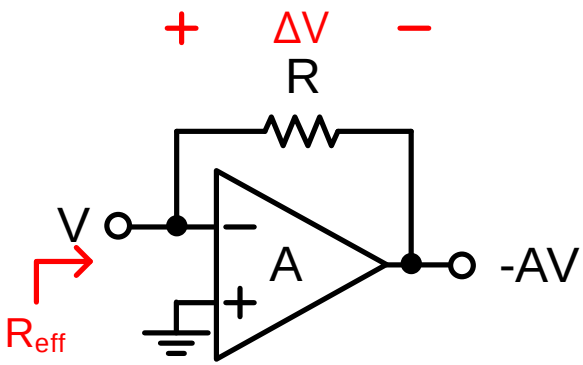
$$I = \frac{V}{R}$$

- Capacitor



$$Q = CV$$

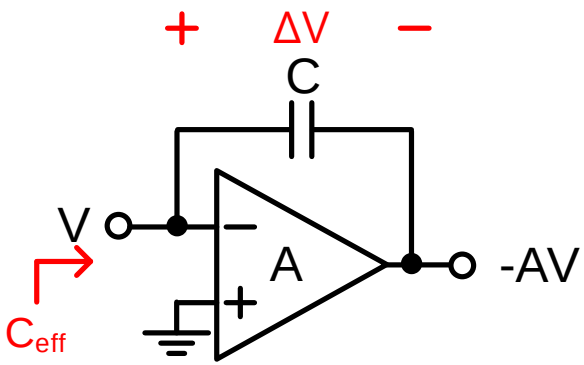
- Miller effect on resistor



$$I = \frac{\Delta V}{R} = \frac{(1+A)V}{R}$$

$$R_{eff} = \frac{R}{1+A}$$

- Miller effect on capacitor



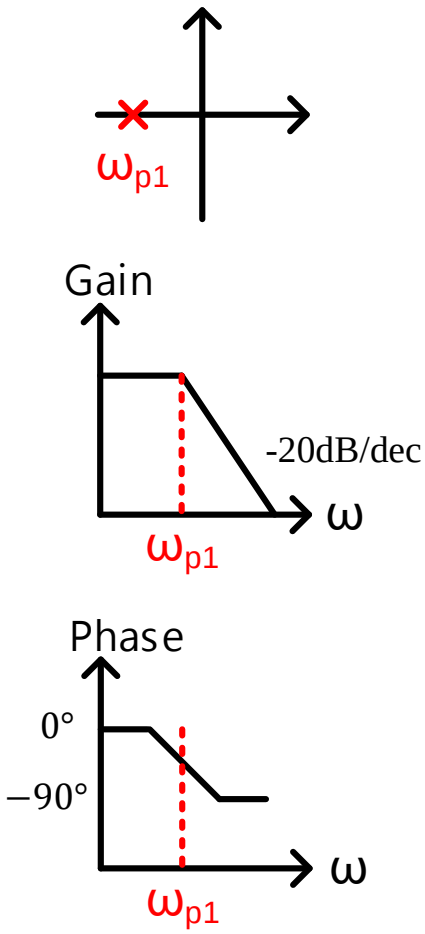
$$Q = C \cdot \Delta V = C(1+A)V$$

$$C_{eff} = (1+A)C$$

Pole and Zero

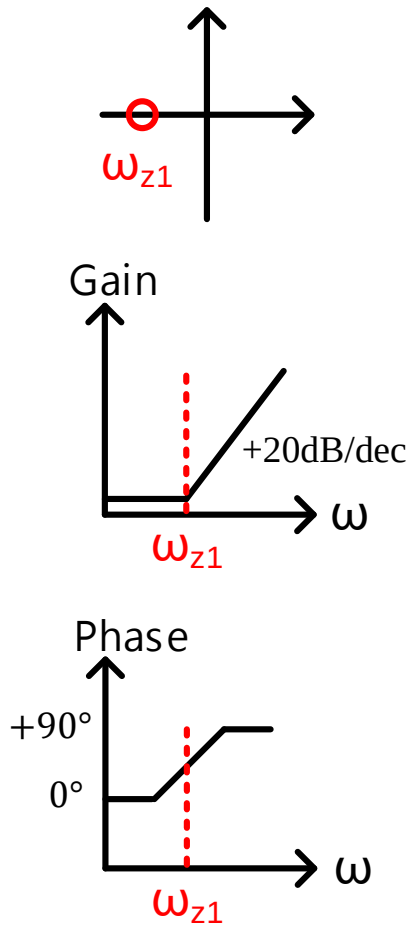
- LHP pole

$$H(s) = \frac{1}{1 + s/\omega_{p1}}$$



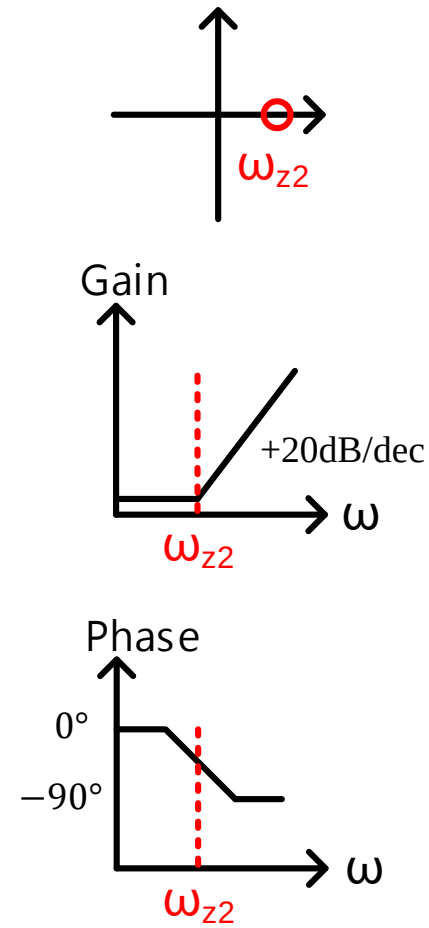
- LHP zero

$$H(s) = 1 + s/\omega_{z1}$$



- RHP zero

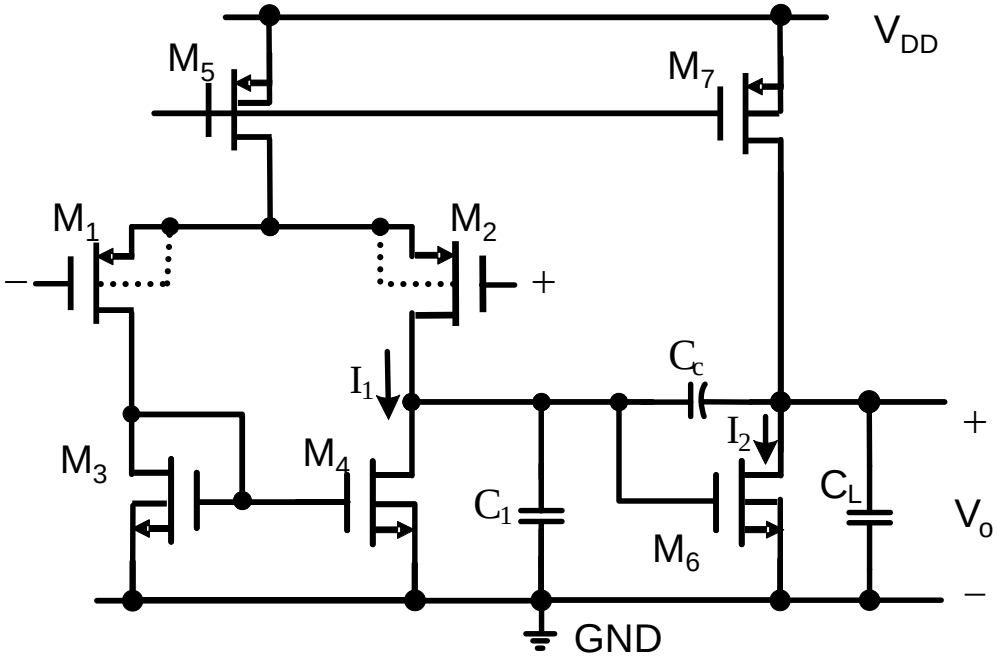
$$H(s) = 1 - s/\omega_{z2}$$



LHP: Left-hand plane, RHP: Right-hand plane

Pole-Splitting of Two-Stage CMOS OPAMP

- Reduce ω_{P1} and increase ω_{P2}



$$A(s) = \frac{A_0(1 - s/\omega_Z)}{(1 + s/\omega_{P1})(1 + s/\omega_{P2})}$$

$$A_0 = g_{m1} R_{01} g_{m6} R_{02}$$

$$g_{m1} = \sqrt{2\mu_p C_{OX} (W/L)_{M_1} I_1}$$

$$g_{m6} = \sqrt{2\mu_n C_{OX} (W/L)_{M_6} I_6}$$

$$R_{01} = r_{ds2} \,//\, r_{ds4}$$

$$R_{02} = r_{ds6} // r_{ds7}$$

$$\omega_Z \approx \frac{g_{m6}}{C_C}$$

If $g_{m6} R_{02} >> 1$

$$\omega_{P1} = \frac{-1}{(1 + g_{m6} R_{02}) C_C R_{01}} \approx \frac{-g_{m1}}{A_0 C_C}$$

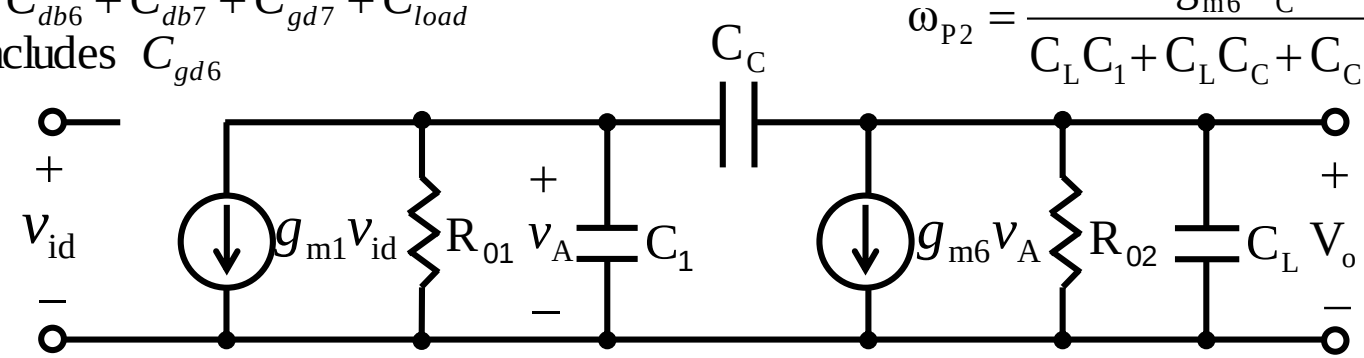
If C_C & $C_L >> C_1$

$$\omega_{P2} = \frac{-g_{m6} C_C}{C_L C_1 + C_L C_C + C_C C_1} \approx \frac{-g_{m6}}{C_L}$$

$$C_1 = C_{gd2} + C_{db2} + C_{gd4} + C_{db4} + C_{gs6}$$

$$C_L = C_{db6} + C_{db7} + C_{gd7} + C_{load}$$

C_C includes C_{gd6}



$\Rightarrow$ Right plane zero causes slower gain drop but quick phase drop

Pole-Splitting of Two-Stage CMOS OPAMP (Cont.)

- Unity-gain frequency $f_t\ (\text{or } f_u) = |A_0|\dfrac{\omega_{P1}}{2\pi} = \dfrac{1}{2\pi}\dfrac{g_{m1}}{C_C}$
- To achieve an uniform -20dB/dec gain rolloff down to 0dB, the following two conditions must be satisfied

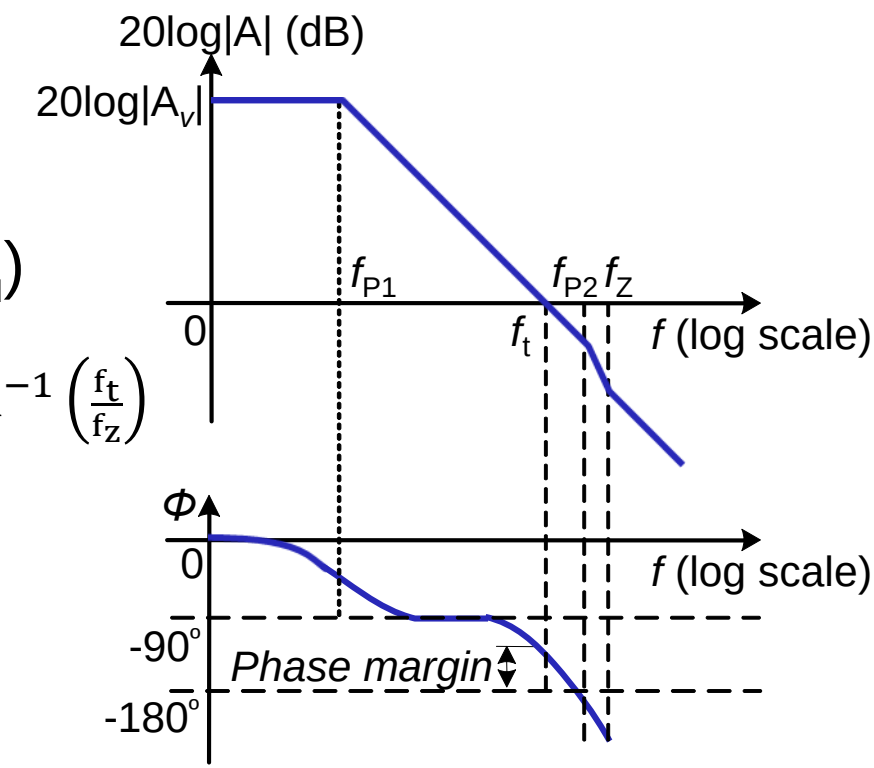
1. $f_t < f_{p2} \Rightarrow \dfrac{g_{m1}}{C_C} < \dfrac{g_{m6}}{C_L}$
2. $f_t < f_z \Rightarrow g_{m1} < g_{m6}$

- At unity-gain frequency f_t (or f_u)

$$\Phi_{total} = \tan^{-1}\left(\frac{f_t}{f_{p1}}\right) + \tan^{-1}\left(\frac{f_t}{f_{p2}}\right) + \tan^{-1}\left(\frac{f_t}{f_z}\right)$$

where $\tan^{-1}\left(\frac{f_t}{f_{p1}}\right) \cong 90°$

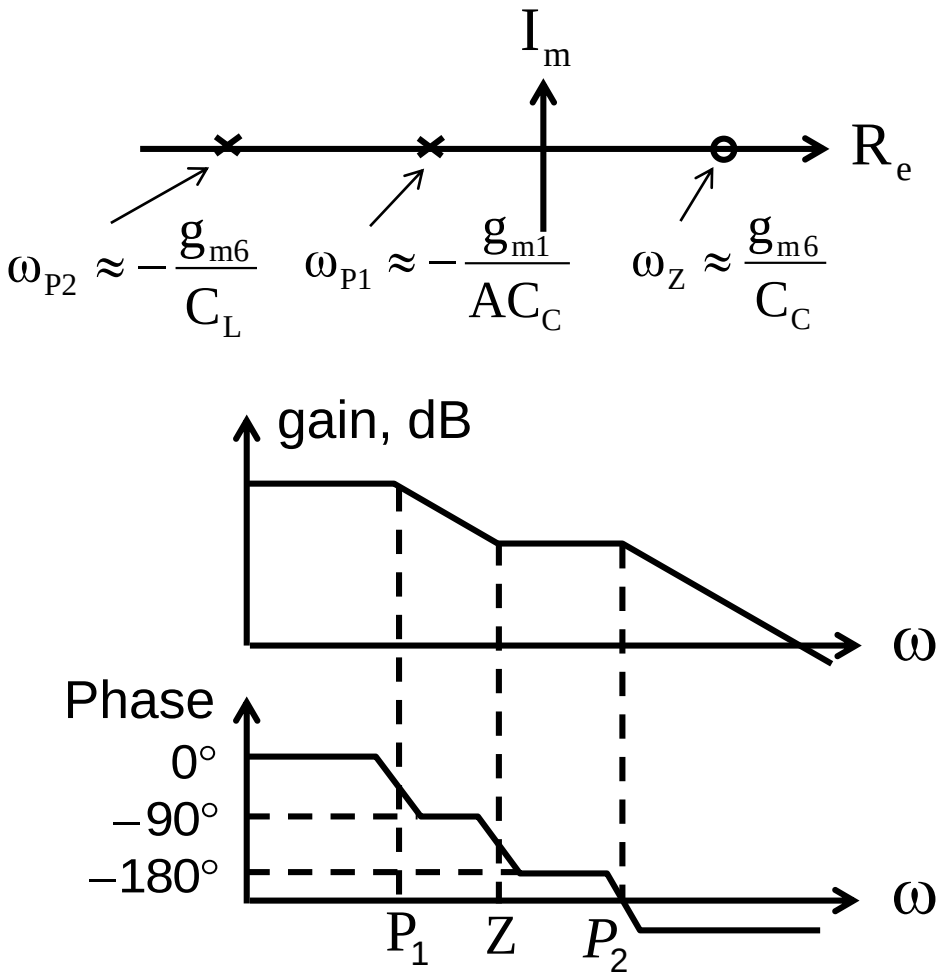
$$\text{Phase margin} = 180° - \Phi_{total}$$
$$= 90° - \tan^{-1}\left(\frac{f_t}{f_{p2}}\right) - \tan^{-1}\left(\frac{f_t}{f_z}\right)$$



Right-Plane Zero

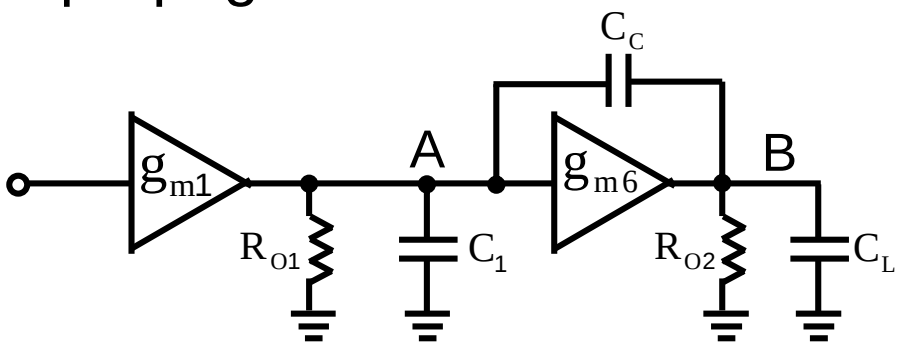
- Causes slower gain drop but quicker phase drop

  Usually moved away if phase margin is not large enough



Right-Plane Zero (Cont.)

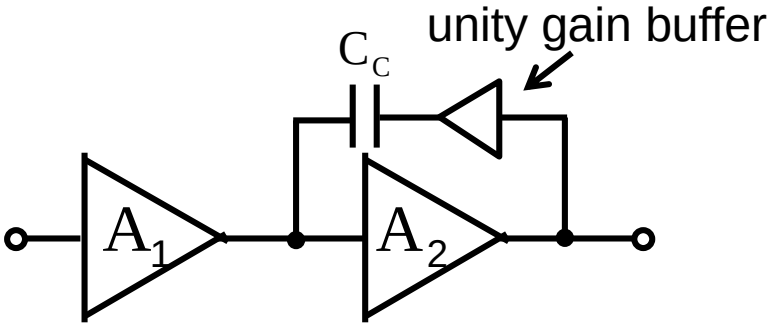
- The zero is due to the existence of two path through which the signal can propagate from node A to node B



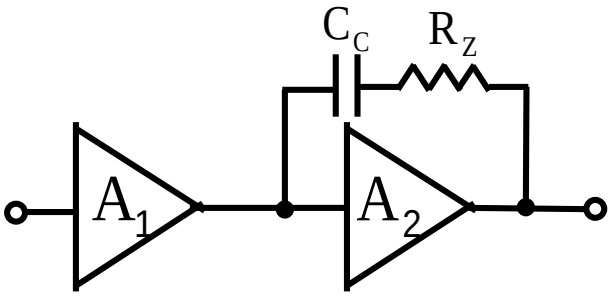
1. through C_C
2. through the controlled source $g_{m6}V_A$

- To eliminate zero ω_z

1. Method-1

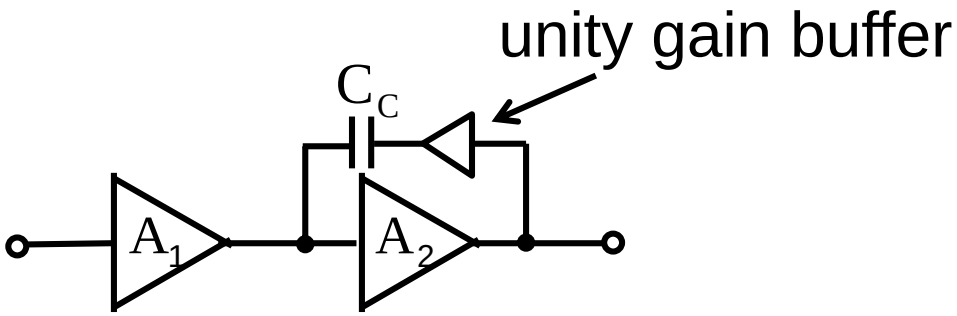


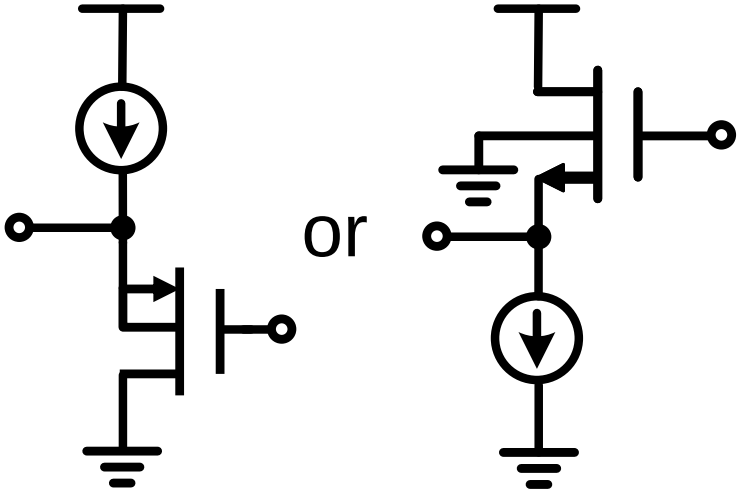
2. Method-2

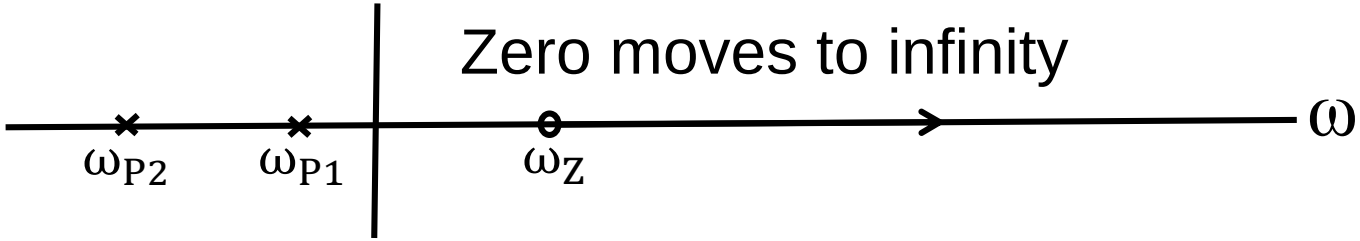


Elimination of Right-Plane Zero

- Method-1: Use unity-gain buffer → Zero moves to infinity







$$A(s) = \frac{A_0}{(1+\frac{s}{\omega_{P1}})(1+\frac{s}{\omega_{P2}})} \quad \text{where } \omega_{P1} \approx -\frac{g_{m1}}{A_0 C_C},\ \omega_{P2} \approx \frac{-g_{m6}}{C_L}$$

Elimination of Right-Plane Zero (Cont.)

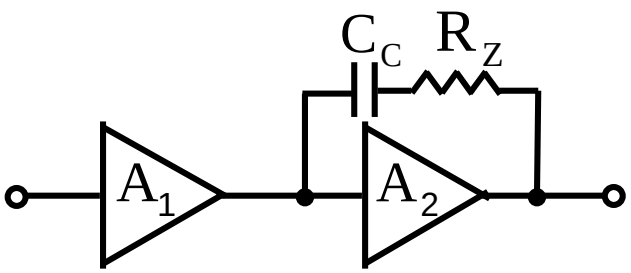
- Method-2: Using R instead of buffer
  - Elimination of zero → Let $R_Z = \frac{1}{g_{m6}}$
  - Pole-zero cancellation → Let $\omega_Z = \omega_{P2}$

$$\omega_{P1} \approx -\frac{g_{m1}}{A_0 C_C}$$

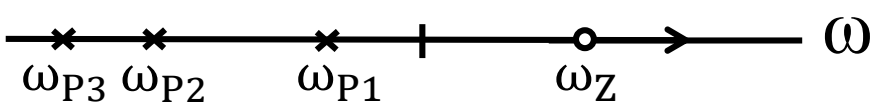
$$\omega_{P2} \approx -\frac{g_{m6}}{C_L}$$

$$\omega_{P3} \approx -\frac{1}{R_Z}\left(\frac{1}{C_C} + \frac{1}{C_1} + \frac{1}{C_L}\right)$$

$$\omega_Z = -\frac{1}{[R_Z - (\frac{1}{g_{m6}})]C_C}$$

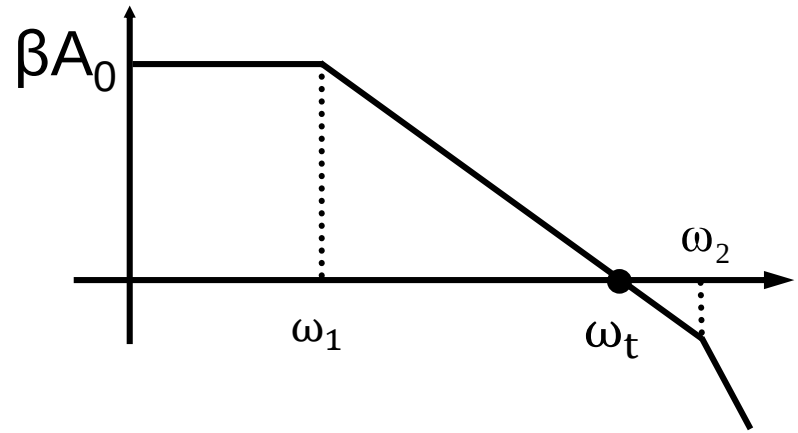


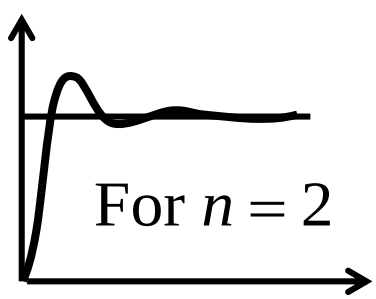
Zero moves toward the left plane as R_Z increase

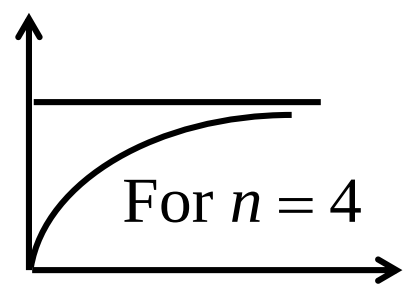


Pole Separation vs. Phase Margin and Speed

- $\omega_t = \frac{1}{n}\omega_2 = \beta A_0 \omega_1$
- Step response (**with fixed ω_2**)
  - n=2
    - Phase margin = 63°
    - Fast
  - n=3
    - Phase margin = 71°
  - n=4
    - Phase margin = 76°
    - Critically damped

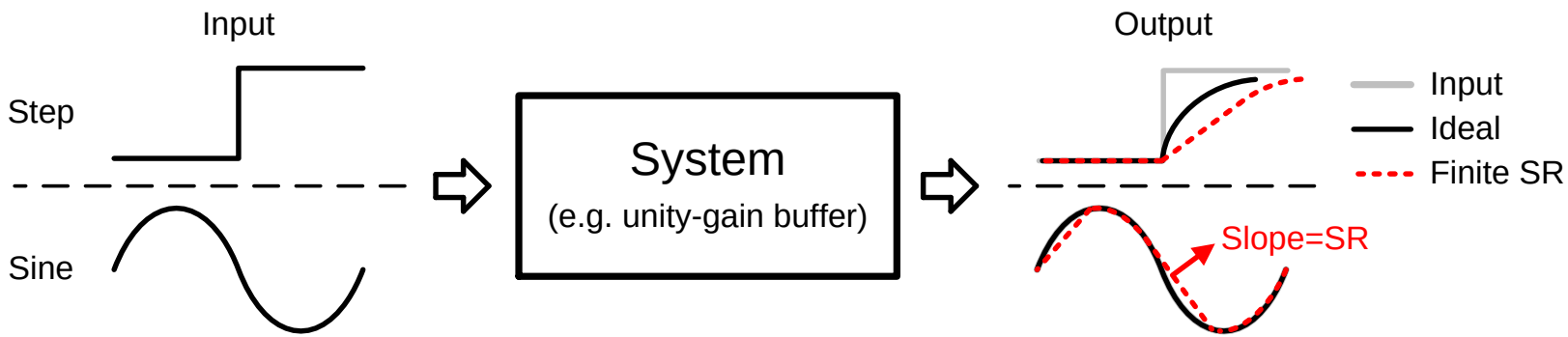






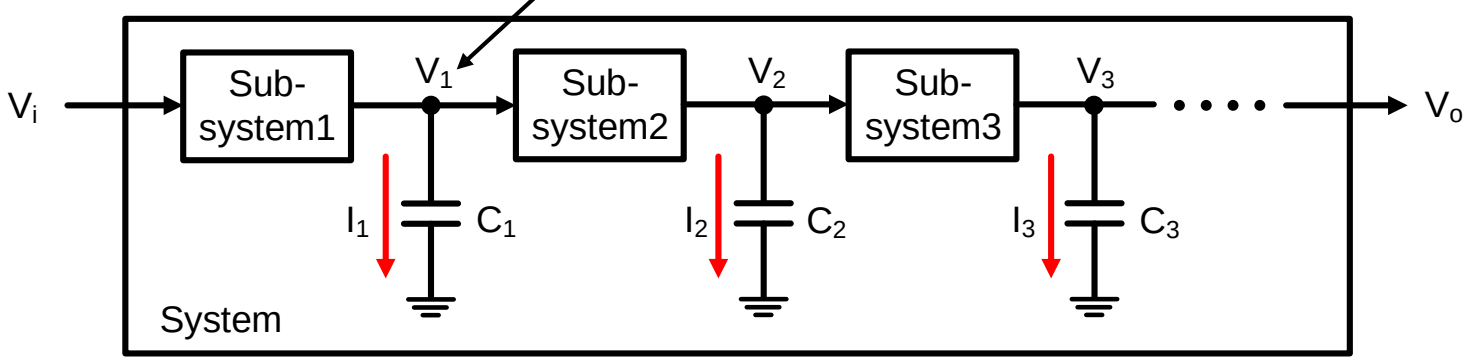
Introduction of Slew Rate (SR)

- Definition: Maximum change rate of voltage



- SR depends on system driving currents and capacitive loads
- SR should be considered at all nodes in circuit, for example:

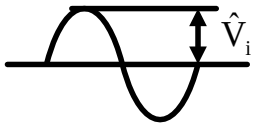
$$SR = \left.\frac{dv_o}{dt}\right|_{max} = \left.\frac{I_i}{C_i}\right|_{min} \quad i = 1,2,3.... \quad V_1 = \frac{1}{C_1}\int_0^t I_1\,dt$$



SR Effect on Sinusoidal Response

- Voltage change rate without SR limitation

$$v_i = v_o = \hat{V}_i \sin\omega t \Rightarrow \frac{dv_o}{dt} = \omega\hat{V}_i \cos\omega t \Rightarrow \left.\frac{dv_o}{dt}\right|_{max} = \omega\hat{V}_i \cos 0 = \omega\hat{V}_i$$

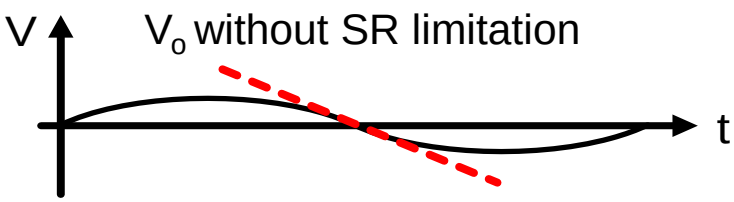


- Full-power bandwidth (f_M)

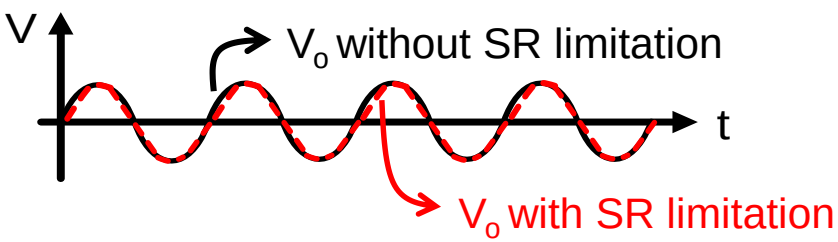
$$SR = \omega_M V_{o\_max} \Rightarrow f_M = \frac{SR}{2\pi V_{o\_max}}$$

V_{o_max}: rated opamp output voltage
ω_M : maximum input frequency without distortion

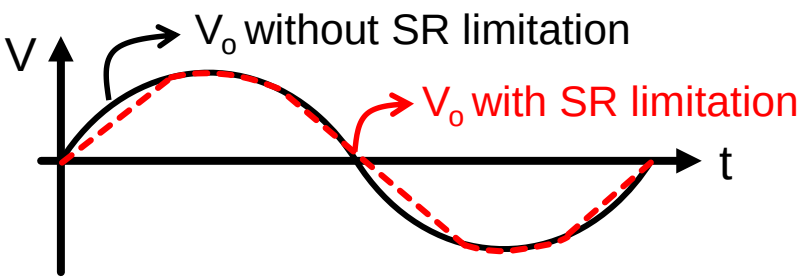
- SR effect on sine waves
  - Small amplitude, low freq.



  - Small amplitude, high freq.



  - Large amplitude, low freq.



SR limitation depends on amplitude and frequency

SR Effect on Step Response of a One-Pole System

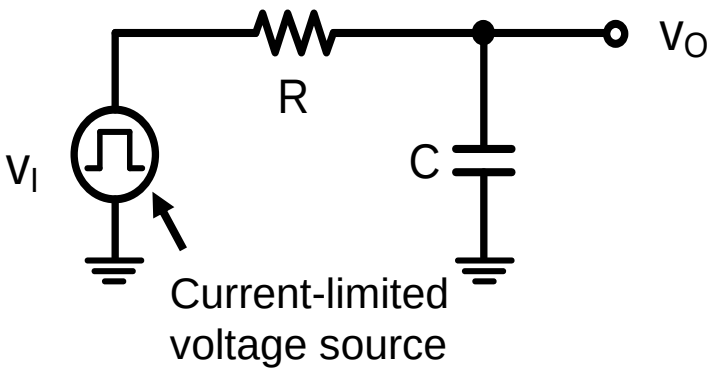
- Step response of a one-pole system
  - Ideal response: Exponential output $v_{O,Ideal}(t)$

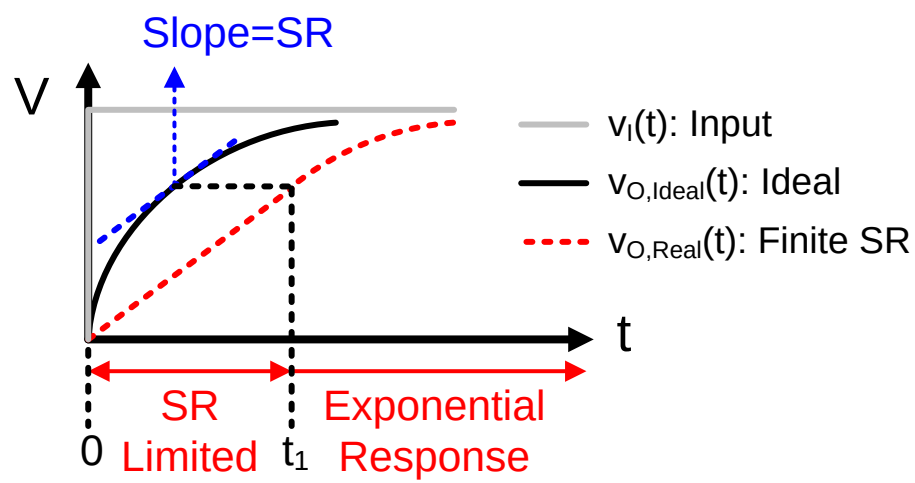
$$v_{O,Ideal}(t) = V_i\left(1 - e^{-t/\tau}\right) \Rightarrow \frac{d}{dt}\left(v_{O,Ideal}(t)\right) = \frac{V_i}{\tau} e^{-t/\tau}$$

  - Without large enough system SR → Slewing happens

$$\text{When SR} < \frac{d}{dt}\left(v_{O,Ideal}(t)\right) \Rightarrow \frac{d}{dt}\left(v_{O,Real}(t)\right) = \text{SR (As } 0\sim t_1 \text{ in the waveform below)}$$

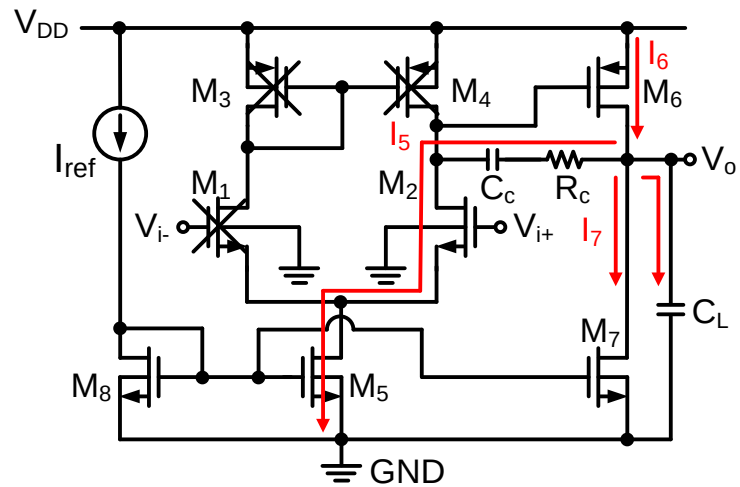
- Example: RC filter with current-limited voltage source

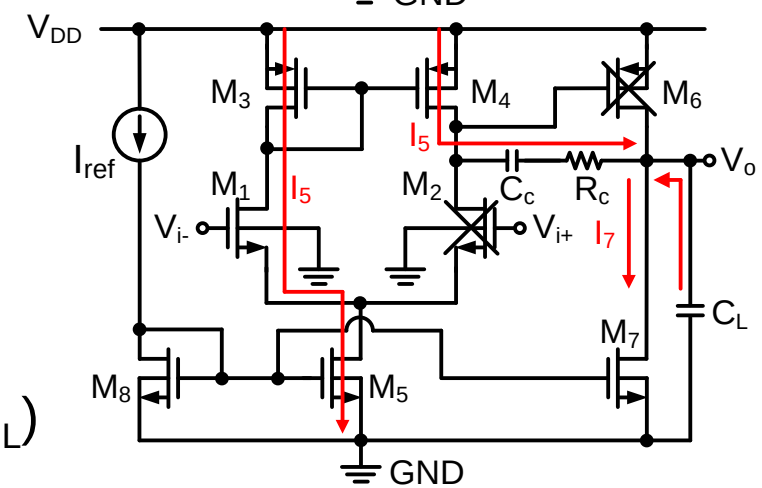




SR Analysis of Two-Stage OPAMP

- V_o rising process
  - Large positive input at V_{i+}
  - M_1 turned off
  - I_5 flows through C_c
  - Driving capability of I_6 is usually large → SR not limited by I_6
  - $SR = I_5 / C_c$
- V_o falling process
  - Large positive input at V_{i-}
  - M_2 turned off
  - I_5 flow through C_c
    - I_7 large enough: $SR = I_5 / C_c$
    - I_7 not large enough: $SR = I_7 / (C_c + C_L)$





- SR when I_7 is large enough

$$g_{m1} = \sqrt{2\mu_n C_{ox} \frac{W_{M1}}{L_{M1}} \frac{I_5}{2}}, \quad \omega_t = \frac{g_{m1}}{C_C} \Rightarrow SR = \left.\frac{dv_o(t)}{dt}\right|_{max} = \frac{I_5}{C_C} = \omega_t \sqrt{\frac{I_5 L_{M1}}{\mu_n C_{ox} W_{M1}}} = (V_{GS1} - V_t)\,\omega_t$$

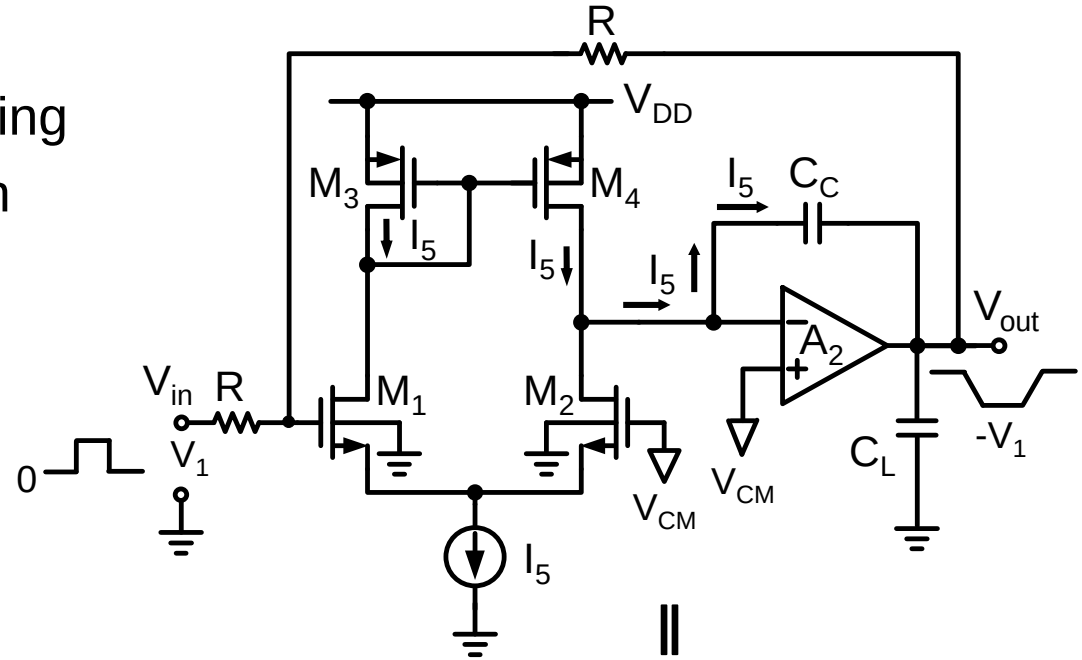
Example - Negative Feedback Amplifier

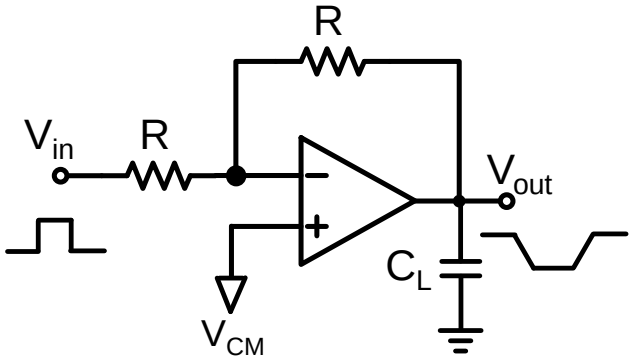
- Slew rate
  - Assume the output driving current is large enough

$$SR = \left|\frac{dV_{out}}{dt}\right| = \left|-\frac{1}{C_C}\frac{dQ_c}{dt}\right| = \frac{I_5}{C_C}$$

$$\text{For}\begin{cases} \omega_t = \dfrac{g_{m1}}{C_C} \Rightarrow C_C = \dfrac{g_{m1}}{\omega_t} \\ g_{m1} = \sqrt{2\mu_n C_{OX}\left(\dfrac{W}{L}\right)_{M1}\dfrac{I_5}{2}} \end{cases}$$

$$\Rightarrow SR = \frac{I_5\omega_t}{g_{m1}} = \omega_t\sqrt{\frac{I_5}{\mu_n C_{OX}\left(\dfrac{W}{L}\right)_{M1}}}$$





- Slew rate can be increased by
  - Increasing the unity-gain bandwidth
  - Increasing bias current of input stage
  - Decreasing the W/L ratio of the input transistors

Power-Supply Rejection Ratio (PSRR)

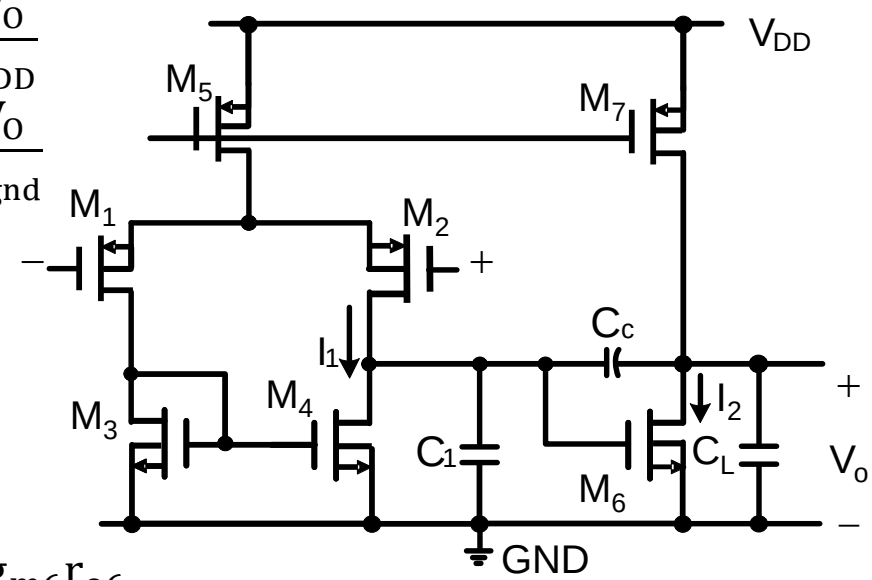
- Mixed-signal circuits combine analog and digital circuits

  $\Rightarrow$ Switching activity in digital portion results in supply ripple
  - ◆ Add large capacitors between supply rails and ground

    $\Rightarrow$ not practical in IC design
  - ◆ High-PSRR analog circuits
- Definition $\begin{cases} \mathrm{PSRR}^{+} \equiv \dfrac{A_d}{A^{+}} \\ \mathrm{PSRR}^{-} \equiv \dfrac{A_d}{A^{-}} \end{cases}$, where $\begin{cases} A^{+} \equiv \dfrac{V_O}{V_{DD}} \\ A^{-} \equiv \dfrac{V_O}{V_{gnd}} \end{cases}$
  - ◆ For a two-stage op amp
    - ➢ $V_o = V_{gnd} \times \dfrac{r_{o7}}{r_{o6} + r_{o7}}$

      $\Rightarrow A^{-} \equiv \dfrac{V_O}{V_{gnd}} = \dfrac{r_{o7}}{r_{o6} + r_{o7}}$

      $\Rightarrow \mathrm{PSRR}^{-} \equiv \dfrac{A_d}{A^{-}} = g_{m1}(r_{o2} \parallel r_{o4}) g_{m6} r_{o6}$
    - ➢ It's insensitive to $V_{DD} \Rightarrow \mathrm{PSRR}^{+}$ is high [Ref.]



[Ref.] P. R. Gray, P. J. Hurst, A. H. Lewis, and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 5th ed., New York: John Wiley & Sons, 2009. pp. 430–432

Design Trade-offs

- To increase the differential gain, CMRR, and PSRR for a two-stage op amp
  - Enlarge the length L for the channel of each MOSFET
  - Lower the $|V_{OV}|$ at which each MOSFET is operated

$$A_O = g_m r_{ds} \propto \sqrt{I} \cdot \frac{1}{\lambda I} = \frac{1}{\lambda\sqrt{I}} \propto \frac{L}{\sqrt{I}}, \text{where } \lambda \propto \frac{1}{L} \text{(roughly)}$$

$$\omega_t = \frac{g_m}{C} \propto \frac{\sqrt{I}}{C} \propto \sqrt{I}$$

- The transition frequency of the MOSFETs can be increased by using a shorter channel and/or a larger $|V_{OV}|$

$$f_t = \frac{g_m}{2\pi(C_{gs} + C_{gd})} = \frac{2 \cdot \frac{1}{2}\mu C_{OX}\frac{W}{L}V_{OV}^2/V_{OV}}{2\pi(\frac{2}{3}WLC_{OX})} \approx \frac{1.5 \cdot \mu \cdot |V_{OV}|}{2\pi L^2}; \text{where } \begin{cases} \mu\text{: carrier mobility} \\ V_{OV}\text{: overdrive voltage} \\ L\text{: channel length} \end{cases}$$

$$g_m = \frac{2I}{V_{OV}}, C_{gs} \approx \frac{2}{3}WLC_{OX} \text{ and } C_{gs} \gg C_{gd}$$

- In conclusion, it's a trade-off between low-frequency performance parameters and high-frequency ones

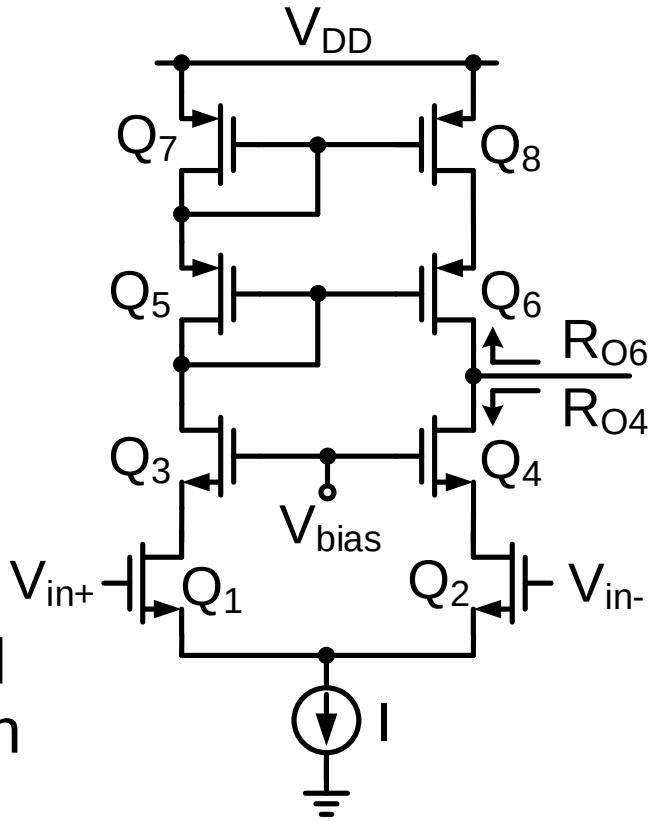
  → For analog circuits in submicron process operated at 1V~1.5V supplies, 0.1V~0.3V of $|V_{OV}|$ is typically used, and the typical channel lengths are usually at least 1.5~2 times the L_{min}

Cascade and Cascode CMOS OPAMPs

- Cascade two-stage CMOS OPAMP
  - Most popular and works well with low capacitive load
  - Problems
    - Limited slew rate due to large C_c
    - Limited bandwidth with large C_L

- If 1. low output resistance is not required,
  2. high open-loop gain is required, and
  3. large phase margin can be maintained with large C_L,
  then cascode configuration can provide attractive solutions for the above problems.
- Cascode CMOS OPAMP
  - Gain of two-stage OPAMP can be increased by adding gain stage in cascade.
    $\Rightarrow$ phase shift is increased (i.e. PM$\downarrow$)
  - Cascode configurations can be used to increase gain in the existing stage.

Cascode CMOS OPAMP



- Output resistance(Ro) is increased

$$R_{O4} \approx (g_{m4} r_{ds4}) r_{ds2}$$
$$R_{O6} \approx (g_{m6} r_{ds6}) r_{ds8}$$
$$R_O = R_{O4} \parallel R_{O6}$$

- Voltage gain $A = -g_{m1} R_O$

  $\Rightarrow$ Gain is increased.

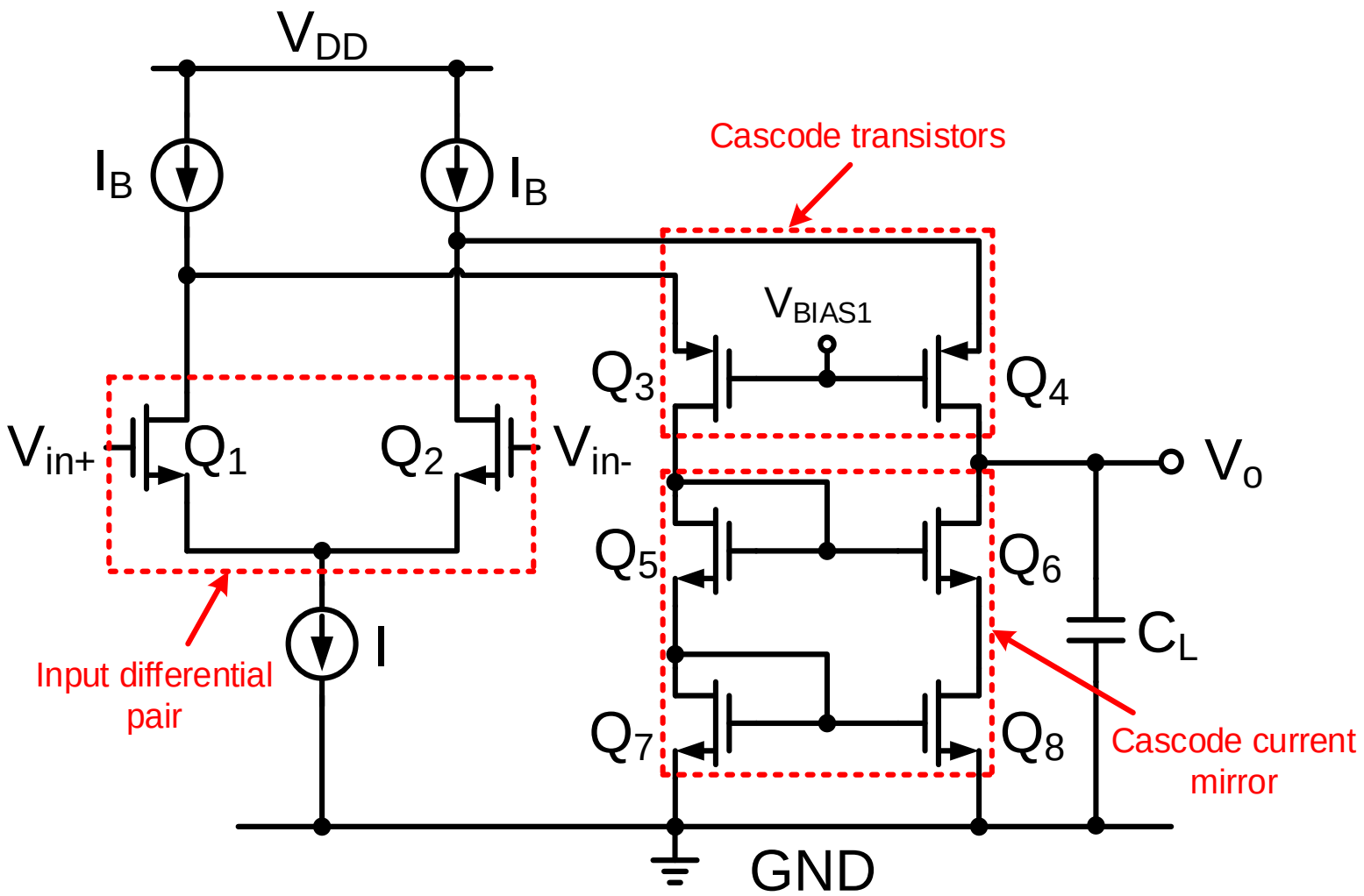
- Common-mode range is lowered and more transistors are stacked between the two power supplies.

  $\Rightarrow$ Folded-cascode has larger common-mode range

- Cascode and folded-cascode OPAMPs are also named as "transconductance OPAMP" or "operational transconductance amplifier (OTA)"

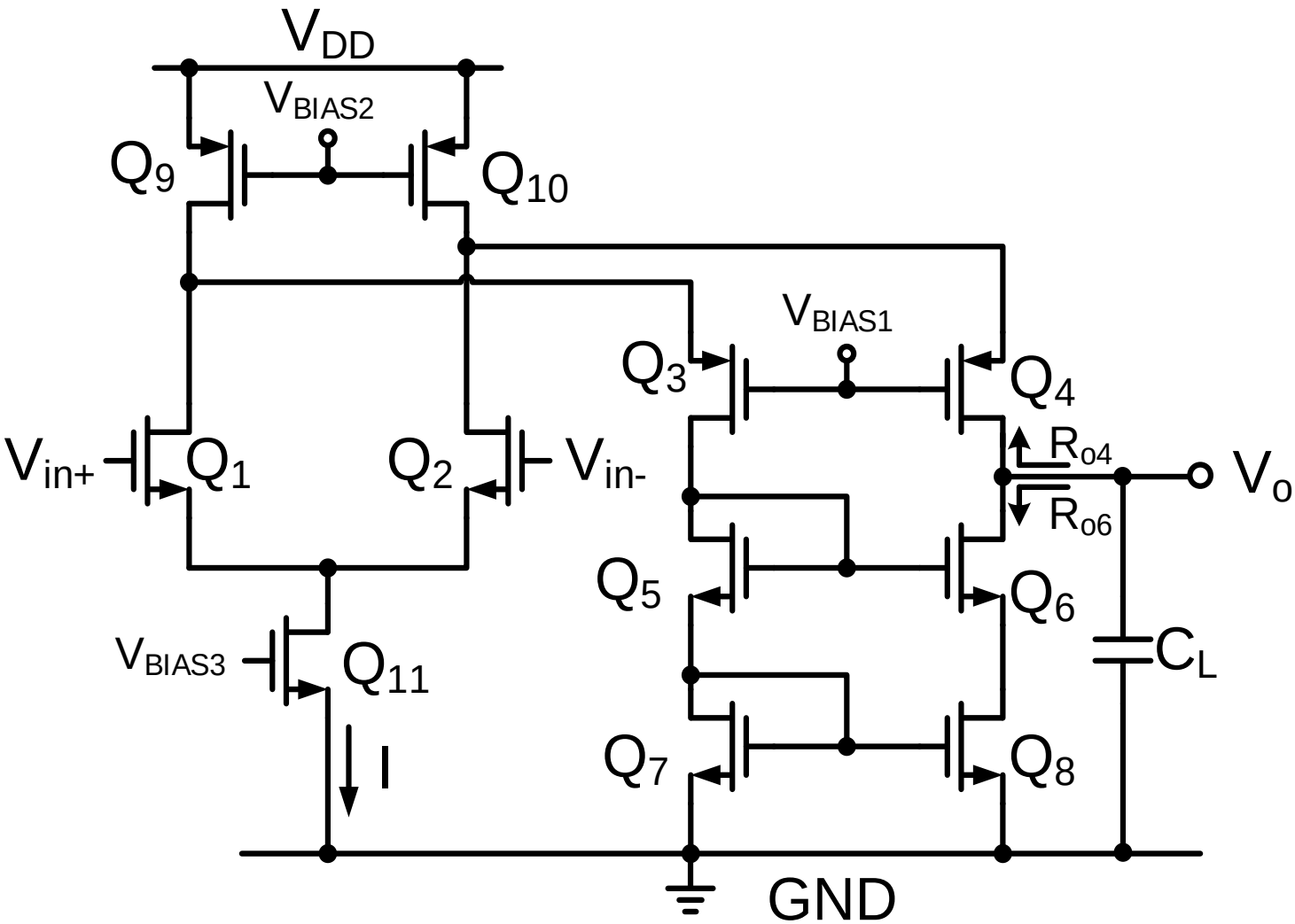
Folded-Cascode CMOS OPAMP

- Q_3 ~ Q_8 are folded and connected to GND



Folded-Cascode CMOS OPAMP (Cont.)

- Q_3, Q_4, Q_9 ~ Q_{11} form externally-biased current sources
  Q_5 ~ Q_8 form self-biased current sources



Folded-Cascode CMOS OPAMP

- Input common-mode range

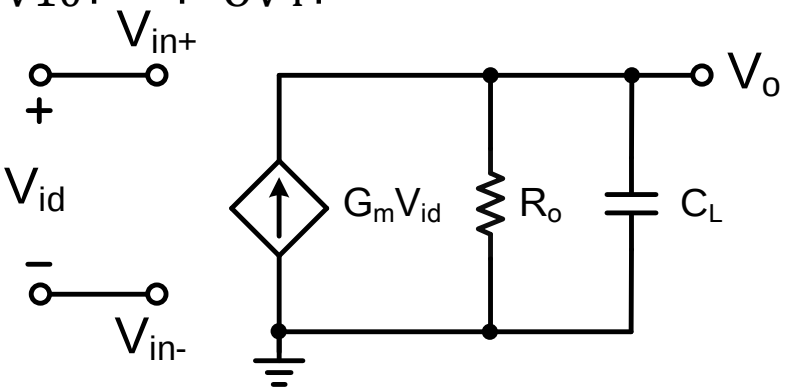
  Common-mode range is increased (compared with cascode OPAMPs). However, it is small compared with 2-stage OPAMPs

$$V_{OV11} + V_{OV1} + V_{tn} \le V_{ICM} \le V_{DD} - |V_{OV9}| + V_{tn}$$

- Output voltage swing

$$V_{OV7} + V_{OV5} + V_{tn} \le V_o \le V_{DD} - |V_{OV10}| - |V_{OV4}|$$

- Voltage gain



$$A = G_m R_O = g_{m1} R_O$$

$$R_O = R_{O4} \parallel R_{O6}$$

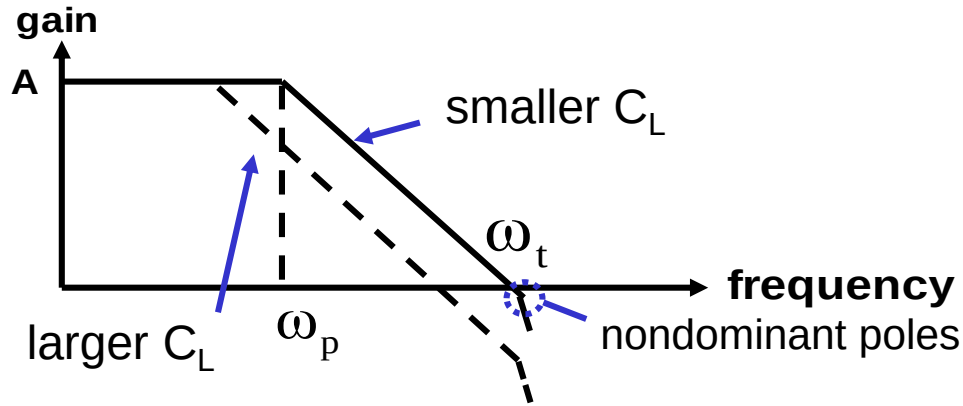
$$= [g_{m4} r_{ds4} (r_{ds2} \parallel r_{ds10})] \parallel [g_{m6} r_{ds6} r_{ds8}]$$

Folded-Cascode CMOS OPAMP

- Frequency response
  - Bode plot

$$\omega_p \approx \frac{1}{R_0 C_L}$$

$$\omega_t \approx \frac{g_{m1}}{C_L}$$

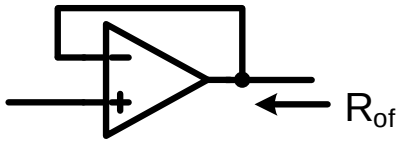


  - The only high-impedance point is the output node.
    $\Rightarrow$ Dominant pole is generated at the output node
  - The resistance of all other nodes at level of 1/gm
    $\Rightarrow$ Nondominant poles occur at all other nodes.
    The 2nd pole is usually at the source of M_3 and M_4.
  - Nondominant poles are usually at frequencies beyond ω_t
    $\Rightarrow$ If C_L is increased, then phase margin is increased.
    $\Rightarrow$ If C_L is not large enough, it can be augmented.
  - No frequency compensation is required
    $\Rightarrow$ wide bandwidth
- If $I_B \geq I$, slew rate $SR = I/C_L = \omega_t V_{OV1}$ ($\because g_{m1} = \frac{I}{V_{OV1}}, f_t = \frac{g_{m1}}{2\pi C_L}$)

Folded-Cascode CMOS OPAMP(Cont.)

- Folded-cascode OPAMPs have high open-loop output resistance It has been given the name **operational transconductance amplifier (OTA)**
- Its high output resistance (in the order of $g_m r_o^2$) is far from that for an ideal OPAMP (which has zero output resistance)
- To alleviate this concern somewhat, let us find the closed-loop output resistance R_{of} of a unity-gain follower ($\beta = 1$) formed by connecting the output terminal back to the negative input terminal

$$R_{of} = \frac{R_o}{1+A\beta} = \frac{R_o}{1+A} \approx \frac{R_o}{A} \Rightarrow R_{of} \approx \frac{1}{G_m}$$



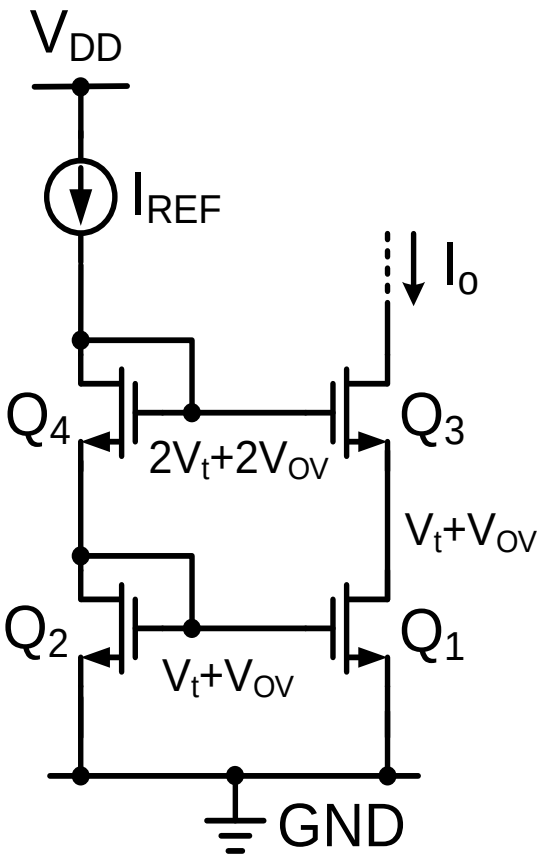
A general result applying to any OTA with 100% voltage feedback.

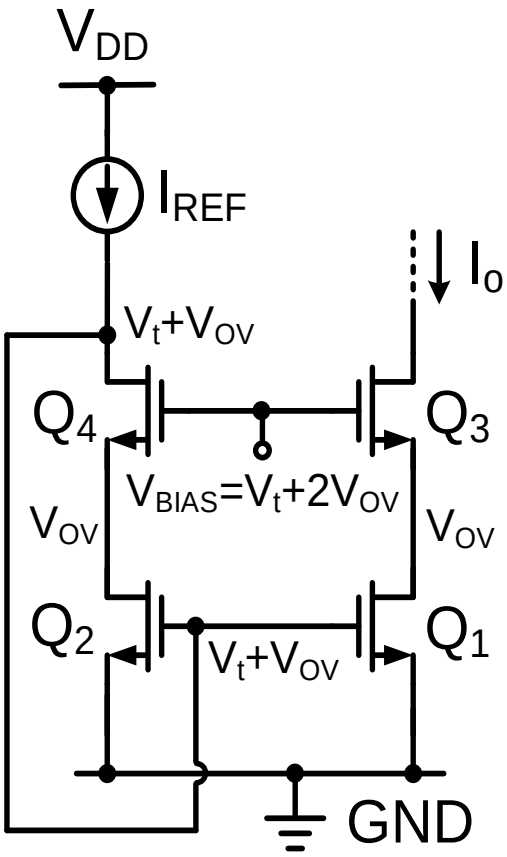
For folded-cascode OPAMPs, $G_m \approx g_{m1} \Rightarrow R_{of} \approx \frac{1}{g_{m1}}$

- g_{m1} is in the order of 1mA/V, and R_{of} will be of the order 1kΩ Although this is not very small, it's reasonable in view of the simplicity of the OPAMP circuit as well as the fact that this type of OPAMP (OTA) is not usually intended to drive low-valued resistive load.

Wide-Swing Current Mirror

- Increased output voltage range
  - $v_{Omin} \geq V_{OV1} + V_{OV3} + V_{tn}$
  - $v_{Omin} \geq V_{OV1} + V_{OV3}$

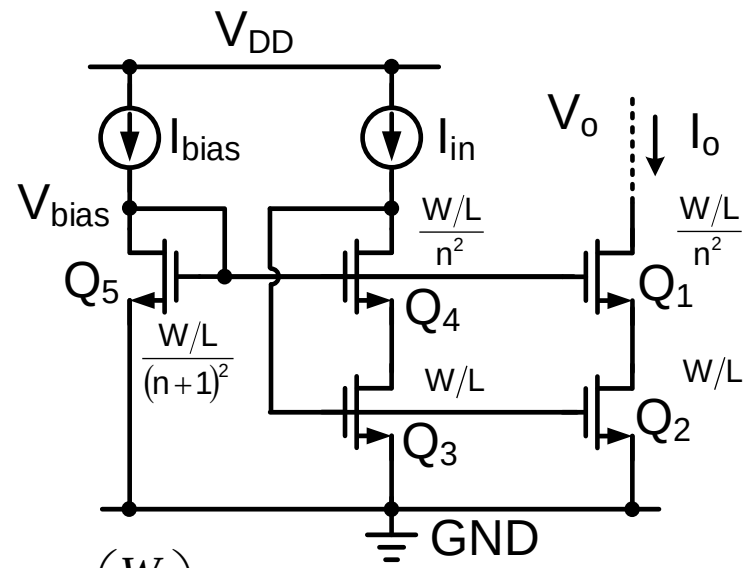




Wide-Swing Current Mirror (Cont.)

- Design example

  a varying signal $I_{in} \le I_{bias}$



$$V_{OV_2} = V_{OV_3} = \sqrt{\frac{2I_{D_2}}{\mu_n C_{ox}(W/L)}} = V_{OV}$$

$$(\because\ I_{D2} = \frac{\mu_n C_{ox}}{2}\frac{W}{L}V_{eff}{}^2)$$

Since $\left(\frac{W}{L}\right)_2 = \left(\frac{W}{L}\right)_3 = (n+1)^2\left(\frac{W}{L}\right)_5 = n^2\left(\frac{W}{L}\right)_1 = n^2\left(\frac{W}{L}\right)_4$

$V_{OV_1} = V_{OV_4} = nV_{OV}$ for the target $I_{in} = I_{bias}$

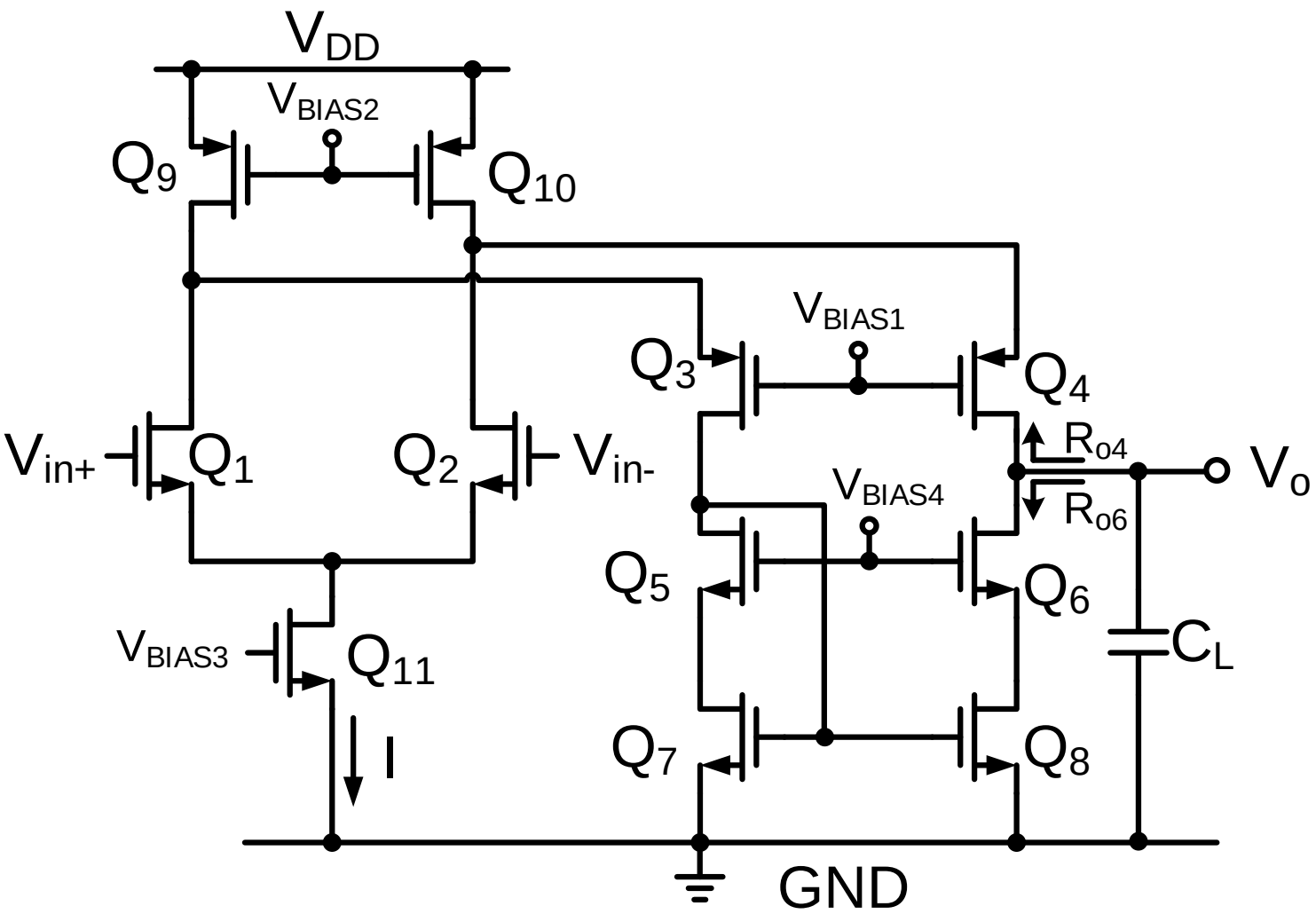
$$V_{G_5} = V_{G_4} = V_{G_1} = (n+1)V_{OV} + V_{th}$$

$$V_{DS_2} = V_{DS_3} = V_{G_5} - V_{GS_1} = V_{G_5} - (nV_{OV} + V_{th}) = V_{OV}$$

$$\Rightarrow V_o > V_{OV_1} + V_{OV_2} = (n+1)V_{OV}$$

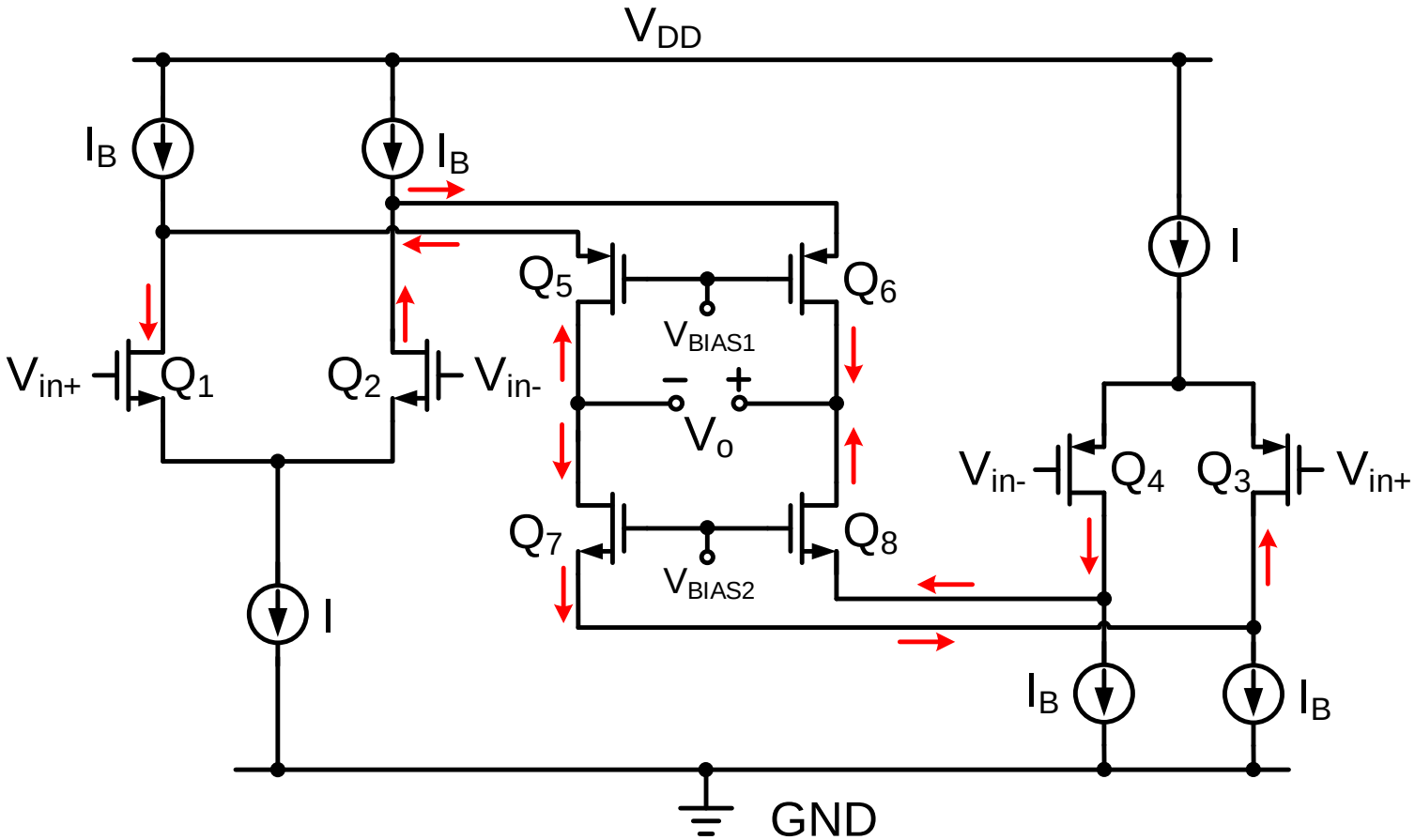
- ◆ A common choice, $n = 1,\ V_{out} > 2V_{OV}$

Folded-Cascode with Wide-Swing Current Mirror



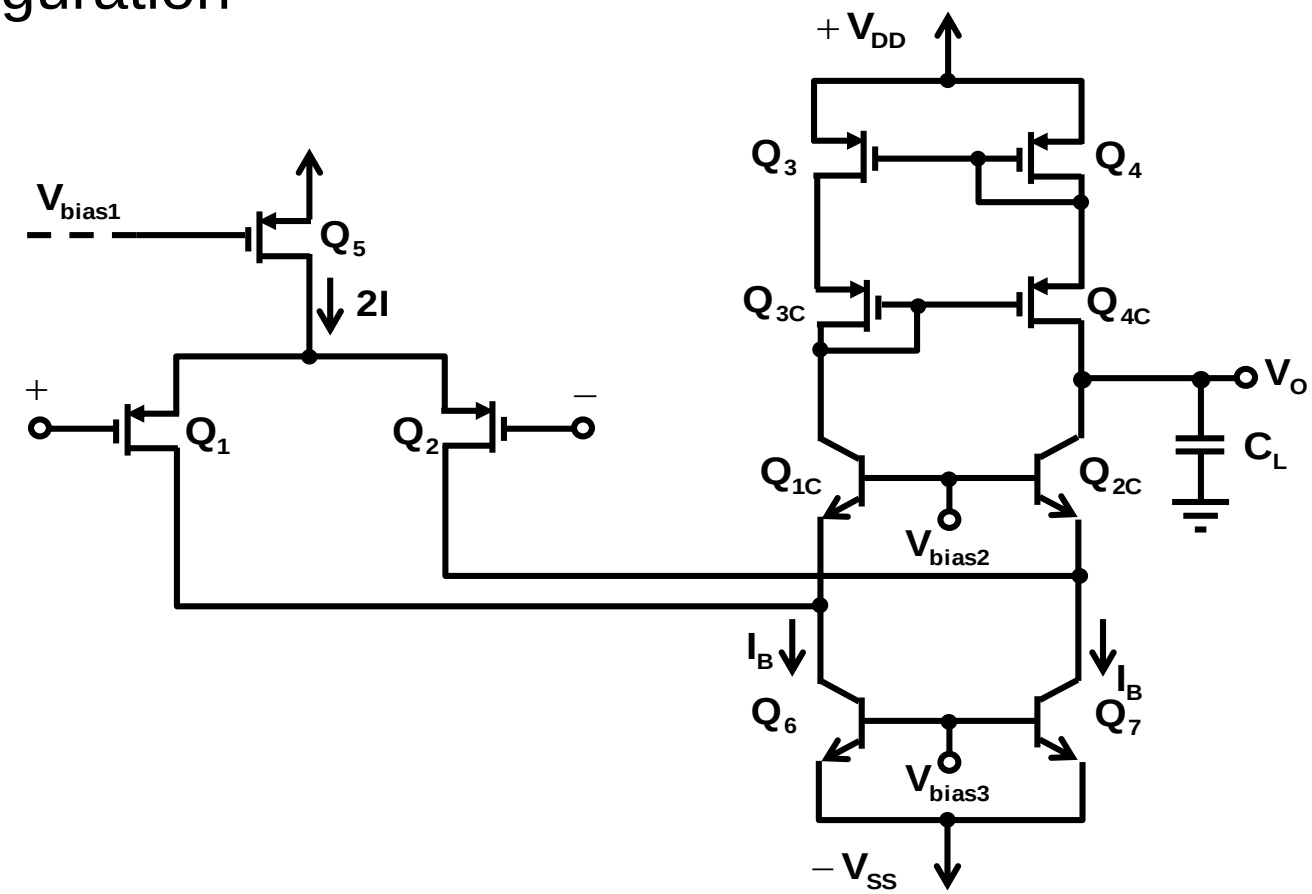
Folded-Cascode with Rail-to-Rail Input Operation

- Increased input common-mode range, rail-to-rail or even larger
- Voltage gain, if $g_{m1}=g_{m3}=G_m$
  - $A = (g_{m1}+g_{m3})R_o = 2G_mR_o$ for middle V_{ICM}
  - $A = g_{m1}R_o$ for high V_{ICM}
  - $A = g_{m3}R_o$ for low V_{ICM}



BiCMOS Folded-Cascode OPAMP

- Configuration



- When it is necessary to drive a resistive load, a low resistance output buffer is needed

BiCMOS Folded-Cascode OPAMP (Cont.)

- The largest nondominant pole is usually generated at the emitter nodes of Q_{1C} and Q_{2C}

$$\omega_{p2} \approx \frac{1}{R_{1C}C_{p1}} \approx \frac{g_{m1C}}{C_{p1}}, \text{where } R_{1C} \approx R_{elc} \parallel r_{O(Q16)} \parallel r_{O(Q1)} \approx R_{elc} = \frac{1}{g_{mlc}}$$

  - The transconductance of BJT can be much larger than that of CMOS

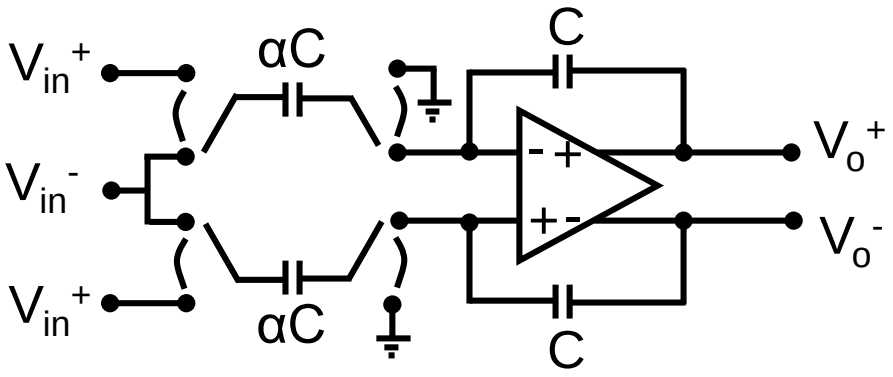
    $\Rightarrow$ ω_{p2} can be increased

    $\Rightarrow$ ω_u can be increased while enough phase margin is maintained

    $\Rightarrow$ Wider bandwidth than that of CMOS folded-cascode OPAMP

Fully Differential CMOS Switched-Capacitor Circuit

- Power supply rejection is high
- Larger chip area compared with single-ended output
- Output swing is doubled
  - Dynamic range (DR) is 6dB greater than single-ended OPAMPs
- The effect of clock feedthrough noise is minimized by the differential configuration since it will appear as a common-mode signal.

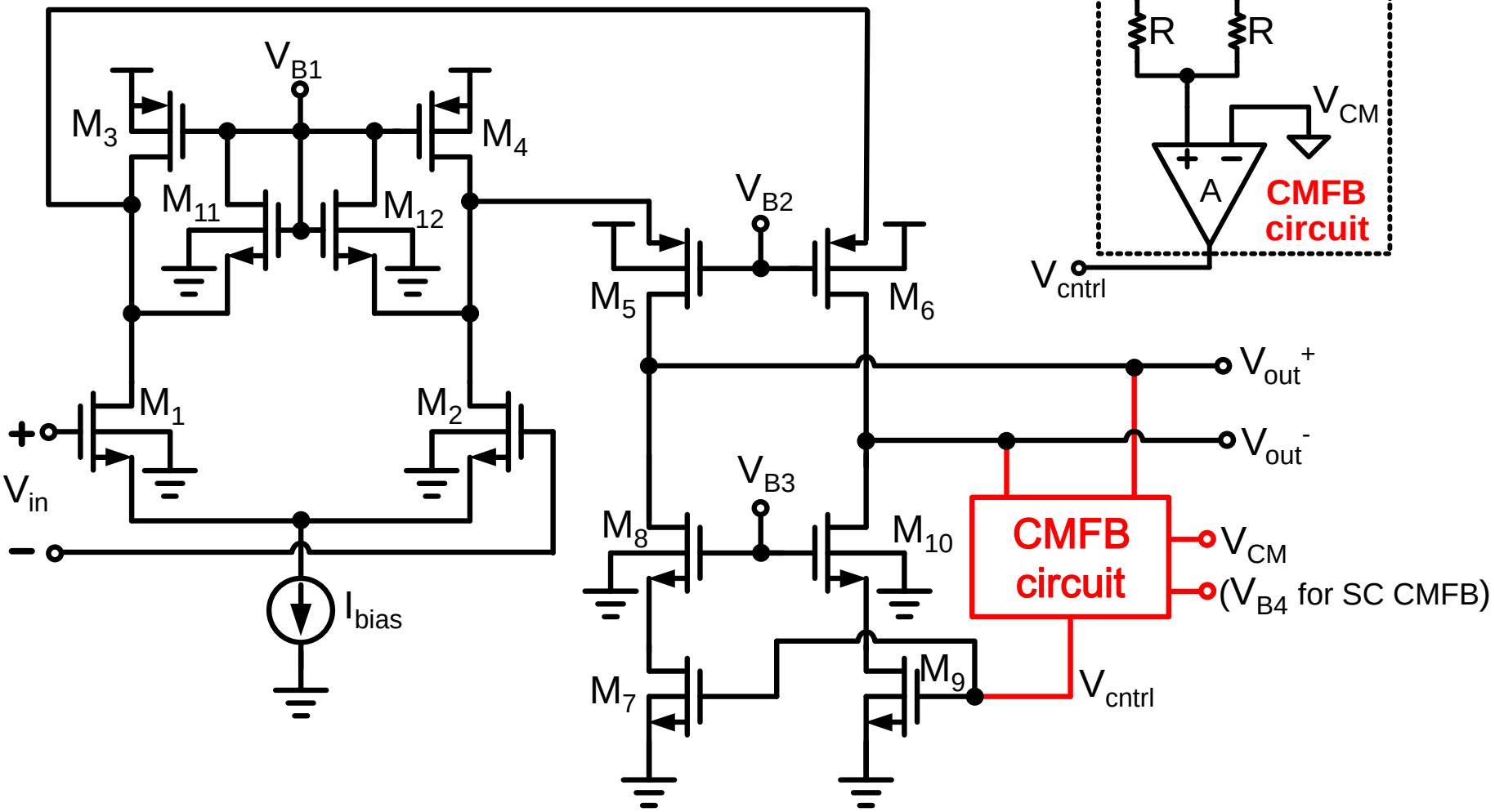


Fully Differential OPAMPs

- Fully differential signal paths
  - Differential input and differential output
  - Used in most modern high-performance analog ICs
- Help reject noise from the substrate as well as from switches turning off in switched-capacitor applications.
  - Ideally, noise affects both signal paths identically and will then be rejected since only the difference between signals is important.
  - In reality, this rejection only partially occurs since the mechanisms introducing the noise are usually nonlinear with respect to voltage levels. For example, substrate noise will usually feed in through junction capacitances, which are nonlinear with voltage.
  - Certainly, the noise rejection of a fully differential design will be much better than that for a single-ended output design. (>20dB can be expected)
- Common-mode feedback (CMFB) circuit must be added to establish the common-mode (i.e. average) output voltage.
- Reduced slew rate in one direction (compared to single-ended design)
  - Maximum current for slewing is often limited by fixed-bias currents in the output stages.

Fully Differential Folded-Cascode OPAMP

- Cascode current source
  (Rather than self-biased current mirror)



Fully Differential Folded-Cascode OPAMP (Cont.)

- CMFB circuit forces the average of the two outputs to a predetermined value
- Maximum negative slew rate is limited by I_{D7} and I_{D9}
- Dominant pole : output node

  2nd pole : node at M_1 (or M_2) drain
  - n-channel input and p-channel for M_5 and M_6
    - High transconductance
    - High gain
  - p-channel input and n-channel for M_5 and M_6
    - Maximize 2nd pole frequency
    - Unity-gain bandwidth can be maximized.

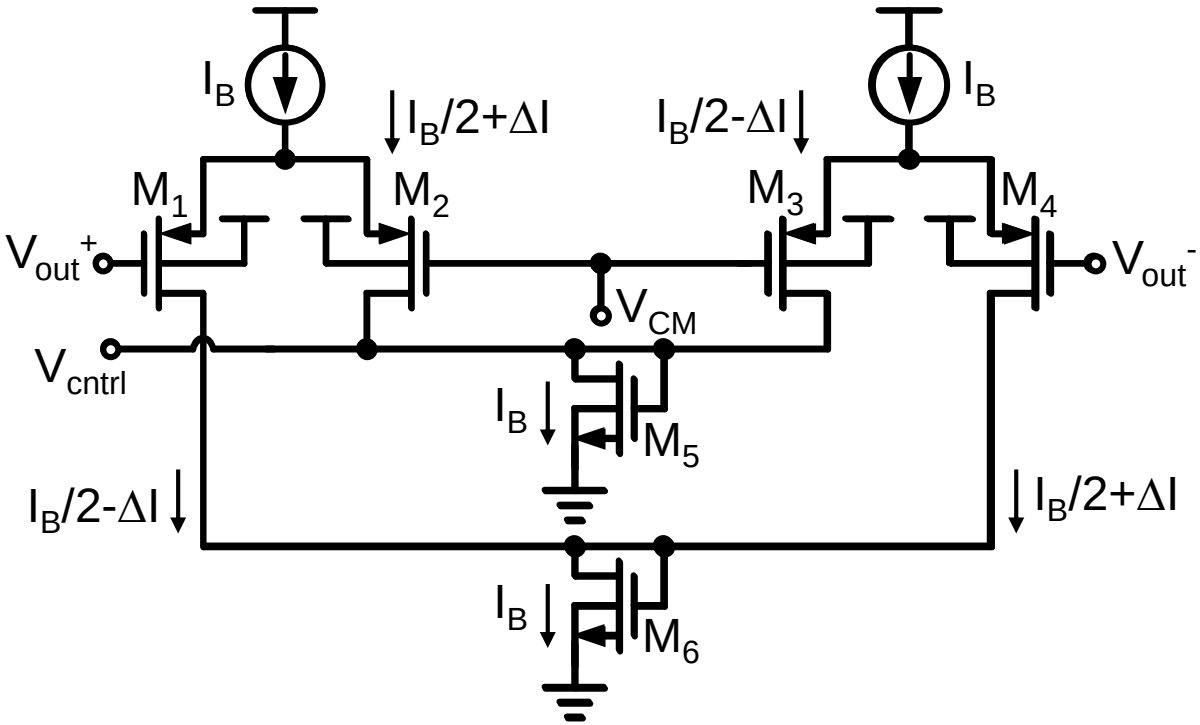
Common-Mode Feedback (CMFB) Circuits

- Force output common-mode voltage to a predetermined value
- CMFB is often the most difficult part of the OPAMP to design.
- Two typical approaches
  - Continuous-time
    - Limited signal swing
  - Switched-capacitor
    - Used in switched-capacitor circuits
    - Signal swings are not limited
    - Becomes a source of noise
    - Increases load capacitance

- By having as few nodes in the common-mode loop as is possible, compensation is simplified without having to severely limit the speed of the CMFB circuit. For this reason, the CMFB circuit is usually used to control current sources in the output stage of the OPAMP.

CMFB Circuits

- A continuous-time CMFB circuit



  - The circuit can not operate correctly if the OPAMP output voltage is so large that transistors in the differential pairs turn off.
  - When common-mode voltage is zero

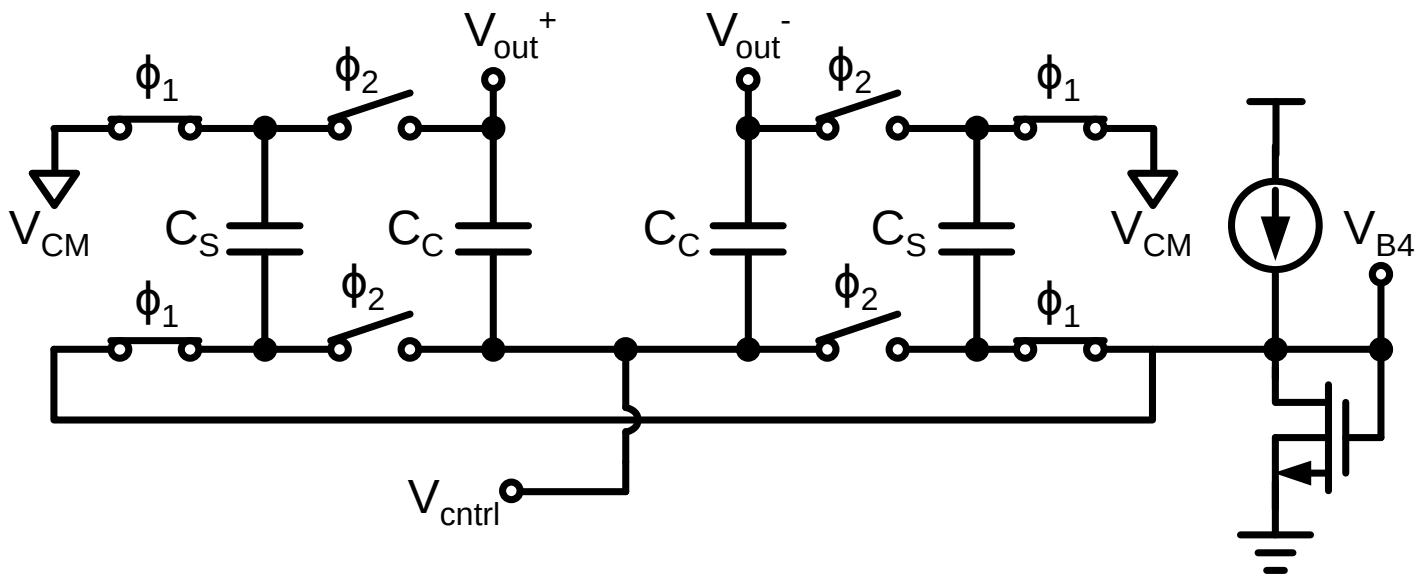
$$I_{D2} = \frac{I_B}{2} + \Delta I, \quad I_{D3} = \frac{I_B}{2} - \Delta I, \quad I_{D5} = I_B$$

CMFB Circuits (Cont.)

- Operational principle of CMFB circuits
  - For example, when a positive common-mode signal is present → I_{M2} and I_{M3} increase → I_{M5} increase → V_{cntrl} increase
  - V_{cntrl} sets the current levels in the n-channel current sources at the output of the OPAMP, thus, bringing the common-mode voltage back to V_{CM}
  - If the common-mode loop gain is large enough, and the differential signals are not so large as to cause transistors in the differential pairs to turn off, the common-mode output voltage will be kept very close to V_{CM}.

CMFB Circuits (Cont.)

- A switched-capacitor circuit



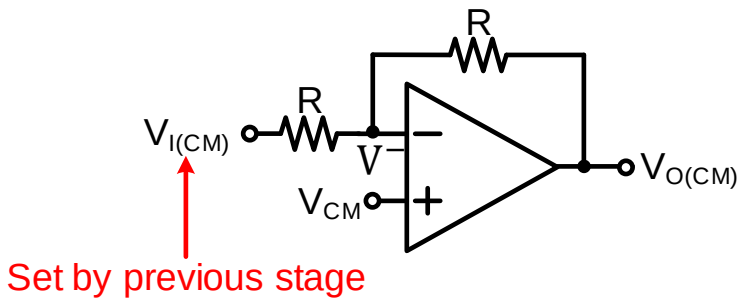
- Using larger capacitance values overloads the OPAMP
- Reducing the capacitors too much caused common-mode offset voltages due to charge injection of the switches.

$$\frac{V_{out}^{+} + V_{out}^{-}}{2} - V_{cntr1} \approx V_{CM} - V_{bias}$$

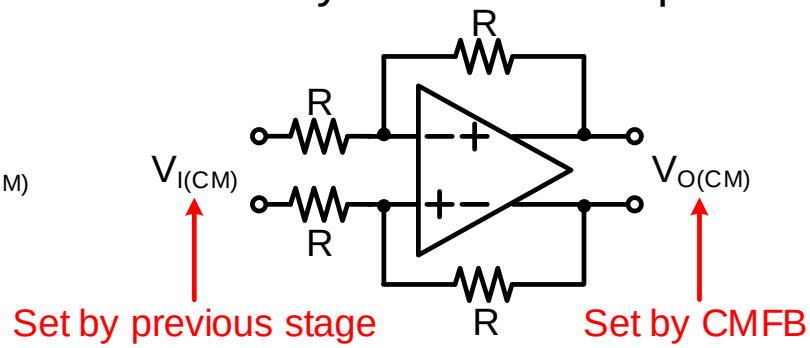
Common-Mode Voltage of OPAMP

- Take inverting amplifier (with ac gain=1) for example

Single-ended amplifier

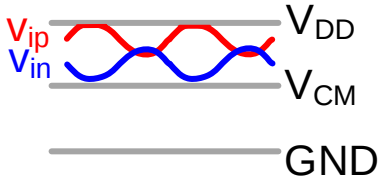


Fully-differential amplifier

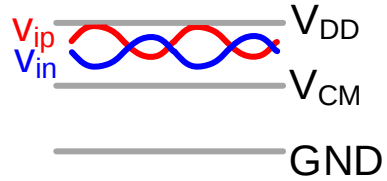


- Single-ended amplifier
  - Input common-mode voltage at $V^- = V_{CM}$ (Virtually shorted to V^+)
  - Output common-mode voltage at $V_{O(CM)} = V_{CM} - (V_{I(CM)} - V_{CM})$
- Fully-differential amplifier
  - Input common-mode voltage at $V^+ = V^- = \frac{1}{2}(V_{I(CM)} + V_{O(CM)})$
  - Output common-mode voltage at $V_{O(CM)}$ → Set by CMFB

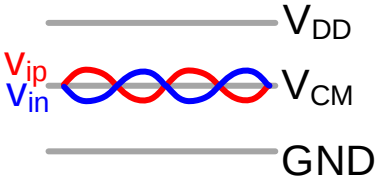
with $V_{os(CMFB)}$ and large $V_{os(diff)}$



with $V_{os(CMFB)}$ and small $V_{os(diff)}$



without $V_{os(CMFB)}$ and $V_{os(diff)}$



Appendix

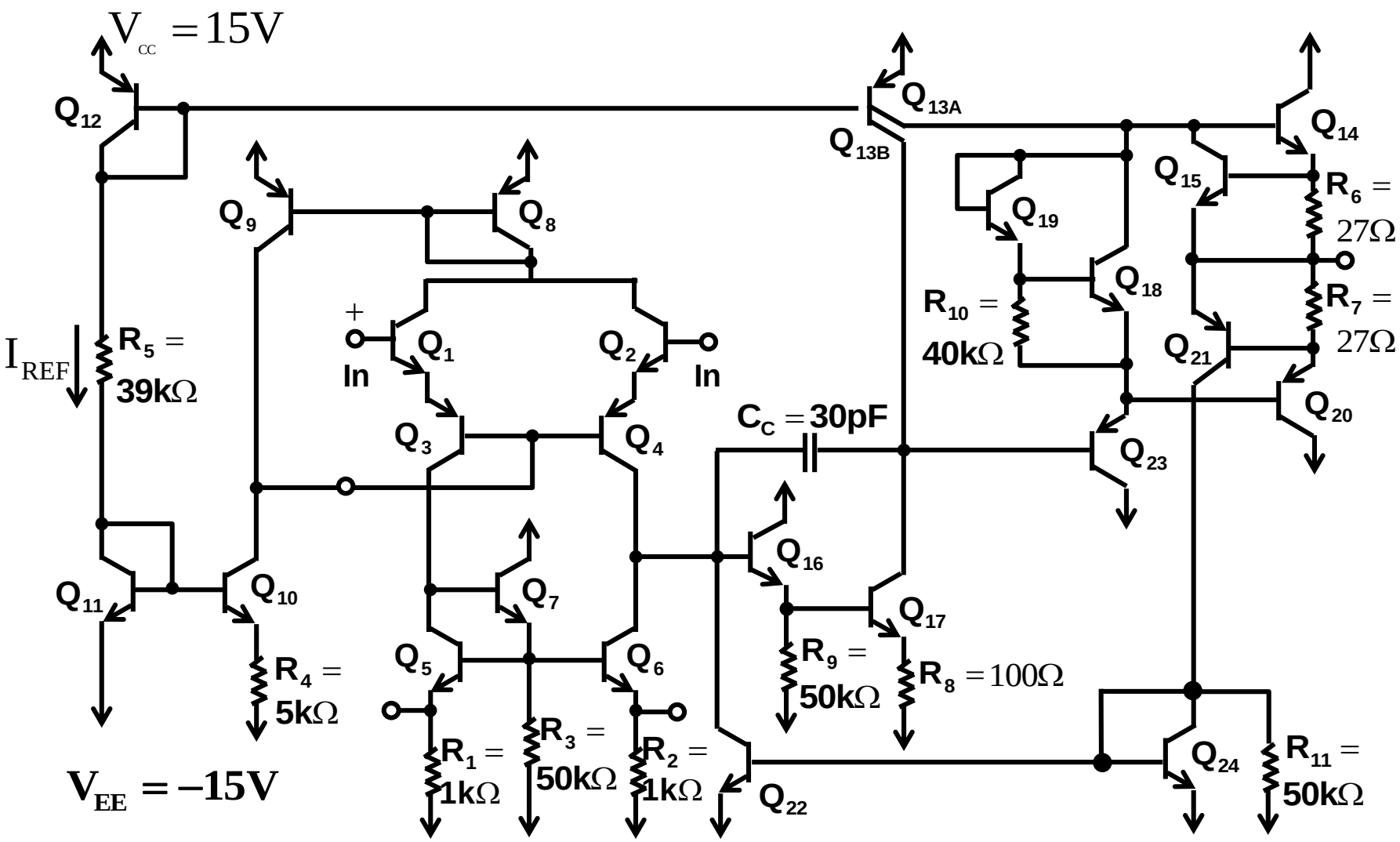
- 741 OPAMP
- Modern techniques for the BJT OPAMP
  - Rail-to-rail input common-mode OPAMP
  - Bias design
  - Input stage design
  - Common-mode feedback (CMF)
  - Output stage with near rail-to-rail output swing
- Full version of the output stage
  - Buffer/driver stage
  - Output-stage current sensing
  - Feedback for the current of inactive transistor
  - Minimum current in the inactive output transistor

741 OPAMP

- Uses a large number of transistors but relatively few resistors and only one capacitor
  - R and C occupy large silicon area .
  - C need more fabrication steps
  - High-quality R&C are not easy to fabricate.

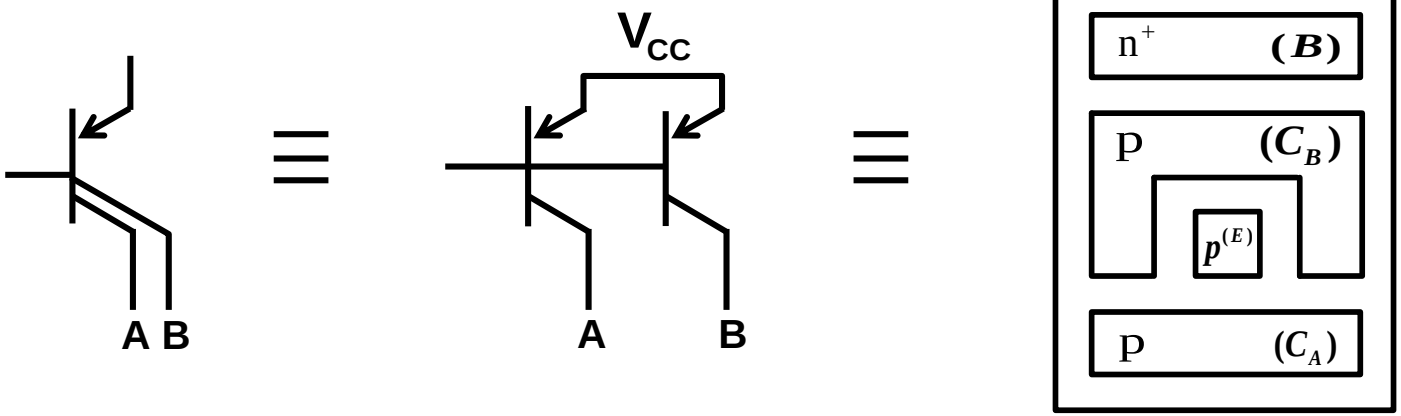
- Circuit Diagram in the next page.

741 OPAMP (Cont.)

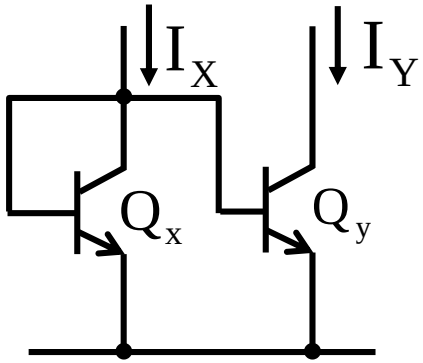


Basic Parts of 741 OPAMP

- Bias circuit
  - I_{ref} is generated by Q_{11},Q_{12},Q_{10},R_4,Q_8,Q_9,Q_{13}
  - Double-collector PNP Q_{13}



  - Current mirror



$$\frac{I_y}{I_x} = \frac{A_{E(Q_y)}}{A_{E(Q_x)}}$$

where A_E is emitter area

Basic Parts of 741 OPAMP(Cont.)

- Short-circuit protection circuitry
  - R_6,R_7,Q_{15},Q_{21},Q_{24},Q_{22}
- 741 OPAMP consists of 3 stages
  - Input differential stage
  - Single-ended high-gain stage
  - Output-buffering stage
- Input stage
  - Q_1~Q_7, R_1~R_3
  - Biased by Q_8~Q_{10} to provide high input impedance.
  - Q_3&Q_4 are lateral PNP (low β)

    Higher emitter-base junction breakdown than NPNs
    - Protect input transistors Q_1&Q_2 when they are accidentally shorted to supply voltages.
  - Q_5~Q_7, R_1~R_3 provide high-resistance load and single-ended output.

Basic Parts of 741 OPAMP(Cont.)

- Second stage
  - Q_{16},Q_{17},Q_{13B},R_8,R_9
  - Q_{16} acts as an emitter follower, thus giving
    - High input resistance
    - Low base current if R_9 is large, hence low loading of the first stage.
  - Q_{17}: common emitter configuration
  - Q_{13B}: active load
  - C_c: Miller capacitor for pole-splitting compensation
    30pF area occupied is about 13 times that of a standard NPN transistor.

- Output stage
  - Provide low output resistance
  - Class AB

DC Analysis of 741 OPAMP

- Device parameters
  - Standard transistors

    NPN: $I_S = 10^{-14}$A, $\beta = 200$, $V_A = 125$V

    PNP: $I_S = 10^{-14}$A, $\beta = 50$, $V_A = 50$V
  - Nonstandard transistors Q_{13},Q_{14},Q_{20}

    1. $Q_{13} = Q_{13A} + Q_{13B}$

       Q_{13A}: $I_{SA} = 0.25 \times 10^{-14}$ A

       Q_{13B}: $I_{SB} = 0.75 \times 10^{-14}$ A
    2. Q_{14} & Q_{20}

       $I_S = 3 \times 10^{-14}$ A
- Reference bias current

$$I_{REF} \approx \frac{V_{CC} - V_{EB12} - V_{BE11} - (-V_{EE})}{R_5}$$

- For $V_{CC} = -V_{EE} = 15$V

  $V_{BE11} = V_{BE12} \approx 0.7$V

  $\Rightarrow I_{REF} \approx 0.73$mA

Input Stage Bias

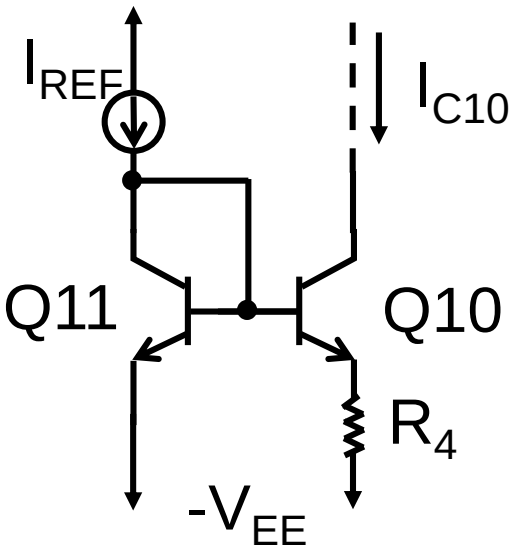
- Widlar current sources
  - Bipolar

$$V_{BE11} - V_{BE10} = I_{C10} R_4$$

$$\Rightarrow V_T \ln \frac{I_{REF}}{I_{C10}} = I_{C10} R_4$$

$$\Rightarrow \text{Trial and error to determine } I_{C10}$$

$$\Rightarrow I_{C10} = 19\mu A$$



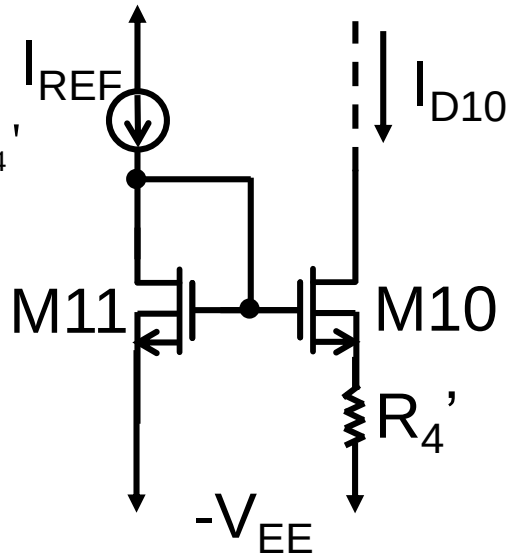
  - MOSFET

$$V_{OV11} = V_{OV10} + I_{D10} \times R_4'$$

$$assume\ \ I_D = K \cdot V_{OV}{}^2 \Rightarrow \sqrt{\frac{I_{REF}}{K}} = \sqrt{\frac{I_{D10}}{K}} + \left(\sqrt{I_{D10}}\right)^2 \times R_4'$$

$$\sqrt{I_{D10}} = \frac{-\sqrt{\frac{1}{K}} \pm \sqrt{\frac{1}{K} + 4R_4' \sqrt{\frac{I_{REF}}{K}}}}{2R_4'} > 0$$

$$\Rightarrow I_{D10} = \frac{1 + 2R_4' \sqrt{KI_{REF}} - \sqrt{1 + 4R_4' \sqrt{KI_{REF}}}}{2K\left(R_4'\right)^2}$$



Input Stage Bias(Cont.)

- Input differential circuitry

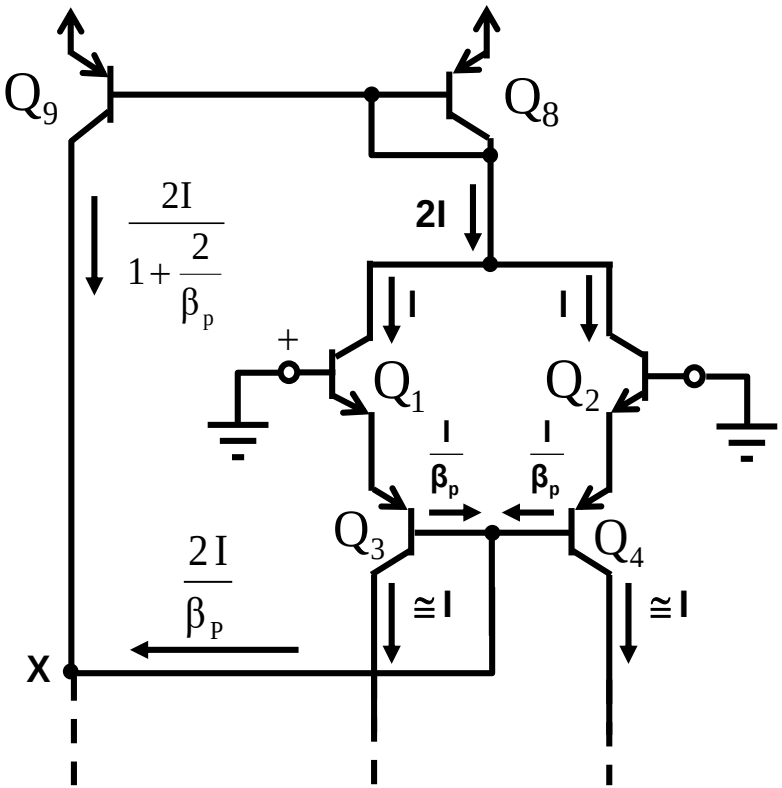
Let $I_{C1} = I_{C2} = I \Rightarrow I_{E3} = I_{E4} \approx I$

$$I_{B3} = I_{B4} = \frac{I}{1+\beta_P} \approx \frac{I}{\beta_P}$$

$$I_{C9} = \frac{2I}{1+\frac{2}{\beta_P}}$$

$I_{C10} \approx 2I \Rightarrow I = 9.5\mu A$

$I_{C1} = I_{C2} \cong I_{C4} = 9.5\mu A$



◆ Q_1~Q_4,Q_8,Q_9 form a negative feedback loop
The feedback stabilize the value of I (i.e. I is kept unchanged and only controlled by I_{C10})

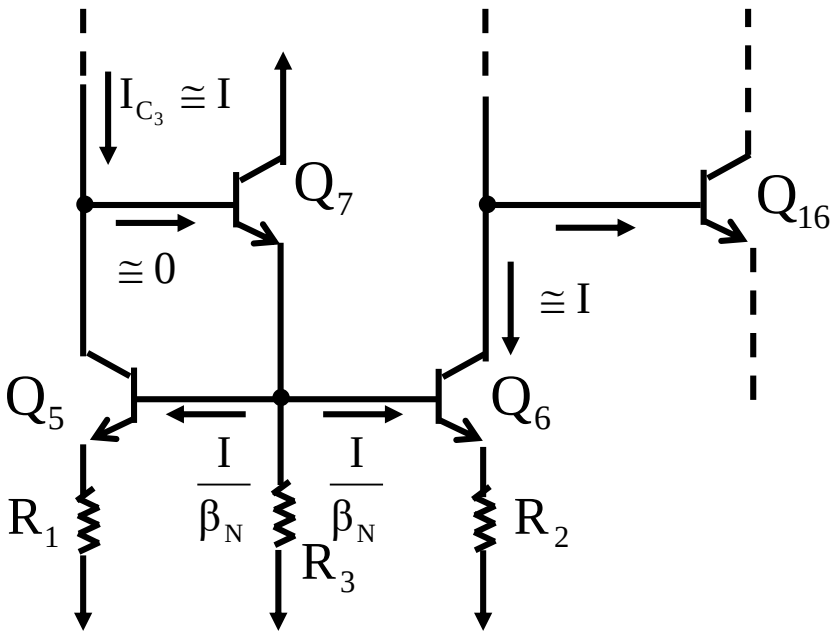
Input Stage Bias(Cont.)

- Active load
  - $I_{C_5} \approx I_{C_6} \approx I$

$$I_{C_7} \approx I_{E_7} = \frac{2I}{\beta_N} + \frac{V_{BE_6} + IR_2}{R_3}$$

$$V_{BE_6} = V_T \ln \frac{I}{I_S} = 517mV$$

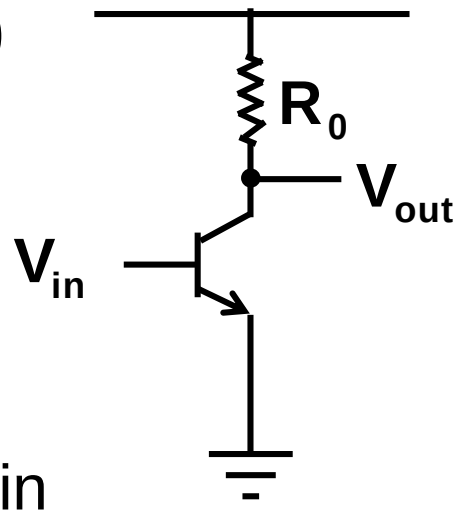
$$\Rightarrow I_{C_7} \approx 10.5\mu A$$

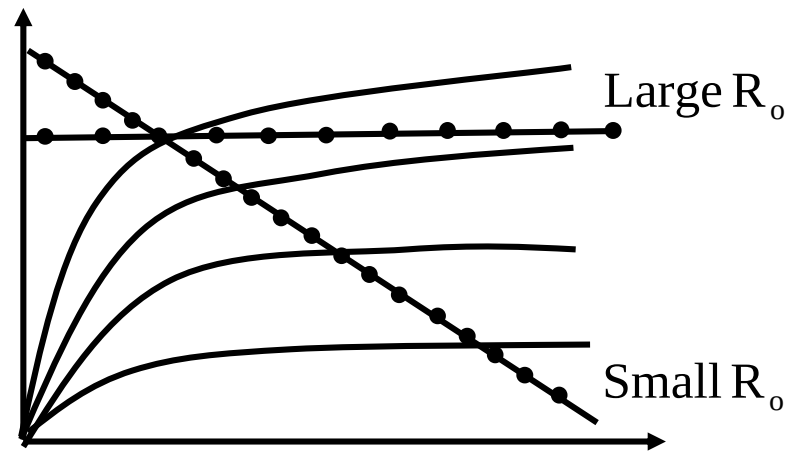


Gain stage with resistor load (Cont.)

- Resistor Load

$$A = g_m\left(R_0 // r_0\right)$$
$$\approx g_m R_0$$
$$\propto \frac{I_C R_0}{V_T}$$





- For High gain
  - ➢ High I_cR_o
  - ➢ High I_cR_o means large voltage drop on R_o
  - ➢ Large power supply
  - ◆ High R_o reduces speed
  - ◆ Use active loads to overcome the above problems

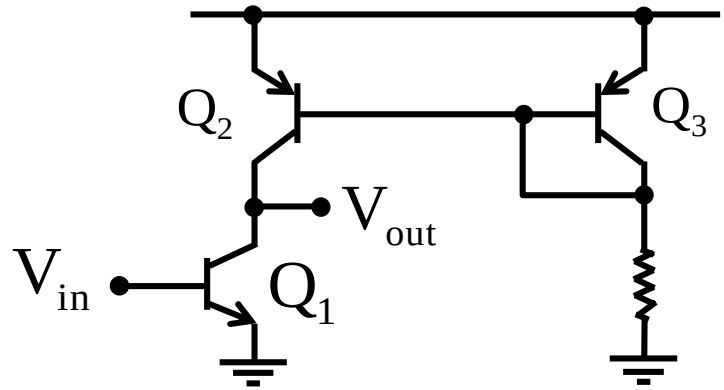
Gain Stage with Active Load

- Transistor can provide large resistance if properly biased.
  - Example

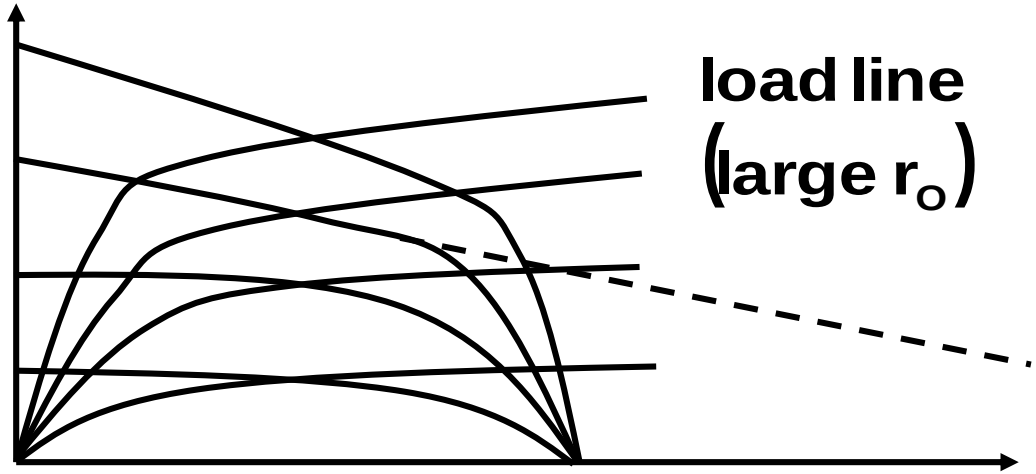
$$A = g_m\left(r_{01}//r_{02}\right)$$

$$\approx g_m\left(\frac{1}{2}r_0\right)$$

$$\propto \frac{\frac{1}{2}I_C r_0}{V_T}$$



  - I-V curve & load line



Input bias

- Input bias
  - Input current

$$I_{B1} = I_{B2} = \frac{I}{\beta_N} = \frac{9.5\mu A}{200} = 47.5\,nA$$

$\Rightarrow$ very small

- Offset current and offset voltage are introduced in chapter 6
- Input common-mode range
  - In this range, the input stage remains in the linear active mode
  - This range is determined at the upper end by saturation of Q_1 and Q_2, and at the lower end by saturation of Q_3 and Q_4.

Second Stage Bias

- $I_{C13B} = 0.75 I_{C12} \approx 0.75 I_{REF} \approx 550\mu A$

  $I_{C17} \approx I_{C13B} = 550\mu A$

$$V_{BE_{17}} = V_T \ln \frac{I_{C_{17}}}{I_S} = 618\,mV$$

$$I_{C_{16}} \approx I_{E_{16}} = I_{B_{17}} + \frac{I_{E_{17}} R_8 + V_{BE_7}}{R_9} \approx 16.2\,\mu A$$

Output Stage Bias

- If short-circuit protection circuitry is omitted

$$I_{C_{13A}} = 0.25 I_{REF} \approx 180\mu A$$

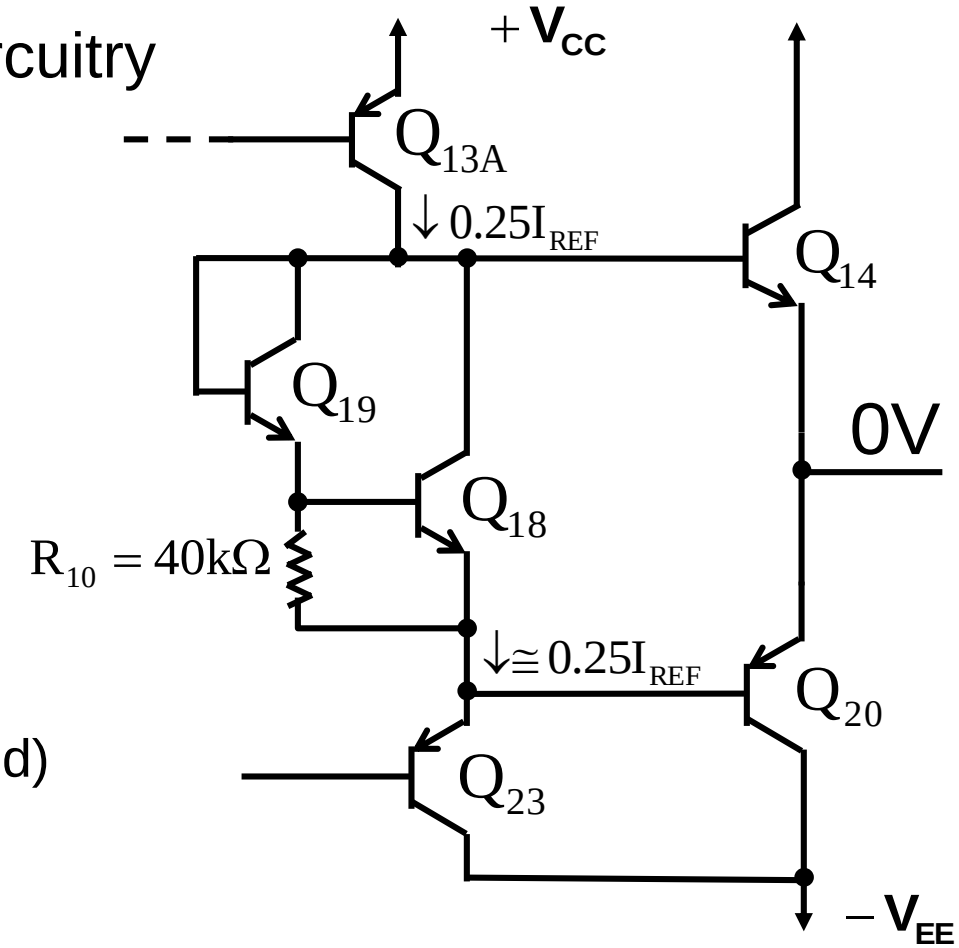
$$I_{B_{23}} = \frac{180}{50} = 3.6\mu A$$

$$I_{C_{18}} \approx I_{E_{18}} = 180 - \frac{V_{BE_{18}}}{R_{10}}$$

$$\approx 180 - \frac{0.6}{40\times 10^3} \approx 165\mu A$$

(V_{BE18} = 0.6V is assumed)

$$= V_T \ln\left(\frac{I_{C18}}{I_S}\right)$$



⇨ $V_{BE18} \approx$ 588mV (This is close to the value assumed)

Output Stage Bias(Cont.)

$$I_{C_{19}} \approx I_{E_{19}} = I_{B_{18}} + I_{R_{10}} = 0.8\,\mu A + \frac{V_{BE_{18}}}{R_{10}} \approx 15.5\,\mu A$$

$$V_{BE_{19}} = V_T \ln \frac{I_{C_{19}}}{I_S} = 530\,mV$$

$$V_{BE_{18}} + V_{BE_{19}} = 588\,mV + 530\,mV = 1.118\,V$$

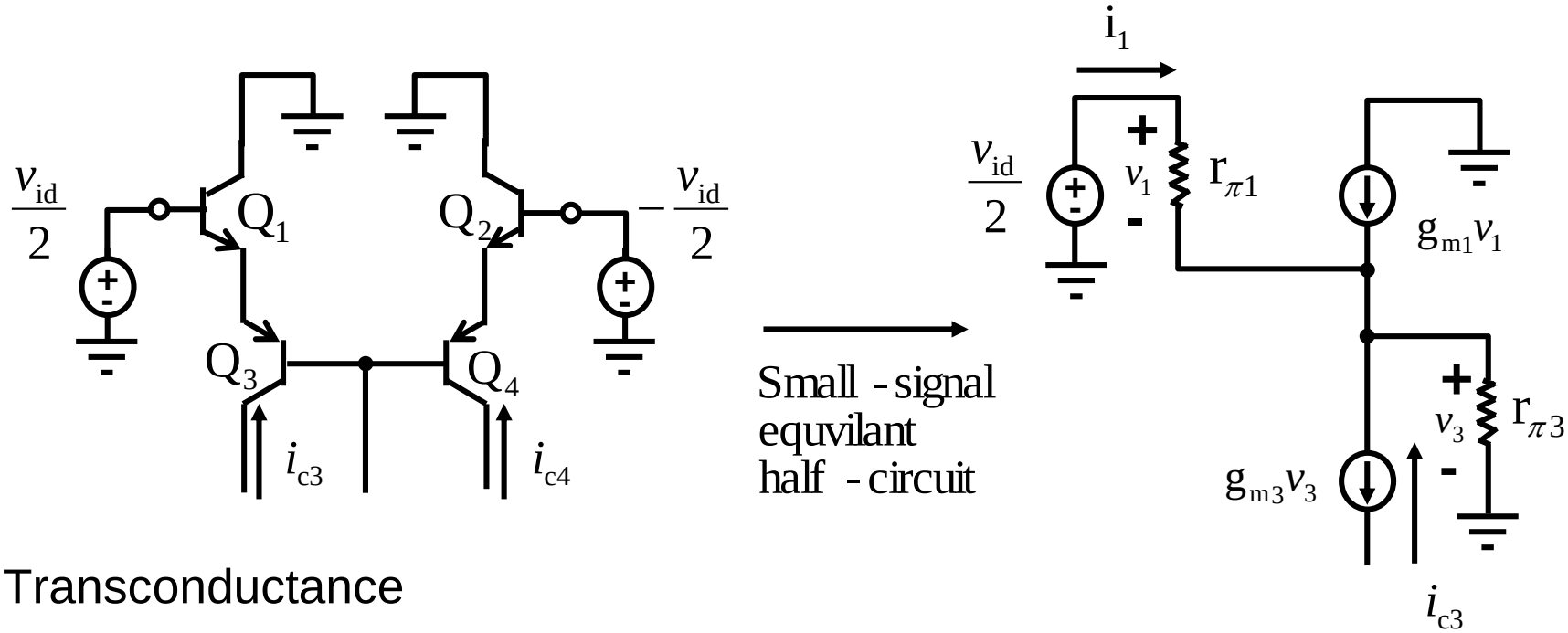
$$V_T \ln \frac{I_{C_{14}}}{I_{S_{14}}} + V_T \ln \frac{I_{C_{20}}}{I_{S_{20}}} = 1.118\,V$$

$$V_T \ln \frac{I_{C_{14}} I_{C_{20}}}{I_{S_{14}} I_{S_{20}}} = 1.118\,V$$

$\Rightarrow$ $I_{C14} = I_{C20} = 154uA$

Small-Signal Analysis of 741 Input Stage

- Simplified ac schematic
  - For differential mode input, biases of Q_3 and Q_4 are at ac ground.



- Transconductance

$$\frac{v_{id}}{2} = v_1 + v_3$$

$$v_1 g_{m1}(1+\frac{1}{\beta_1}) = v_3 g_{m3}(1+\frac{1}{\beta_3})$$

Small-Signal Analysis of 741 Input Stage(Cont.)

$$\Rightarrow \frac{v_{id}}{2} = v_3\left[\frac{g_{m3}\left(1+\frac{1}{\beta_3}\right)}{g_{m1}\left(1+\frac{1}{\beta_1}\right)}+1\right]$$

since $|I_{c3}| = I_{c3}$, $g_{m1} = g_{m3}$, $\beta_1 = 200 >> 1$, $\beta_3 = 50 >> 1$

$$\Rightarrow v_3 = \frac{v_{id}}{4} \text{.....(1)}$$

$$i_{c3} = -\frac{g_{m3}v_{id}}{4}$$

$$i_{c4} = \frac{g_{m3}v_{id}}{4}$$

$$i_{out} = -i_{c4} + i_{c3} = -\frac{g_{m3}v_{id}}{2}$$

$$G_{m1} = -\frac{i_{out}}{v_{id}} = \frac{g_{m1}}{2} = \frac{I_{c1}}{2V_T} \approx \frac{1}{5.26k\Omega}$$

Small-Signal Analysis of 741 Input Stage (Cont.)

- Input Resistance R_{id}

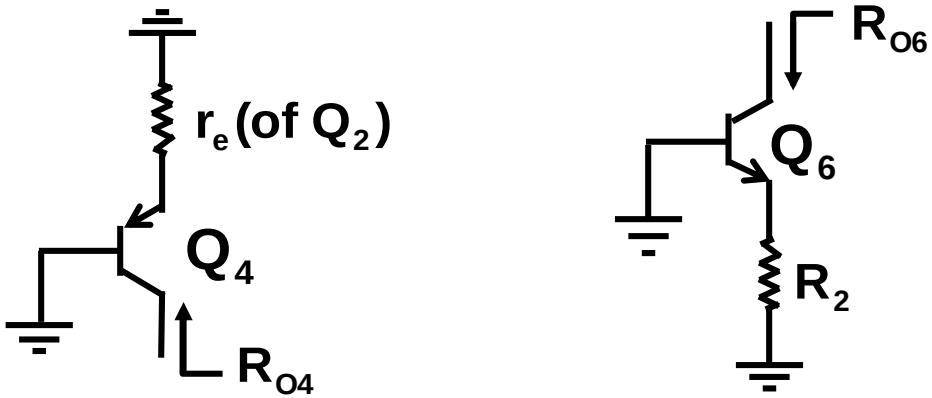
$$\text{From(1)}, v_1 = v_3 = \frac{v_{id}}{4}$$

$$R_{id} = \frac{v_{id}}{i_i} = \frac{v_{id}}{\left(V_1/r_{\pi_1}\right)} = 4r_{\pi 1} = 4\left(\beta_1 + 1\right)r_e = 2.1M\Omega$$

$$where\ r_e = \frac{V_T}{I_C} = \frac{25mV}{9.5\mu A} = 2.63K\Omega = \frac{1}{g_m}$$

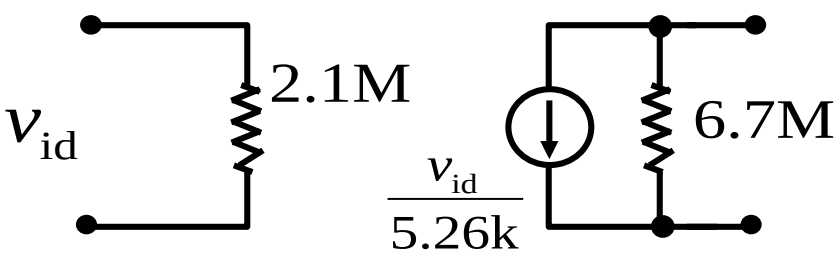
Small-Signal Analysis of 741 Input Stage (Cont.)

- Output resistance R_{O1}-simplified circuit



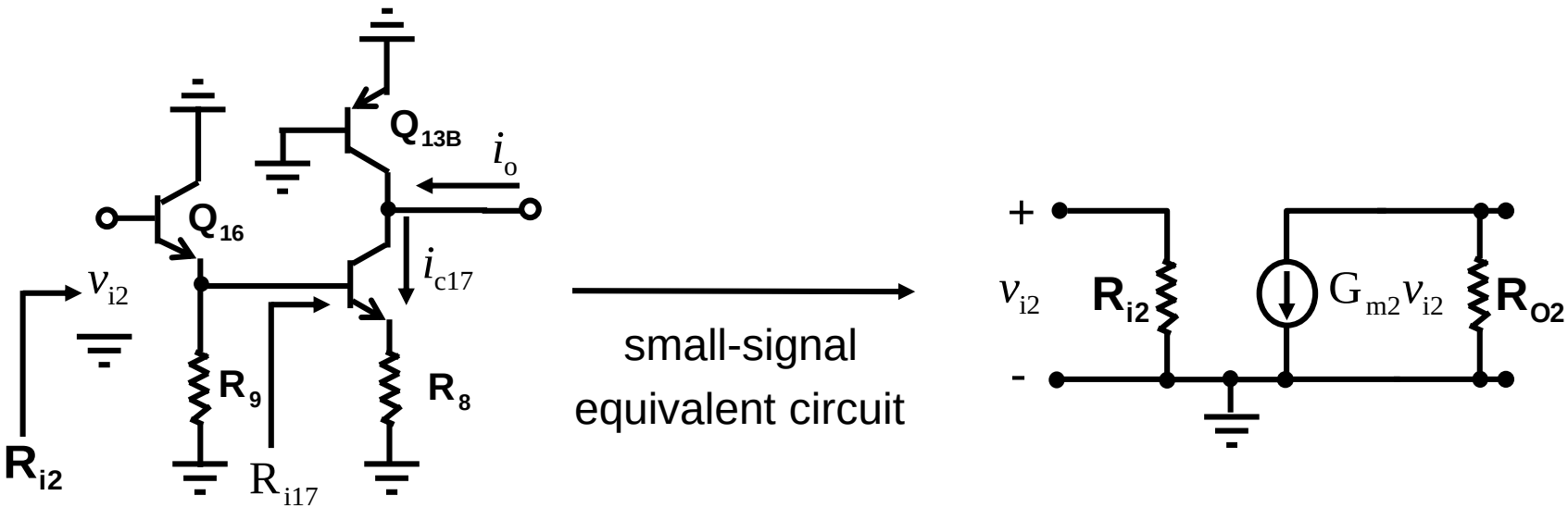
  - Refer to chapter 6
    - $R_{o4} = r_{o(Q4)}\{1+g_{m4}(r_e // r_{\pi 4})\} \cong 10.5M\Omega$
    - $R_{o6} = r_{o(Q6)}\{1+g_{m6}(R_2 // r_{\pi 6})\} \cong 18.2M\Omega$ where $r_o = V_A/I$
  - $R_{o1} = R_{o4} // R_{o6} \cong 6.7M\Omega$

- Two-port equivalent circuit of input stage



Small-Signal Analysis of the 741 Second Stage

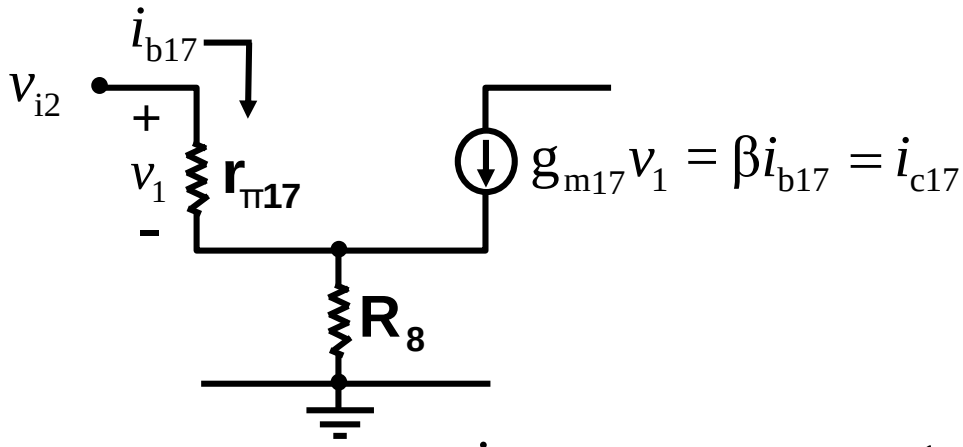
- Simplified circuit



- Input resistance R_{i2}
  - $R_{i17} = (\beta_{17}+1)(r_{e17}+R_8)$
  - $R_{i2} = (\beta_{16}+1)(r_{e16}+(R_9//R_{i17})) \cong 4M\Omega$

Small-Signal Analysis of the 741 Second Stage (Cont.)

- Transconductance G_{m2}
  - Voltage gain of the emitter follower Q_{16} is nearly unity.



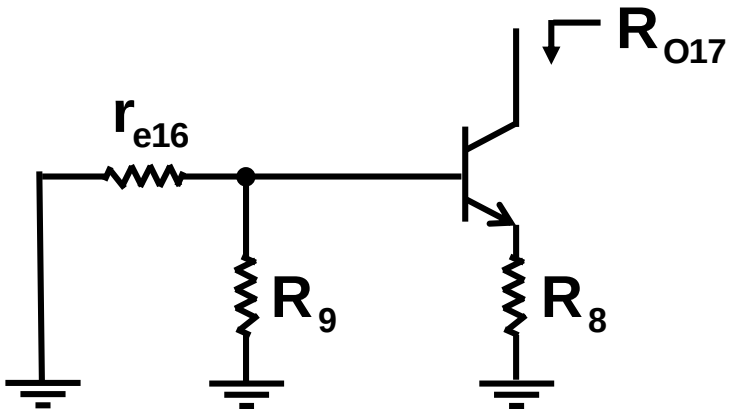
$$v_{i2} = i_{b17} r_{\pi 17} + (i_{b17} + i_{c17}) R_8 = \frac{i_{c17}}{\beta_{17}} r_{\pi 17} + i_{c17}\left(1 + \frac{1}{\beta_{17}}\right) R_8$$

$$= i_{c17}\left[\frac{1}{g_{m17}} + \left(1 + \frac{1}{\beta_{17}}\right) R_8\right] \approx i_{c17}\left(\frac{1 + g_{m17} R_8}{g_{m17}}\right)$$

$$\Rightarrow G_{m2} = \frac{i_{c17}}{v_{i2}} \approx \frac{g_{m17}}{1 + g_{m17} R_8} \approx 6.5 mA/V$$

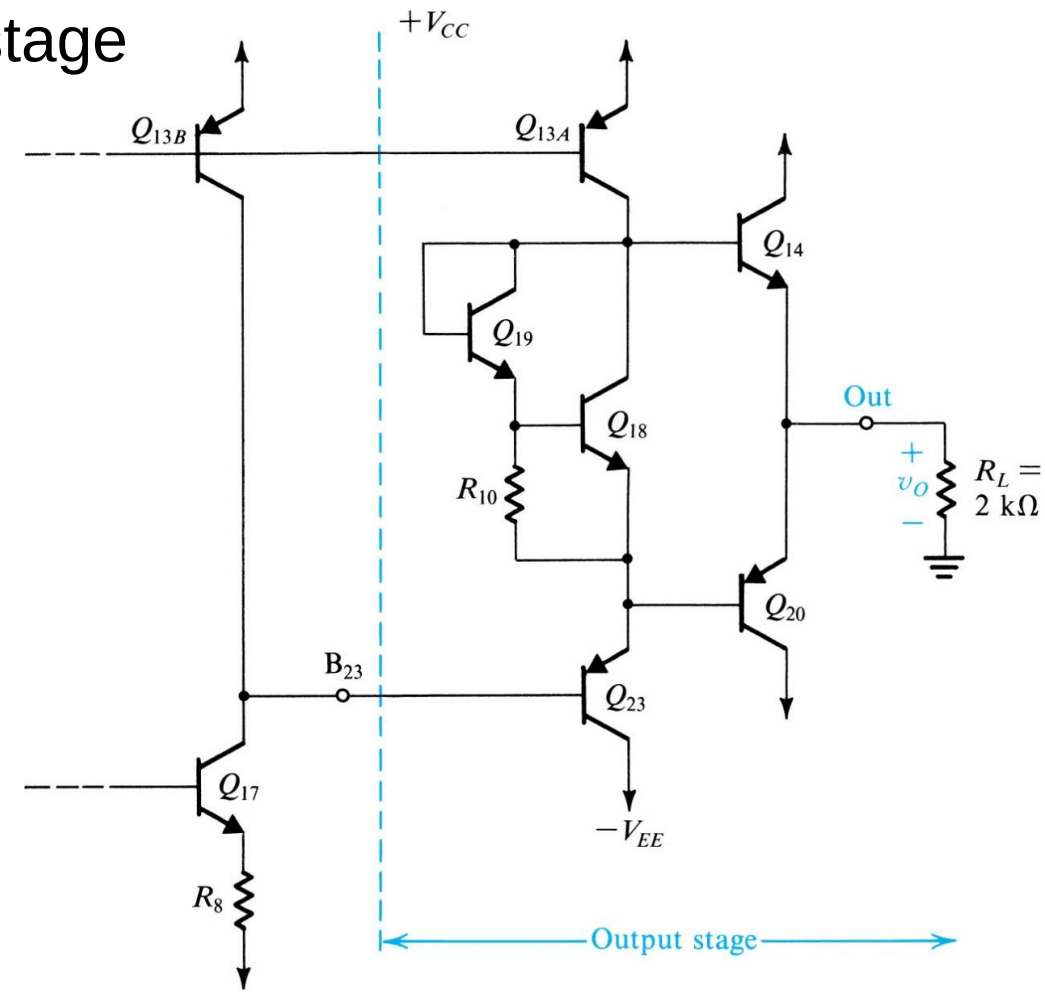
Small-Signal Analysis of the 741 Second Stage (Cont.)

- Output Resistance
  - $R_{o2} = R_{o17} // R_{o13B}$
  - $R_{o13B} = r_{o(Q13B)}$
  - $R_{o17} \cong r_{o(Q17)}[1+gm_{17}(R_8 // r_{\pi 17})]$
  - $R_{o2} = R_{o17} // R_{o13B} \cong 787k\Omega // 90.9k\Omega \cong 81k\Omega$



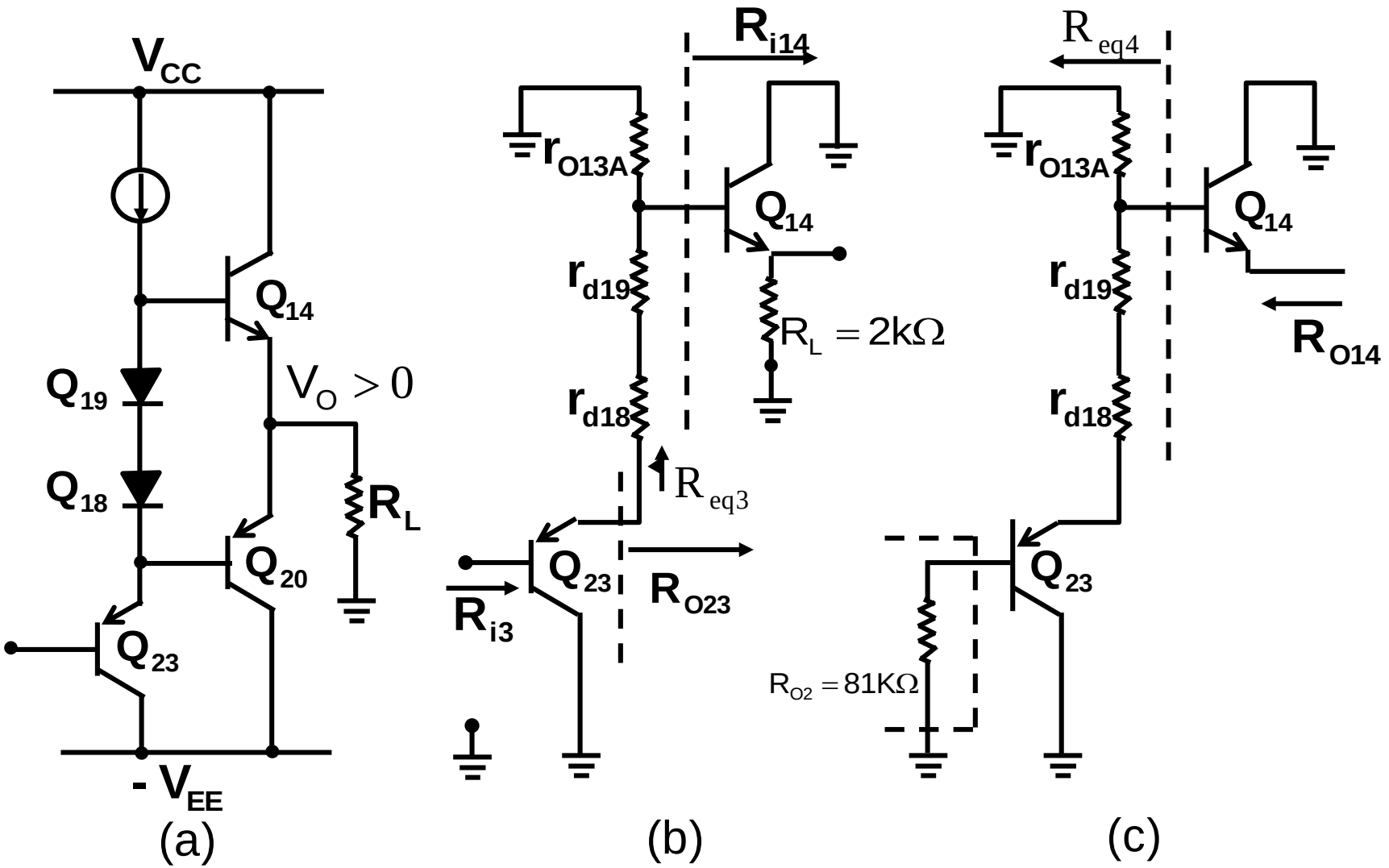
741 Output Stage

- Output voltage limits
  - $V_{omax} = V_{CC} - |V_{CE13A(sat)}| - V_{BE14}$
  - $V_{omin} = -V_{EE} + V_{CE17(sat)} + V_{EB23} + V_{EB20}$
- Class AB stage



Small-Signal Analysis of the 741 Output Stage

- Simplified circuit for positive V_o, $V_{BE14}>V_{EB20}$



Small-Signal Analysis of the 741 Output Stage(Cont.)

- Input resistance R_{i3}
  - For positive V_o with Q_{20} neglected (Q_{14} conducts more current)

    $R_{i14} = r_{\pi 14}+(1+\beta_{14})R_L$

    $R^+_{eq3} = r_{d18}+r_{d19}+(r_{o(Q13A)}//R_{i14})$ where $r_{d18}+r_{d19}$ is very small.

    $R^+_{i3} = r_{\pi 23}+(1+\beta_{23})R^+_{eq3}$
  - For negative V_o with Q_{14} neglected (Q_{20} conducts more current)

    $R_{i20} = r_{\pi 20}+(1+\beta_{20})R_L$

    $R^-_{eq3} = r_{d18}+r_{d19}+r_{o(Q13A)}$ where $r_{d18}+r_{d19}$ is very small.

    $R^-_{i3} = r_{\pi 23}+(1+\beta_{23})(R^-_{eq3}//R_{i20})$
  - Actual R_{i3} is between R^+_{i3} and R^-_{i3}

Small-Signal Analysis of the 741 Output Stage(Cont.)

- Output Resistance R_{out}
  - For positive V_o with Q_{20} neglected

$$R_{out}^{+} \approx R_{o14}$$

$$R_{eq4} = r_{o(Q13A)} // \left[r_{d19} + r_{d18} + r_{e23} + \frac{R_{o2}}{1+\beta_{23}} \right]$$

$$R_{o14} = r_{e14} + \frac{R_{eq4}}{1+\beta_{14}}$$

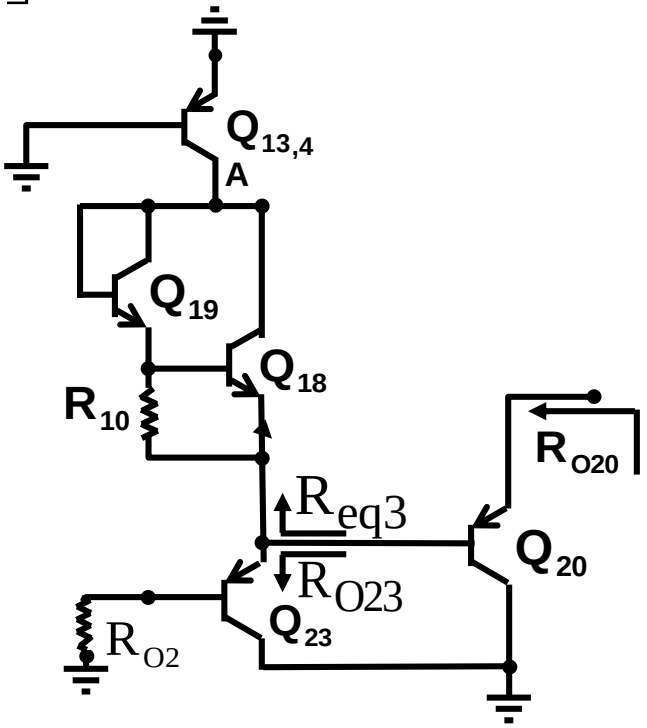
  - For negative V_o with Q_{14} neglected

$$R_{out}^{-} \approx R_{O20}$$

$$R_{O23} = r_{e23} + \frac{R_{O2}}{1+\beta_{23}}$$

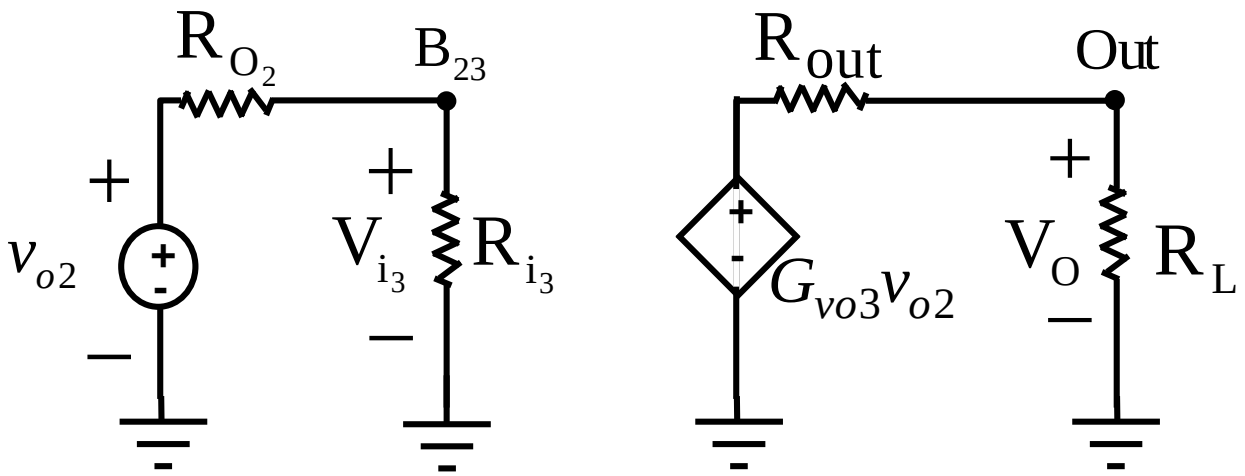
$$R_{O20} = r_{e20} + \frac{R_{eq3} // R_{O23}}{1+\beta_{20}}$$

  - Actual R_{out} is between R^{+}_{out} and R^{-}_{out}



Small-Signal Analysis of the 741 Output Stage(Cont.)

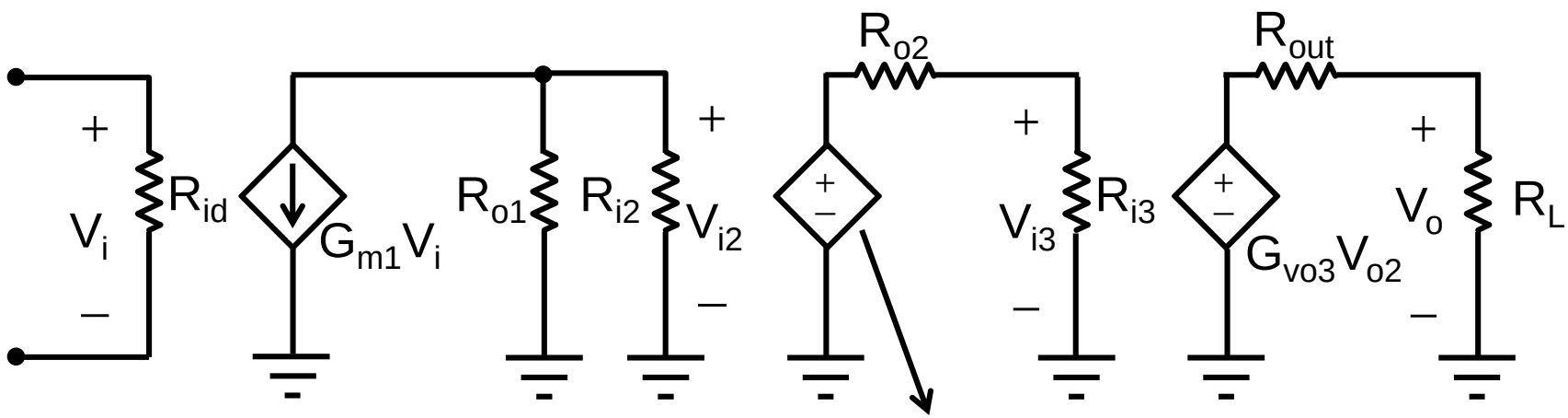
- Small-signal equivalent circuit model



$$G_{vo3} = \frac{R_{i_3}}{R_{i_3} + R_{O_2}} \approx 0.978$$

Gain and Frequency Response of the 741OPAMP

- Equivalent circuit of the 741 OPAMP



$V_{o2} = -G_{m2}R_{O2}V_{i2}$

- Gain

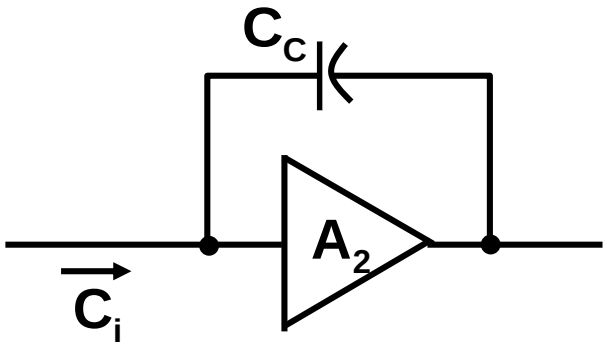
$$\frac{V_o}{V_i} = \frac{V_{i2}}{V_i} \times \frac{V_{o2}}{V_{i2}} \times \frac{V_o}{V_{o2}}$$

$$= \left[-G_{m1}(R_{o1} // R_{i2})\right] \times \left[-G_{m2}R_{o2}\right] \times G_{vo3} \times \frac{R_L}{R_{out} + R_L}$$

$$\approx 107.7dB$$

Gain and Frequency Response of 741 OPAMP (Cont.)

- Frequency Response
  - 741 is an internally compensated OPAMP
  - Miller Compensation



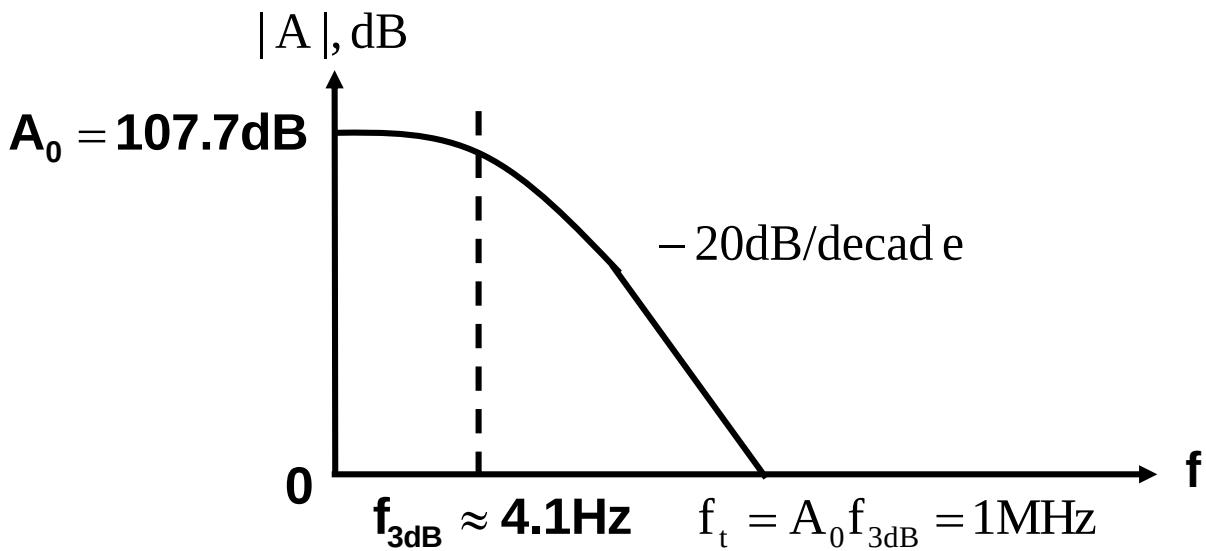
$$\begin{cases} C_i = C_C(1+|A_2|) --- \textit{Miller theorem} \\ A_2 = -G_{m_2} R_{O_2} \left(\dfrac{R_{i_3}}{R_{O_2}+R_{i_3}}\right) = -526.5 \times 0.978 \approx -515 \end{cases}$$

$$\Rightarrow \mathrm{C_i} \approx 30\,\mathrm{pF} \cdot (1+|-515|) = 15480\,\mathrm{pF}$$

Gain and Frequency Response of 741 OPAMP (Cont.)

- Neglecting the parasitic capacitance at the base of Q_{16}
- Total resistance at this node $R_t=(R_{O1}//R_{i2})$

  $\Rightarrow$ Dominant pole $f_p = \dfrac{1}{2\pi R_t C_i} \approx 4.1Hz$
- Bode plot (Neglecting nondominant poles)

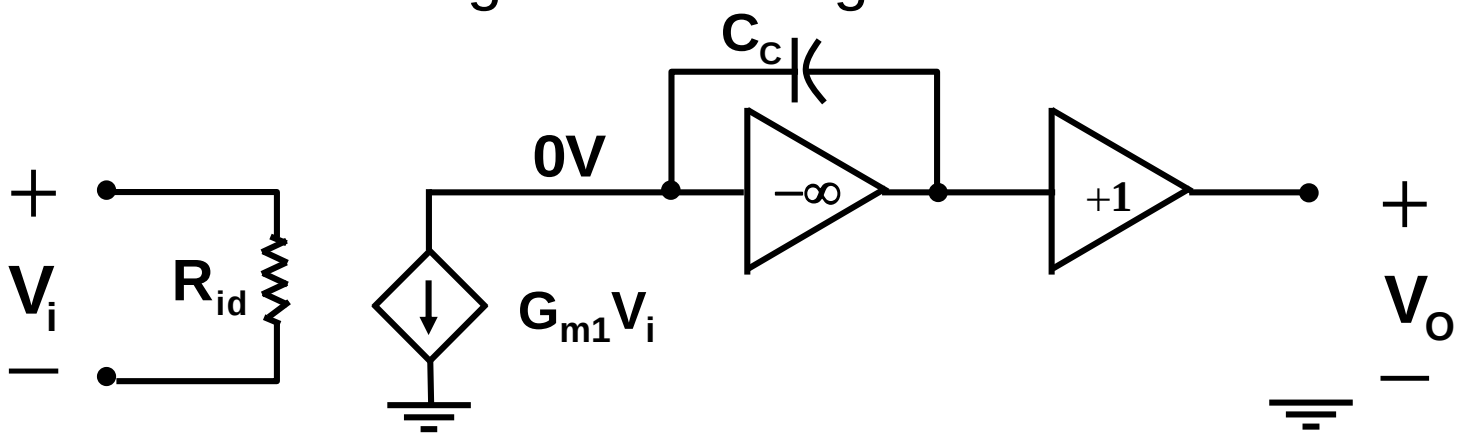


- 3dB bandwidth $f_{3dB} = f_p = 4.1Hz$

  unity-gain bandwidth $f_t = A_0 f_{3dB} = 1MHz$

Gain and Frequency Response of 741 OPAMP (Cont.)

- Simplified model
  - Model the 2nd stage as an integrator



$$A(s) = \frac{V_O(s)}{V_i(s)} = \frac{G_{m1}}{sC_C} \Rightarrow A(j\omega) = \frac{G_{m1}}{j\omega C_C}$$

$$\left|A(j\omega_t)\right| = 1 \Rightarrow \omega_t = \frac{G_{m1}}{C_C}$$

$$For\ G_{m1} = \frac{1}{5.26k\Omega}\ and\ C_C = 30\,pF,\ f_t = \frac{\omega_t}{2\pi} \approx 1MHz$$

(equal to the value calculated before)

Slew Rate

- Large signal behavior
- Output voltage slew limitation

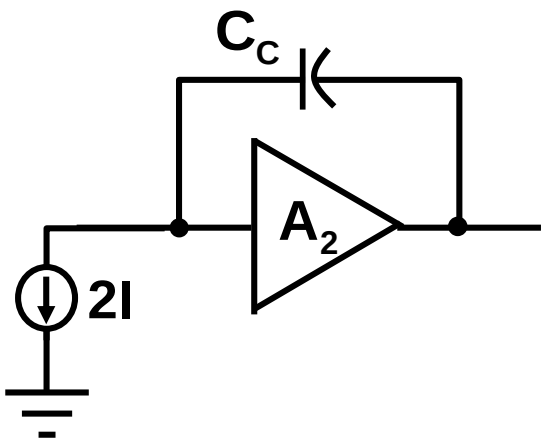
$$\frac{dV}{dt}\Big|_{\max} = slew\ rate = \frac{2I}{C_C}$$

$$f_t = \frac{G_{m1}}{2\pi C_C} \qquad (as\ shown\ previously)$$

$$\Rightarrow \text{slew rate} = \frac{4\pi I}{G_{m1}} f_t$$

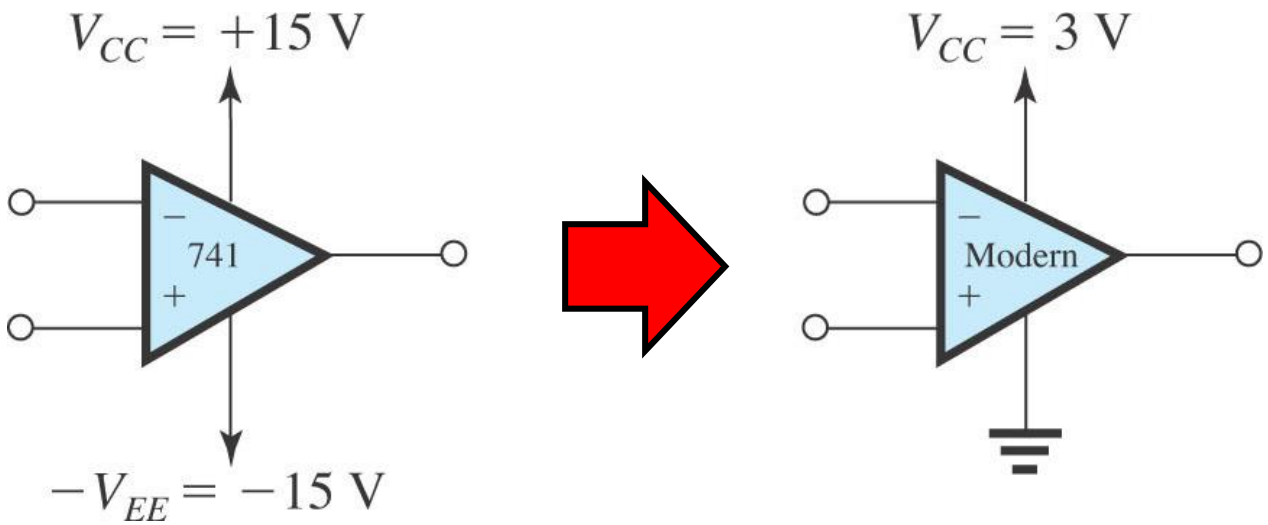
$$G_{m1} = \frac{I}{2V_T} = \frac{1}{2} g_{m1}$$

$$slew\ rate = 8\pi V_T f_t$$



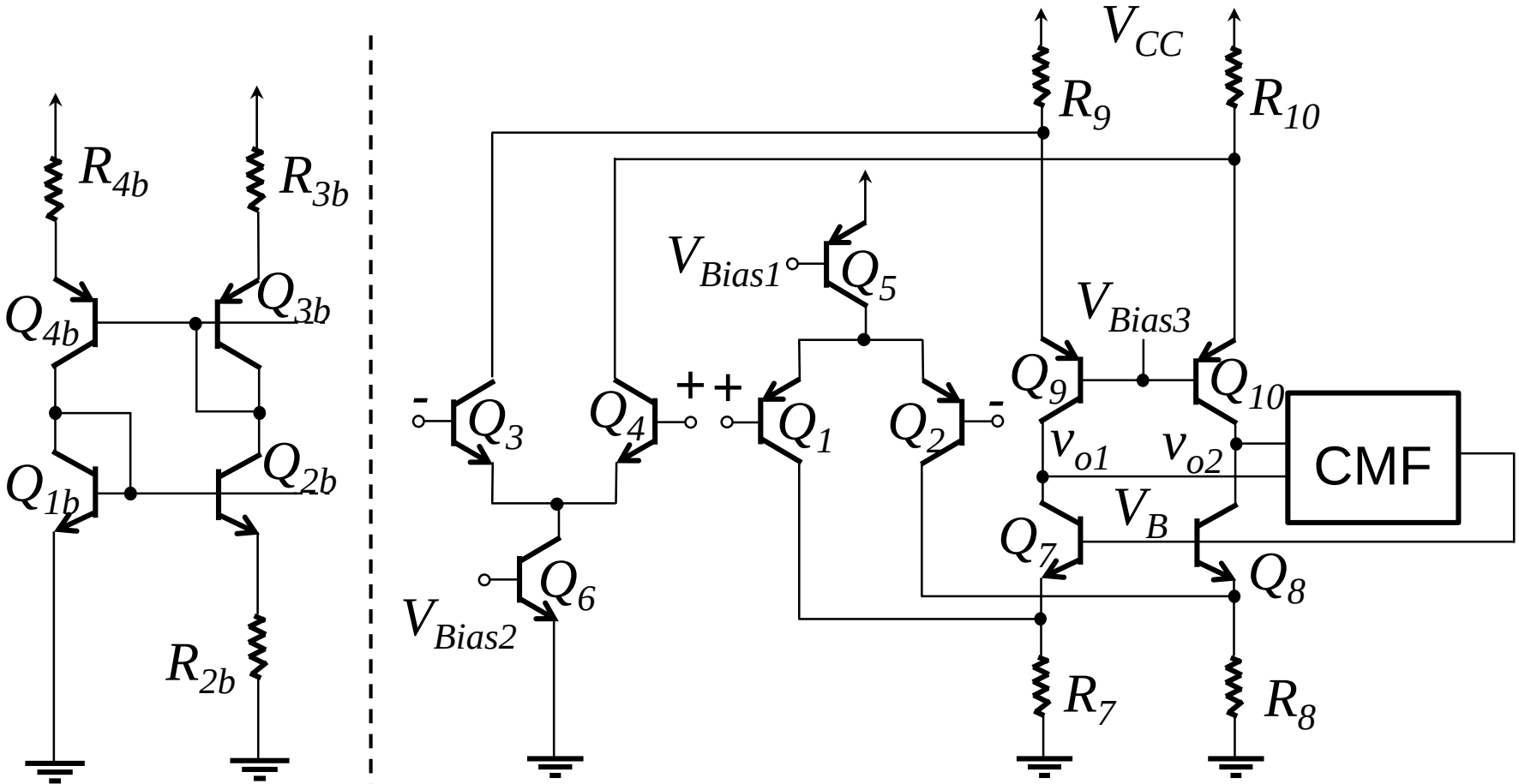
Modern Techniques for the BJT OPAMP

- Reasons for single-supply operation with much lower V_{CC}
  - Meet modern small-feature-size fabrication technologies
  - Be compatible with other low-power-supply systems
  - Minimize the power dissipation, $P = I_{V_{DD}} \cdot V_{DD}$, especially for battery-operated systems



- For a low-voltage single-supply system, rail-to-rail input common-mode range may be required because of its inherent low supply voltages

Rail-to-Rail Input Common-Mode OPAMP



Bias circuit

Input stage

Cascode stage with Common-Mode Feedback (CMF)

Bias Design

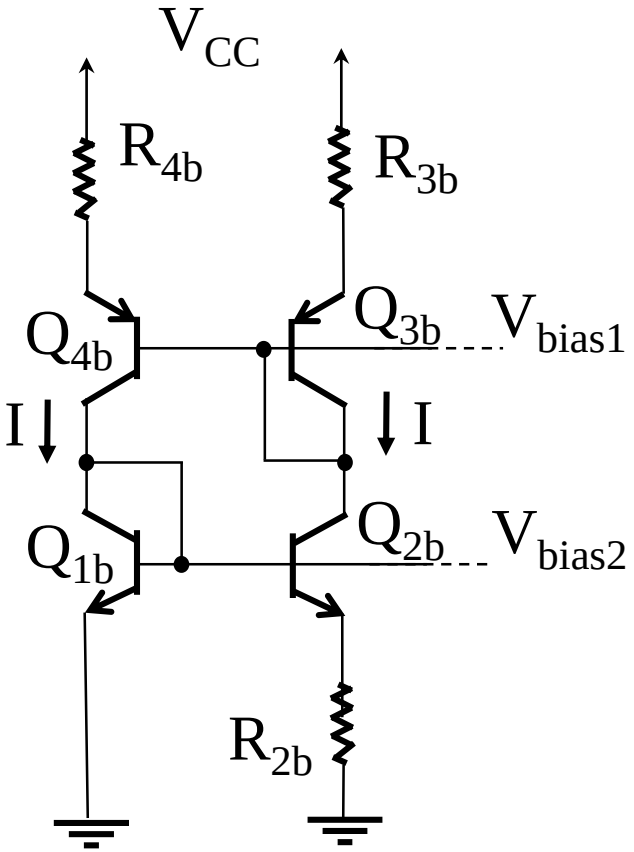
- Widlar current source

$$V_{BE1} = V_T \ ln\left(\frac{I}{I_{S1}}\right)$$

$$V_{BE2} = V_T \ln\left(\frac{I}{I_{S2}}\right)$$

$$\Rightarrow V_{BE1} - V_{BE2} = V_T \ln\left(\frac{I_{S2}}{I_{S1}}\right) = I \times R_{2b}$$

$$\Rightarrow I = \frac{V_T}{R_{2b}} \ln\left(\frac{I_{S2}}{I_{S1}}\right)$$



- ◆ I is independent of V_{CC}
- ◆ I is directly PTAT, **p**roportional **t**o **a**bsolute **t**emperature

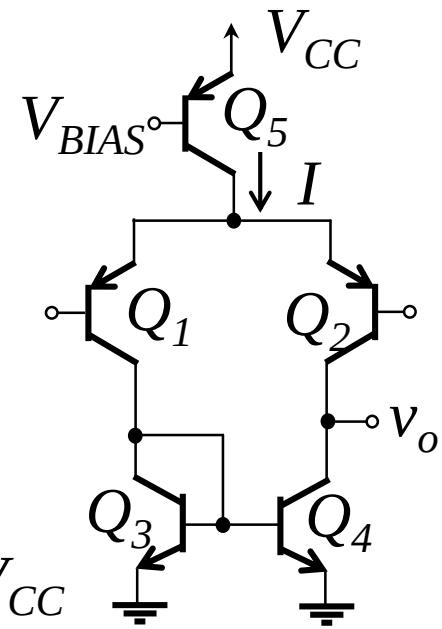
  Mirrored transistors' $g_m = \frac{I}{V_T}$ are independent of temperature

Input Stage Design

- With active load

$$V_{EC1} > |V_{ECsat}| \approx 0.1\ V$$

$$V_{ICM\min} = V_{C1} - 0.6 = V_{BE3} - 0.6 = 0.1$$



- With passive load
  - $V_{ICM\min} = V_{R_C} - 0.6$

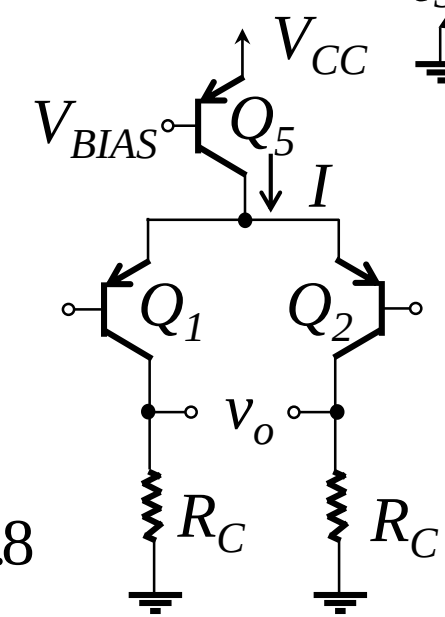
    if V_{R_C} is selected to 0.2V ~ 0.3V

    $\rightarrow V_{ICM\min}$ will be -0.4V ~ -0.3V
  - Differential gain is degraded

$$A = -g_{m1,2}R_C = -\frac{I/2}{V_T}R_C = -\frac{V_{R_C}}{V_T}$$

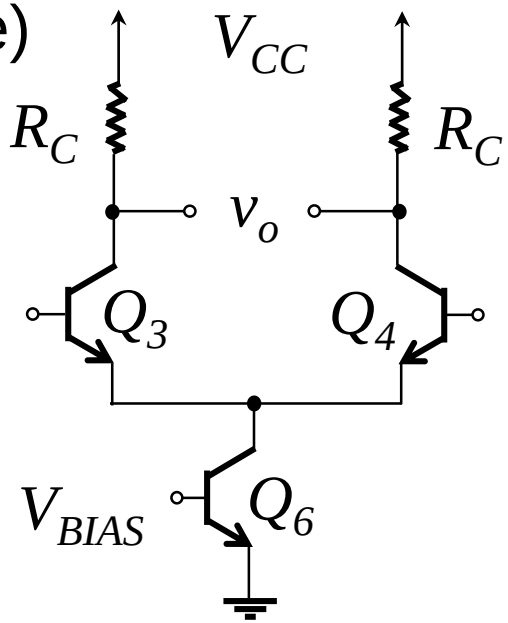
  - $V_{ICM\max} = V_{CC} - |V_{ECsat}| - V_{EB1}$

$$= V_{CC} - 0.1 - 0.7 = V_{CC} - 0.8$$



Input Stage Design (Cont.)

- Assume that $V_{R_C} = 0.3V$
  - For pnp differential-pair (previous page)
    $-0.3 \leq V_{ICM} \leq V_{CC} - 0.8$
  - For npn differential-pair (right figure)
    $0.8 \leq V_{ICM} \leq V_{CC} + 0.3$



- Connecting the two circuits in parallel
  - A rail-to-rail V_{ICM} range
    $-0.3 \leq V_{ICM} \leq V_{CC} + 0.3$
  - For the overlap region $0.8 \leq V_{ICM} \leq V_{CC} - 0.8$, both pnp and npn circuits are active

    → higher effective transconductance (X2) → higher gain
- Adding a folded-cascode stage can also increase gain

Common-Mode Feedback (CMF)

- Without CMF

  Two mismatched BJT-pairs, i.e. (Q_9 - Q_{10}) and (Q_7 - Q_8)

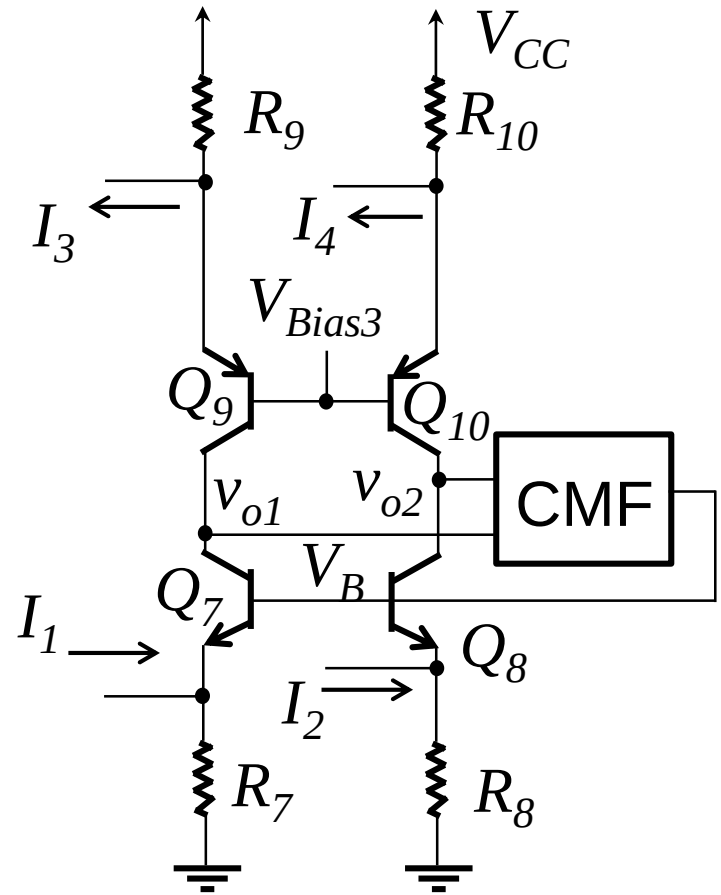
  → An increment ΔI will be multiplied by large R_{out}

  → Large changes at v_{o1} & v_{o2}

  → One set of BJT-pair saturates

- With CMF
  - ◆ It ensures $Q_{7,8}$ remain active
  - ◆ V_{CM} is regulated

    if $V_{CM}\uparrow \Rightarrow V_B\uparrow \Rightarrow I_{7,8}\uparrow \Rightarrow V_{CM}\downarrow$



CMF Circuit Configuration

$$V_{CM} = (v_{o1} + v_{o2})/2$$

$$v_{o1} = V_{CM} + \frac{v_d}{2}$$

$$v_{o2} = V_{CM} - \frac{v_d}{2}$$

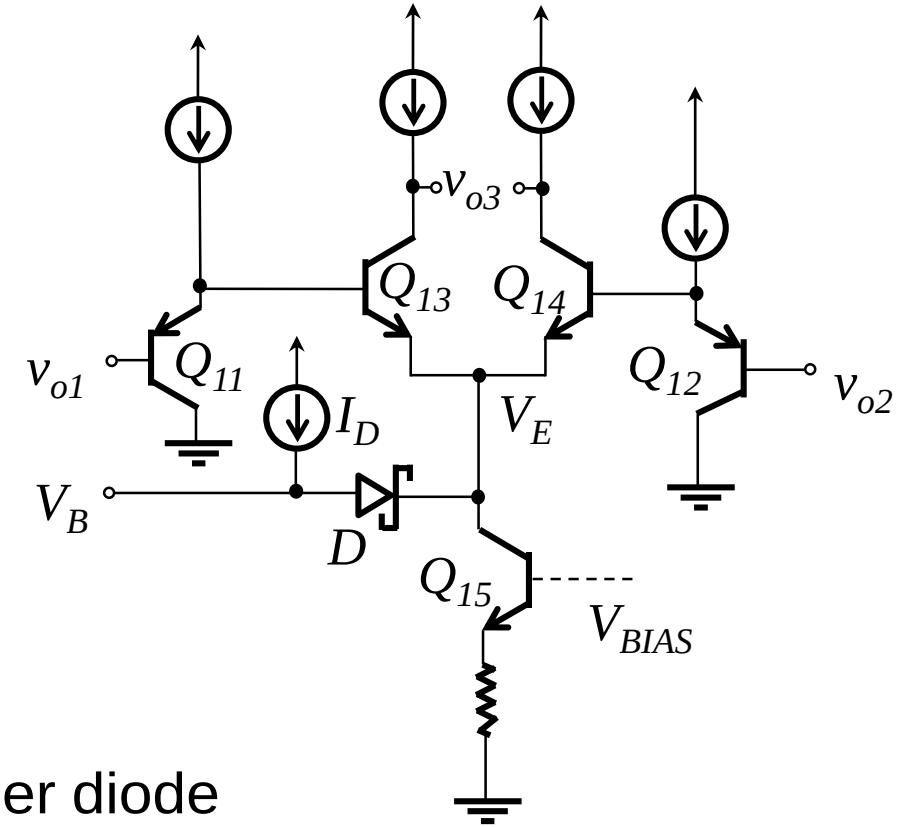
$Q_{11} \sim Q_{14}$ act as emitter followers

$$V_E = V_{CM} + V_{EB11,12} - V_{EB13,14}$$

$$\approx V_{CM}$$

$$\Rightarrow V_B = V_E + V_D = V_{CM} + 0.4$$

V_D : Voltage drop of Schottky barrier diode



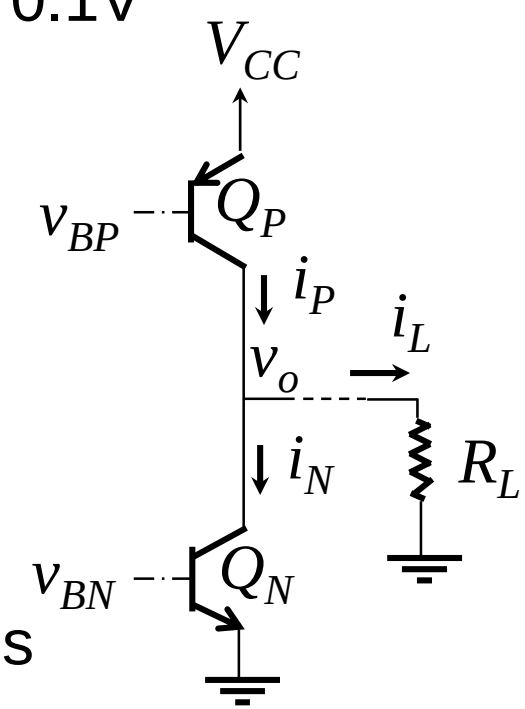
Output Stage with Near Rail-to-Rail Output Swing

- Classical emitter-follower-based class AB output stage would consume too much supply voltage

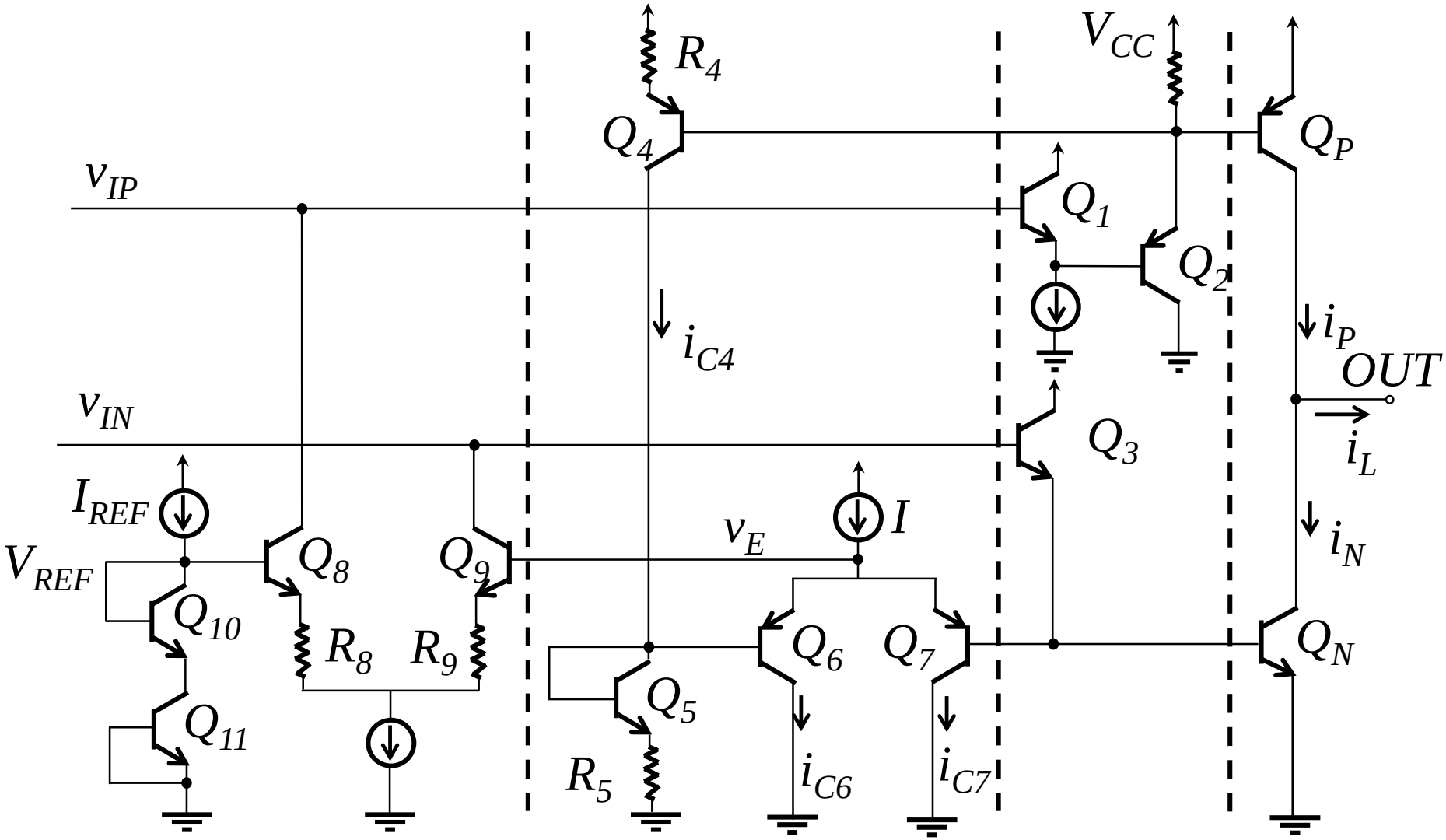
  → Smaller output-swing range
- Utilizing a pair of common-emitter transistors

  → 0.1V ≈ $V_{CENsat} \le v_O \le V_{CC} - V_{CEPsat} \approx V_{CC}$ - 0.1V
- When v_{BP} and v_{BN} are high
  - ◆ Q_N supplies the load current
  - ◆ Q_P is inactive

    To minimize crossover distortion, Q_P is forced to bias at about $I_Q/2$ instead of being turned-off
- The similar but opposite behavior happens when v_{BP} and v_{BN} are low



Full Version of the Output Stage



Feedback control of i_N and i_P

Measuring the relative Value of i_N and i_p

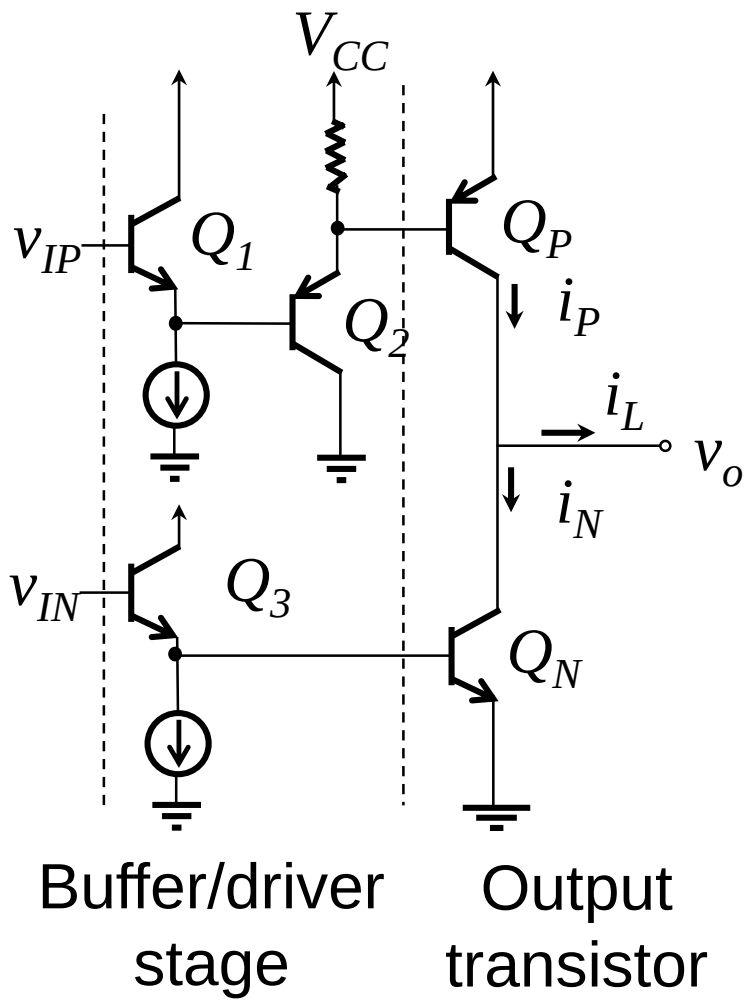
Buffer/driver

Output transistor

Buffer/Driver Stage

- Q_P and Q_N may need to supply large load current
  → Base currents of Q_P and Q_N will be substantial since $\beta_P \approx 10$ and $\beta_N \approx 40$
  → Driver stages are added

  - ◆ Q_3 is used to drive Q_N
  - ◆ Q_1 and Q_2 are used to drive Q_P because of the low β_P



Output-Stage Current Sensing

assume $R_4 = R_5$ and $\dfrac{I_{SP}}{I_{S4}} = \dfrac{I_{SN}}{I_{S5}}$

$$v_{B6} = v_{BE5} + i_{C4}R_5 = v_{BE5} + i_{C4}R_4$$

$$= v_{BE5} + v_{BEP} - v_{BE4}$$

$$= V_T \ln\left(\frac{i_{C4}}{I_{S5}} \cdot \frac{i_P}{I_{SP}} \cdot \frac{I_{S4}}{i_{C4}}\right)$$

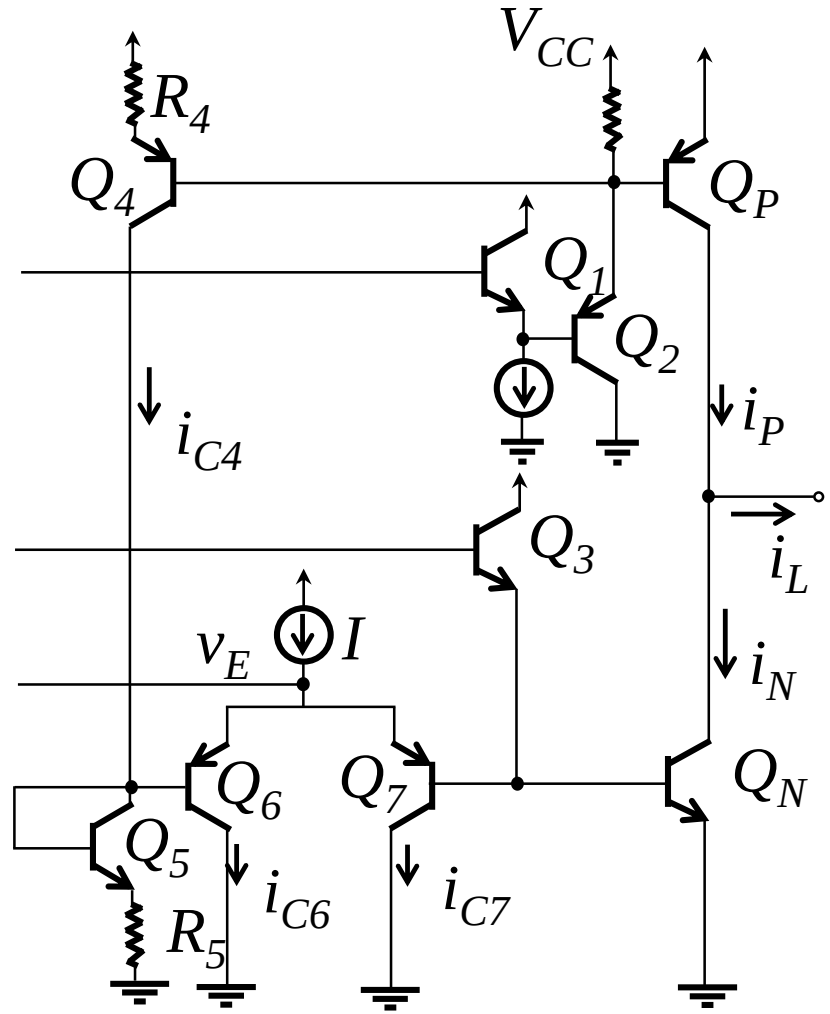
$$= V_T \ln\left(\frac{i_P}{I_{SN}}\right)$$

$$v_E = v_{B6} + v_{BE6} = v_{B7} + v_{BE7}$$

$$\Rightarrow \frac{i_P}{I_{SN}} \cdot \frac{i_{C6}}{I_{S6}} = \frac{i_N}{I_{SN}} \cdot \frac{i_{C7}}{I_{S7}}$$

assume $I_{S6} = I_{S7} \Rightarrow i_P \cdot i_{C6} = i_N \cdot i_{C7}$

$$i_{C6} = I \cdot \frac{i_N}{i_P + i_N} \quad \text{and} \quad i_{C7} = I \cdot \frac{i_P}{i_P + i_N}$$



Output-Stage Current Sensing (Cont.)

since $i_{C6} = I \cdot \dfrac{i_N}{i_P + i_N}$ and $i_{C7} = I \cdot \dfrac{i_P}{i_P + i_N}$

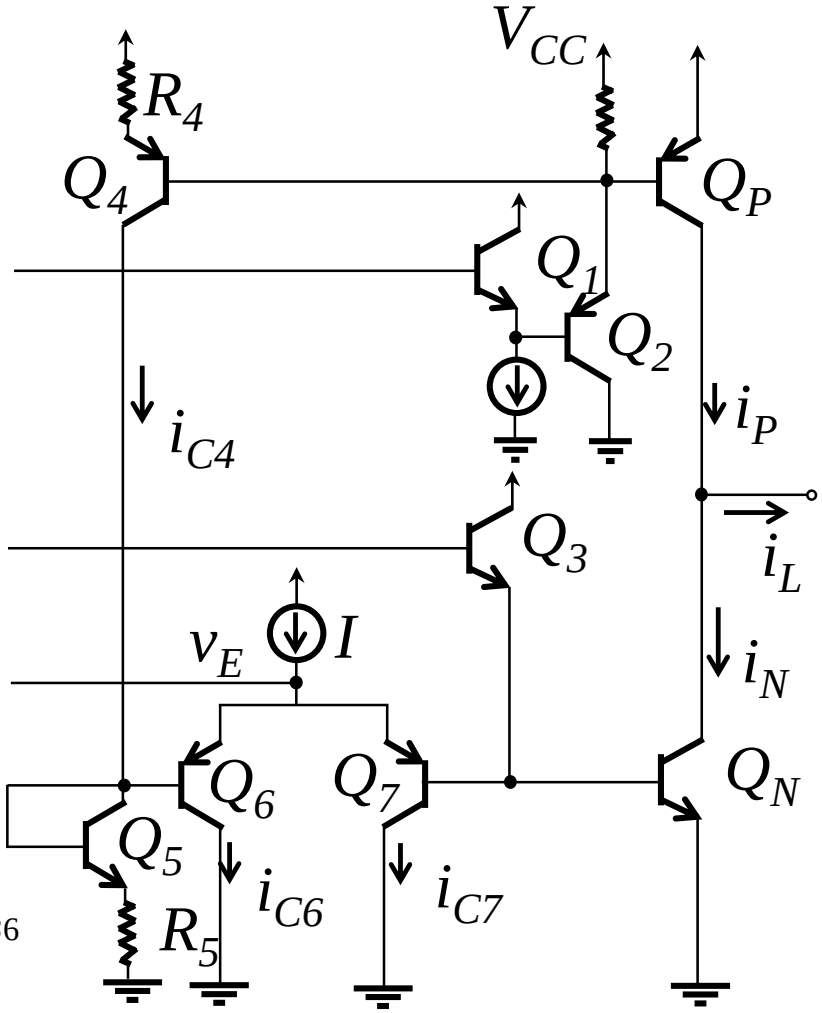
$$v_E = v_{B7} + v_{BE7} = V_T \ln\left(\frac{i_N}{I_{SN}} \cdot \frac{i_{C7}}{I_{S7}}\right) v_E$$

$$= v_{B7} + v_{BE7} = V_T \ln\left(\frac{i_N}{I_{SN}} \cdot \frac{i_{C7}}{I_{S7}}\right)$$

$$= V_T \ln\left(\cdot \frac{i_P \cdot i_N}{i_P + i_N} \cdot \frac{I}{I_{SN} I_{S7}}\right)$$

if $i_P >> i_N \Rightarrow v_E = V_T \ln\left(\dfrac{i_N}{I_{SN}}\right) + V_{EB7}$

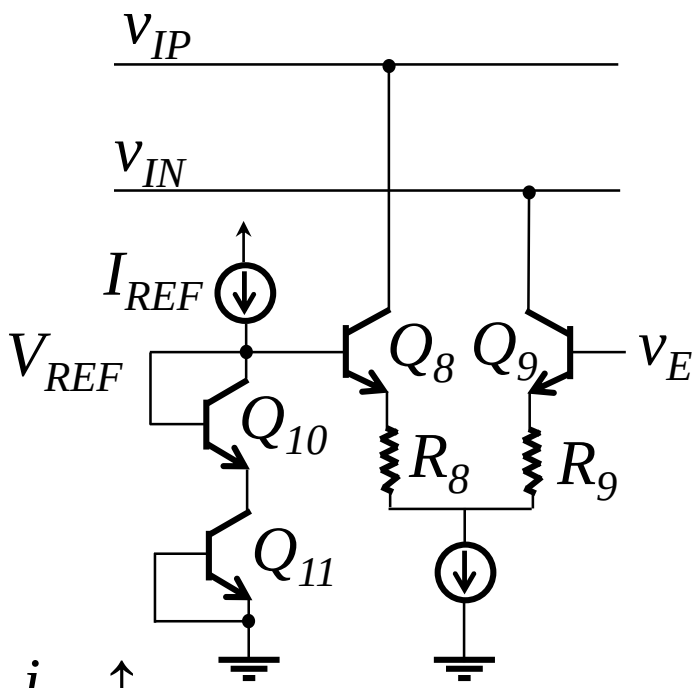
similarly, if $i_P << i_N \Rightarrow v_E = V_T \ln\left(\dfrac{i_P}{I_{SN}}\right) + V_{EB6}$



- v_E is determined by the current of inactive transistor

Feedback for the Current of Inactive Transistor

- for $i_P >> i_N$
  - ◆ Q_N is the inactive transistor
  - ◆ If i_N is too small $\Rightarrow v_E \downarrow \Rightarrow i_{C9} \downarrow$
    $\Rightarrow v_{IN} \uparrow \Rightarrow i_N \uparrow$



- for $i_P << i_N$
  - ◆ Q_P is the inactive transistor
  - ◆ If i_P is too small $\Rightarrow v_E \downarrow \Rightarrow i_{C9} \downarrow \Rightarrow i_{C8} \uparrow$
    $\Rightarrow v_{IP} \downarrow \Rightarrow i_{C1} \downarrow \Rightarrow i_{C2} \uparrow \Rightarrow i_P \uparrow$

$\rightarrow$ Minimum current of inactive transistor is maintained

Minimum Current in the Inactive Output Transistor

- Assume the loop gain is high enough

since $v_E = V_T \ln\left(\frac{i_P \cdot i_N}{i_P + i_N} \cdot \frac{I}{I_{SN} I_{S7}}\right)$

and $v_E = V_{REF} = V_T \ln\left(\frac{I_{REF}}{I_{S10}}\right) + V_T \ln\left(\frac{I_{REF}}{I_{S11}}\right)$

$$\Rightarrow \frac{i_P \cdot i_N}{i_P + i_N} = \left(\frac{I_{REF}^2}{I}\right)\left(\frac{I_{SN}}{I_{S10}}\right)\left(\frac{I_{S7}}{I_{S11}}\right)$$

In the quiescent case, $i_P = i_N = I_Q$

$$\Rightarrow I_Q = 2\left(\frac{I_{REF}^2}{I}\right)\left(\frac{I_{SN}}{I_{S10}}\right)\left(\frac{I_{S7}}{I_{S11}}\right) \Rightarrow \frac{i_P \cdot i_N}{i_P + i_N} = \frac{1}{2} I_Q$$

$$\Rightarrow \begin{cases} i_P \approx 0.5 \cdot I_Q & \text{for } i_N >> i_P \\ i_N \approx 0.5 \cdot I_Q & \text{for } i_N << i_P \end{cases}$$