

Electronics(3) Homework1

For an OPAMP with $V_{DD} = 3.3V$ and input common-mode voltage(V_{CM})= $\frac{V_{DD}}{2}$, the MOSFET model parameters are listed in **page B-9** of Appendix B on Smith's CD.

(1) As shown in Fig. 1, please calculate $\frac{v_o}{v_{id}}(s)$ with its DC gain and pole locations, where $v_{id}=v_{in}^+-v_{in}^-$. (refer to Sections 8.5.3 and 9.7.2 in textbook). Then verify your results by PSpice with **0.5 μ m CMOS model** (in sedra_lib.lib).

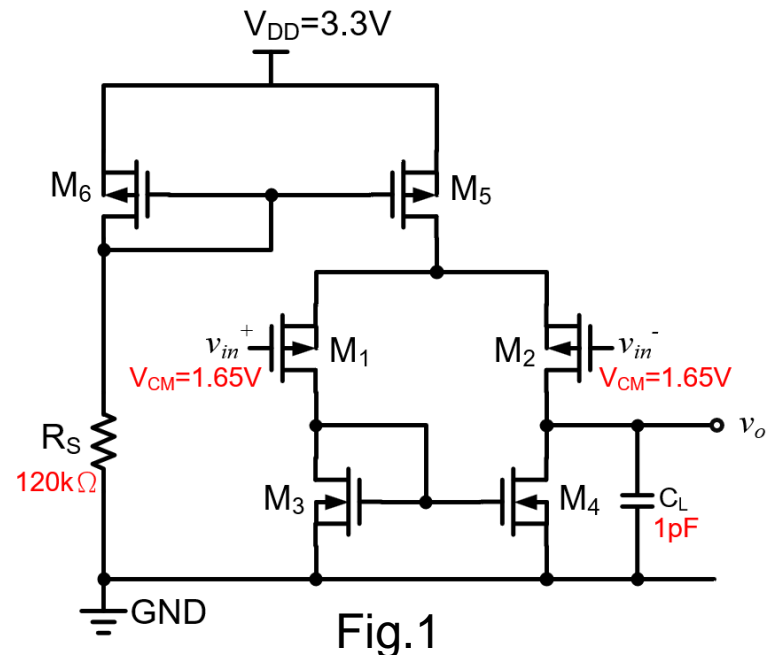
The sizes of all MOSFETs are listed below.

$$(W/L)_{M1,M2} = 10\mu\text{m}/0.5\mu\text{m}$$

$$(W/L)_{M3,M4} = 3\mu\text{m}/0.5\mu\text{m}$$

$$(W/L)_{M5} = 5\mu\text{m}/0.5\mu\text{m}$$

$$(W/L)_{M6} = 2\mu\text{m}/0.5\mu\text{m}$$



Electronics(3) Homework1

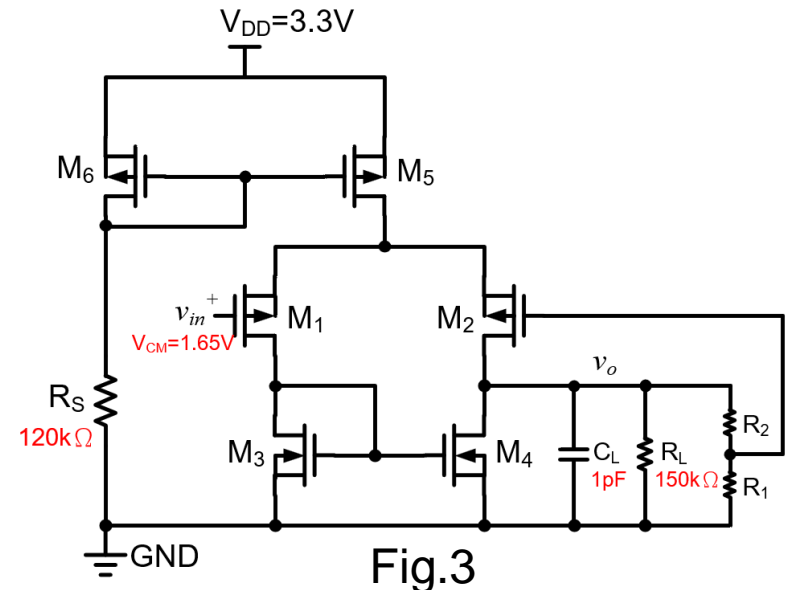
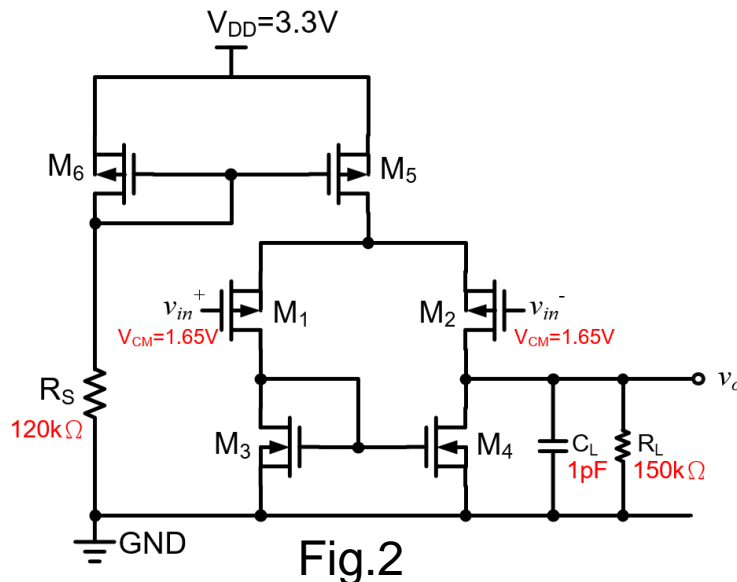
(2) As shown in Fig. 2, for a given resistive load R_L of $150\text{k}\Omega$, please calculate $\frac{v_o}{v_{id}}(s)$ with its DC gain and pole locations. Then verify your results by PSpice.

(3) In Fig. 3, assume that $R_1 + R_2 = R_L$ ($120\text{k}\Omega$) and $(R_2/R_1) = (X+1)/30$, where X is the last number of your student ID. Find the loop gain $\beta A(s)$ with its DC gain and pole locations. Then verify your results by PSpice.

(Example: E24032119 $\rightarrow X = 9 \rightarrow R_2/R_1 = 10/30 \rightarrow R_1 = 90\text{k}\Omega$, $R_2 = 30\text{k}\Omega$)

<Hint> You have to **break the feedback loop** to find $\beta A(s)$ (refer to section 10.4.2)

(4) Please **show** the common-mode voltages of v_o in Figs. 1, 2, and 3, and explain the reasons for their difference.



Notes

- When verifying your hand calculation by PSpice
 - ◆ Correct the value of LAMBDA for NMOS0P5 to 0.1 (the same as in page B-9 of Appendix B on Sedra's CD)
 - ◆ Use 4-terminal MOSFET models (NMOS0P5_BODY and PMOS0P5_BODY)
 - ◆ Clearly mark the verification results(DC gain, pole locations...) on Bode plots
- **Upload your report to MOODLE in Word format**
 - ◆ Your report should include
 - Hand calculation progress
 - PSpice schematic graphs
 - PSpice verification results (i.e Bode plots)
 - ◆ Deadline: **23:59:59 on 09/24/2025(Wed.)** (遲交一天原則上扣 5 分)
 - ◆ Filename example: HW1_劉奕均_E2409XXXX_v1.doc (如有更新請用 v2,v3...)
 - ◆ 檔案應小於**2MB**, 若有特殊需求可向助教提出

Notes (Cont.)

● Others

- ◆ 作業題目下載: <http://msic.ee.ncku.edu.tw/ch.html>
(IC設計課程→大學部課程→電子學(三))
- ◆ 作業繳交: <http://moodle.ncku.edu.tw/>
- ◆ 請勿抄襲，抄襲等同考試作弊，將依校規處理。
- ◆ 此次作業將佔學期成績之5%。
- ◆ 作業上若有遇到問題可於下列時段至奇美樓 95302室。
 - 原定office hours: 每週一17:00~18:00 and 每週四18:00~19:00
 - 新增時段: 09/12/2025(Fri.) and 09/19/2025(Fri.) 16:00~17:00
- ◆ 手算過程若為掃描圖檔務必清晰並轉正以利助教判讀
- ◆ Word format
 - 字體12pt、單行間距、中英文字體分別為標楷體與Times New Roman
 - 頁碼置中於頁尾、各邊界2.54公分 (上下邊界可依內容量縮減，但不得小於1.28公分)
 - 分別在每個繪圖下方與表格上方依序編號，並輔以caption描述
 - 圖表中的字體不小於10pt，尤其注意驗證波形圖的座標值
 - 驗證波形圖以白色為底，且重要驗證結果應清楚標記

PSpice Tutorial for Homeworks

- PSpice Installation
- New a Project
- Create a Schematic Graph
- Circuit Analysis
 - ◆ AC Sweep Analysis
 - ◆ Transient Analysis

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Password*

.....

Show

- ✓ Must be between 8 and 30 characters long.
- ✓ At least 1 uppercase (A-Z) and 1 lowercase (a-z) character.
- ✓ At least one digit (0-9).
- ✓ Must not contain a space.
- ✓ Must not contain parts of your username, does not include your first name, does not include your last name.
- ✓ Must contain at least one symbol. Allowed symbols - !#\$%&`()*+,-./\:;<=>?@[^_`~{ }~

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Yu Cheng

Last name *

Cheng

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外籍生：學生證後四碼+生日月日四碼(mmdd)
密碼過期:請點選[\[忘記密碼\]](#)重新設定


[忘記密碼](#)

First login

Default password: Last 4 digits of ID + 4 digits of date of birth
International student: Last 4 digits of student ID + 4 digits of date of birth (mmdd)

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- Upload some proven file



We need your ID & class schedule

Your documents must include:

- Your **full name** as entered into this form
- The full or abbreviated **academic institution name** or logo
- **Date** within the current academic year OR no more than 90 days from today's date

Add documents

Suggested document types ^


- School ID card with expiration date
- Class schedule
- Tuition receipt
- File must be .jpg .jpeg .png .pdf

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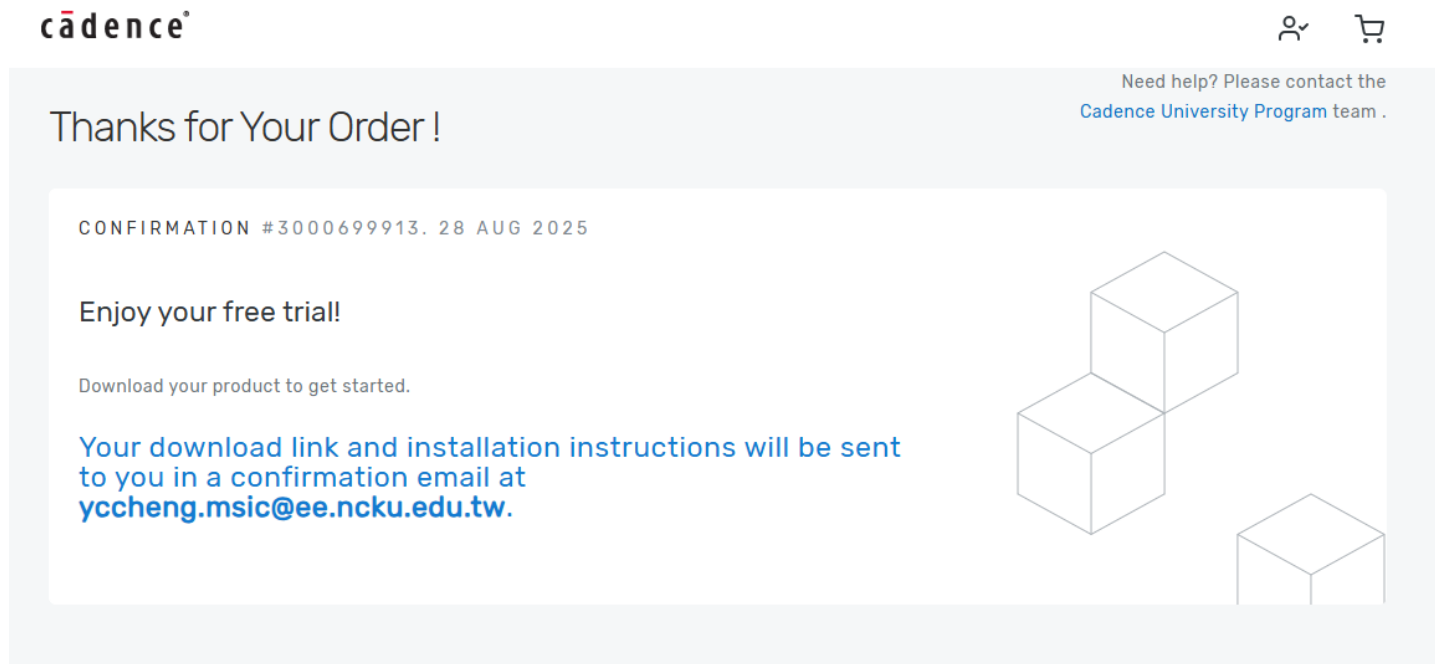
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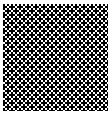
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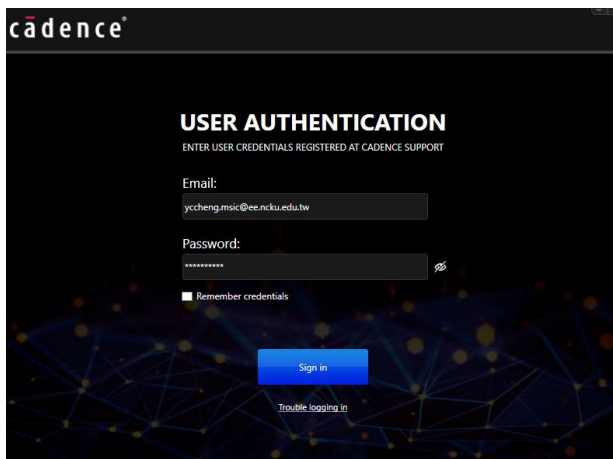
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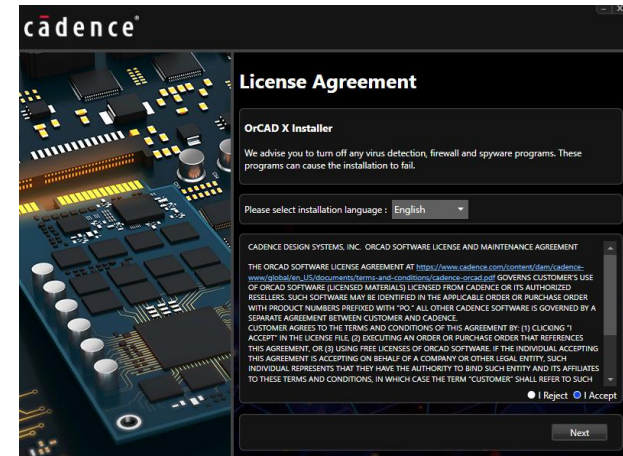
- Install software

名稱	修改日期	類型	大小
✓ 今天			
 OrCADXInstall	8/28/2025 10:13 AM	應用程式	8,434 KB

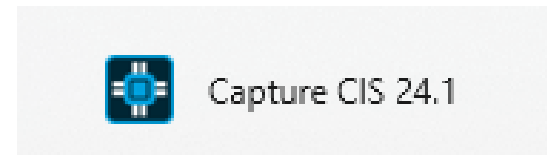
- Authentication



- License agreement

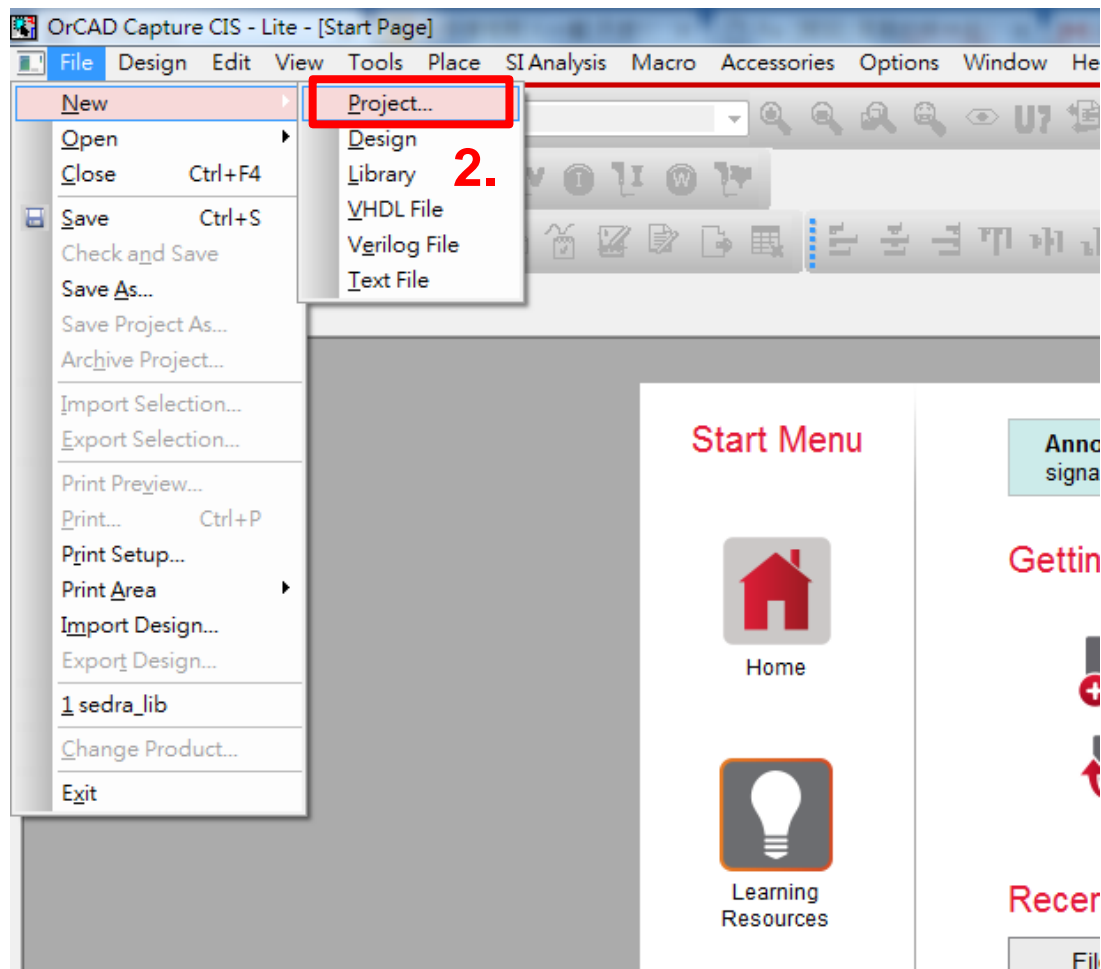
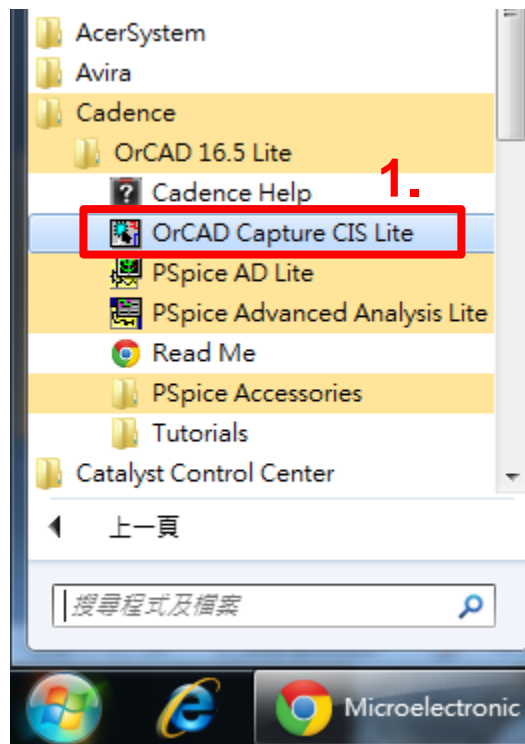


- After finished installation, open Capture CIS 24.1 software

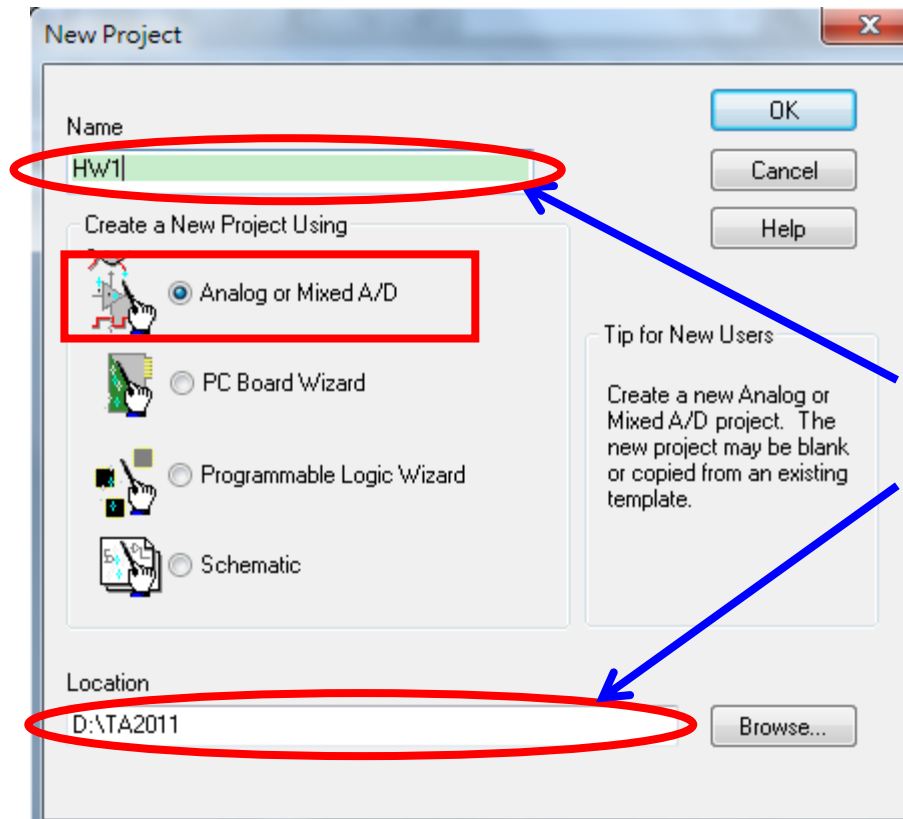


New a Project

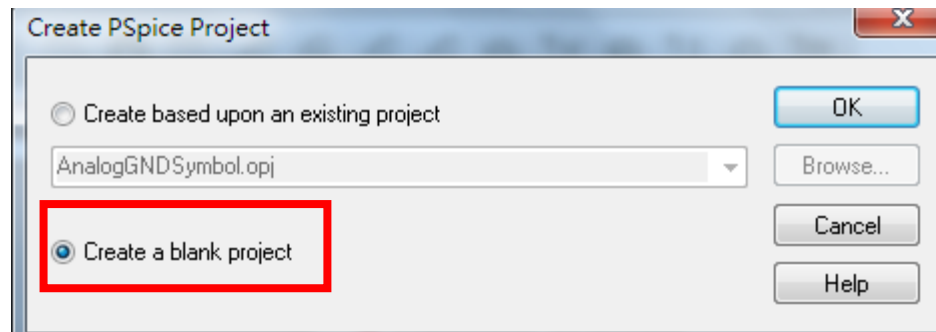
- Start the program and New a project



New a Project (Cont.)

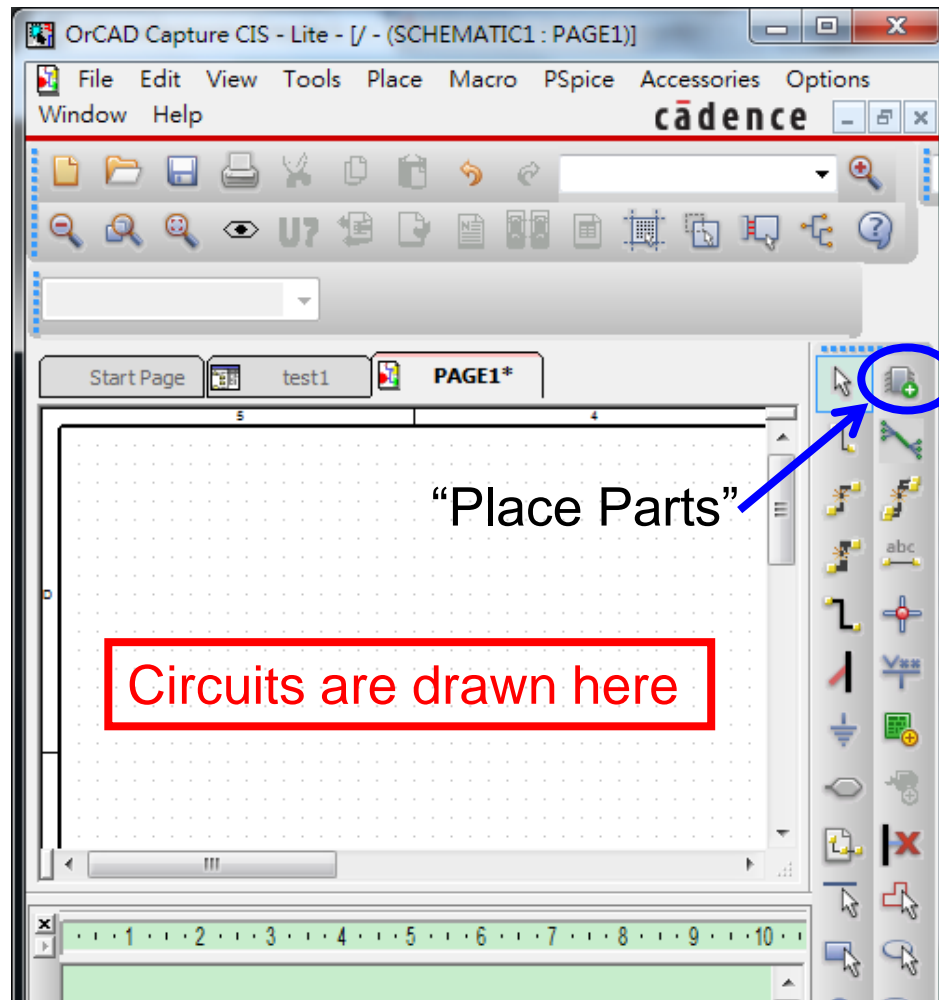


No Chinese while setting “Name” and “Location”



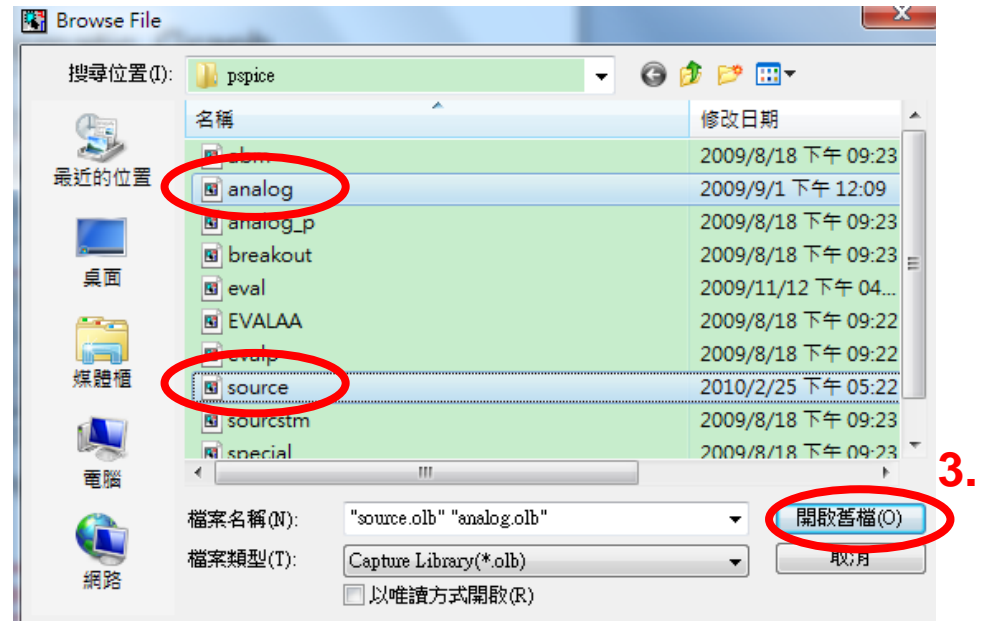
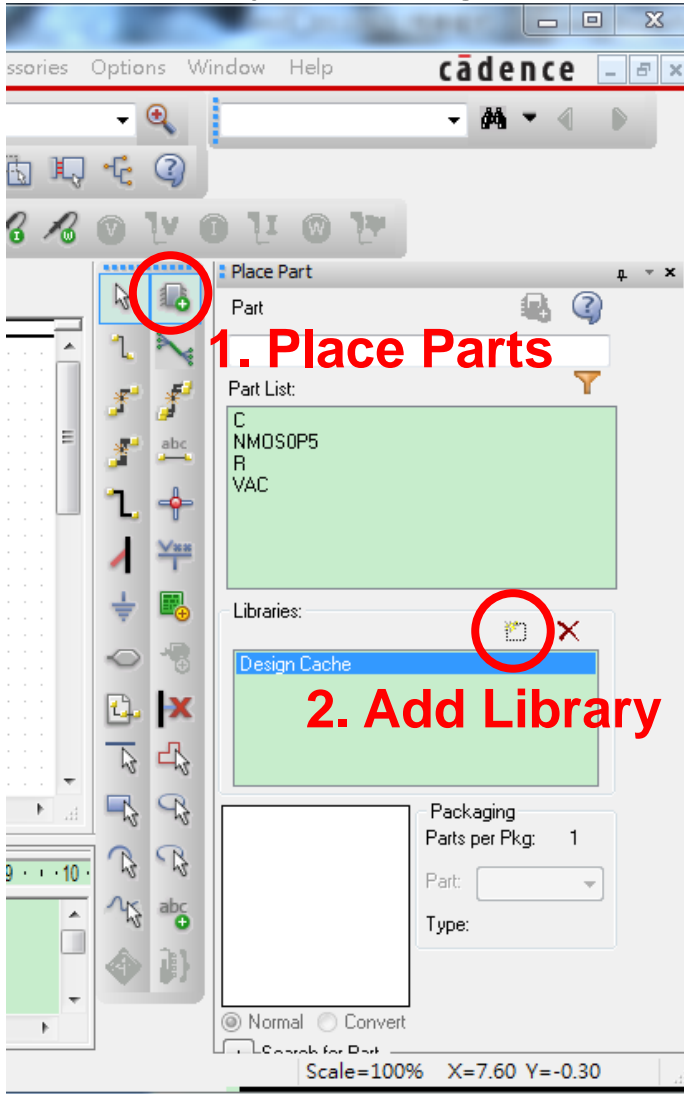
Create a Schematic Graph

- Project and blank schematic are NEWed
 - ◆ Going to place parts on the blank schematic



Place Parts

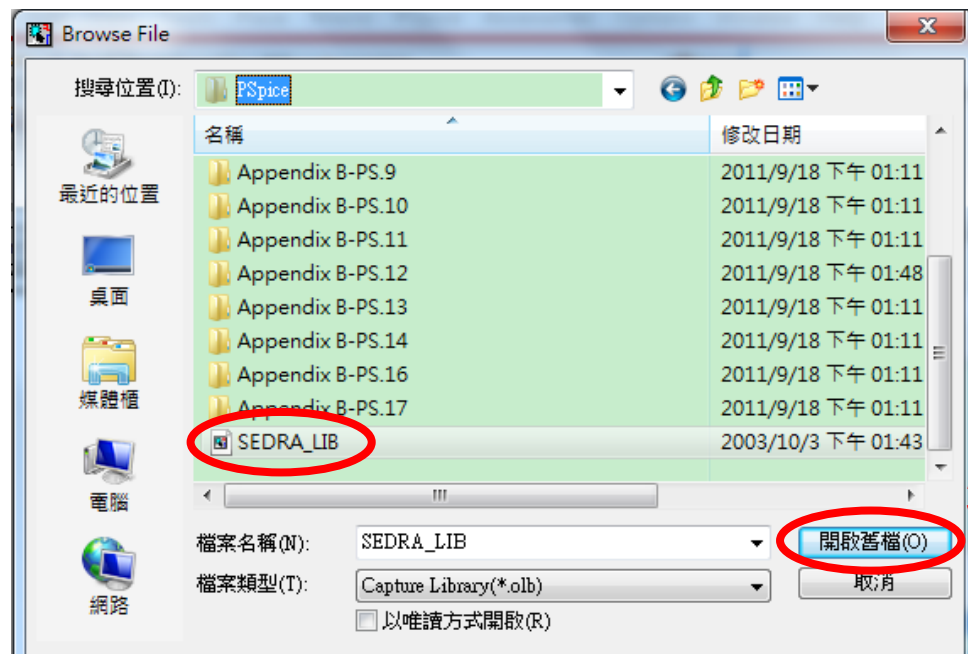
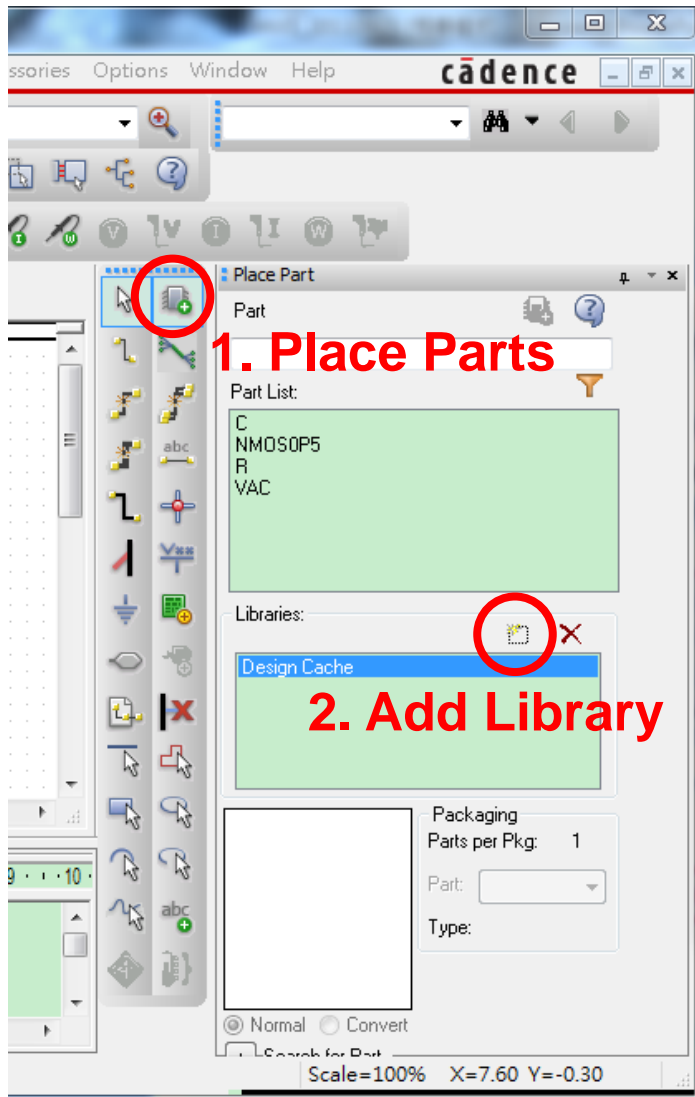
- Add library: “analog.olb” and “source.olb” @ C:\OrCAD\OrCAD_17.2_Lite\tools\capture\library\pspice



Place Parts (Cont.)

- Add library SEDRA_LIB.olb in the “SPICE examples” file

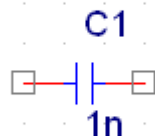
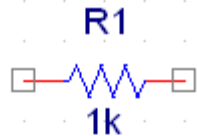
@ C:\Program Files (x86)\OUP\Sedra International 6e SPICE Simulations for Students\PSpice



Place Parts (Cont.)

- Different parts are in different .olb files
 - ◆ Frequently used components

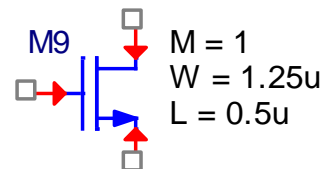
ANALOG



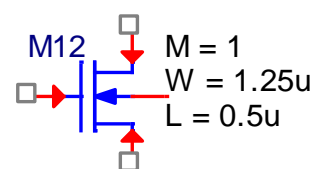
SEDRA_LIB

NMOS0P5 model

NMOS0P5

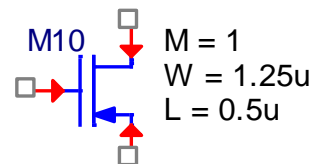


NMOS0P5_BOBY

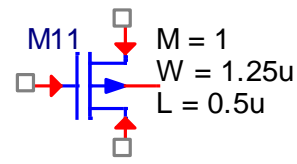


PMOS0P5 model

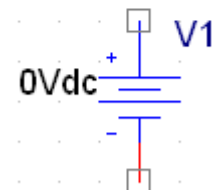
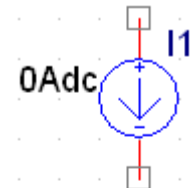
PMOS0P5



PMOS0P5_BOBY

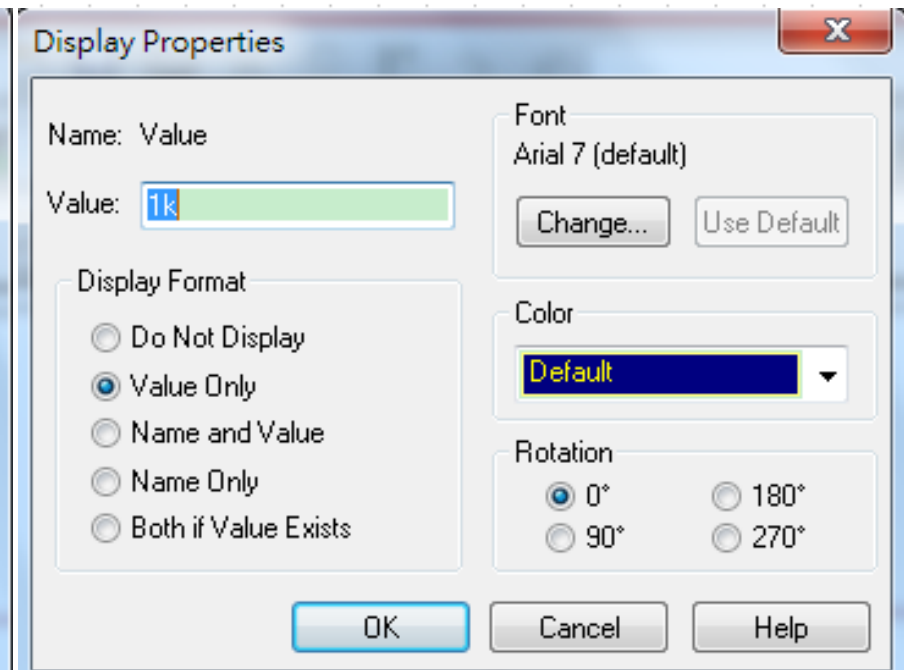
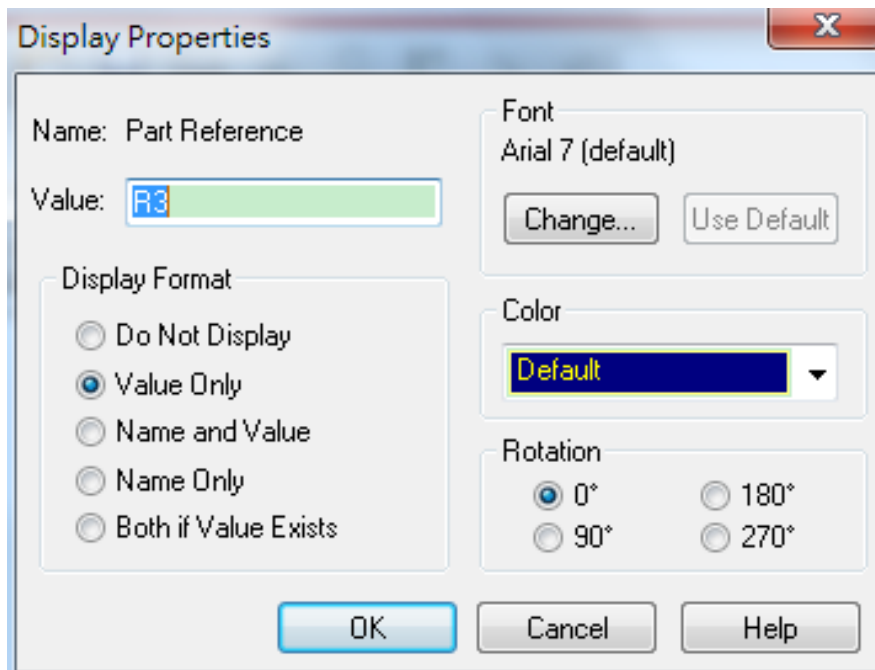
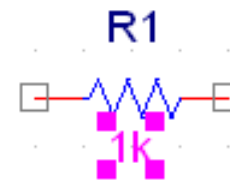
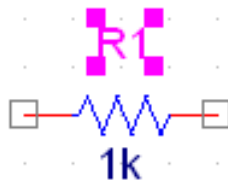


SOURCE



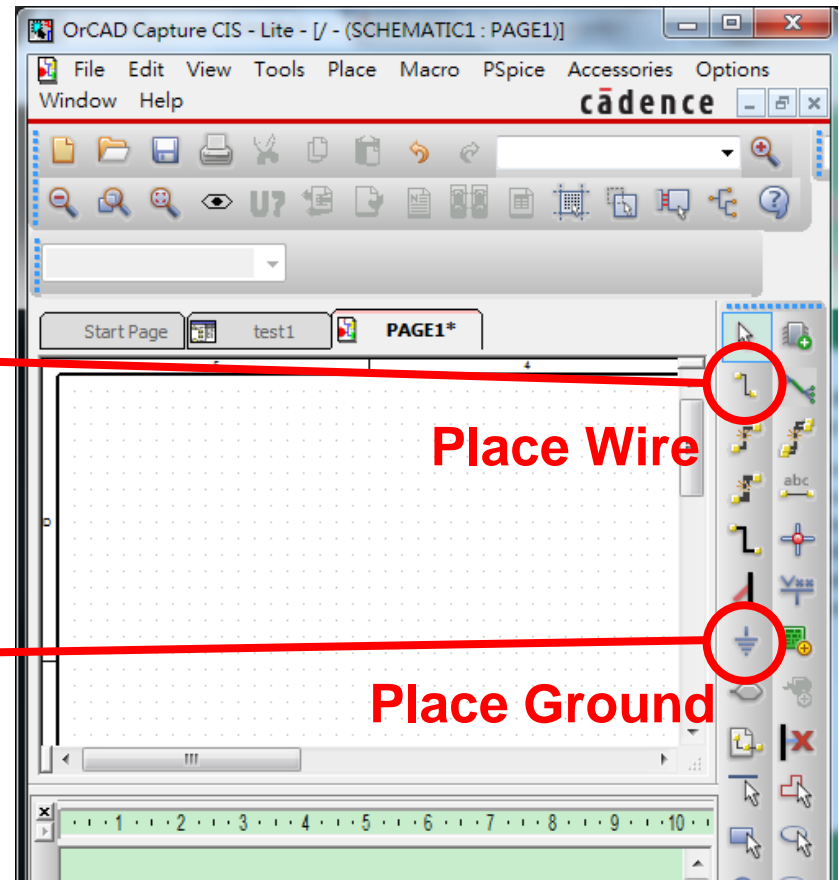
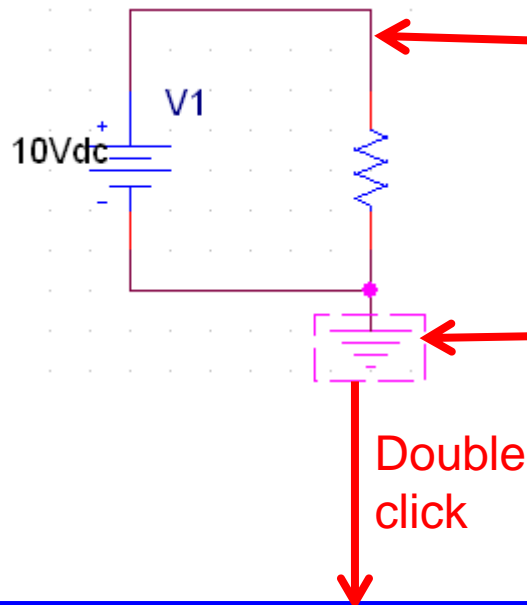
Part Properties

- Double click “R1” to edit its name
 - ◆ Same name will not be accepted while compiling (netlist generating)
- Double click “1k” to edit its resistance (capacitance for capacitor)



Wiring and Ground Setting

- Double click on the “ground” part
 - ◆ Edit the “Name” column into “0”



New Column...

Apply

Display...

Delete Property

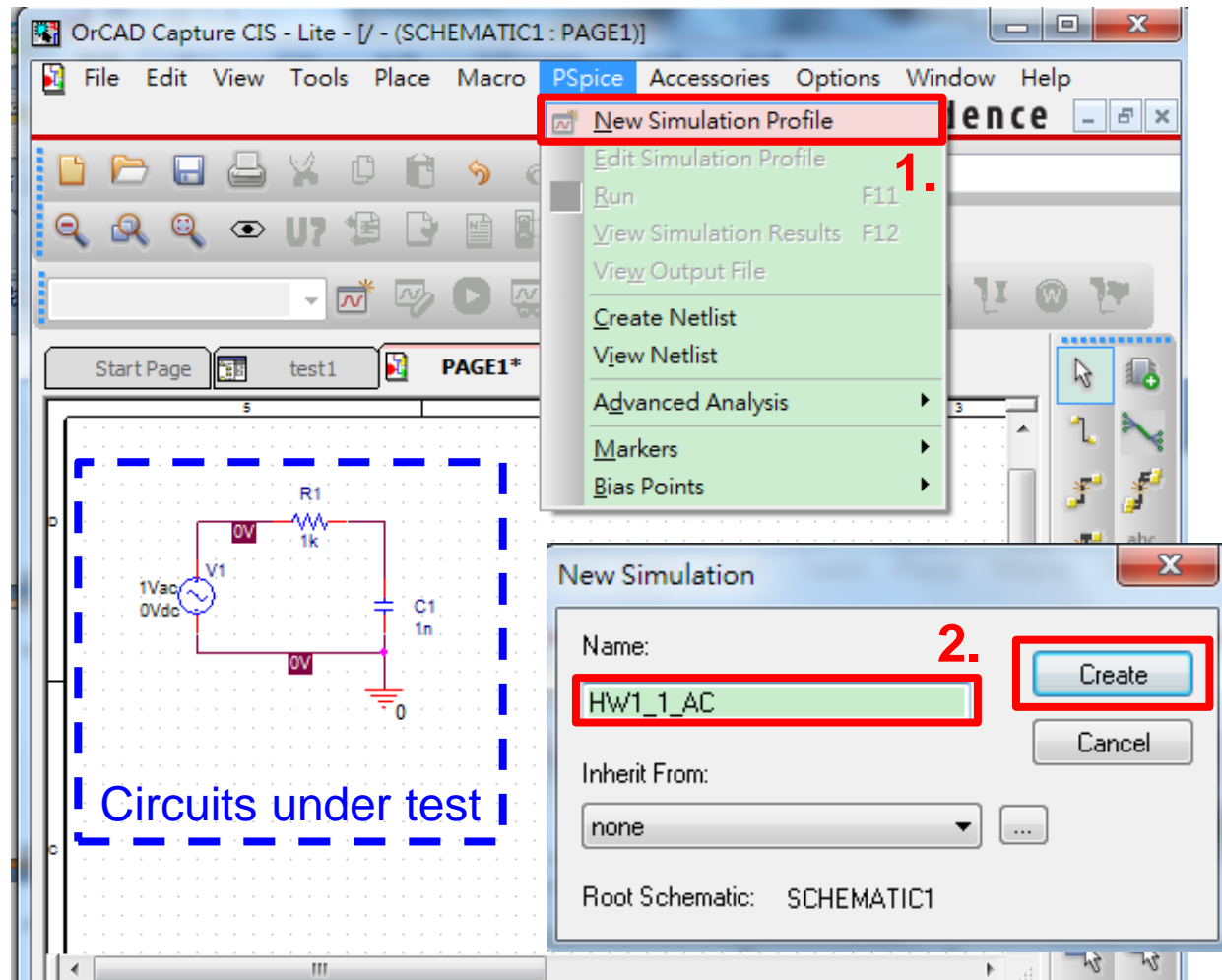
Filter by: < Current properties >

Help

		Color	Location X-Coordinate	Location Y-Coordinate	Name	NODENA
1	SCHEMATIC1 : PAGE1 : 0	Default	310	240	0	0

New Simulation Profile

- Settings before simulation



AC Sweep Analysis

The screenshot displays the OrCAD Capture CIS interface. The main workspace shows a circuit diagram with a 1Vac AC voltage source (V1), a 1k resistor (R1), and a 1nF capacitor (C1). The output voltage is labeled VOUT. A red arrow points to the AC source, and a blue arrow points to the net alias 'V'.

Simulation Settings - HW1_1_AC

Analysis type: AC Sweep/Noise

Options:

- ☒ General Settings
- ☐ Monte Carlo/Worst Case
- ☐ Parametric Sweep
- ☐ Temperature (Sweep)
- ☐ Save Bias Point
- ☐ Load Bias Point

AC Sweep Type

- ☐ Linear
- ☒ Logarithmic

Decade

Start Frequency: 1k
End Frequency: 1G
Points/Decade: 10

Noise Analysis

- ☐ Enabled
- Output Voltage:
- I/V Source:
- Interval:

Output File Options

- ☐ Include detailed bias point information for nonlinear controlled sources and semiconductors (.OP)

Buttons: 確定 (OK), 取消 (Cancel), 套用 (Apply), 說明 (Help)

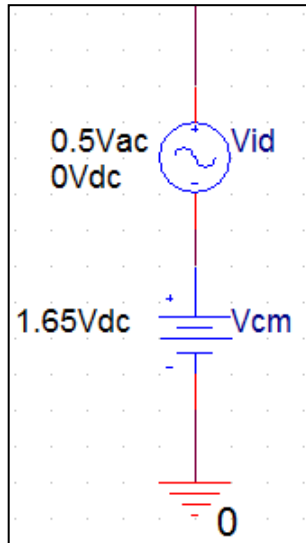
Note that VAC is necessary for AC Sweep Analysis

Place net alias

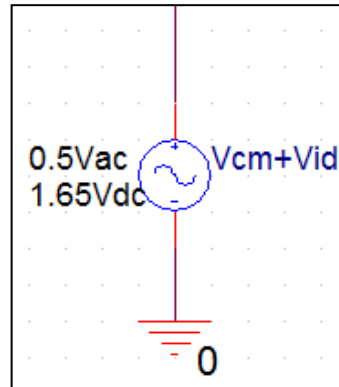
AC Sweep Analysis (Cont.)

- Three methods to place AC source V_{id} with common-mode voltage V_{cm}

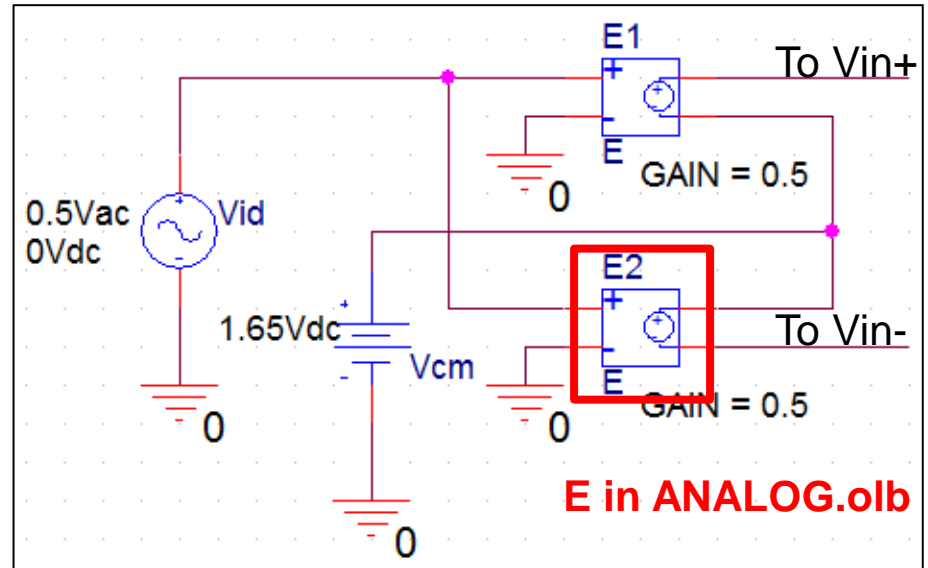
(1)



(2)



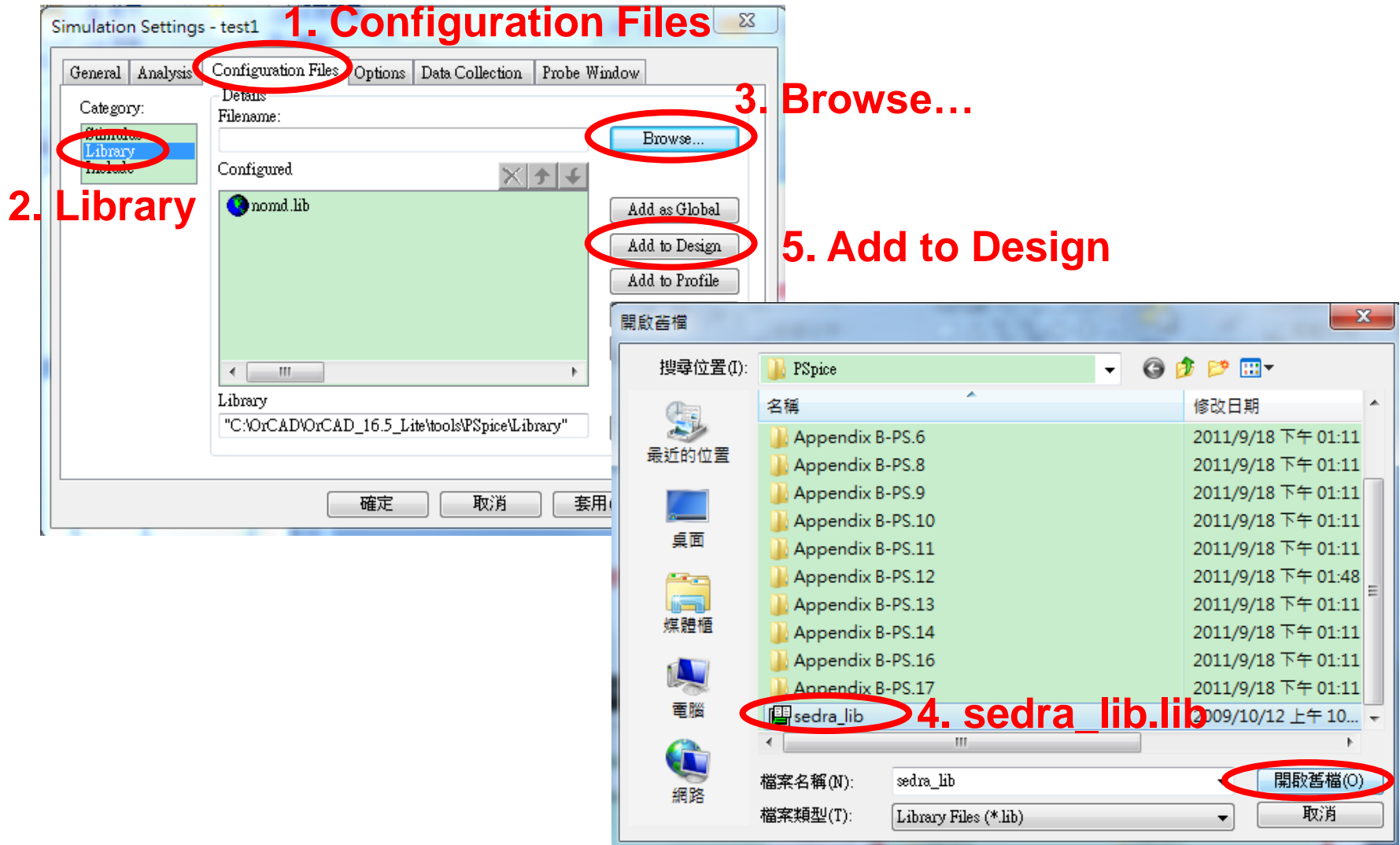
(3)



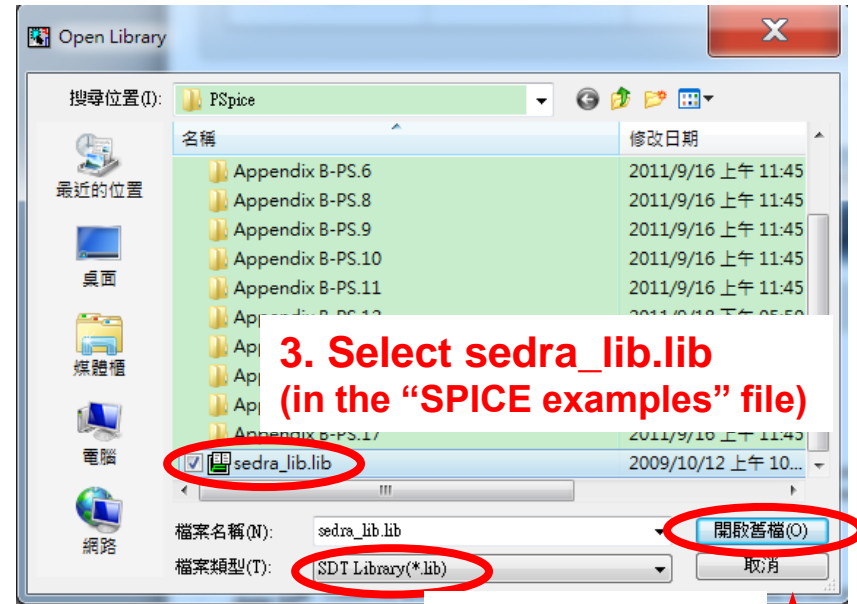
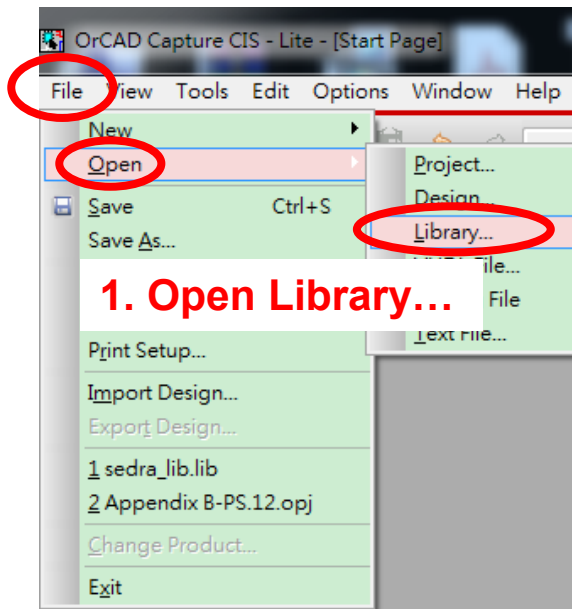
Reference: Adel S. Sedra and Kenneth C. Smith, *Microelectronic Circuits*, 6th ed. New York, Oxford Univ. Press, 2011, app. B-16

Include Sedra_lib Library

- Add the sedra_lib.lib to design (in the “SPICE examples” file)



Correct the PSpice Parameters



```

135 *      Level-1 Model for PMOS in model 0.5um CMOS Technology
136 *      (created by Anas Hamoui & Olivier Trespases)
137 .model PMOS0P5 PMOS(Level=1 VTO=0.8 GAMMA=0.45 F
138 +      LD=0.09E-06 WD=0 UO=200 LAMBDA=0.2 TOX=9.5
139 +      CJSW=170E-12 MJ=0.5 MJSW=0.35 CGDO=0.35E-9
140 +      CGSO=0.35E-9)
141 *$
142 *      Level-1 Model for NMOS in model 0.5um CMOS
143 *      (created by Anas Hamoui & Olivier Trespases)
144 .model NMOS0P5 NMOS(Level=1 VTO=0.7 GAMMA=0.5 PHI
145 +      LD=0.08E-06 WD=0 UO=680 LAMBDA=0.1 TOX=9.5
146 +      CJSW=120E-12 MJ=0.5 MJSW=0.4 CGDO=0.4E-9 J
147 +      CGSO=0.4E-9)
148 *$
    
```

4. Correct the LAMBDA of the PMOS0P5 to 0.2 @line 138 NMOS0P5 to 0.1 @line 158

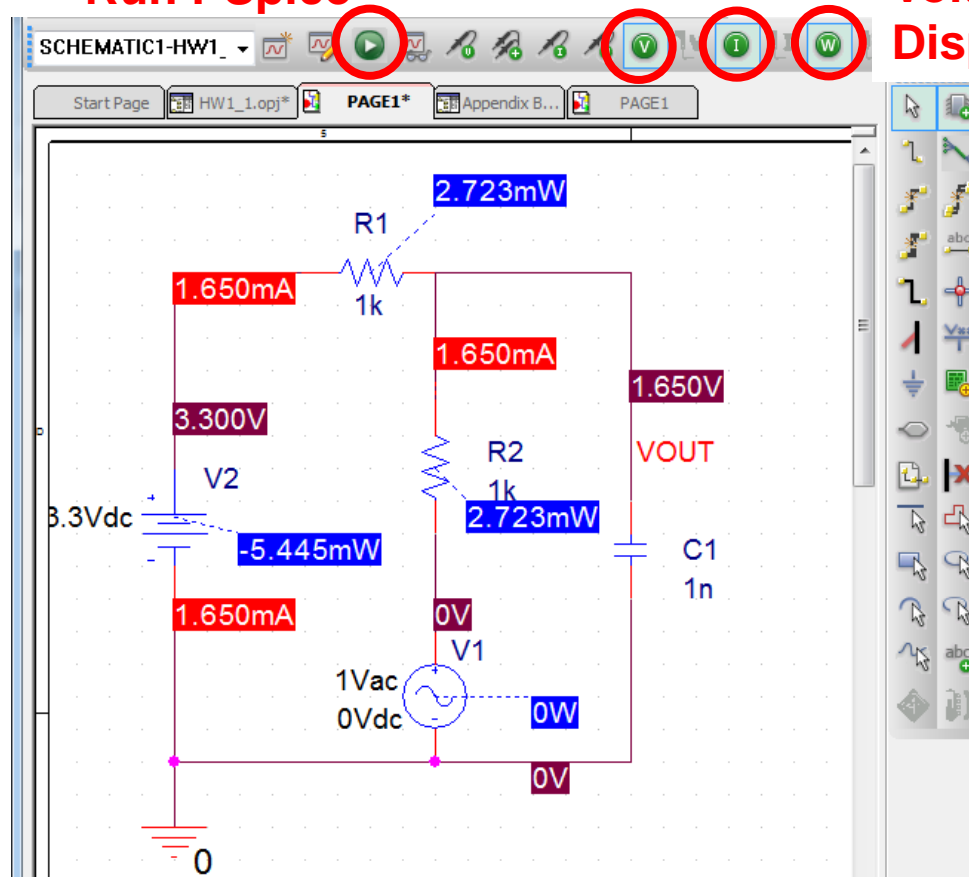
5. Correct the UO of the PMOS0P5 to 200 @line 138 NMOS0P5 to 680 @line 158

Run PSpice

- After editing the Simulation Profile
 - ◆ Run PSpice
 - ◆ Enable Bias Voltage/Current/Power Display

Run PSpice

**Enable Bias
Voltage/Current/Power
Display**



AC Sweep Analysis (Cont.)

- After “Run PSpice” → Add traces in “PSpice A/D Lite”

1. Add Trace

2. Click the needed function in right column

3. Click the variable in left column

4.

DB(): Magnitude [dB]
P(): Phase [degree]

Trace Expression: DB(V[OUT])

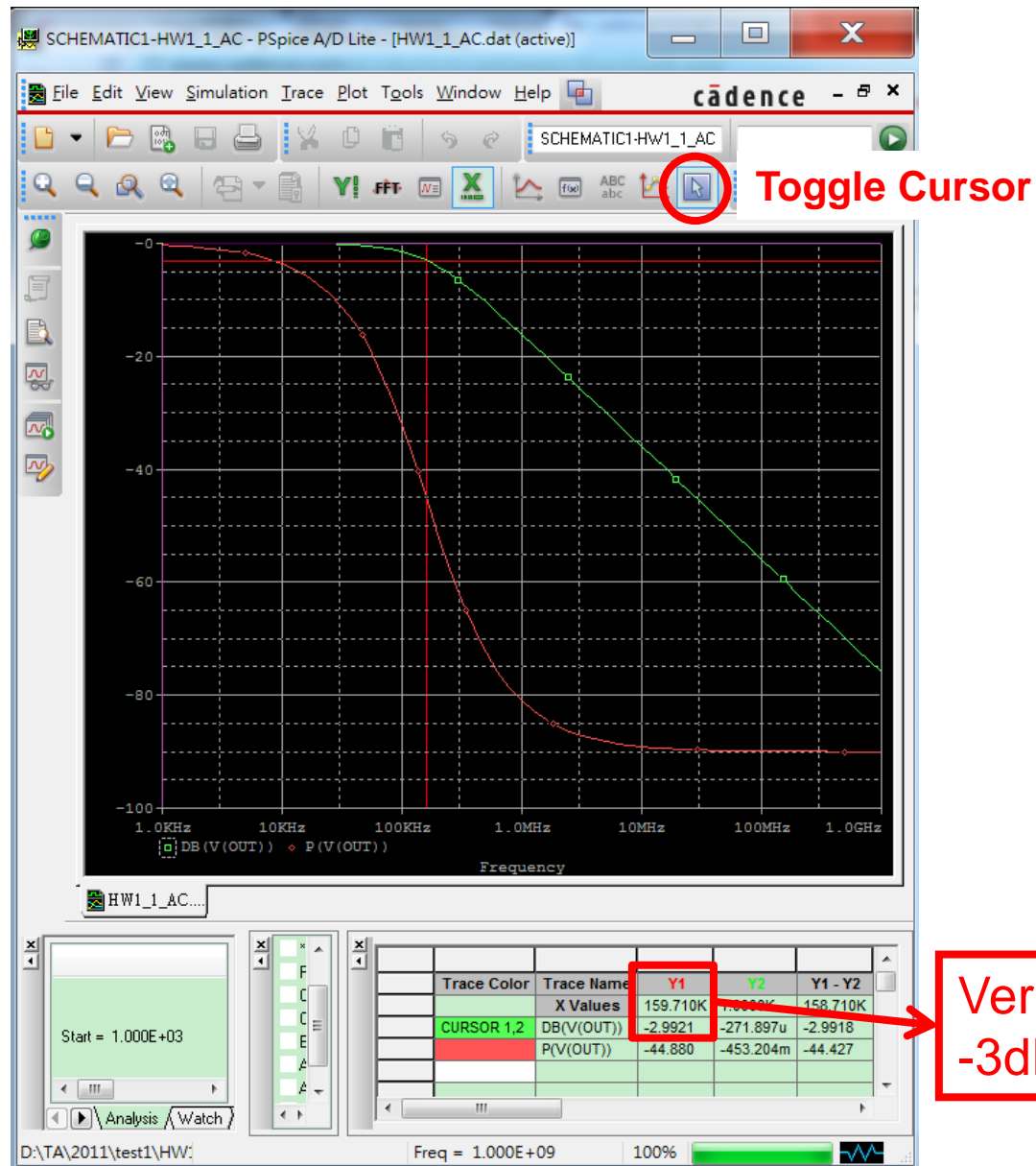
OK Cancel Help

Start = 1.000E+03 Freq = 1.000E+09 End = 1.000E+...

For Help, press F1

Freq = 1.000E+09 100%

AC Sweep Analysis (Cont.)



Transient Analysis

VPULSE in
SOURCE.olb

V1 = 0
V2 = 3.3
TD = 1n
TR = 1n
TF = 1n
PW = 0.1u
PER = 0.2u

