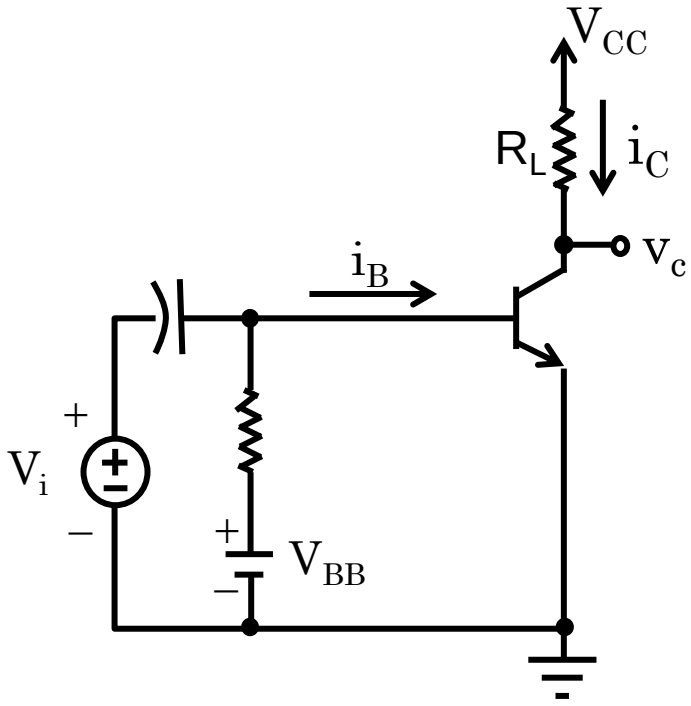
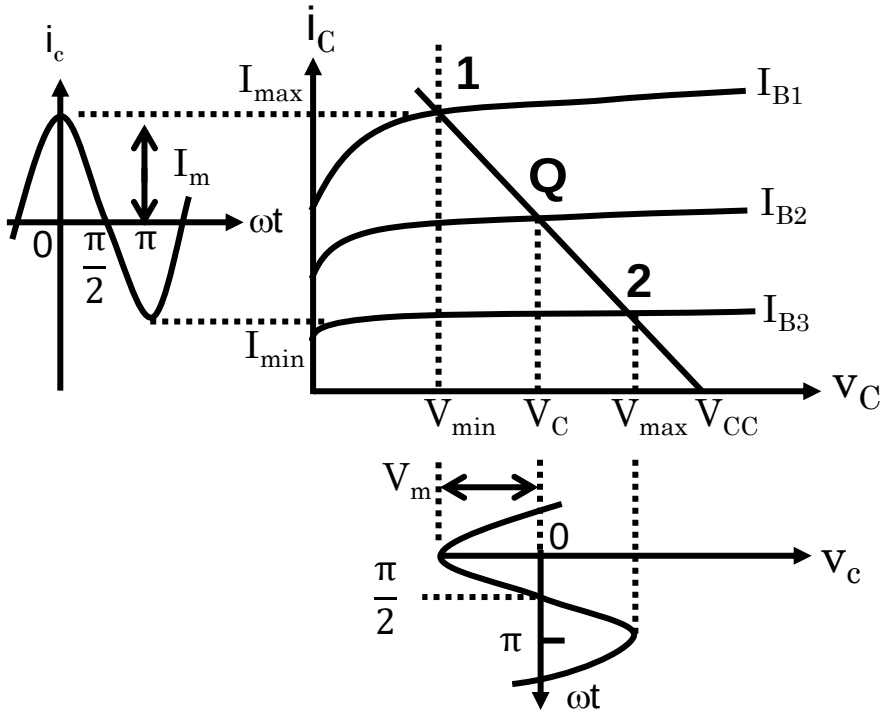
Output Stages and Power Amplifiers

- Output stages with a low output resistance can deliver the output voltage to the load without loss of gain
- Large signal amplifier are used to drive a CRT, a loud speaker, a servomotor, etc.
  - Power amp = large signal amp
  - Power amp can deliver large voltage or current or a large amount of power
  - Thermal considerations are important for power amp

Large-Signal Amplifiers

- I_C is the quiescent collector current (DC signal)
- i_c is the instantaneous variation from I_C (Small signal)
- i_C is the instantaneous collector current (i_c+I_C)
- I_c and V_c are the rms values of i_c and v_c
- I_m is the amplitude of sinusoidal current swing
- V_m is the amplitude of sinusoidal voltage swing





Large-Signal Amplifiers (Cont.)

$$I_c = \frac{I_m}{\sqrt{2}} = \frac{I_{max} - I_{min}}{2\sqrt{2}}$$

$$V_c = \frac{V_m}{\sqrt{2}} = \frac{V_{max} - V_{min}}{2\sqrt{2}}$$

- Assuming perfect linearity, i.e. no nonlinear distortion)

  Output power $P = V_c I_c = \frac{V_m I_m}{2}$

$$P = {I_c}^2 R_L = \frac{{I_m}^2 R_L}{2} = \frac{{V_m}^2}{2R_L}$$

$$P = \frac{(V_{max} - V_{min})(I_{max} - I_{min})}{8}$$

Harmonic Distortion

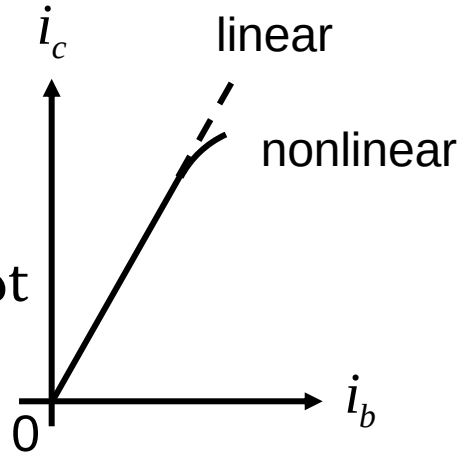
- Nonlinear: transfer function is not a straight line
- Nonlinear issue occurs in both small and large signals
- 2nd harmonic distortion
  - Nonlinear relationship between i_b and i_c is assumed
  - $i_c = G_1 i_b + G_2 i_b^2$ where G1 & G2 are constant.

$$i_b = I_{bm}\cos\omega t$$

$$i_c = G_1 I_{bm}\cos\omega t + G_2 I_{bm}^2 \cos^2\omega t$$

$$= G_1 I_{bm}\cos\omega t + \frac{1}{2} G_2 I_{bm}^2 + \frac{1}{2} G_2 I_{bm}^2 \cos 2\omega t$$

$$= B_0 + B_1\cos\omega t + B_2\cos 2\omega t$$



$$i_C = I_C + i_c = \underline{I_C + B_0} + B_1\cos\omega t + B_2\cos 2\omega t$$

DC level is changed

2nd harmonic distortion is introduced

Harmonic Distortion (Cont.)

- 2nd harmonic distortion $D_2 = \left|\frac{B_2}{B_1}\right|$
- Inter-modulation

  For $i_b = I_{bm1}\cos\omega_1 t + I_{bm2}\cos\omega_2 t$

  i_c contains $\omega_1, \omega_2, \underline{2\omega_1, 2\omega_2}, \underline{\omega_1 + \omega_2, \omega_1 - \omega_2}$

  2nd harmonic distortion **Inter-modulation**

- Higher order harmonic distortion

  $i_c = G_1 i_b + G_2 i_b^2 + G_3 i_b^3 + \cdots$

  $i_C = I_C + B_0 + B_1\cos\omega t + B_2\cos 2\omega t + B_3\cos 3\omega t + \cdots$

  $D_2 = \left|\frac{B_2}{B_1}\right|,\ D_3 = \left|\frac{B_3}{B_1}\right|,\ \cdots$

  where D_n represents the nth harmonic distortion HD_n

Total Harmonic Distortion(THD)

- Power delivered at the fundamental frequency ω is

$$P_1 = I_{1(\mathrm{rms})}^2 R_L = \left(\frac{B_1}{\sqrt{2}}\right)^2 R_L = \frac{B_1^2 R_L}{2}$$

- Total power output is

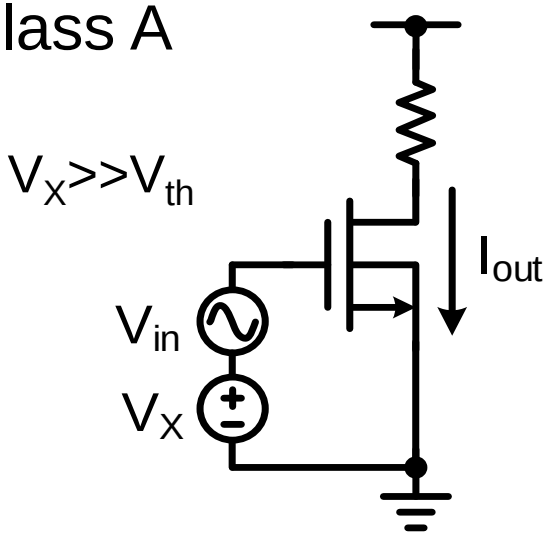
$$P = (B_1^2 + B_2^2 + B_3^2 + \cdots) \times \frac{R_L}{2}$$

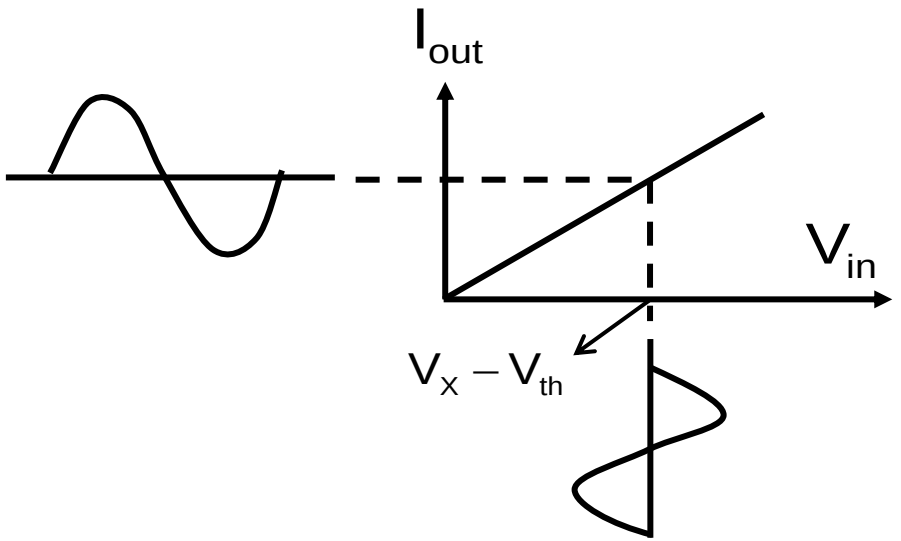
$$= (1 + D_2^2 + D_3^2 + \cdots) \times P_1$$

$$\mathrm{THD} = \sqrt{D_2^2 + D_3^2 + D_4^2 + \cdots}$$

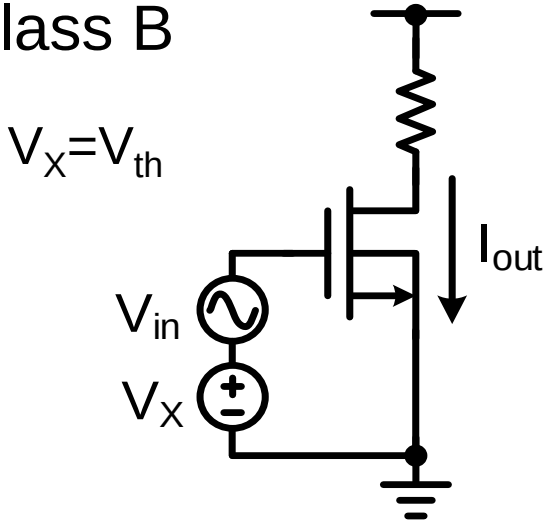
Amplifier Classification

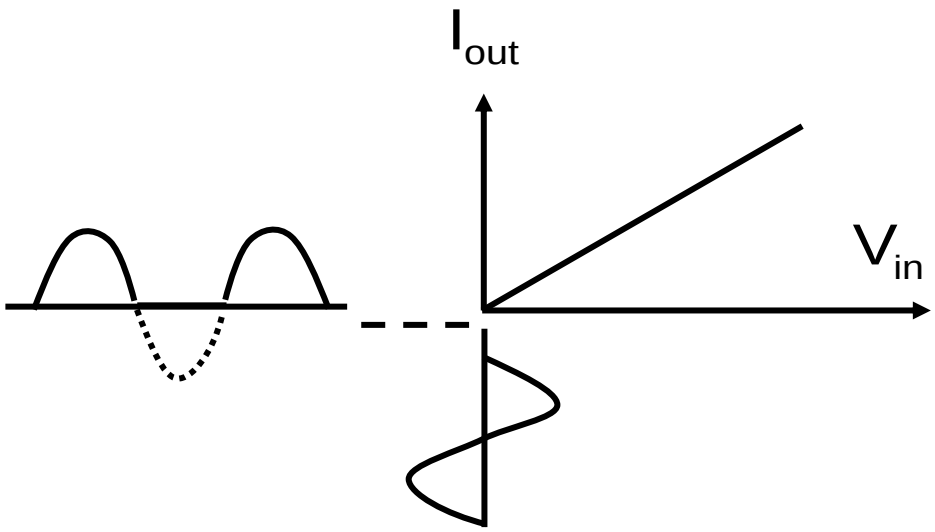
- Class A





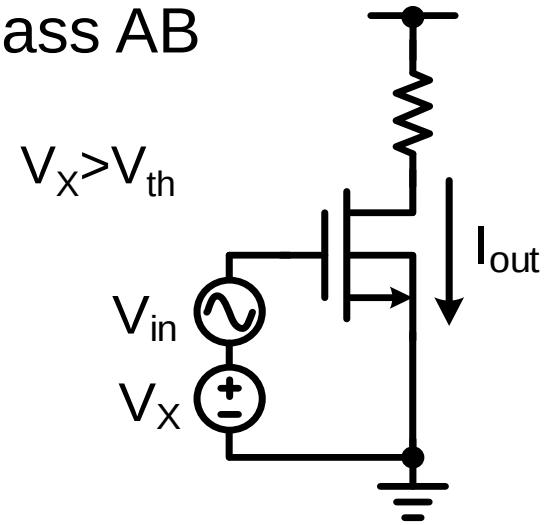
- Class B

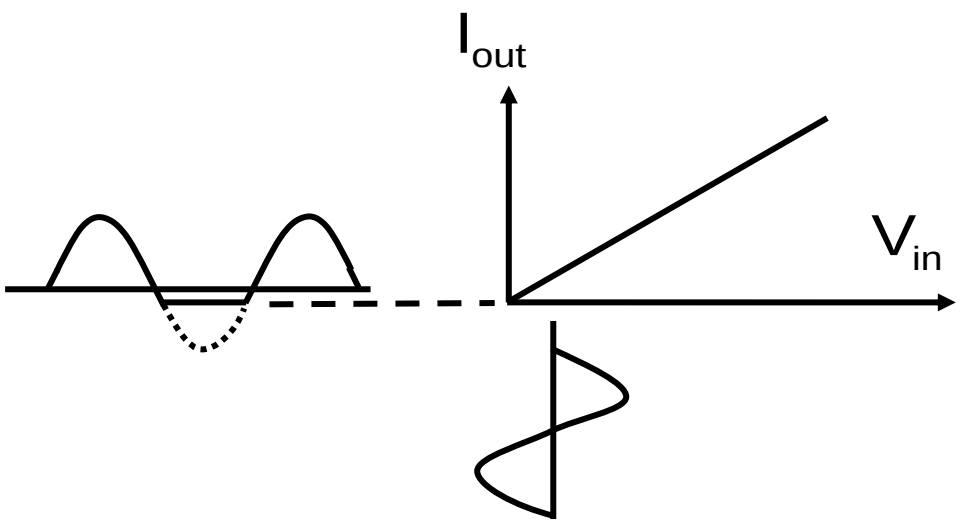




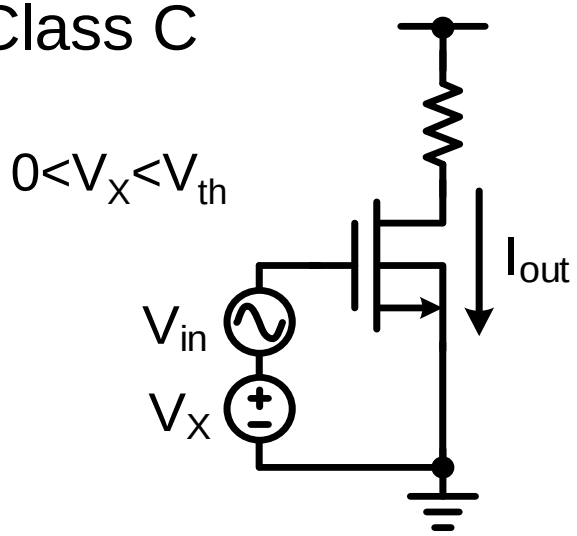
Amplifier Classification (Cont.)

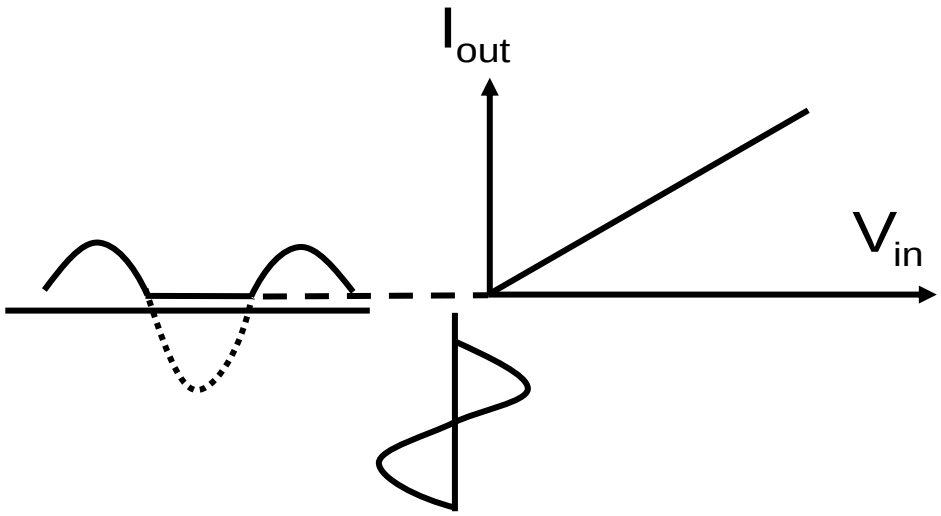
- Class AB





- Class C





Power Conversion Efficiency

- Important under
  1. limited source of power. (e.g. in a satellite)
  2. maximum power-dissipating consideration.
- Conversion efficiency

$$\eta = \frac{\textbf{signal power delivered to load}}{\textbf{dc power supplied to output circuit}} \times \textbf{100\%}$$

- Class-A amplifier with i_c and v_c output

$$i_C = I_C + i_c$$

$$i_c = I_m \sin \omega t$$

$$v_c = V_m \sin \omega t$$

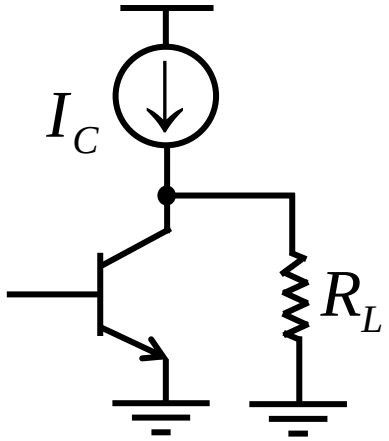
$$\eta = \frac{\frac{1}{2} V_m I_m}{V_{CC} I_C} \times 100\% = \frac{50 V_m I_m}{V_{CC} I_C}\%$$

Power Conversion Efficiency (Cont.)

- Small signal, i.e.($\frac{I_m}{V_m}$) are small
  1. $\eta \rightarrow 0$
  2. static power consumption $V_{CC}I_C$ even no excitation
- Maximum signal, i.e. $I_m=I_C$,$V_m=0.5V_{CC}$

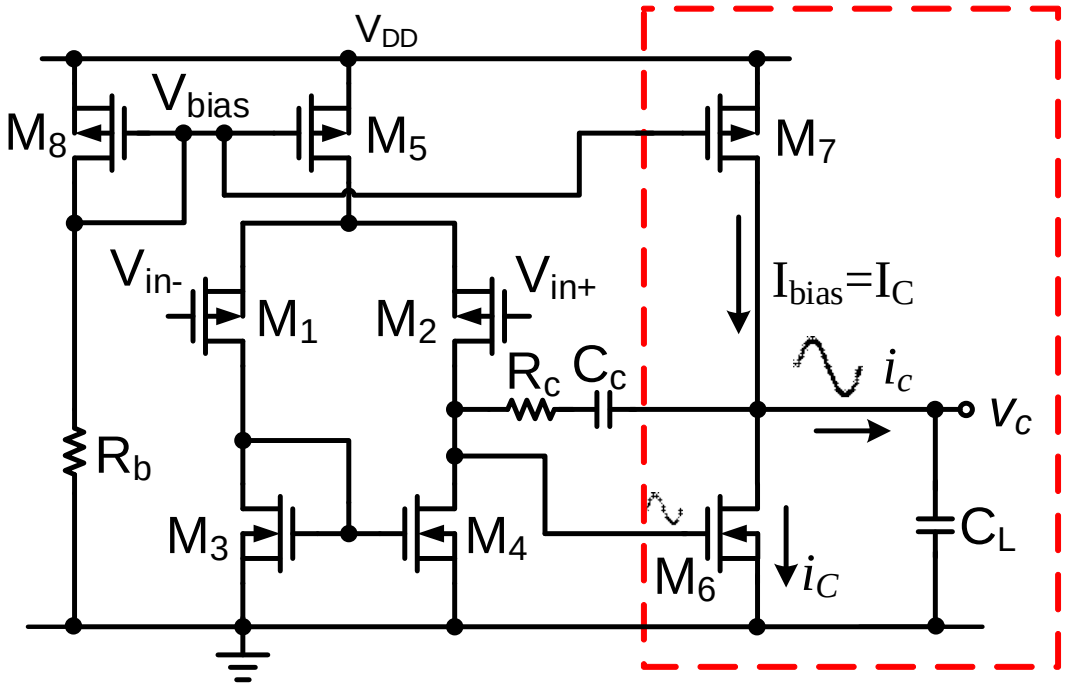
  $\eta=25\%$

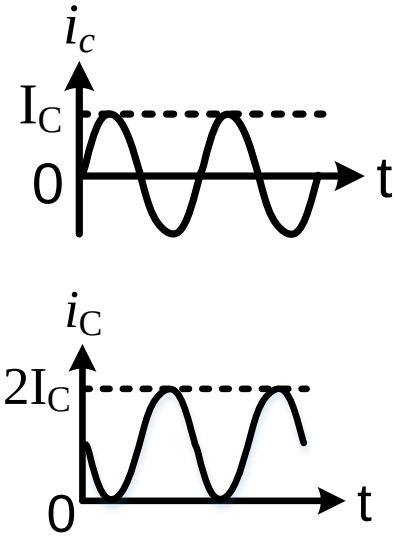
- Class-A operation is a poor choice for power amplification.



Class-A Amplifier

- Example : 2nd stage of two-stage OPAMP

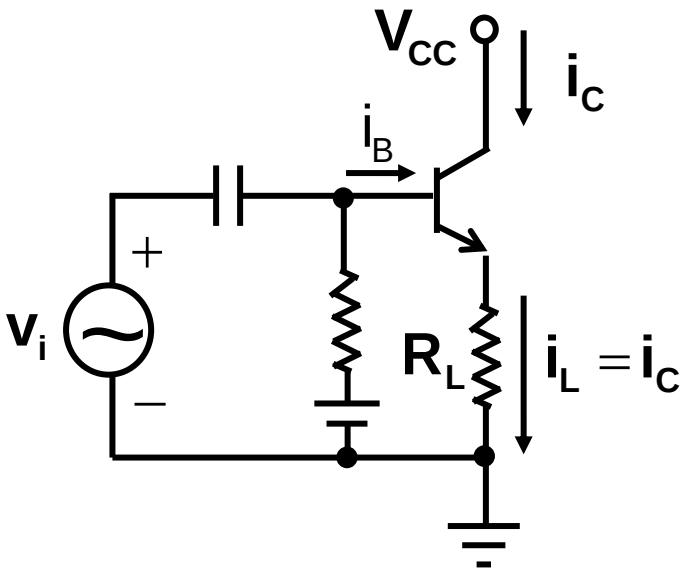


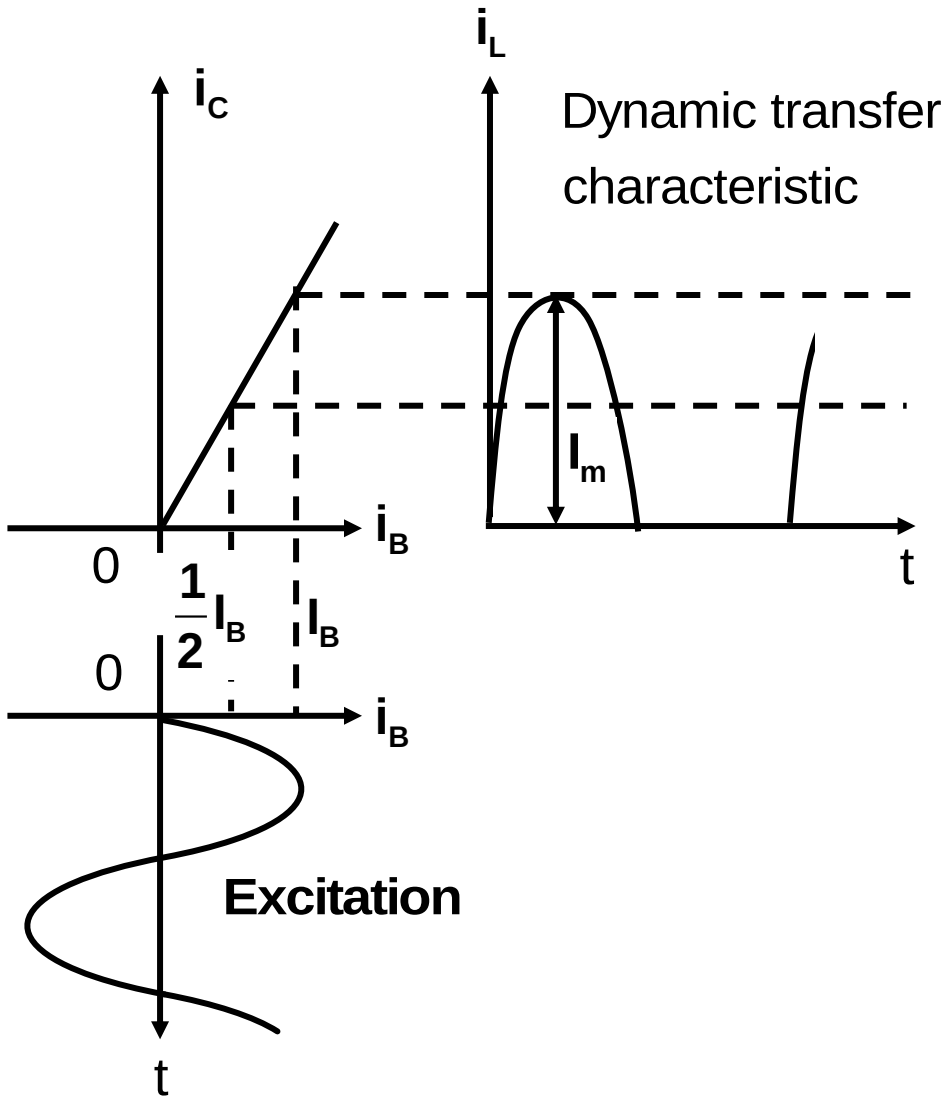


- M_6 conducts for entire cycle of the input signal

Class-B Push-Pull Amplifier

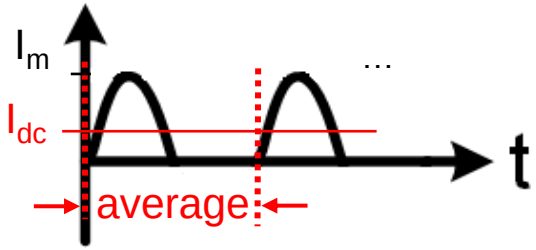
- Class-B amplifier

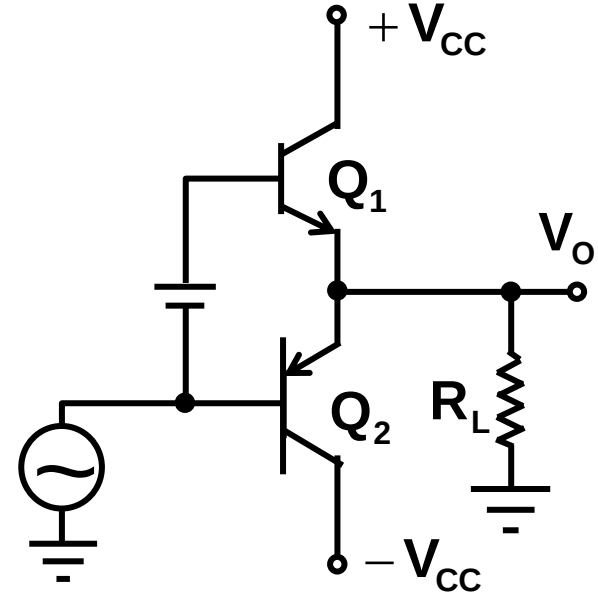




Class-B Push-Pull Amplifier (Cont.)

- Efficiency of Class-B push-pull
  - Output power $P_o = \frac{I_m V_m}{2}$
  - DC power (supplied by V_{CC})
    - Avg. $I_{dc} = \frac{I_m}{\pi}$





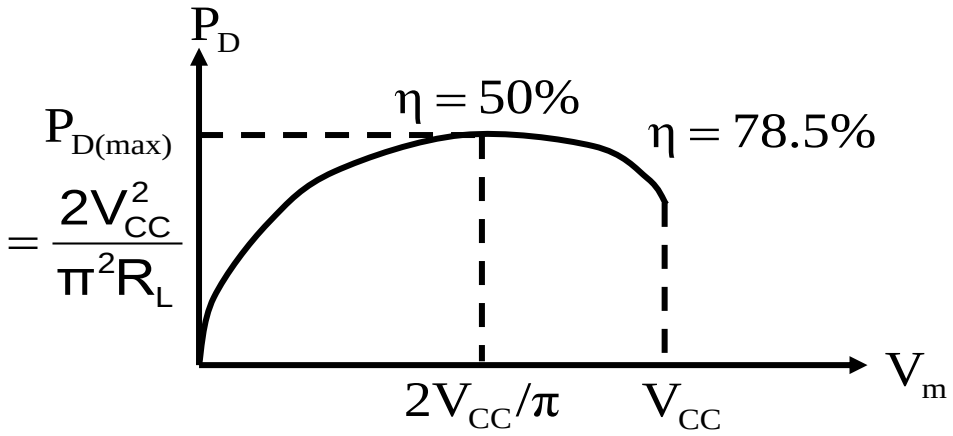
    - $P_i = 2 \times \frac{I_m}{\pi} \times V_{CC}$ ← Two transistors for push-pull
  - Efficiency
    - $\eta = \frac{P_o}{P_i} \times 100\% = \frac{\pi}{4} \frac{V_m}{V_{CC}} \times 100\% \quad \Rightarrow \eta \propto V_m$
    - For $V_m \approx V_{CC} \Rightarrow \eta_{max} = \frac{\pi}{4} \times 100\% \approx 78.5\%$
  - No static power consumption under zero excitation

Class-B Push-Pull Amplifier (Cont.)

- Average power dissipated in the class-B stages.
  - $P_D = P_i - P_o = \frac{2}{\pi}\frac{V_m V_{CC}}{R_L} - \frac{V_m^2}{2R_L} \cdots (A)$ (Two transistors push-pull)
  - Differentiating Eq.(A) with respect to V_m and equating the derivative to zero gives the V_m that results in maximum P_D

$$\Rightarrow V_m = \frac{2V_{CC}}{\pi} \Rightarrow P_{D(max)} = \frac{2V_{CC}^2}{\pi^2 R_L}$$

  - For $V_m = V_{CC} \Rightarrow P_{o,max} = \frac{V_{CC}^2}{2R_L}$ ⋯ power output



Distortion in the Class-B Push-Pull Stage

- Harmonic distortion
  - For matched devices Q_1 & Q_2
  - i_1 and i_2 are identical except shifted in phase by 180°

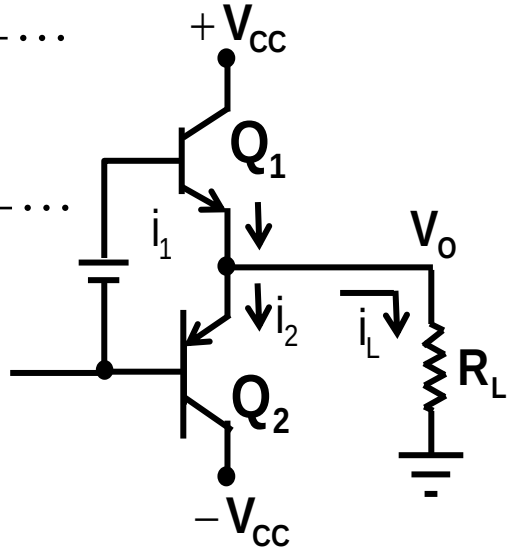
$$i_1 = I_C + B_0 + B_1\cos\omega t + B_2\cos 2\omega t + B_3\cos 3\omega t + \cdots$$

$$i_2(\omega t) = i_1(\omega t + \pi)$$

$$i_2 = I_C + B_0 - B_1\cos\omega t + B_2\cos 2\omega t - B_3\cos 3\omega t + \cdots$$

$$i_L = i_1 - i_2 = 2(B_1\cos\omega t + B_3\cos 3\omega t + \cdots)$$

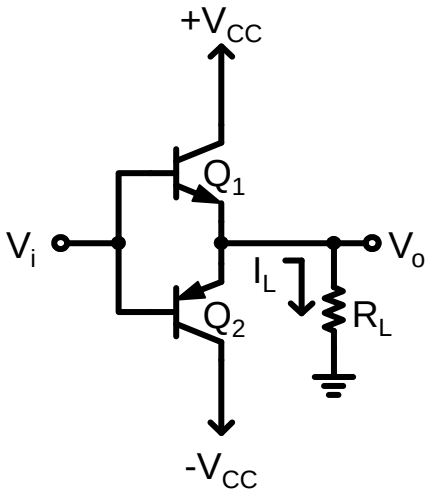
→ Even-order harmonic distortions have been eliminated

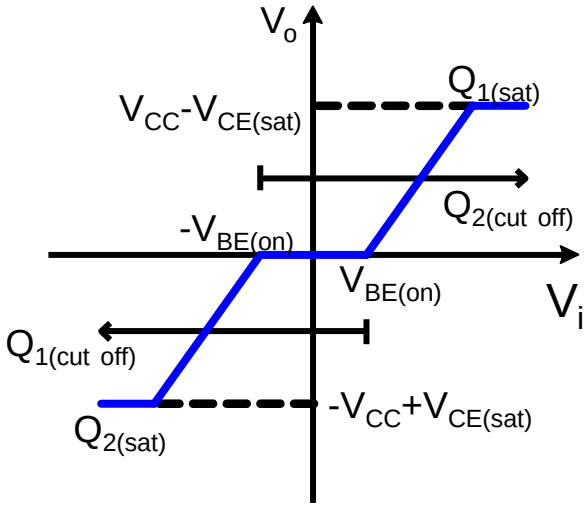


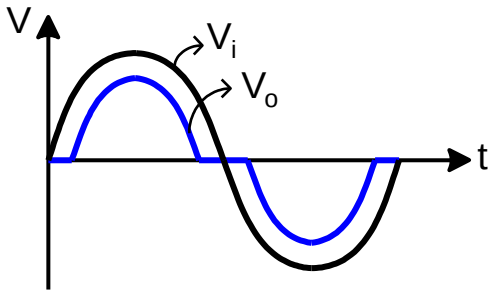
  - If the I-Vs of Q_1 & Q_2 are not identical, then even-order harmonic distortions are expected
  - Crossover distortion (will be discussed later)

Output Stages

- Ideal output stages
  - Supply external load current
  - Low output impedance
  - Large output swing $\approx V_{CC} - V_{CE(sat)}$ (ideally)
- Commonly used complementary emitter follower
  - Each transistor is on for only half the time
- Crossover distortion

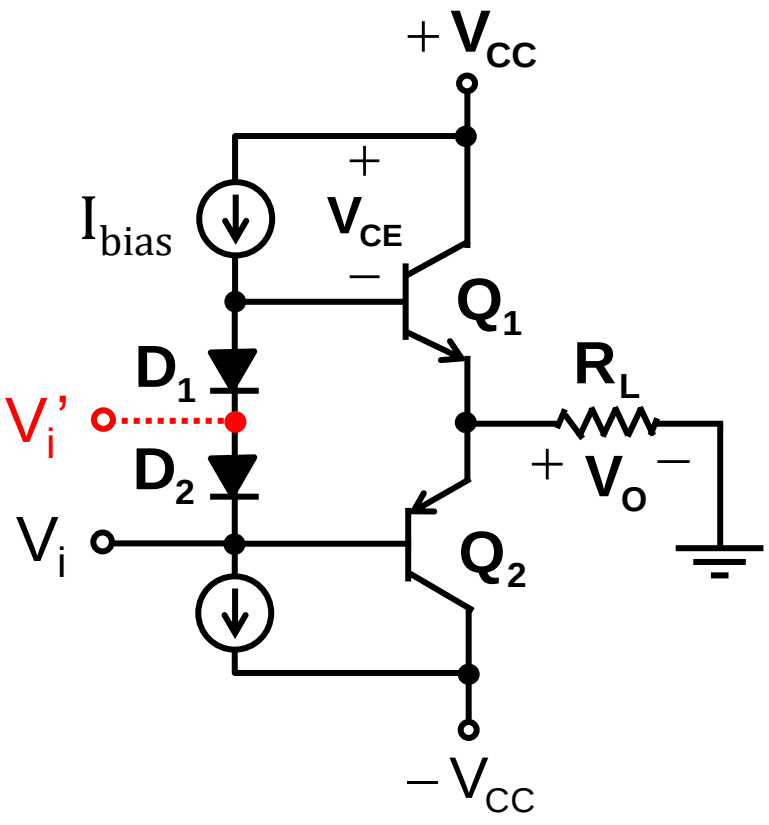


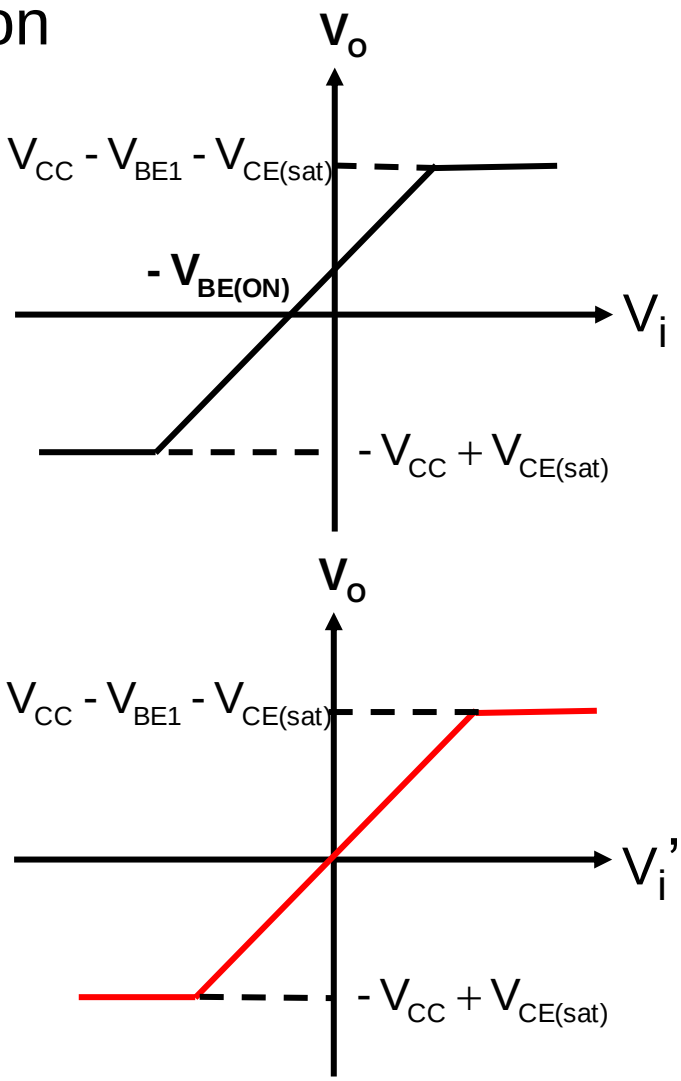




Output Stages (Cont.)

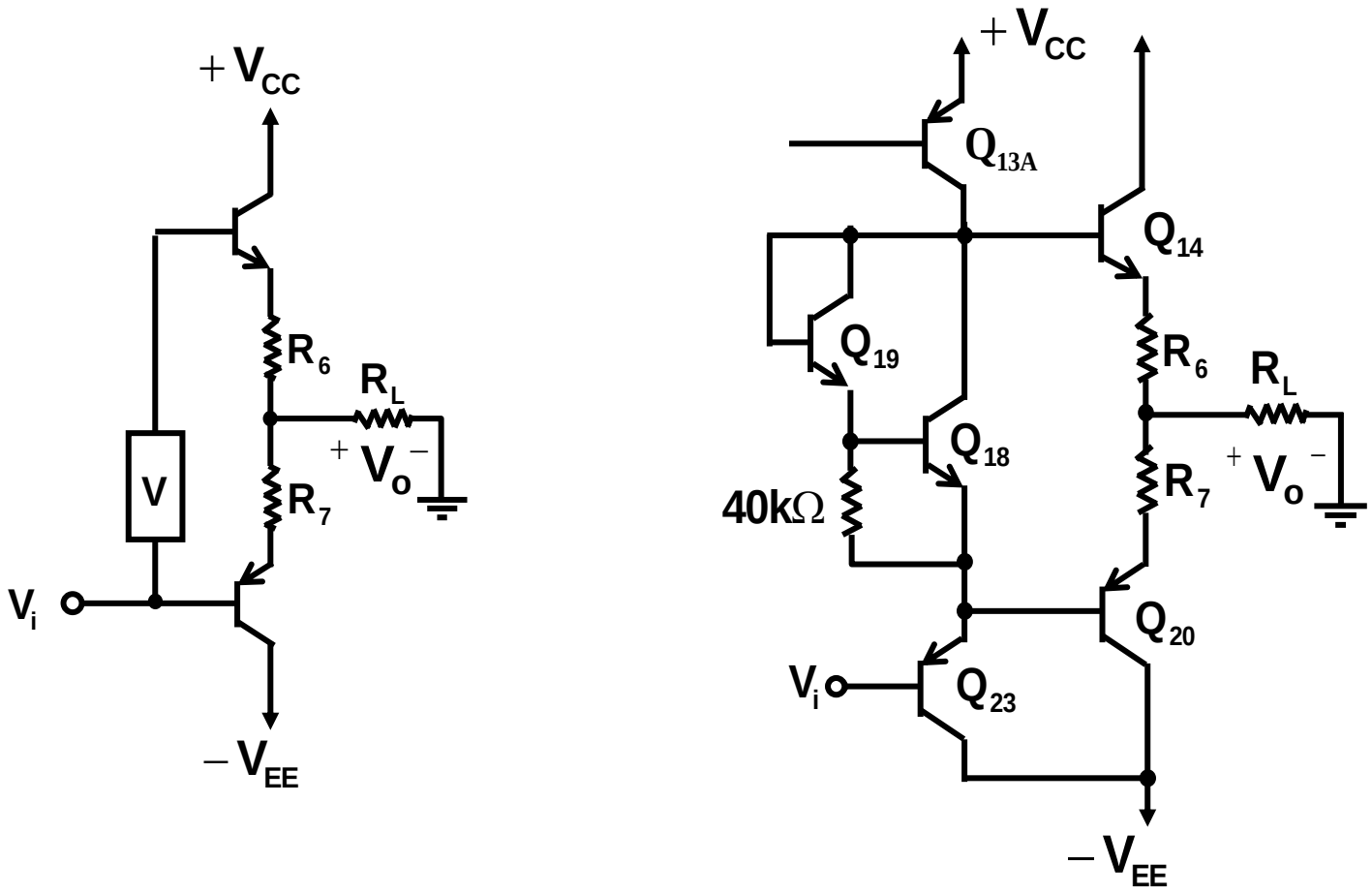
– Elimination of crossover distortion



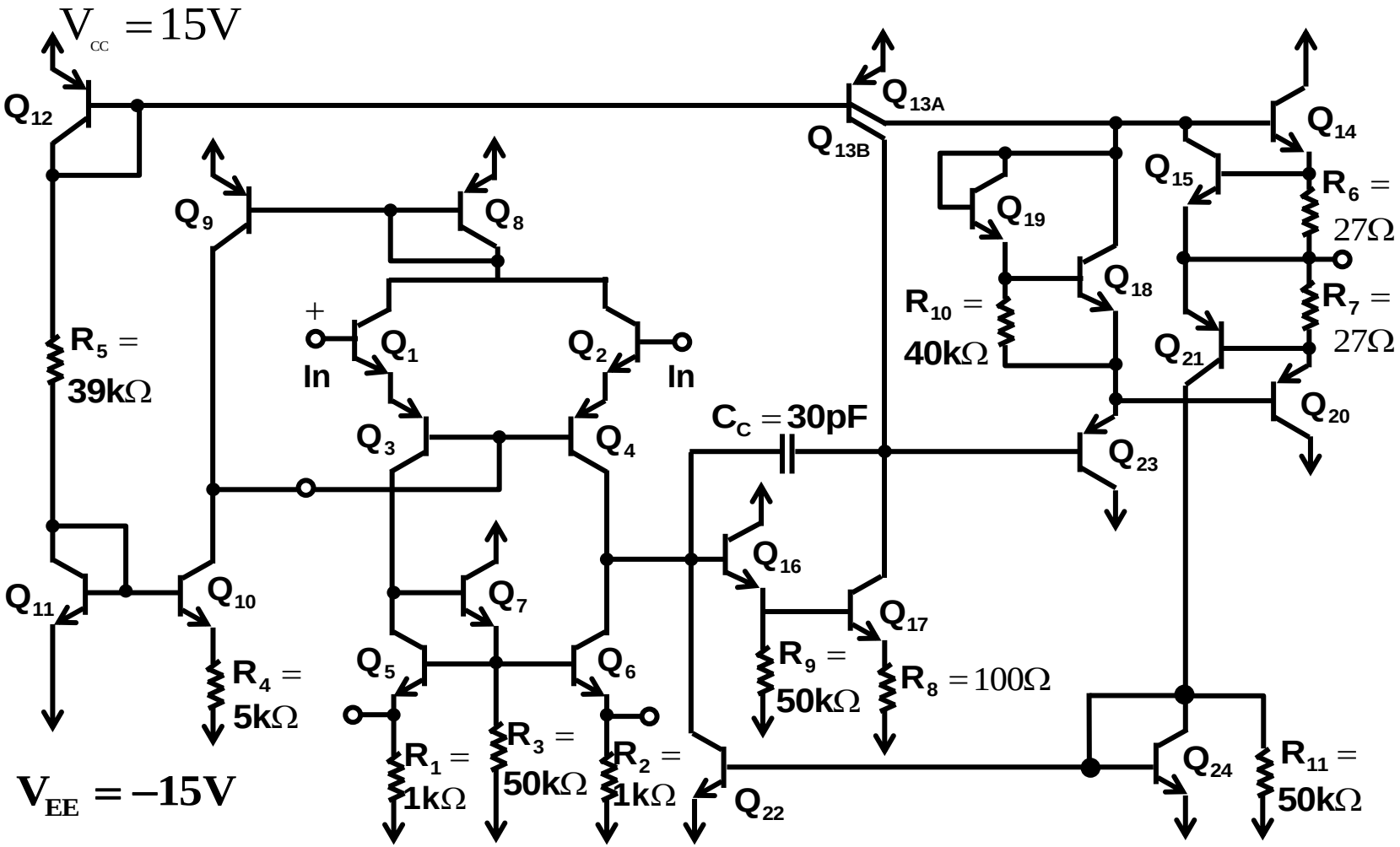


Elimination of Crossover Distortion of 741-Type OPAMP

- Output stage



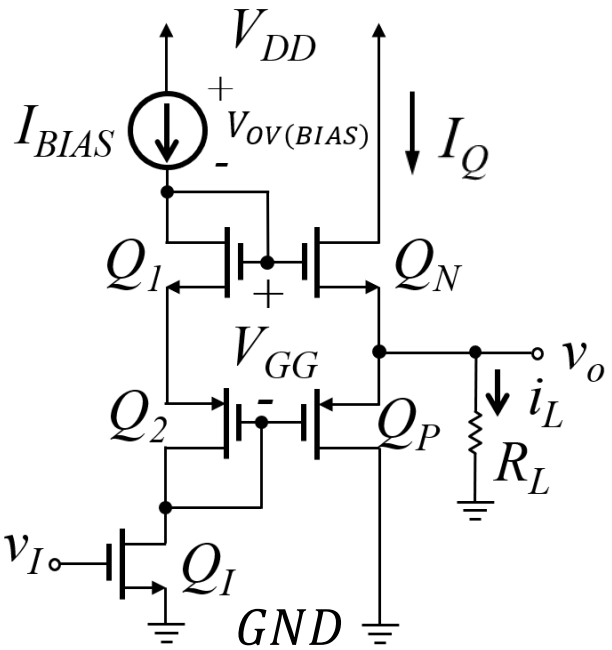
Elimination of Crossover Distortion of 741-Type OPAMP (Cont.)



- Small R_6 and R_7 are included to guard against the possibility of thermal runaway

Classical CMOS Class-AB Output Stage

- Q_N and Q_P are source followers
- Q_1 and Q_2 are diode-connected
  $\rightarrow$ eliminate crossover distortion
- Quiescent current I_Q of Q_1 and Q_2



$$I_{D1} = I_{BIAS} = \frac{1}{2} k_n' \left(W/L\right)_1 (V_{GS1} - V_{tn})^2$$

$$I_{D2} = I_{BIAS} = \frac{1}{2} k_p' \left(W/L\right)_2 (V_{SG2} - |V_{tp}|)^2$$

$$\Rightarrow V_{GG} = V_{GS1} + V_{SG2} = V_{tn} + |V_{tp}| + \sqrt{2 \cdot I_{BIAS}} \cdot \left(\sqrt{k_n' \left(W/L\right)_1}^{-1} + \sqrt{k_p' \left(W/L\right)_2}^{-1} \right)$$

similar for Q_N and Q_P,

$$\Rightarrow V_{GG} = V_{GSN} + V_{SGP} = V_{tn} + |V_{tp}| + \sqrt{2 \cdot I_Q} \cdot \left(\sqrt{k_n' \left(W/L\right)_n}^{-1} + \sqrt{k_p' \left(W/L\right)_p}^{-1} \right)$$

assume $k_n' \left(W/L\right)_1 = k_p' \left(W/L\right)_2$ and $k_n' \left(W/L\right)_n = k_p' \left(W/L\right)_p$ $\Rightarrow I_Q = I_{BIAS} \cdot \dfrac{\left(W/L\right)_n}{\left(W/L\right)_1}$

Restricted Output Swing of Classical Class-AB

$$v_{Omax} = V_{DD} - V_{OV(BIAS)} - v_{GSN}$$
$$= V_{DD} - V_{OV(BIAS)} - V_{tn} - v_{OVN}$$

where

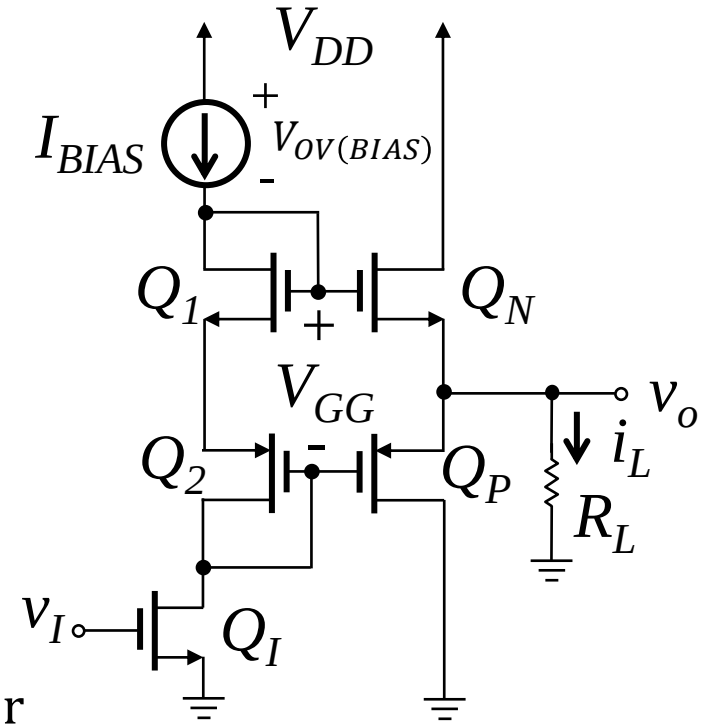
- $V_{OV(BIAS)}$: min. voltage across current source
- v_{OVN}: V_{OV} of Q_N when it is supplying i_{Lmax}

similarly,

$$v_{Omin} = V_{OV(I)} + |V_{tp}| + |v_{OVP}|$$

where

- $V_{OV(I)}$: min. voltage across the input transistor
- $|v_{OVP}|$: $|V_{OV}|$ of Q_P when sinking the max. i_L



⇒ One drawback of classical CMOS class-AB output stage is the restricted output swing range

⇒ Lower efficiency η with smaller $v_{o(pp)}$ since η ∝ $\frac{v_{o(pp)}}{V_{DD}}$

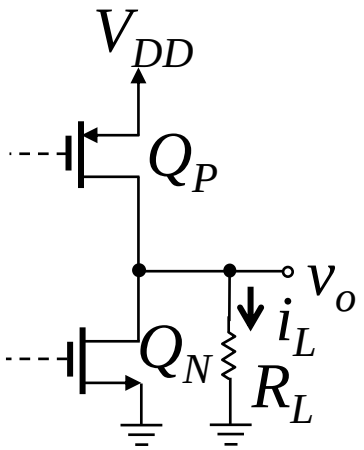
where $v_{o(pp)}$ is the peak-to-peak v_o

Class-AB Utilizing Common-Source Transistors

- Allowable range of v_O

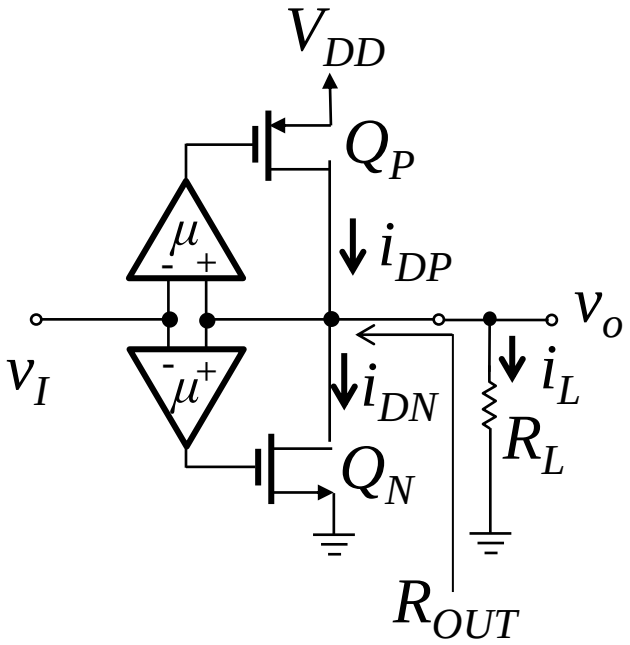
$$\begin{cases} v_{Omax} = V_{DD} - |v_{OVP}| \\ v_{Omin} = v_{OVN} \end{cases}$$

$\Rightarrow$ output swing range is increased



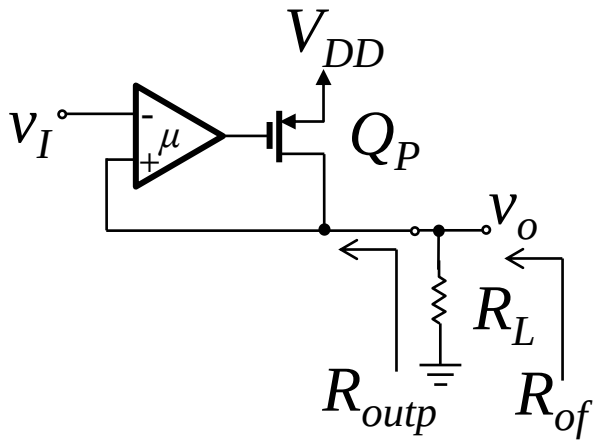
- High output resistance $R_{out} = R_{out\,n} // R_{out\,p}$

- Negative series-shunt feedback
  - reduce the R_{out} of the amplifier
  - $v_O \approx v_I$ if the loop gain is large

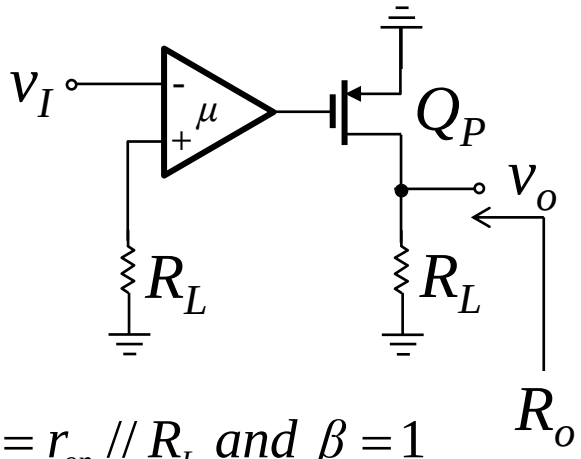


Reading Assignment:
R_{out} Reduction by Series-Shunt Feedback

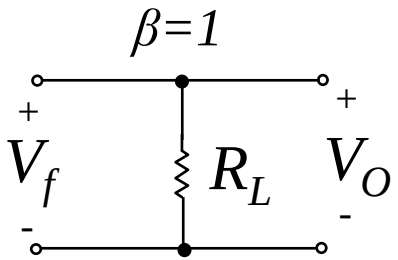
- The top half circuit



◆ the A circuit



◆ the β circuit



$$A\beta = \mu \cdot g_{mp} \cdot (r_{op} \,//\, R_L),\ R_o = r_{op} \,//\, R_L \ and\ \beta = 1$$

$$\Rightarrow R_{of} = \frac{R_o}{1 + A\beta} = \frac{r_{op} \,//\, R_L}{1 + \mu \cdot g_{mp} \cdot (r_{op} \,//\, R_L)},\ R_{of} = R_{outp} \,//\, R_L$$

$$\Rightarrow R_{outp} = \left(1/R_{of} - 1/R_L \right)^{-1} = r_{op} \,//\, \frac{1}{\mu \cdot g_{mp}} \approx \frac{1}{\mu \cdot g_{mp}}$$

$$\Rightarrow R_{out} = R_{outp} \,//\, R_{outn} \approx \left(\frac{1}{\mu g_{mp}} \,//\, \frac{1}{\mu g_{mn}} \right) \approx \frac{1}{\mu g_{mp} + \mu g_{mn}}$$

Reading Assignment: Voltage Transfer Characteristic

- In the quiescent state

$v_I = 0$ and $v_O = 0$

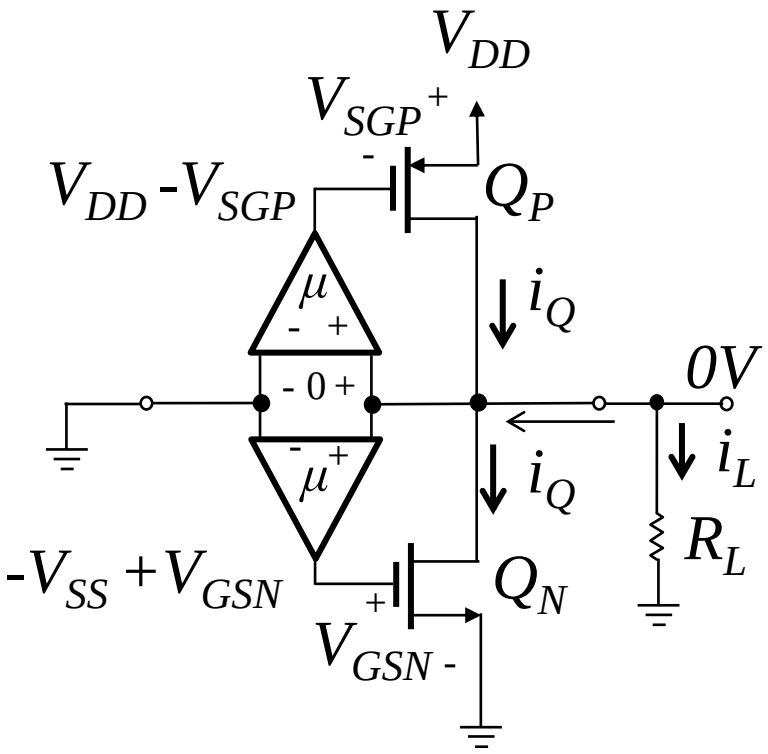
$$I_{DP} = I_Q = \frac{1}{2} k_p' \left(W/L \right)_p V_{OV}^{\ 2}$$

$$I_{DN} = I_Q = \frac{1}{2} k_n' \left(W/L \right)_n V_{OV}^{\ 2}$$

assume Q_P and Q_N are matched

i.e. $k_p' \left(W/L \right)_p = k_n' \left(W/L \right)_n = k$

$$\Rightarrow I_Q = \frac{1}{2} k V_{OV}^{\ 2}$$



Reading Assignment: Voltage Transfer Characteristic (Cont.)

- When v_I is applied

$$i_{DP} = \frac{1}{2}k\left[V_{OV} - \mu(v_O - v_I)\right]^2 = \frac{1}{2}kV_{OV}^2\left(1 - \mu\frac{v_O - v_I}{V_{OV}}\right)^2 = I_Q \cdot \left(1 - \mu\frac{v_O - v_I}{V_{OV}}\right)^2$$

$$\text{similarly, } i_{DN} = I_Q \cdot \left(1 + \mu\frac{v_O - v_I}{V_{OV}}\right)^2$$

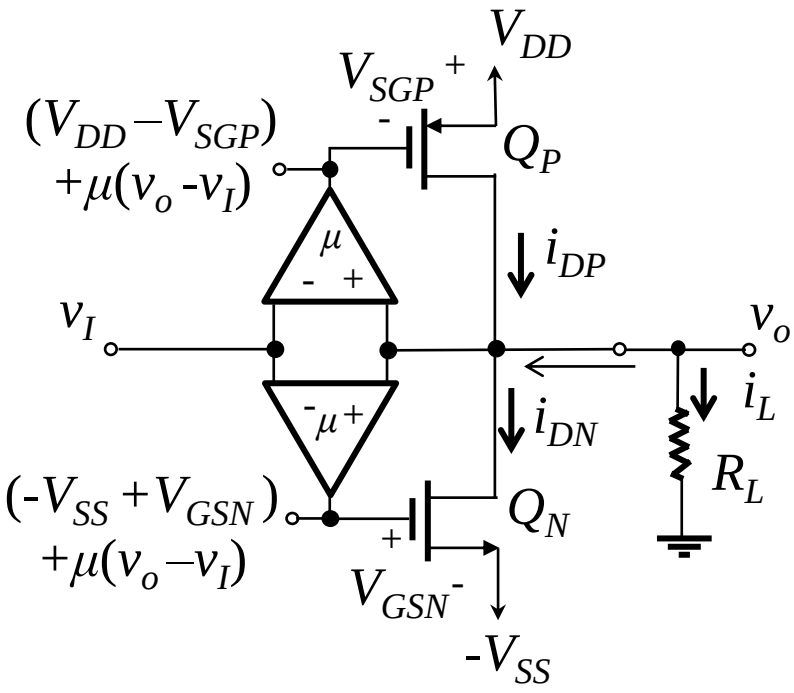
$$v_O = i_L \cdot R_L = (i_{DP} - i_{DN}) \cdot R_L$$

$$\Rightarrow v_O = \frac{v_I}{1 + \dfrac{V_{OV}}{4\mu I_Q R_L}} \approx v_I\left(1 - \frac{V_{OV}}{4\mu I_Q R_L}\right)$$

$$\Rightarrow \text{Gain error} \equiv v_O - v_I = -\frac{V_{OV}}{4\mu I_Q R_L}v_I$$

$$\text{since } g_{mp} = g_m = \frac{2I_Q}{V_{OV}}$$

$$\Rightarrow \text{Gain error} = -\frac{1}{2\mu g_m R_L}$$



Reading Assignment: Design Trade-Offs

- Error amplifiers' gain μ
  - larger μ

    $\rightarrow$ Smaller gain error and R_{out}
  - smaller μ

    $\rightarrow$ I_Q is more insensitive to the input offset voltages of the error amplifiers
- Quiescent current I_Q
  - larger I_Q

    $\rightarrow$ Smaller crossover distortion, gain error, and R_{out}
  - smaller I_Q

    $\rightarrow$ Less power dissipation

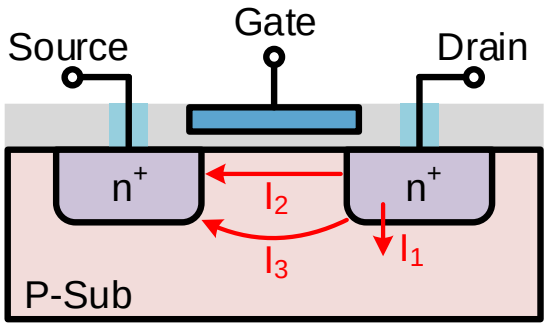
Power Dissipation

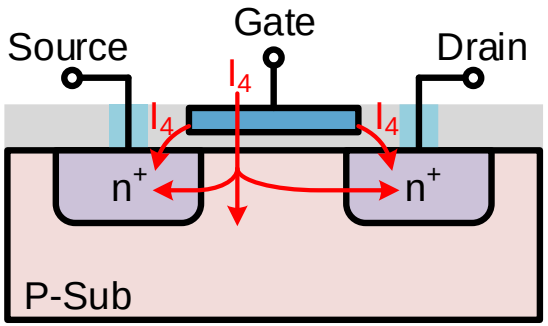
- Static dissipation due to
  - Leakage current
  - Bias current
- Dynamic dissipation due to
  - Short-circuit shoot-through current
  - Charging and discharging of load capacitances

Static Power Dissipation

- Leakage current
  - Junction leakage current
    - pn-junction reverse-bias leakage (I_1)
    - Subthreshold leakage (I_2)
    - Channel punch through leakage (I_3)
  - Gate leakage current
    - Tunneling into and through gate oxide leakage (I_4)

*Leakage current maybe non-negligible in advanced process < 28nm

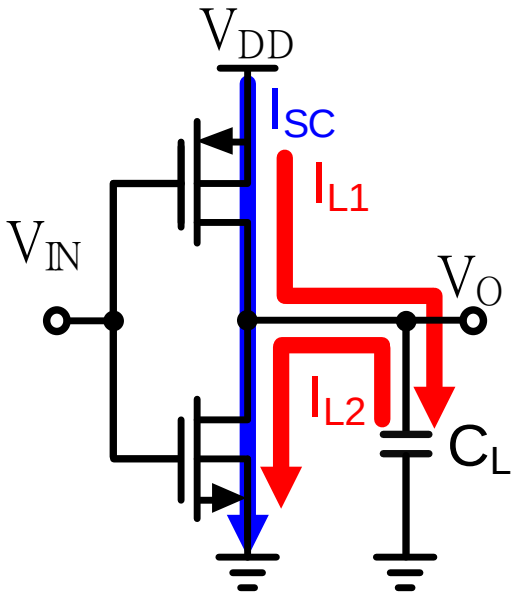




- Bias current (e.g. for analog circuits including OPAMPs)
- Total static power dissipation

$$P_s = \sum_{1}^{n} \text{leakage/bias current} \times \text{supply voltage}, \text{where n} = \text{number of devices}$$

Dynamic Power Dissipation of CMOS Inverter



a. Current is required to charge and discharge the output capacitive load (I_{L1}, I_{L2})

b. Short-circuit shoot-through current (I_{SC})
   - ◆ During transition from either “0” to “1” or “1” to “0”, both n- and p-transistors are ON for a short period of time. This results in a short current pulse from V_{DD} to GND.

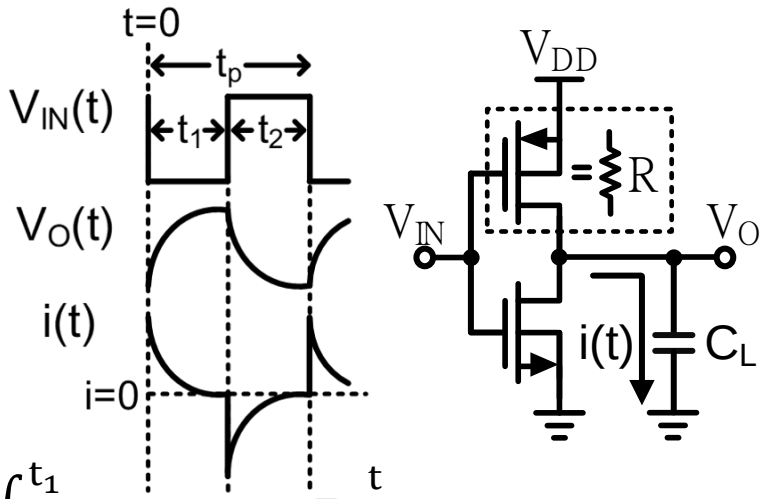
*Note: a. is the dominant term in general circuits

Capacitive-Load Charging/Discharging Dissipation of CMOS Inverter

- For step-input example
  - Energy flow during t_1 , i.e. $V_O \uparrow$

$$V_O(t) = V_{DD}(1 - e^{-t/RC_L})$$

Total energy supplied by V_{DD}:



$$\int_0^{t_1} V_{DD} \times i(t)dt = V_{DD} \int_0^{t_1} \frac{V_{DD} - V_o(t)}{R} dt = \frac{{V_{DD}}^2}{R} \int_0^{t_1} [1 - (1 - e^{-\frac{t}{RC_L}})]\, dt = = C_L {V_{DD}}^2$$

Energy dissipated in R:

$$\int_0^{t_1} \frac{[V_{DD} - V_O(t)]^2}{R} dt = \frac{1}{2} C_L {V_{DD}}^2$$

Energy stored in C_L:

$$C_L {V_{DD}}^2 - \frac{1}{2} C_L {V_{DD}}^2 = \frac{1}{2} C_L {V_{DD}}^2$$

  - Energy flow during t_2, i.e. $V_O \downarrow$

Energy stored in C_L is exhaustively dissipated $= \frac{1}{2} C_L {V_{DD}}^2$

  - During a period t_p, power dissipated $P_d = C_L {V_{DD}}^2 f_p$, where $f_p = \frac{1}{t_p}$

Short-Circuit Dissipation of CMOS Inverter

- Without considering C_L

$$P_{SC} = I_{mean} V_{DD}$$

$$I_{mean} = 2 \cdot \frac{1}{t_p}\left[\int_{t_1}^{t_2} I(t)\,dt + \int_{t_2}^{t_3} I(t)\,dt\right] = \frac{4}{t_p}\int_{t_1}^{t_2} \frac{\beta}{2}\left[V_{in}(t) - V_{th}\right]^2 dt$$

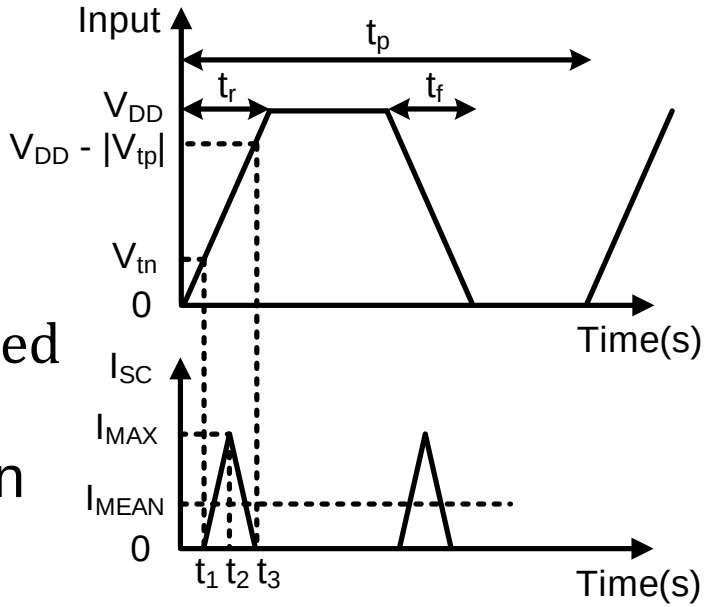
where $V_{tn} = -V_{tp}$, $\beta_n = \beta_p = \beta = \mu C_{ox}\frac{W}{L}$ are assumed

If $V_{in}(t) = \frac{V_{DD}}{t_r}t$, $t_1 = \frac{V_{th}}{V_{DD}}t_r$, and $t_2 = \frac{t_r}{2}$

then $P_{SC} = \frac{\beta}{12}(V_{DD} - 2V_{th})^3 \cdot t_{rf} \cdot f_p$

where $t_r = t_f = t_{rf}$, and $f_p = \frac{1}{t_p}$ are assumed

→ short-circuit dissipation is dependent on the input waveform rise and fall times

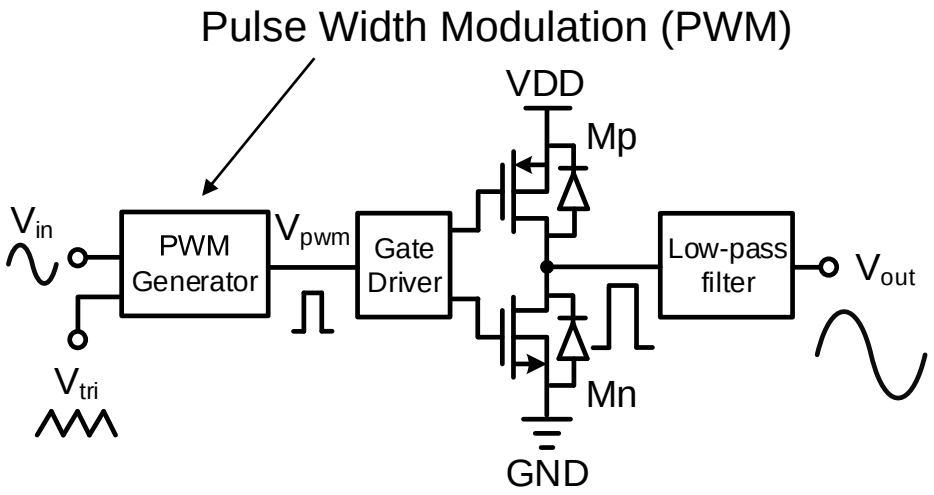


Power Economy of CMOS Inverter

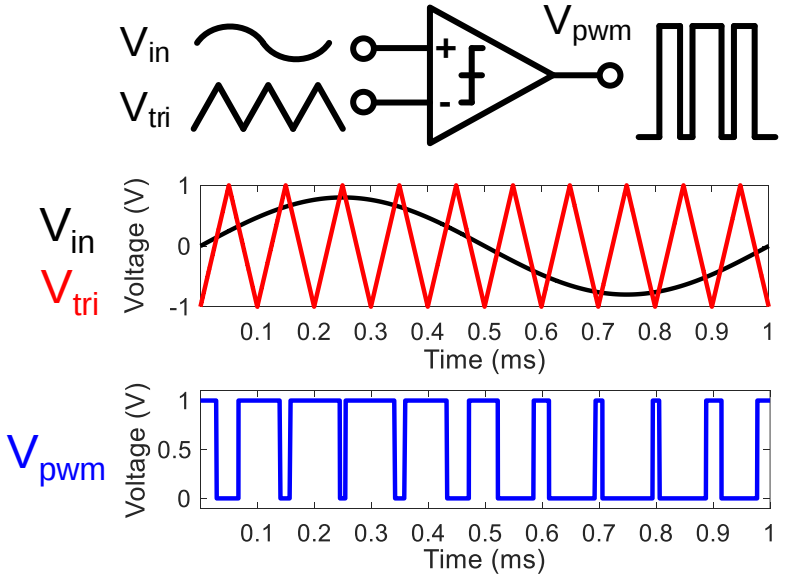
- Total power dissipation $P_{total} = P_s + P_d + P_{sc}$
  - where $P_d = \text{activity}-\text{percentage} \cdot (C_{total} V_{DD}^2 f_p)$
  - P_{sc} is also multiplied by an activity−percentage
- Power dissipation constraint must be met in a design because of low-power and thermal-dissipation concerns
- Methods to minimize power dissipation
  1. Reduce supply voltage
  2. Operate circuitry at the lowest possible speed
  3. Use dynamic voltage and frequency scaling (DVFS)
  4. Use smaller devices to reduce dynamic power
     a. use layout techniques to reduce diffusion and routing capacitance
     b. small load capacitance if possible
  5. Many other clever methods of manipulating architecture, circuit, and layout to achieve low-power goals.

Class-D Amplifier

- Class A, B and AB amplifiers → Linear amplifier
- Class-D amplifier → Switching amplifier
  - Block diagram



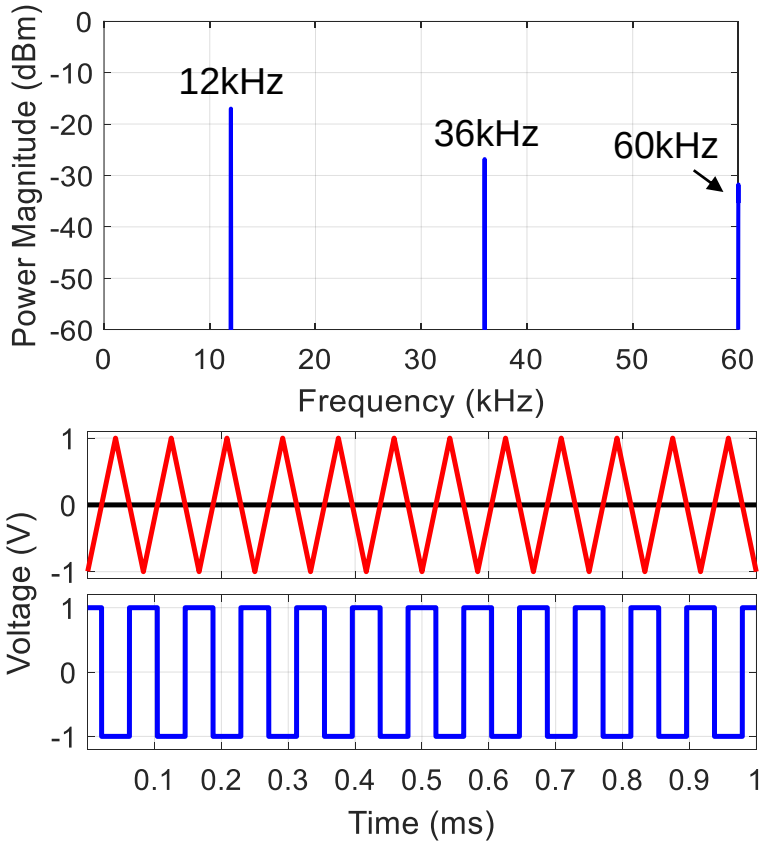
  - Common PWM Generator



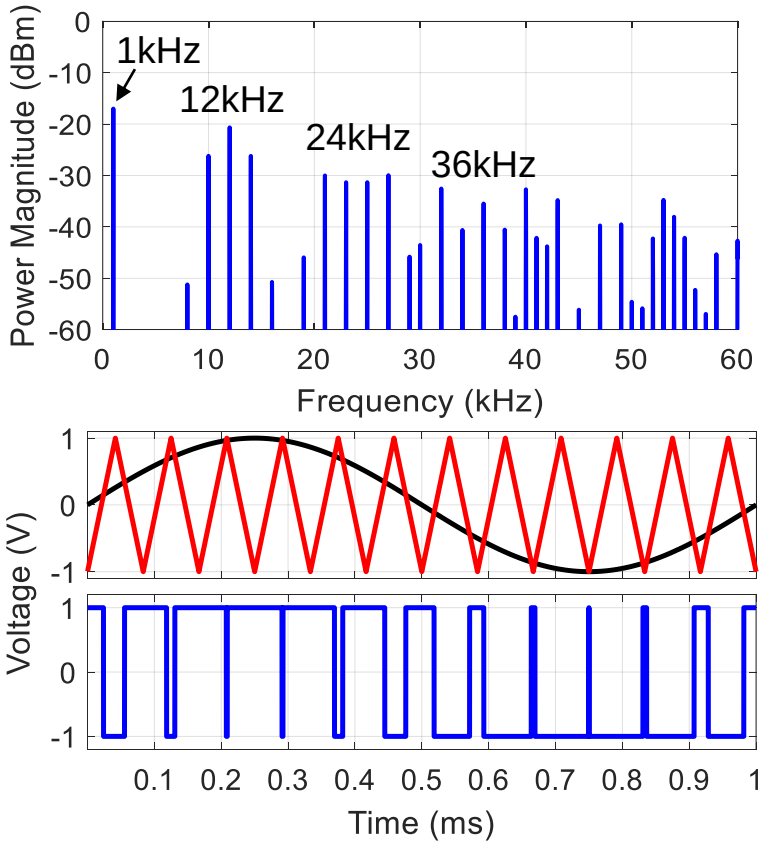
- Characteristics
  - Low power dissipation → High efficiency
  - Small heat sink → Small size
  - Distortion problem due to switching scheme

Spectrum of Class-D Output

- Verification condition:
  - Input sine wave: $V_m \sin 2\pi ft$, f=1kHz
  - Triangular wave: V_{pp}=2V, freq.=12kHz
- Square wave when V_m=0V

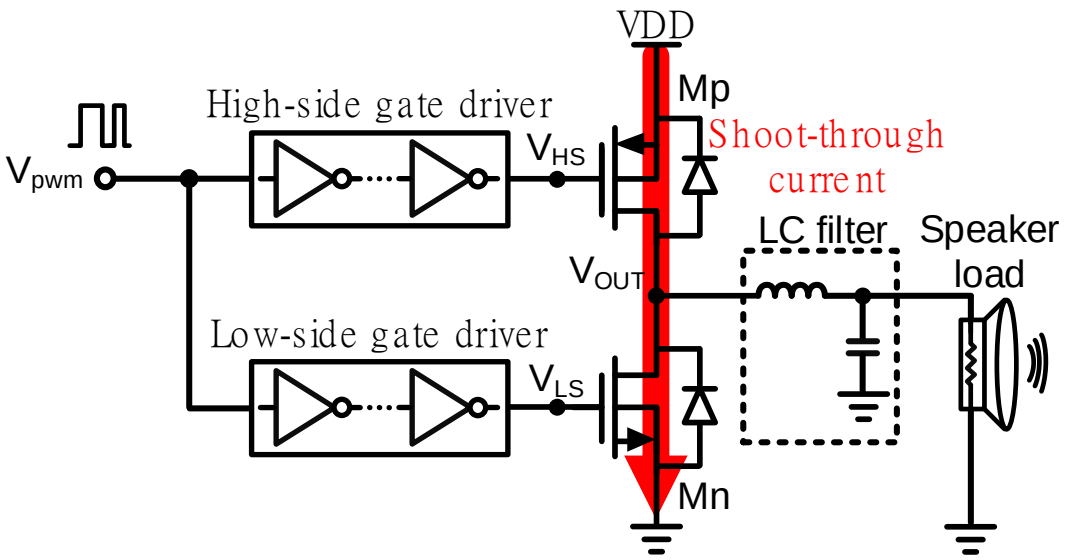


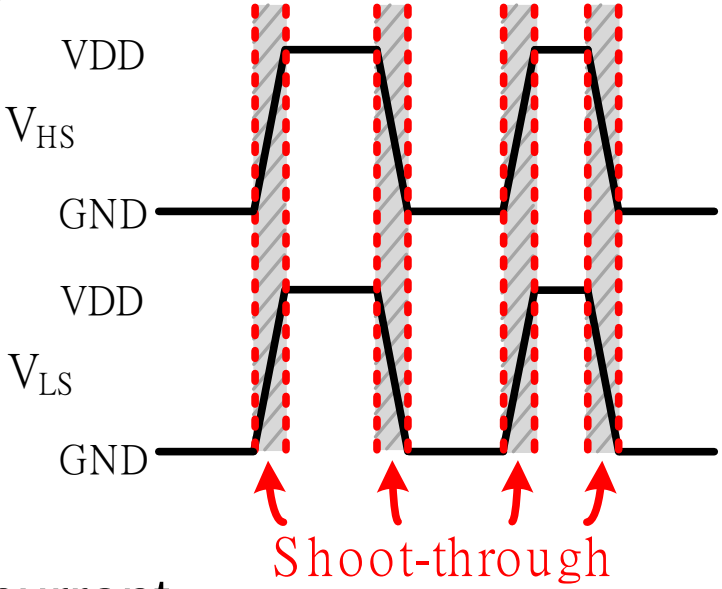
- PWM when $V_m \neq 0$V



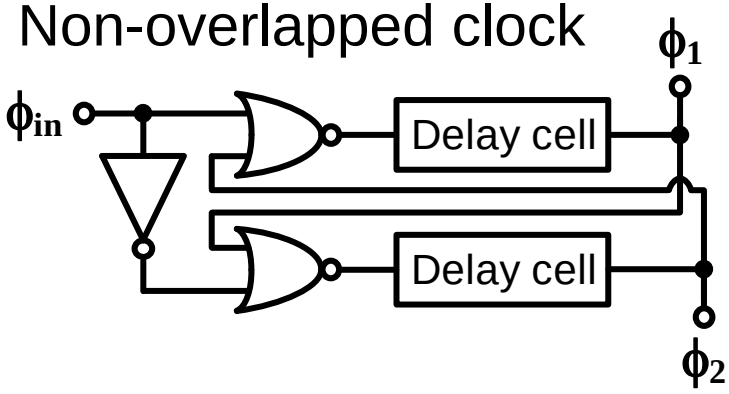
Shoot-through Current of Class-D Amplifier

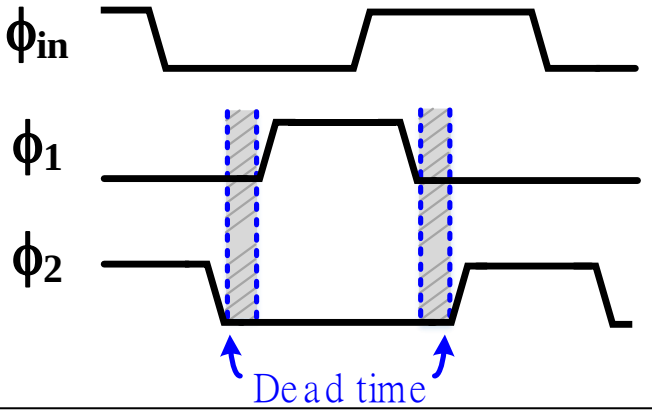
- Must be reduced due to large Mp and Mn
- Without dead time → large shoot-through current





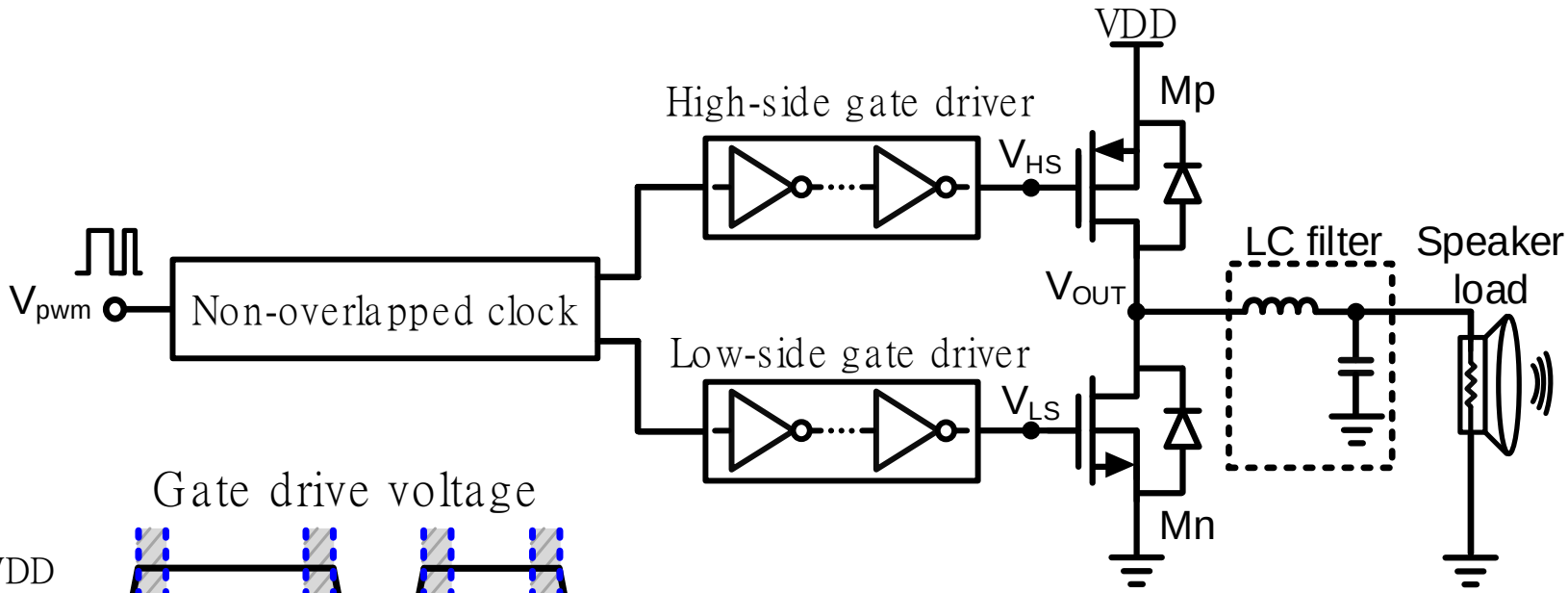
- With dead time → small shoot-through current
  - Non-overlapped clock

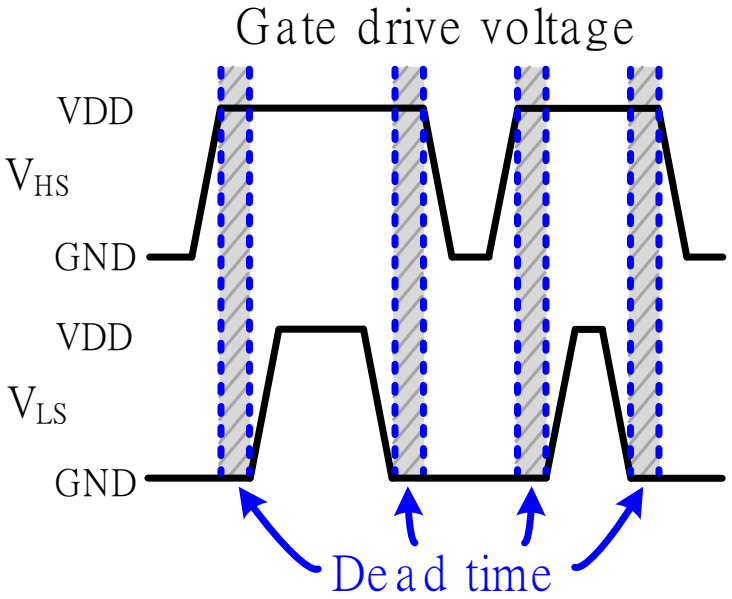




Shoot-through Current of Class-D Amplifier (cont.)

- Avoid Mp, Mn turn ON at the same time

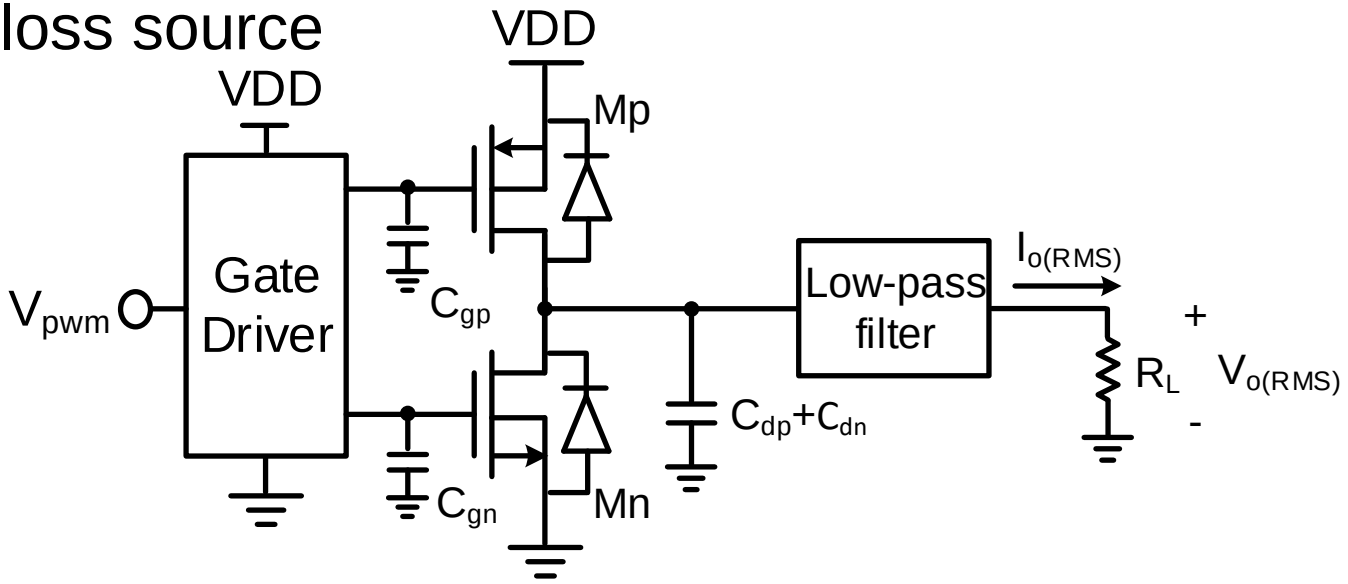




Both Mp, Mn turn OFF during dead time
→ Output waveform distortion

Efficiency of Class-D Amplifier

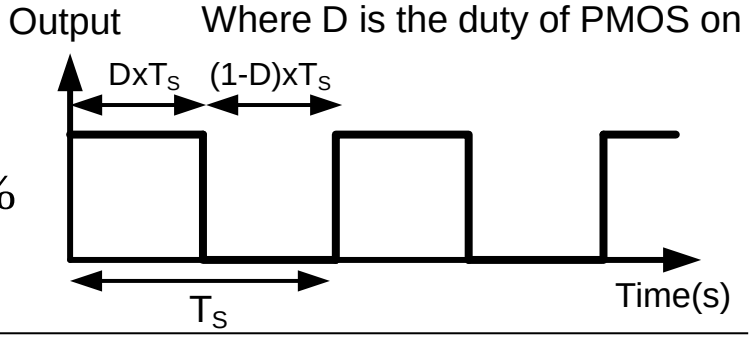
- Resistor load instead of capacitor load as in inverter
- Power loss source



  - Switching loss (P_{sw}): $P_{sw}=(C_{gp}+C_{dp}+C_{gn}+C_{dn})\times VDD^2 \times f_{sw}$
  - Conduction loss (P_{con}): $P_{con}=[D\times R_{on}(M_p)+(1-D)\times R_{on}(M_n)]\times I_{o(RMS)}^2$

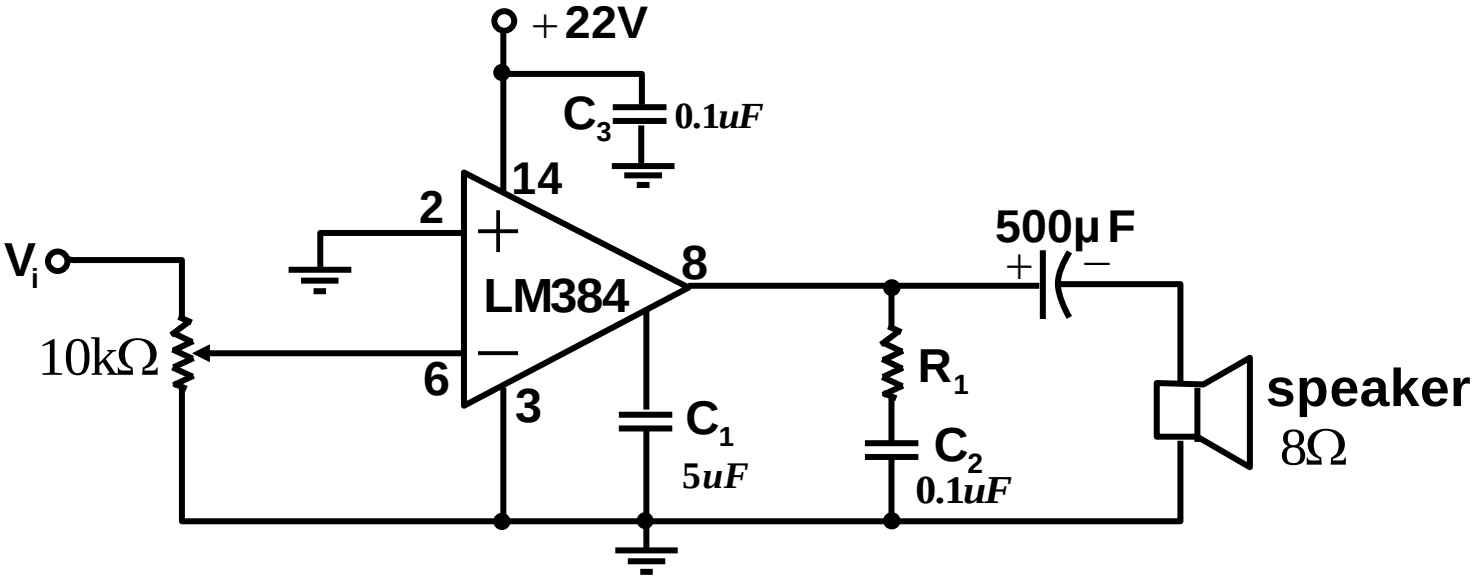
- Efficiency estimation

$$\eta = \frac{P_o}{P_i}\times 100\% = \frac{I_{o(RMS)}^{\ 2}\times R_L}{I_{o(RMS)}^{\ 2}\times R_L + P_{sw} + P_{con}}\times 100\%$$



Thermal Design Considerations

- IC power amplifier
  - Capable of delivering large power to external load
  - Example: a 5-W audio amplifier



  - The maximum possible power conversion efficiency is about 75% (Class-B or AB) i.e. for every 3-W output, 1W is dissipated within the amplifier.

Thermal Design Considerations (Cont.)

- $P_D \nearrow \rightarrow T \nearrow$

  $T > T_{J(max)} \rightarrow$ irreversible failure occurs

  where $T_{J(max)}$ is the maximum operating junction temperature of semiconductor device.

  - Thermal resistance θ_{JC} (between junction and case)

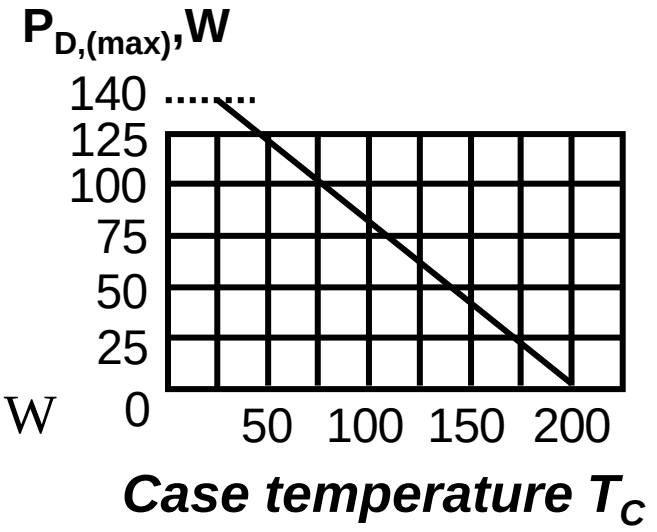
    $$T_J - T_C = \Delta T_{JC} = P_D \theta_{JC}$$

    unit: P_D :Watt θ:^{0}C/Watt

Dissipation Derating Curve

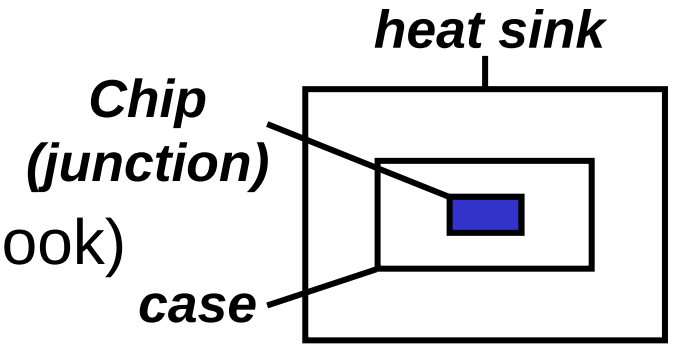
- Example : 2N5671 power transistor
  - Maximum allowable dissipation

    $P_{D(\max)} = 140\text{W}$
  - Dissipation derating curve



Thermal resistance: $\theta_{JC} = \dfrac{200-25}{140} = 1.25^0\,\text{C/W}$

Power derating factor $= \dfrac{1}{\theta_{JC}} = 0.8\,\text{W}/^0\text{C}$



- Example 11-7 and 11-8 (8th ed. textbook)

$$T_J = \Delta T_{JC} + \Delta T_{CS} + \Delta T_{SA} + T_A$$

Dissipation Derating Curve (Cont.)

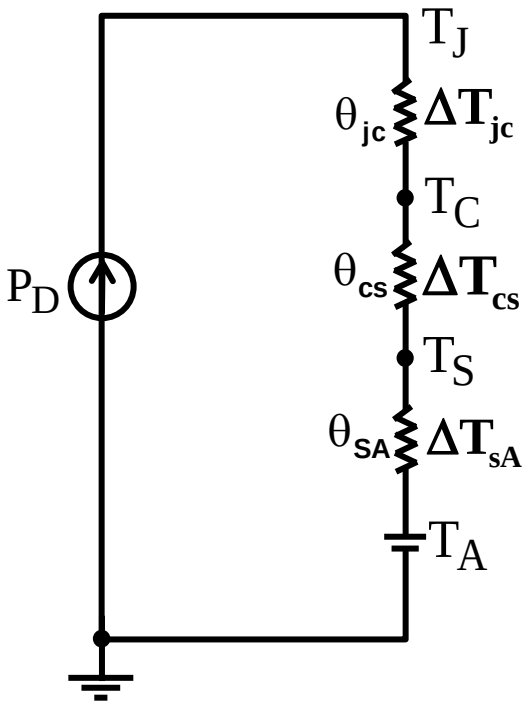
J: semiconductor device junction

C: case

S: heat sink

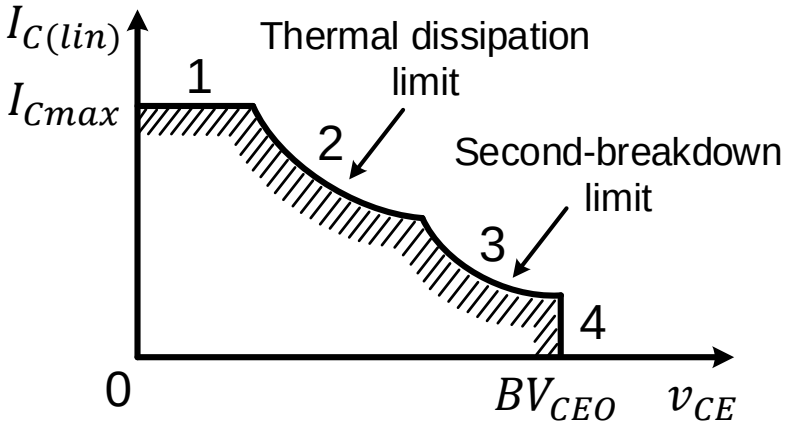
A: ambient

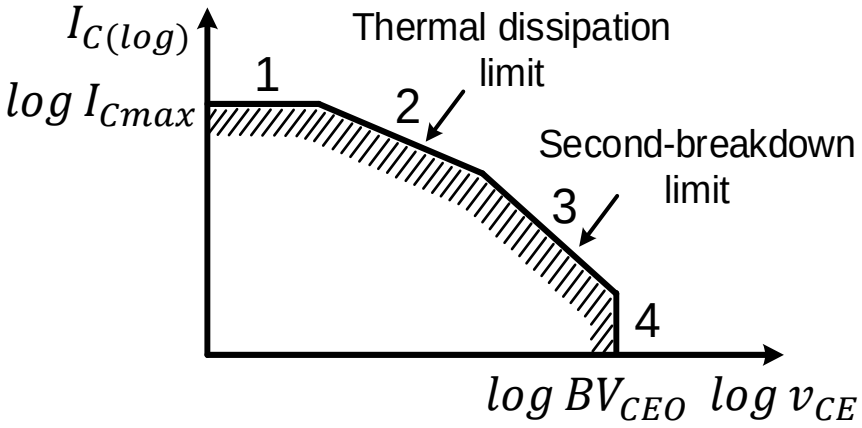
$$T_J = P_D(\theta_{JC} + \theta_{CS} + \theta_{SA}) + T_A$$



The BJT Safe Operating Area (SOA)

- SOA sketches



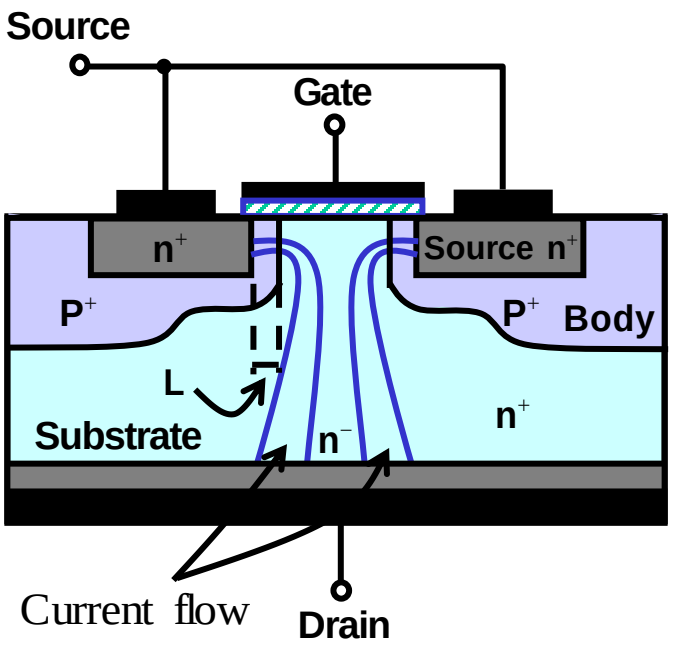


- Boundary on the sketches
  1. Maximum allowable current I_{Cmax}
  2. $v_{CE} i_C = P_{Dmax}$ (at T_{C0})
  3. "Current crowding" increases localized power dissipation and hence temperature (hot spots)
  4. Instantaneous value of v_{CE} never allowed to exceed BV_{CEO}

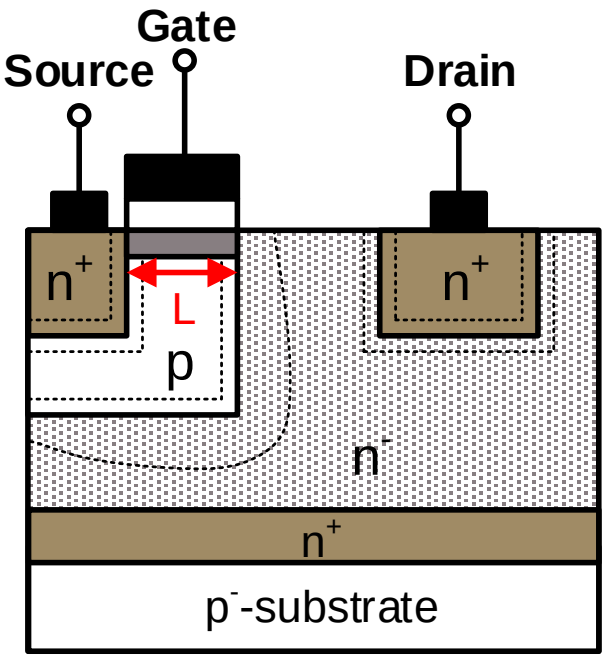
Power FET

- Example: DMOS (Double-diffused MOS)
  - Asymmetric source and drain
    S and D may not be interchanged

  – Conventional

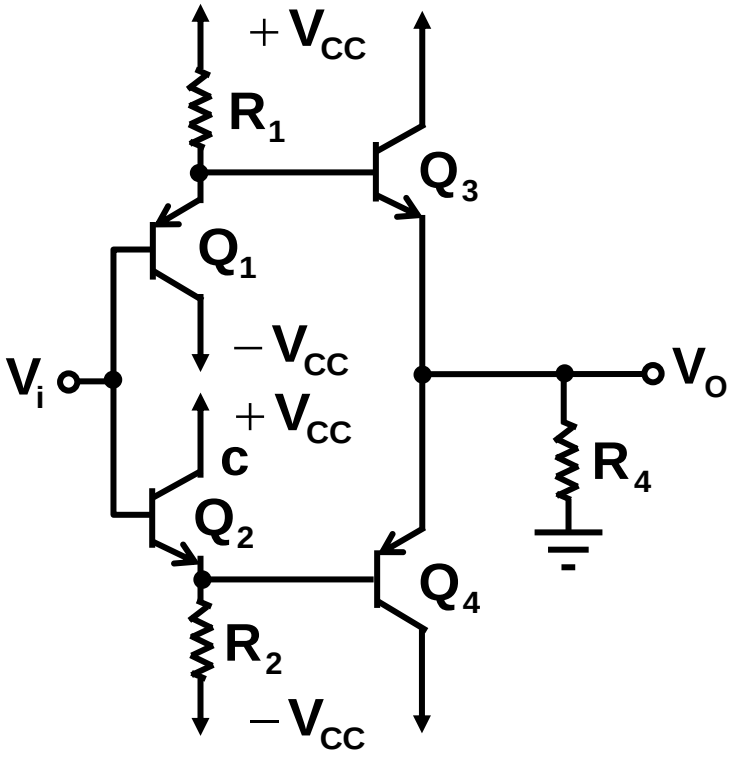


  – Currently popular



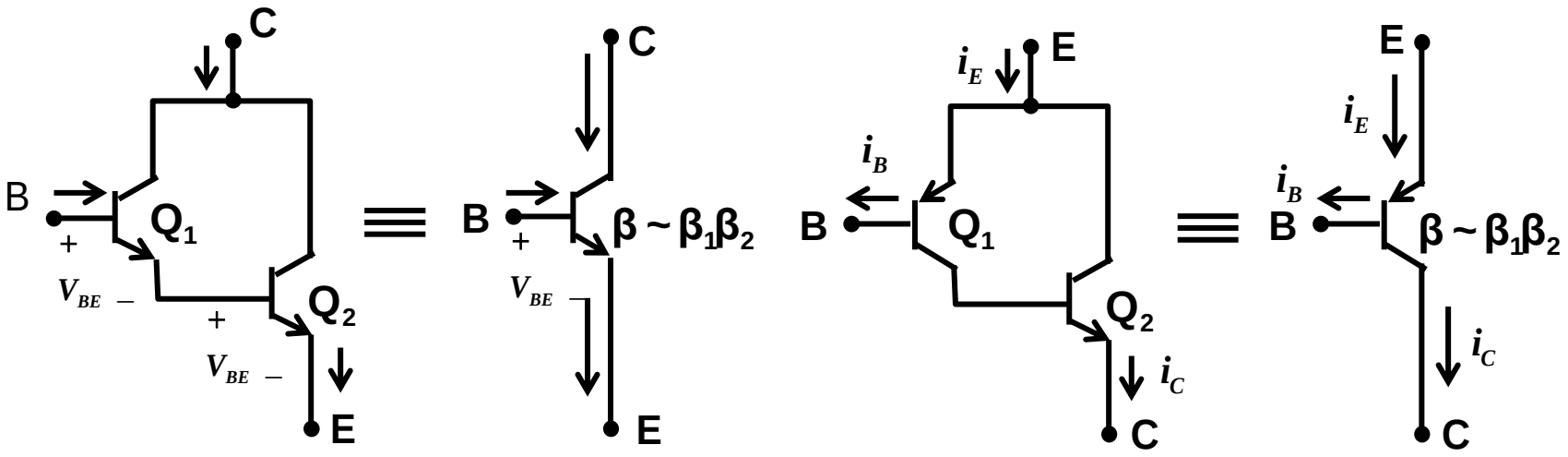
Variation on Class AB Configuration

- Use of input emitter followers
  - High input resistance
  - Quiescent current in Q_3 and Q_4 is equal to that in Q_1 and Q_2, if $R_L = \infty$ and $Q_1 \sim Q_4$ are identical



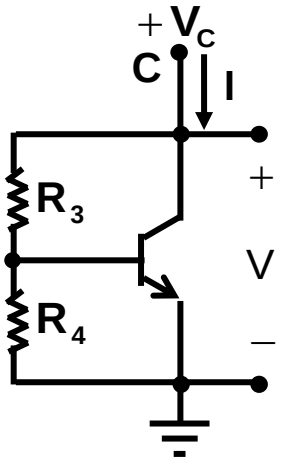
Compound Devices

- Darlington configuration
  1. Increase current gain
  2. Reduce base current drive
  3. Equivalent $V_{BE(eq.)} = 2V_{BE}$
  4. Can be used for both NPN and PNP transistors
- Compound PNP configuration
  1. Used to improve PNP configuration
  2. Q_1 is usually a lateral PNP having low β ($\approx 5-10$)



V_{BE} Multiplier

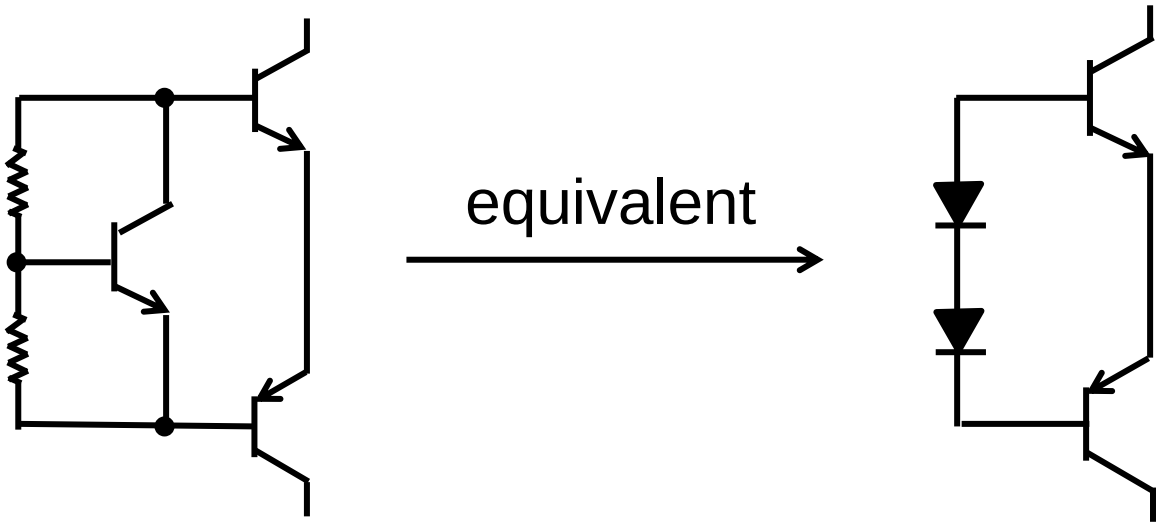
- Circuit



$$V = \frac{V_{BE}}{R_4}(R_3 + R_4)$$

$$= V_{BE}(1 + \frac{R_3}{R_4})$$

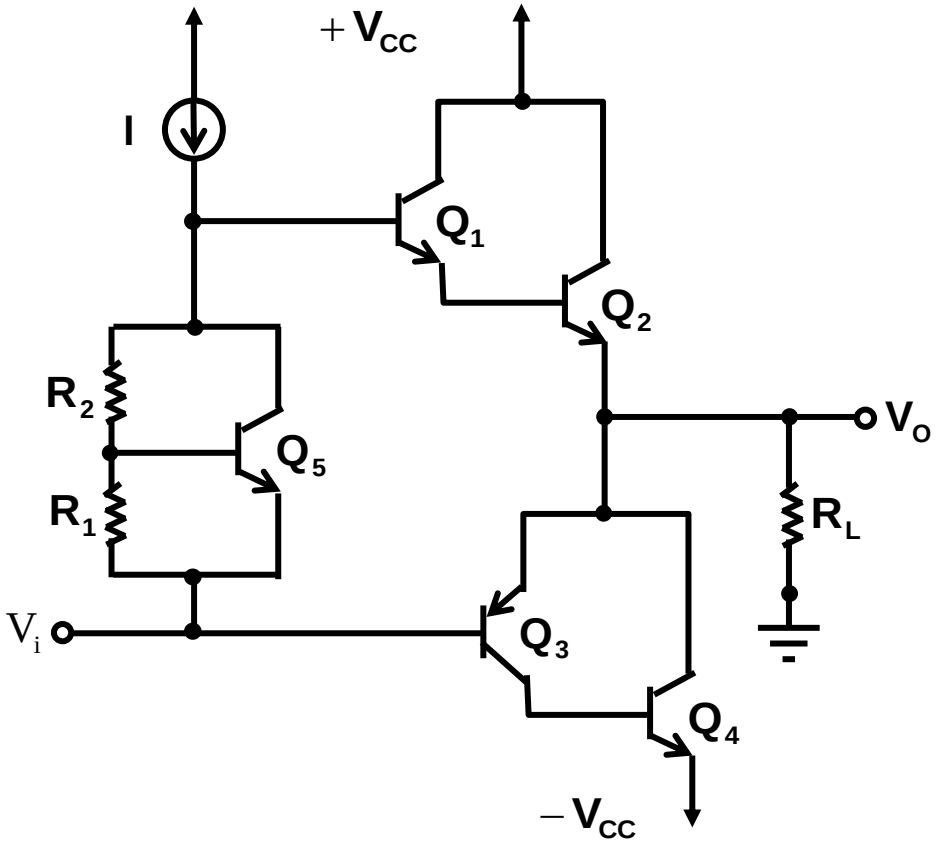
- Elimination of crossover distortion using V_{BE} multiplier



Class AB utilizing a Darlington NPN and a Compound

- Bias is obtained using a V_{BE} multiplier
- V_{BE} multiplier is required to provide $3V_{BE}$

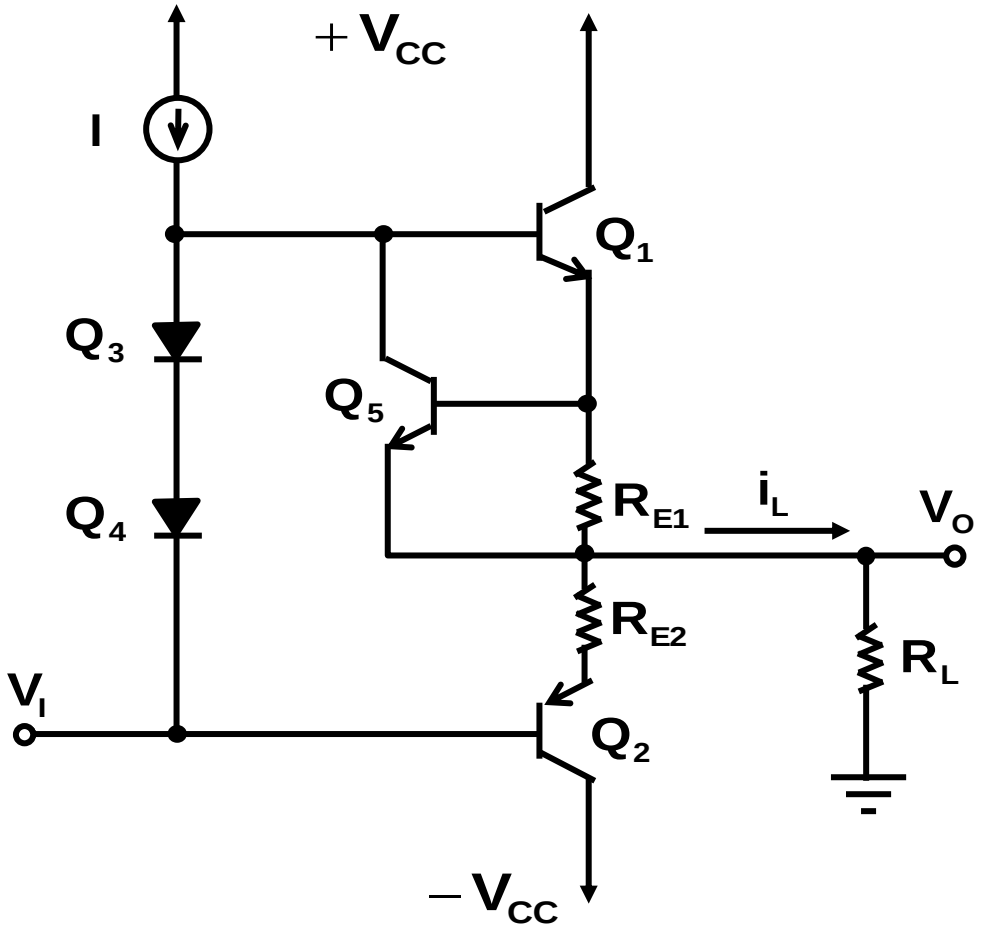
$$\frac{R_2}{R_1} = 2$$



Class AB utilizing a Darlington NPN and a Compound (Cont.)

- Short-circuit protection

$$i_L \uparrow \Rightarrow V_{BE5} \uparrow \Rightarrow I_{C5} \uparrow \Rightarrow I_{B1} \downarrow \Rightarrow I_{C1} \downarrow$$



Class AB utilizing a Darlington NPN and a Compound (Cont.)

- Thermal shutdown

$$T\uparrow \Rightarrow V_Z\uparrow,\ V_{BE}\downarrow \Rightarrow V_{R2}\uparrow \Rightarrow I_{C2}\uparrow$$

$\Rightarrow$ Q_2 absorbs bias current of OPAMP