Operational Amplifier (OPAMP)

• Analog ICs Include
  ◆ Operational Amplifier
  ◆ Filters
  ◆ Analog-to-Digital Converter (ADC)
  ◆ Digital-to-Analog Converter (DAC)
  ◆ Analog Modulator
  ◆ Phase-Locked Loop
  ◆ Analog Multiplier
  ◆ Others

• Basic Building Blocks of Analog ICs
  ◆ Single-Stage Amplifier
  ◆ Differential Pairs
  ◆ Current Mirrors
  ◆ MOS Switches
  ◆ Others
Operational Amplifier (Cont.)

● OPAMP design
  ◆ CMOS OPAMPs are adequate for VLSI implementation.
    ➢ Main stream
    ➢ Two-stage and folded-cascode OPAMPs will be introduced.
  ◆ Bipolar OPAMPs
    ➢ Can achieve better performance than CMOS OPAMPs.
    ➢ Less popular
    ➢ 741 OPAMP will be introduced.
  ◆ BiCMOS OPAMPs
    ➢ combine the advantages of bipolar and CMOS devices.
    ➢ Less popular
    ➢ First published by H. C. Lin in 1960’s.
CMOS Operational Amplifier (OPAMP)

- Two-stage
  I guess, it is suitable for 50% of applications with OPAMPs.
- Folded-cascode
  I guess, it is good for 20% applications.
- Others
Stability and Compensation of OPAMP

- Operational amplifier with negative feedback

\[ V_{in} = V_i + \beta V_{out} \]
\[ V_{out} = -A_v(s)V_{in} \]
\[ A_{vf}(s) = \frac{V_{out}(s)}{V_i(s)} = \frac{-A_v(s)}{1 + \beta A_v(s)} \]

Open-loop : always stable (no internal feedback)
Closed-loop : stability depends on $\beta A(s)$
Stability and Compensation of OPAMP (Cont.)

- For stable system, the real part of all poles must be negative.
  - Gain margin = \(20\log|\beta A_v(j\omega_{180})|\)
  - Unity-gain frequency \(\omega_u\)
  - Phase Margin = \(\angle \beta A_v(j\omega_u) + 180^\circ\)

At least 45\(^\circ\) ~ 60\(^\circ\) (or larger) margin is preferred. This will also give a desirable (i.e., small or no ringing) step response for the closed-loop amplifier.
CMOS Differential Stage with Active Load

- Used in CMOS technology
- Performs as a combination of differential gain stage and differential to single-ended converter
- Self-biased active load
  – Model of $A_{CM}$

\[
g_{m,Q1}, g_{m,Q2}, g_{m,Q3}, g_{m,Q4} \gg \frac{1}{r_{ds}}
\]

\[
r_{out} \approx r_{ds2} // r_{ds4}
\]

\[
A_{dm} \approx g_{m1} \left( r_{ds2} // r_{ds4} \right)
\]

\[
A_{cm} \approx \frac{1}{2} \frac{1}{r_{ds0}} \left( \frac{1}{g_{m3}} // \frac{1}{r_{ds1} // r_{ds3}} \right)
\]

\[
\approx \frac{1}{2g_{m3}r_{ds0}}
\]

\[
CMRR = \frac{A_{dm}}{A_{cm}} \approx 2g_{m1} \left( r_{ds2} // r_{ds4} \right) g_{m3} r_{ds0}
\]
CMOS Differential Stage with Active Load (Cont.)

- With external bias

Why not?

Quiescent point can’t be determined
Uncompensated Two-Stage CMOS OPAMP

\[ A(s) = \frac{A_0}{(1 - s/\omega_{p1})(1 - s/\omega_{p2})} \]

\[ A_0 = g_{m1}R_{01}g_{m6}R_{02} \]

\[ g_{m1} = \sqrt{2\mu\text{Cox}(W/L)_{M_1}I_1} \]

\[ g_{m6} = \sqrt{2\mu\text{Cox}(W/L)_{M_6}I_2} \]

\[ R_{01} = r_{ds2} // r_{ds4} \]

\[ R_{02} = r_{ds6} // r_{ds7} \]

\[ \omega_{p1} = -1/R_{01}C_1 \]

\[ \omega_{p2} = -1/R_{02}C_L \]

- P1 & P2 are dominant poles since \( R_{01} \) and \( R_{02} \) are normally large.
  The effects of other poles are usually negligible.
Uncompensated Two-Stage CMOS OPAMP (Cont.)

- For low frequency, \[ A(j\omega) = A(0) \]

For high frequency, \[ A(j\omega) \approx -\frac{g_m g_m}{\omega^2 C_1 C_L} \]

Hence, for high frequency, the amplifier inverts the input voltage. If feedback is used, then positive feedback occurs.

\[ V_{out} = -A_V(s)V_{in} \]

- Two dominant poles
  \[ \Rightarrow \text{phase margin is not large enough} \]
  \[ \Rightarrow \text{pole-splitting technique to solve this problem} \]
Offset Voltage of Two-Stage CMOS OPAMPs

- Input voltage needed to restore the output to zero
- Two components
  - Systematic offset
  - Random offset
- To avoid systematic offset, design must follow the rule

\[
\frac{(W/L)_{M3}}{(W/L)_{M5}} = \frac{(W/L)_{M4}}{(W/L)_{M5}}
\]

\[
= \frac{1}{2} \frac{(W/L)_{M6}}{(W/L)_{M7}}
\]

- To minimize random offset
  - \(L_1=L_2, W_1=W_2, L_3=L_4, W_3=W_4, L_3=L_6\) and \(L_5=L_7\) to minimize the offsets of channel length and channel width variations
  - Large \(L\) and \(W\) such that \(\Delta L/L\) and \(\Delta W/W\) can be ignored
Input Common-Mode Range and Output Swing of Two-Stage CMOS OPAM

- **Input common-mode range, \(V_{ICM}\)**
  - **Minimum \(V_{ICM}\)**
    
    To keep \(M_1\) and \(M_2\) in saturation, \(V_{gd1,2} < V_{tn}\). Hence,
    \[
    V_{ICM} \geq -V_{ss} + V_{tn} + V_{OV3} - |V_{tp}| \\
    \text{where } V_{ov} \text{ is effective or overdrive voltage}
    \]
  - **Maximum \(V_{ICM}\)**
    
    To keep \(M_5\) and in saturation, \(V_{ds5} > V_{ov5}\). Hence,
    \[
    V_{ICM} \leq V_{DD} - |V_{OV5}| - |V_{tp}| - |V_{OV1}|
    \]
    
    \[
    \Rightarrow V_{OV3} + V_{tn} - |V_{tp}| \leq V_{ICM} \leq V_{DD} - |V_{tp}| - |V_{OV1}| - |V_{OV5}|
    \]

- **Output swing, \(V_o\)**
  
  To keep \(M_6\) and \(M_7\) in saturation
  
  \[
  V_{OV6} \leq v_o \leq V_{DD} - |V_{OV7}|
  \]
Pole-Splitting of Two-Stage CMOS OPAMP

- reduce $P_1$ and increase $P_2$

$$A(s) = \frac{A_0(1 - s/\omega_Z)}{(1 - s/\omega_{P1})(1 - s/\omega_{P2})}$$

$$A_0 = g_{m1}R_{01}g_{m6}R_{02}$$

$$g_{m1} = \sqrt{2\mu\text{Cox}(W/L)_{M_1}I_1}$$

$$g_{m6} = \sqrt{2\mu\text{Cox}(W/L)_{M_6}I_2}$$

$$R_{01} = \frac{r_{ds2}}{r_{ds4}}$$

$$R_{02} = \frac{r_{ds6}}{r_{ds7}}$$

$$\omega_Z \approx \frac{g_{m6}}{C_C} \quad \text{If } g_{m6}R_{02} >> 1$$

$$\omega_{P1} = \frac{-1}{(1 + g_{m6}R_{02})C_CR_{01}} \approx \frac{A_0C_C}{g_{m1}} \quad \text{If } C_C & C_L >> C_1$$

$$\omega_{P2} = \frac{-g_{m6}C_C}{C_CLC_1CLC_C + C_CC_1} \approx \frac{-g_{m6}}{C_L}$$

$\Rightarrow$ Right plane zero causes slower gain drop but quick phase drop
Pole-Splitting of Two-Stage CMOS OPAMP (Cont.)

- Unity-gain frequency $f_t$ (or $f_u$)
  \[
  f_t = \left| A_0 \right| \frac{\omega_{p1}}{2\pi} = \frac{1}{2\pi} \frac{g_{m1}}{C_C}
  \]

- To achieve a uniform -20dB/dec gain rolloff down to 0dB, the following two conditions must be satisfied
  1. $f_t < f_{p2} \implies \frac{g_{m1}}{C_C} < \frac{g_{m6}}{C_2}$
  2. $f_t < f_z \implies g_{m1} < g_{m6}$
  where $G_{m1} = g_{m1}$ and $G_{m2} = g_{m6}$

- At unity-gain frequency $f_t$
  \[
  \Phi_{\text{total}} = \tan^{-1}(f_t/f_{p1}) + \tan^{-1}(f_t/f_{p2}) + \tan^{-1}(f_t/f_z), \text{ where } \tan^{-1}(f_t/f_{p1}) \approx 90^\circ
  \]
  Phase margin = $180^\circ - \Phi_{\text{total}} = 90^\circ - \tan^{-1}(f_t/f_{p2}) - \tan^{-1}(f_t/f_z)$
Right-Plane Zero

- Causes slower gain drop but quick phase drop
- Usually moved away if phase margin is not large enough

\[
\begin{align*}
\omega_p^2 & \approx -\frac{g_{m6}}{C_L} \\
\omega_p^1 & \approx -\frac{g_{m1}}{AC_C} \\
\omega_Z & \approx \frac{g_{m6}}{C_C}
\end{align*}
\]
Right-Plane Zero (Cont.)

- The zero is due to the existence of two paths through which the signal can propagate from node A to node B:
  1. through $C_C$
  2. through the controlled source $g_{m6} V_A$

- To eliminate zero $\omega_z$
  1. Method-1
  2. Method-2
Eliminating Right-Plane Zero

- Method-1: Using unity-gain buffer

Zero moves to infinity

\[ A(s) = \frac{A_0}{(1 - \frac{s}{\omega_{p1}})(1 - \frac{s}{\omega_{p2}})} \]

where \( \omega_{p1} \approx \frac{-g_{m1}}{A_0 C_C}, \omega_{p2} \approx \frac{-g_{m6}}{C_L} \)

or

unity gain buffer
Eliminating Right Plane Zero (Cont.)

- Method-2: Using R instead of buffer
  a. eliminating zero, let $R_z = \frac{1}{g_{m6}}$
  b. pole-zero cancellation, let $\omega_z = \omega_{p2}$

\[
\begin{align*}
\omega_{p1} & \approx -\frac{g_{m1}}{A_0 C_C} \\
\omega_{p2} & \approx -\frac{g_{m6}}{C_L} \\
\omega_{p3} & \approx -\frac{1}{R_z} \left( \frac{1}{C_C} + \frac{1}{C_1} + \frac{1}{C_L} \right) \\
\omega_z & = -\frac{1}{[R_z - \left( \frac{1}{g_{m6}} \right)] C_C}
\end{align*}
\]
Pole Separation vs. Phase Margin and Speed

\[ \omega_2 = n\omega_u = n\beta A_0 \omega_1 \quad \text{where} \quad \omega_u = \beta A_0 \omega_1 \]

- **n=2**
  - phase margin=63°
  - fast (step response)
- **n=3**
  - phase margin=71°
- **n=4**
  - phase margin=76°
  - critically damped (step response)
Slew Rate

- Discussed in chapter 2 of the textbook by Smith
- A unity-gain follower
  - Schematic

\[ v_o(t) = \frac{I}{C_C} t \]  where  \( I = I_{M5} \)

\[ SR = \frac{I}{C_C} \]

\[ g_{m1} = \frac{I}{V_{GS1} - V_{th}} = \frac{I}{V_{OV1}} \]

\[ SR = 2 \pi f_t V_{OV1} = \omega_t V_{OV1} \]
Power-Supply Rejection Ratio (PSRR)

Mixed-signal circuits combine analog and digital circuits
⇒ Switching activity in digital portion results in supply ripple
♦ Add large capacitors between supply rails and ground
⇒ not practical in IC design
♦ High-PSRR analog circuits

Definition
\[
\begin{align*}
PSRR^+ & \equiv \frac{A_d}{A^+}, \\
PSRR^- & \equiv \frac{A_d}{A^-}
\end{align*}
\]
, where
\[
\begin{align*}
A^+ & \equiv \frac{v_o}{v_{dd}} \\
A^- & \equiv \frac{v_o}{v_{gnd}}
\end{align*}
\]

For a two-stage op amp

➢ \[ v_o = v_{gnd} \frac{r_{o7}}{r_{o6} + r_{o7}} \]
⇒ \[ A^- = \frac{v_o}{v_{gnd}} = \frac{r_{o7}}{r_{o6} + r_{o7}} \]
⇒ \[ PSRR^- \equiv \frac{A_d}{A^-} = g_{m1} \left( \frac{r_{o2}}{r_{o4}} \right) g_{m6} r_{o6} \]

➢ It’s insensitive to \( V_{DD} \) ⇒ \( PSRR^+ \) is very high [Ref.]

Design Trade-offs

- To increase the differential gain, CMRR, and PSRR for a two-stage op amp
  - Enlarge the length L for the channel of each MOSFET
  - Lower the \(|V_{OV}|\) at which each MOSFET is operated

- The transition frequency of the MOSFETs can be increased by using a shorter channel and/or a larger \(|V_{OV}|\)

\[
f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \approx \frac{1.5 \cdot \mu \cdot |V_{OV}|}{2\pi L^2} \quad \text{where} \quad \begin{cases} 
\mu & \text{carrier mobility} \\
V_{OV} & \text{overdrive voltage} \\
L & \text{channel length}
\end{cases}
\]

- In conclusion, it’s a trade-off between low-frequency performance parameters and high-frequency ones
  ⇒ For analog circuits in submicron process operated at 1V~1.5V supplies, 0.1V~0.3V of \(|V_{OV}|\) is typically used, and the typical channel lengths are at least 1.5~2 times the \(L_{\text{min}}\)
Cascode CMOS and BiCMOS OPAMPs

- Cascaded two-stage CMOS OPAMP
  - most popular and works well with low capacitive load
  - problems
    - limited slew rate due to large $C_c$
    - limited bandwidth with large $C_L$
    - PSRR is reduced by pole-splitting

- If 1. low output resistance is not required, 2. high open-loop gain is required, and 3. large phase margin can be maintained with large $C_L$, then cascode configuration can provide attractive solutions for the above problems.

- Cascode CMOS OPAMP
  - Gain of two-stage OPAMP can be increased by adding gain stage in cascade.
    ⇒ phase shift is increased (i.e. PM↓)
  - Cascode configurations can be used to increase gain in the existing stage.
Cascode CMOS OPAMP

- Output resistance ($R_{O6}$) is increased
  \[ R_{O6} \approx (g_{m6} r_{ds6}) r_{ds8} \]
  \[ R_{O4} \approx (g_{m4} r_{ds4}) r_{ds2} \]
  \[ R_O = R_{O4} // R_{O6} \]
- Voltage gain $A_1 = -g_{m1} R_O$
  \[ \Rightarrow \text{Gain is increased.} \]
- Common-mode range is lowered and more transistors are stacked between the two power supplies.
  \[ \Rightarrow \text{Folded-cascode has large common-mode range} \]
- Cascode and folded-cascode OPAMPs are also named as “transconductance OPAMP” or “operational transconductance amplifier (OTA)”
Folded-Cascode CMOS OPAMP

- \( Q_3 \sim Q_8 \) are folded and connected to \(-V_{SS}\)
Folded-Cascode CMOS OPAMP (Cont.)

- $Q_9 \sim Q_{11}$ form externally-biased current sources
- $Q_6$ and $Q_7$ form self-biased current sources
Folded-Cascode CMOS OPAMP

• Input common-mode range
  Common-mode range is increased (compared with cascode OPAMPs). However, it is small compared with 2-stage OPAMPs
  \[ V_{OV11} + V_{OV1} + V_{tn} \leq V_{ICM} \leq V_{DD} - |V_{OV9}| + V_{tn} \]

• Output voltage swing
  \[ -V_{SS} + V_{OV7} + V_{OV5} + V_{tn} \leq v_o \leq V_{DD} - |V_{OV10}| - |V_{OV4}| \]

• Voltage gain
  \[ A = G_m R_o = g_{m1} R_o \]
  \[ R_o = \frac{R_{o4}}{R_{o6}} = \frac{[g_{m4} r_{ds4} (r_{ds2} // r_{ds10})]}{(g_{m6} r_{ds6} r_{ds8})} \]
Folded-Cascode CMOS OPAMP

- Frequency response
  - Bode plot
    \[ \omega_p \approx \frac{1}{R_0 C_L} \]
    \[ \omega_t \approx \frac{g_{m1}}{C_L} \]
  - The only high-impedance point is the output node.
    \[ \Rightarrow \text{Dominant pole is generated at the output node} \]
  - The resistance of all other node at level of 1/gm
    \[ \Rightarrow \text{Nondominant poles occur at all other nodes.} \]
    The 2nd pole is usually at the source of M3 and M4.
  - Nondominant poles are usually at frequencies beyond \( \omega_t \)
    \[ \Rightarrow \text{If } C_L \text{ is increased, then phase margin is increased.} \]
    \[ \Rightarrow \text{If } C_L \text{ is not large enough, it can be augmented.} \]
  - No frequency compensation is required
    \[ \Rightarrow \text{wide bandwidth} \]
- If \( I_B \geq I \), slew rate \( SR = I/C_L = 2\pi f_t V_{OV1} = \omega_t V_{OV1} \)
Folded-Cascode CMOS OPAMP (Cont.)

- Folded-cascode OPAMPs have high open-loop output resistance. It has been given the name operational transconductance amplifier (OTA).
- Its high output resistance (in the order of \( g_m r_o^2 \)) is far from that for an ideal OPAMP (which has zero output resistance).
- To alleviate this concern somewhat, let us find the closed-loop output resistance \( R_{of} \) of a unity-gain follower (\( \beta = 1 \)) formed by connecting the output terminal back to the negative input terminal:

\[
R_{of} = \frac{R_o}{1 + A\beta} = \frac{R_o}{1 + A} \approx \frac{R_o}{A} \quad \Rightarrow \quad R_{of} \approx \frac{1}{G_m}
\]

A general result applying to any OTA with 100% voltage feedback. For folded-cascode OPAMPs, \( G_m \approx g_{m1} \) \( \Rightarrow \) \( R_{of} \approx \frac{1}{g_{m1}} \)

- \( g_{m1} \) is in the order of 1mA/V, and \( R_{of} \) will be of the order 1kΩ. Although this is not very small it’s reasonable in view of the simplicity of the OPAMP circuit as well as the fact that this type of OPAMP (OTA) is not usually intended to drive low-valued resistive load.
Folded-Cascode with Rail-to-Rail Input Operation

- Increased input common-mode range, rail-to-rail or even larger
- Voltage gain, if $g_{m1}=g_{m3}=G_m$
  - $A = (g_{m1}+g_{m3})R_o = 2G_mR_o$ for middle $V_{ICM}$
  - $A = g_{m1}R_o$ for high $V_{ICM}$
  - $A = g_{m3}R_o$ for low $V_{ICM}$
Folded-Cascode with Wide-Swing Current Mirror

- Increased output voltage range
  - $V_{Omin} \geq V_{OV1} + V_{OV3} + V_{tn}$
  - $V_{Omin} \geq V_{OV1} + V_{OV3}$

\[ I_{REF} \quad \uparrow I_D \]
\[ Q_4 \quad 2V_t + 2V_{ov} \quad Q_3 \]
\[ V_t + V_{ov} \]
\[ Q_2 \quad V_t + V_{ov} \quad Q_1 \]

\[ I_{REF} \quad \uparrow I_D \]
\[ Q_4 \quad V_{BIAS} = V_t + 2V_{ov} \]
\[ V_{ov} \]
\[ Q_2 \quad V_t + V_{ov} \quad Q_1 \]

(a) (b)
Folded-Cascode with Wide-Swing Current Mirror (Cont.)

- Design example

\[ V_{\text{eff}2} = V_{\text{eff}3} = \sqrt{\frac{2I_{D2}}{\mu n C_{ox} (W/L)}} = V_{\text{eff}} \]

\( \therefore I_{D2} = \frac{\mu n C_{ox} W}{2} \frac{V_{\text{eff}}^2}{L} \)

Since

\[ \left( \frac{W}{L} \right)_2 = \left( \frac{W}{L} \right)_3 = (n+1)^2 \left( \frac{W}{L} \right)_5 = n^2 \left( \frac{W}{L} \right)_1 = n^2 \left( \frac{W}{L} \right)_4 \]

\[ V_{\text{eff}1} = V_{\text{eff}4} = nV_{\text{eff}} \]

\[ V_{G5} = V_{G4} = V_{G1} = (n+1)V_{\text{eff}} + V_{th} \]

\[ V_{DS2} = V_{DS3} = V_{G5} - V_{GS1} = V_{G5} - (nV_{\text{eff}} + V_{th}) = V_{\text{eff}} \]

\[ \Rightarrow V_{out} > V_{\text{eff}1} + V_{\text{eff}2} = (n+1)V_{\text{eff}} \]

- A common choice \( n = 1, \ V_{out} > 2V_{\text{eff}} \)
Folded-Cascode BiCMOS OPAMP

- Configuration

![Folded-Cascode BiCMOS OPAMP Diagram]
Folded-Cascode BiCMOS OPAMP (Cont.)

- The largest nondominant pole is usually generated at the emitter nodes of $Q_{1c}$ and $Q_{2c}$

$$\omega_{p2} \approx \frac{1}{R_{1c}C_{p1}} \approx \frac{g_{m1c}}{C_{p1}}$$

where

$$R_{1c} \approx R_{e1c}/r_{o(Q1c)}/r_{o(Q1)} \approx R_{e1c} = \frac{1}{g_{m1c}}$$

- The transconductance of BJT can be much larger than that of CMOS

$\Rightarrow \omega_{p2}$ can be increased

$\Rightarrow \omega_u$ can be increased while enough phase margin is maintained

$\Rightarrow$ wider bandwidth than that of CMOS folded-cascode OPAMP
741 OPAMP

- uses a large number of transistors but relatively few resistors and only one capacitor
  - R and C occupy large silicon area.
  - C need more fabrication steps
  - High-quality R&C are not easy to fabricate.

- Circuit Diagram in the next page.
741 OPAMP (Cont.)

$V_{cc} = 15V$

$V_{EE} = -15V$

$R_5 = 39k\Omega$

$R_4 = 5k\Omega$

$R_1 = 1k\Omega$

$R_3 = 50k\Omega$

$R_2 = 1k\Omega$

$R_9 = 50k\Omega$

$R_8 = 100\Omega$

$R_6 = 27\Omega$

$R_7 = 27\Omega$

$R_{11} = 50k\Omega$

$C_C = 30pF$

$Q_{12}$

$Q_{13A}$

$Q_{13B}$

$Q_{14}$

$Q_{15}$

$Q_{16}$

$Q_{17}$

$Q_{18}$

$Q_{19}$

$Q_{20}$

$Q_{21}$

$Q_{22}$

$Q_{23}$

$Q_{24}$
Basic Parts of 741 OPAMP

- Bias circuit
  - $I_{\text{ref}}$ is generated by $Q_{11}, Q_{12}, Q_{10}, R_4, Q_8, Q_9, Q_{13}$
  - double-collector PNP $Q_{13}$

- Current mirror

\[
\frac{I_y}{I_x} = \frac{A_{E(Q_y)}}{A_{E(Q_x)}} \quad \text{where } A_E \text{ is emitter area}
\]
Basic Parts of 741 OPAMP (Cont.)

- Short-circuit protection circuitry
  - $R_6, R_7, Q_{15}, Q_{21}, Q_{24}, Q_{22}$

- 741 OPAMP consists of 3 stages
  - input differential stage
  - single-ended high-gain stage
  - output-buffering stage

- Input stage
  - $Q_1 \sim Q_7, R_1 \sim R_3$
  - biased by $Q_8 \sim Q_{10}$ to provide high input impedance.
  - $Q_3 \& Q_4$ are lateral PNP (low $\beta$)
    - higher emitter-base junction breakdown than NPNs
      - protect input transistors $Q_1 \& Q_2$ when they are accidentally shorted to supply voltages.
  - $Q_5 \sim Q_7, R_1 \sim R_3$ provide high-resistance load and single-ended output.
Basic Parts of 741 OPAMP (Cont.)

- Second stage
  - $Q_{16}, Q_{17}, Q_{13}, R_8, R_9$
  - $Q_{16}$ acts as an emitter follower, thus giving
    - high input resistance
    - low base current if $R_9$ is large, hence low loading of the first stage.
  - $Q_{17}$: common emitter configuration
  - $Q_{13B}$: active load
  - $Cc$: Miller capacitor for pole-splitting compensation
    30pF area occupied is about 13 times that of a standard NPN transistor.

- Output stage
  - provide low output resistance
  - class AB
DC Analysis of 741 OPAMP

- Device parameters
  - Standard transistors
    - NPN: $I_S = 10^{-14} \text{A}$, $\beta = 200$, $V_A = 125 \text{V}$
    - PNP: $I_S = 10^{-14} \text{A}$, $\beta = 50$, $V_A = 50 \text{V}$
  - Nonstandard transistors $Q_{13}, Q_{14}, Q_{20}$
    1. $Q_{13} = Q_{13A} + Q_{13B}$
      - $Q_{13A}$: $I_{SA} = 0.25 \times 10^{-14} \text{A}$
      - $Q_{13B}$: $I_{SB} = 0.75 \times 10^{-14} \text{A}$
    2. $Q_{14} & Q_{20}$
      - $I_S = 3 \times 10^{-14} \text{A}$

- Reference bias current
  \[
  I_{REF} \approx \frac{V_{CC} - V_{EB12} - V_{BE11} - (-V_{EE})}{R_5}
  \]

- For $V_{CC} = -V_{EE} = 15 \text{V}$
  - $V_{BE11} = V_{BE12} \approx 0.7 \text{V}$
  - $I_{REF} \approx 0.73 \text{mA}$
Input Stage Bias

- Widlar current sources

  - Bipolar
    
    \[ V_{BE11} - V_{BE10} = I_{C10} R_4 \]
    
    \[ \Rightarrow V_T \ln \frac{I_{REF}}{I_{C10}} = I_{C10} R_4 \]
    
    \[ \Rightarrow \text{Trial and error to determine } I_{C10} \]
    
    \[ \Rightarrow I_{C10} = 19 \mu A \]

  - MOSFET

    \[ V_{OV11} = V_{OV10} + I_{D10} R'_4 \]
    
    \[ \text{assume } I_D = K \cdot V_{OV}^2 \Rightarrow \sqrt{\frac{I_{REF}}{K}} = \sqrt{\frac{I_{D10}}{K}} + \left( \sqrt{I_{D10}} \right)^2 \times R'_4 \]

    \[ \sqrt{I_{D10}} = \frac{-1}{K} \pm \frac{1}{K} + 4R'_4 \sqrt{I_{REF}} \]

    \[ \Rightarrow I_{D10} = \frac{1 + 2R'_4 \sqrt{K I_{REF}} - \sqrt{1 + 4R'_4 \sqrt{K I_{REF}}}}{2K(R'_4)^2} \]
Input Stage Bias (Cont.)

- Input differential circuitry

Let $I_{C1} = I_{C2} = I \Rightarrow I_{E3} = I_{E4} \approx I$

$$I_{B3} = I_{B4} = \frac{I}{1 + \beta_p} \approx \frac{I}{\beta_p}$$

$$I_{C9} = \frac{2I}{1 + \frac{2}{\beta_p}}$$

$$I_{C10} \approx 2I \Rightarrow I = 9.5 \mu A$$

$I_{C1} = I_{C2} \approx I_{C4} = 9.5 \mu A$

- $Q_1\sim Q_4, Q_8, Q_9$ form a negative feedback loop
  The feedback stabilize the value of $I$ (i.e. $I$ is kept unchanged and only controlled by $I_{C10}$)
Input Stage Bias (Cont.)

- Active load
  - $I_{C5} \approx I_{C6} \approx I$

\[
I_{C7} \approx I_{E7} = \frac{2I}{\beta_N} + \frac{V_{BE6} + IR_2}{R_3}
\]

\[
V_{BE6} = V_T\ln\frac{I}{I_S} = 517\text{mV}
\]

$\Rightarrow I_{C7} \approx 10.5\mu\text{A}$
Gain stage with resistor load (Cont.)

- **Resistor Load**

\[ A = g_m \left( \frac{R_0}{r_0} \right) \]
\[ \approx g_m R_0 \]
\[ \alpha \frac{I_c R_0}{V_T} \]

- **For High gain**
  - High \( I_c R_0 \)
  - High \( I_c R_0 \) means large voltage drop on \( R_0 \)
  - Large power supply

  - High \( R \) reduces speed
  - Use active loads to overcome the above problems.
Gain Stage with Active Load

- Transistor can provide large resistance if properly biased.

- Example

\[ A = g_m \left( \frac{r_{01}}{r_{02}} \right) \]
\[ \approx g_m \left( \frac{1}{2} r_0 \right) \]
\[ \frac{1}{2} I_C r_0 \]
\[ \frac{\alpha}{2} \frac{V_T}{r} \]

- I-V curve & load line
Input bias

- Input bias
  - Input current
    \[ I_{B1} = I_{B2} = \frac{I}{\beta_N} = \frac{9.5 \mu A}{200} = 47.5 \text{nA} \]
    \[ \Rightarrow \text{very small} \]

- Offset current and offset voltage are introduced in chapter 6

- Input common-mode range
  - In this range, the input stage remains in the linear active mode
  - This range is determined at the upper end by saturation of Q_1 and Q_2, and at the lower end by saturation of Q_3 and Q_4.
Second Stage Bias

- \( I_{C13} = 0.75I_{C12} \approx 0.75I_{REF} \approx 550\mu A \)
- \( I_{C17} \approx I_{C13B} = 550\mu A \)

\[
V_{BE17} = V_T \ln \frac{I_{C17}}{I_S} = 618 \text{ mV}
\]

\[
I_{C16} \approx I_{E16} = I_{B17} + \frac{I_{E17} R_8 + V_{BE7}}{R_9} \approx 16.2 \mu A
\]
Output Stage Bias

- If short-circuit protection circuitry is omitted

\[ I_{C13A} = 0.25 I_{REF} \approx 180 \mu A \]
\[ I_{B23} = \frac{180}{50} = 3.6 \mu A \]
\[ I_{C18} \approx I_{E18} = 180 - \frac{V_{BE18}}{R_{10}} \]
\[ \approx 180 - \frac{0.6}{40 \times 10^3} \approx 165 \mu A \]
\[ (V_{BE18} = 0.6V \text{ is assumed}) \]

\[ \Rightarrow V_{BE18} \approx 588mV \text{ (This is close to the value assumed)} \]
Output Stage Bias (Cont.)

\[ I_{C19} \approx I_{E19} = I_{B18} + I_{R10} = 0.8 \mu A + \frac{V_{BE18}}{R_{10}} \approx 15.5 \mu A \]

\[ V_{BE19} = V_T \ln \left( \frac{I_{C19}}{I_S} \right) = 530 \text{ mV} \]

\[ V_{BE18} + V_{BE19} = 588 \text{ mV} + 530 \text{ mV} = 1.118 \text{ V} \]

\[ V_T \ln \left( \frac{I_{C14}}{I_{S14}} \right) + V_T \ln \left( \frac{I_{C20}}{I_{S20}} \right) = 1.118 \text{ V} \]

\[ V_T \ln \left( \frac{I_{C14} I_{C20}}{I_{S14} I_{S20}} \right) = 1.118 \text{ V} \]

\[ \Rightarrow I_{C14} = I_{C20} = 154 \mu A \]
Small-Signal Analysis of 741 Input Stage

- Simplified ac schematic
  - For differential mode input, biases of Q₃ and Q₄ are at ac ground.

- Transconductance
  \[ \frac{V_{id}}{2} = V_1 + V_3 \]
  \[ V_1 g_{m1} \left( 1 + \frac{1}{\beta_1} \right) = V_3 g_{m3} \left( 1 + \frac{1}{\beta_3} \right) \]
Small-Signal Analysis of 741 Input Stage (Cont.)

\[
\frac{V_{id}}{2} = V_3 \left[ \frac{g_{m3} \left(1 + \frac{1}{\beta_3}\right)}{g_{m1} \left(1 + \frac{1}{\beta_1}\right)} + 1 \right]
\]

since \(|Ic_1| = Ic_3, g_{m1} = g_{m3}, \beta_1 = 200 \gg 1, \beta_3 = 50 \gg 1\)

\[
\Rightarrow V_3 = \frac{V_{id}}{4} \ldots (1)
\]

\[
i_{c3} = -\frac{g_{m3}V_{id}}{4}
\]

\[
i_{c4} = \frac{g_{m3}V_{id}}{4}
\]

\[
i_{out} = -i_{c4} + i_{c3} = -\frac{g_{m3}V_{id}}{2}
\]

\[
Gm1 = -\frac{i_{out}}{V_{id}} = \frac{g_{m1}}{2} = \frac{Ic_1}{V_T} \approx \frac{1}{5.26k\Omega}
\]
Small-Signal Analysis of 741 Input Stage (Cont.)

- **Input Resistance** $R_{id}$

\[
\begin{align*}
\text{From (1), } V_1 &= V_3 = \frac{V_{id}}{4} \\
R_{id} &= \frac{V_{id}}{i_i} = \frac{V_{id}}{(V_1 / r_{\pi_1})} = 4r_{\pi_1} = 4(\beta_1 + 1)r_e = 2.1M\Omega \\
\text{where } r_e &= \frac{V_T}{I_C} = \frac{25mV}{9.5\mu A} = 2.63K\Omega = \frac{1}{gm}
\end{align*}
\]
Small-Signal Analysis of 741 Input Stage (Cont.)

- Output resistance $R_{O1}$-simplified circuit

\[ R_{o4} = r_o(Q4)\left\{1+gm_4(r_e//r_\pi4)\right\} \approx 10.5\,\text{M}\Omega \]

\[ R_{o6} = r_o(Q6)\left\{1+gm_6(R_2//r_\pi6)\right\} \approx 18.2\,\text{M}\Omega \quad \text{where} \quad r_o = \frac{V_A}{I} \]

- Two-port equivalent circuit of input stage

$R_{o1} = R_{o4} // R_{o6} \approx 6.7\,\text{M}\Omega$
Small-Signal Analysis of the 741 Second Stage

- Simplified circuit

\[ R_{i17} = (\beta_{17} + 1)(r_{e17} + R_8) \]
\[ R_{i2} = (\beta_{16} + 1)(r_{e16} + (R_9//R_{i17})) \approx 4M\Omega \]

- Input resistance \( R_{i2} \)

\[ R_{i17} = (\beta_{17} + 1)(r_{e17} + R_8) \]
\[ R_{i2} = (\beta_{16} + 1)(r_{e16} + (R_9//R_{i17})) \approx 4M\Omega \]
Small-Signal Analysis of the 741 Second Stage (Cont.)

- Transconductance $G_{m2}$
  - Voltage gain of the emitter follower $Q_{16}$ is nearly unity.

\[
\begin{align*}
V_{i2} &= i_{b17} r\Pi_{17} + (i_{b17} + i_{C17}) R_8 = \frac{i_{C17}}{\beta_{17}} r\Pi_{17} + i_{C17} (1 + \frac{1}{\beta_{17}}) R_8 \\
&= i_{C17} \left[ \frac{1}{g_{m17}} + \left( 1 + \frac{1}{\beta_{17}} \right) R_8 \right] \approx i_{C17} \left( \frac{1 + g_{m17} R_8}{g_{m17}} \right) \\
\Rightarrow G_{m2} &= \frac{i_{C17}}{V_{i2}} \approx \frac{g_{m17}}{1 + g_{m17} R_8} \approx 6.5 \text{mA/V}
\end{align*}
\]
Small-Signal Analysis of the 741 Second Stage (Cont.)

- **Output Resistance**
  - \( R_{o2} = R_{o17} // R_{o13B} \)
  - \( R_{o13B} = r_o(Q13B) \)
  - \( R_{o17} \approx r_o(Q17) [1 + gm_{17}(R_8 // r_{\pi17})] \)
  - \( R_{o2} = R_{o17} // R_{o13B} \approx 787\,\text{k}\Omega // 90.9\,\text{k}\Omega \approx 81\,\text{k}\Omega \)
741 Output Stage

- Output voltage limits
  - $V_{omax} = V_{CC} - |V_{CE13A(sat)}| - V_{BE14}$
  - $V_{omin} = -V_{EE} + V_{CE17(sat)} + V_{EB23} + V_{EB20}$

- Class AB stage

---

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Electronics(3), 2012
Small-Signal Analysis of the 741 Output Stage

- Simplified circuit for positive $V_o$, $V_{BE14} > V_{EB20}$

(a) $V_{CC}$ $Q_{19}$ $Q_{18}$ $Q_{20}$ $Q_{23}$ $V_{EE}$ $R_L$

(b) $r_{o13A}$ $r_{d19}$ $r_{d18}$ $Q_{14}$ $R_L = 2k\Omega$

(c) $R_{eq4}$ $r_{o13A}$ $r_{d19}$ $r_{d18}$ $Q_{14}$ $R_{O14}$

$R_{eq3}$ $Q_{23}$ $R_{i3}$ $R_{O23}$

$R_{o2} = 81K\Omega$

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Small-Signal Analysis of the 741 Output Stage (Cont.)

- **Input Resistance $R_{i3}$**
  - For positive $V_o$ with $Q_{20}$ neglected ($Q_{14}$ conducts more current)
    \[
    R_{i14} = r_{\pi 14} + (1 + \beta_{14}) R_L \\
    R^+_{eq3} = r_{d18} + r_{d19} + (r_o(Q_{13A})/R_{i14}) \text{ where } r_{d18} + r_{d19} \text{ is very small.} \\
    R^+_{i3} = r_{\pi 23} + (1 + \beta_{23} R^+_{eq3}
    \]
  - For negative $V_o$ with $Q_{14}$ neglected ($Q_{20}$ conducts more current)
    \[
    R_{i20} = r_{\pi 20} + (1 + \beta_{20}) R_L \\
    R^-_{eq3} = r_{d18} + r_{d19} + r_o(Q_{13A}) \text{ where } r_{d18} + r_{d19} \text{ is very small.} \\
    R^-_{i3} = r_{\pi 23} + (R^-_{eq3}/R_{i20})
    \]
  - Actual $R_{i3}$ is between $R^+_{i3}$ and $R^-_{i3}$
Small-Signal Analysis of the 741 Output Stage (Cont.)

- Output Resistance $R_{out}$
  - For positive $V_o$ with $Q_{20}$ neglected
    \[ R_{out}^+ \approx R_{o14} \]
    \[
    R_{eq4} = r_o(Q_{13A}) \parallel \left[ r_{d19} + r_{d18} + r_{e23} + \frac{R_{o2}}{1 + \beta_{23}} \right]
    \]
    \[
    R_{o14} = r_{e14} + \frac{R_{eq4}}{1 + \beta_{14}}
    \]
  - For negative $V_o$ with $Q_{14}$ neglected
    \[ R_{out}^- \approx R_{O20} \]
    \[
    R_{O23} = r_{e23} + \frac{R_{O2}}{1 + \beta_{23}}
    \]
    \[
    R_{O20} = r_{e20} + \frac{R_{eq3} \parallel R_{O23}}{1 + \beta_{20}}
    \]
  - Actual $R_{out}$ is between $R_{out}^+$ and $R_{out}^-$
Small-Signal Analysis of the 741 Output Stage (Cont.)

- Small-signal equivalent circuit model

\[ \mu = \frac{R_{i3}}{R_{i3} + R_{O2}} \approx 0.978 \]
Gain and Frequency Response of the 741 OPAMP

- Equivalent circuit of the 741 OPAMP

\[ V_o = \frac{V_{i2}}{V_i} \times \frac{V_{o2}}{V_{i2}} \times \frac{V_o}{V_{o2}} \]

\[ = \left[-G_{m1}(R_{o1} \parallel R_{i2})\right] \times \left[-G_{m2}R_{o2}\right] \times \mu \frac{R_L}{R_{out} + R_L} \]

\[ \approx 107.7 \text{dB} \]
Gain and Frequency Response of 741 OPAMP (Cont.)

- Frequency Response
  - 741 is an internally compensated OPAMP
  - Miller Compensation

\[
\begin{align*}
C_i &= C_c (1 + |A_2|) \quad \text{--- Miller theorem} \\
A_2 &= -Gm_2 R_{O2} \left( \frac{R_{i3}}{R_{O2} + R_{i3}} \right) = -526.5 \times 0.978 \approx -515 \\
\implies C_i &\approx 30 \text{ pF} = C_c \times (1 + |-515|) = 15,480 \text{ pF}
\end{align*}
\]
Gain and Frequency Response of 741 OPAMP (Cont.)

- Neglecting the parasitic capacitance at the base of Q\textsubscript{16}
- Total resistance at this node \( R_t = \left( R_{O1} / R_{i2} \right) \)
  \( \Rightarrow \) Dominant pole \( f_p = \frac{1}{2\pi R_t C_i} \approx 4.1 \text{Hz} \)
- Bode plot (Neglecting nondominant poles)

\[
|A|, \text{dB} = 107.7 \text{dB}
\]

\[ f_{3dB} \approx 4.1 \text{Hz} \quad f_t = A_0 f_{3dB} = 1 \text{MHz} \]

- 3dB bandwidth \( f_{3dB} = f_p = 4.1 \text{Hz} \)
- Unity-gain bandwidth \( f_t = A_0 f_{3dB} = 1 \text{MHz} \)
Gain and Frequency Response of 741 OPAMP (Cont.)

- Simplified model
  - model the 2nd stage as an integrator

\[ A(s) = \frac{V_O(s)}{V_i(s)} = \frac{Gm_1}{sCC} \Rightarrow A(j\omega) = \frac{Gm_1}{j\omega CC} \]

\[ |A(j\omega)| = 1 \Rightarrow \omega t = \frac{Gm_1}{CC} \]

For \( Gm_1 = \frac{1}{5.26k\Omega} \) and \( CC = 30PF \), 
\[ f_t = \frac{\omega t}{2\pi} \approx 1MHz \]
( equal to the value calculated before)
Slew Rate

- Large signal behavior
- Output voltage slew limitation

\[ \frac{dV}{dt} \bigg|_{\text{max}} = \text{slew rate} = \frac{2I}{C_c} \]

\[ f_t = \frac{G_{m1}}{2\pi C_c} \quad \text{(as shown previously)} \]

\[ \Rightarrow \text{slew rate} = \frac{4\pi I_c}{G_{m1}} f_t \]

\[ G_{m1} = \frac{I_c}{2V_T} \]

\[ \text{slew rate} = 8\pi V_T f_t \]
Effect of Slew Rate (Cont.)

- Effect of slew rate on an unity-gain follower

\[ V_o = V_i = V_m \sin \omega_i \]

\[ \frac{dV_o}{dt} = \omega V_m \cos \omega t \quad ; \quad \left. \frac{dV_o}{dt} \right|_{\text{max}} = \omega V_m \]

Let \( V_m = V_{DD} \), then \( f = \frac{\text{slew rate}}{2\pi V_{DD}} \) is called full-power bandwidth.
Effect of Slew Rate (Cont.)

- for small-amplitude sinusoidal signal

\[ \frac{dv_o}{dt} \leq \text{slew rate limitation} \]

- for large-amplitude sinusoidal signal

\[ v_o \] without slew rate limitation

\[ v_o \] with slew rate limitation
Two-Stage CMOS OPAMP

- **Topology**

- **Voltage gain**

- **Frequency response (以上参考之前授課内容)**
Two-Stage CMOS OPAMP (Cont.)

- **Slew rate**
  
  \[
  \text{SR} = \frac{2I}{C_c} ; \quad \omega_t = \frac{G_{m1}}{C_c} = \frac{2I}{(V_{GS} - V_t)C_c}
  \]
  
  \[\Rightarrow \text{SR} = (V_{GS} - V_t)\omega_t \quad \text{for CMOS OPAMP} \]
  
  \[\text{(SR} = 4V_T \omega_t \quad \text{for BJT OPAMP}) \]
  
  \[(V_{GS} - V_t) \text{ is usually larger than } 4V_T \]
  
  \[\Rightarrow \text{For the same } \omega_t , \text{ CMOS OPAMPs exhibit higher slew rate than BJT OPAMPs} \]
  
  \[\text{(i.e. for the same slew rate, } \omega_t(\text{BJT}) > \omega_t(\text{CMOS}) \) \]

- **G_m reduction method**

  \[\text{SR}_{\text{BJT}} = 4V_T\omega_t = \frac{I}{G_{m1}}\omega_t \]

  \[\text{SR}_{\text{CMOS}} = (V_{GS} - V_t)\omega_t = \frac{I}{G_{m1}}\omega_t \]

  For a given \( \omega_t \), a higher SR can be obtained by making \( G_m \) smaller while bias current \( I \) is kept constant.
Modern Techniques for the BJT Op Amps

- Reasons for single-supply operation with much lower $V_{CC}$
  - Meet modern small-feature-size fabrication technologies
  - Be compatible with other low-power-supply systems
  - Minimize the power dissipation, $P = I_{VDD} \cdot V_{DD}$, especially for battery-operated systems

For a low-voltage single-supply system, rail-to-rail input common-mode range may be required because of its inherent low supply voltages.

$V_{CC} = +15 \text{ V}$

$-V_{EE} = -15 \text{ V}$

$V_{CC} = 3 \text{ V}$
Rail-to-Rail Input Common-Mode OPAMP

Bias circuit

Input stage

Cascode stage with Common-Mode Feedback (CMF)
Bias Design

- Widlar current source

\[ V_{BE1} = V_T \ln \left( \frac{I}{I_{S1}} \right) \]

\[ V_{BE2} = V_T \ln \left( \frac{I}{I_{S2}} \right) \]

\[ V_{BE1} - V_{BE2} = V_T \ln \left( \frac{I_{S2}}{I_{S1}} \right) = I \times R_{2b} \]

\[ I = \frac{V_T}{R_{2b}} \ln \left( \frac{I_{S2}}{I_{S1}} \right) \]

- \( I \) is independent of \( V_{CC} \)
- \( I \) is directly PTAT, proportional to absolute temperature.

Mirrored transistors’ \( g_m = \frac{I}{V_T} \) are independent of temperature.
**Input Stage Design**

- with active load
  \[ V_{EC1} > |V_{ECsat}| \approx 0.1 \, V \]
  \[ V_{ICM\,min} = V_{C1} - 0.6 = V_{BE3} - 0.1 = 0.1 \]

- with passive load
  - \( V_{ICM\,min} = V_{Rc} - 0.6 \)
    
    if \( V_{Rc} \) is selected to \( 0.2V \sim 0.3V \)
    
    \( \rightarrow V_{ICM\,min} \) will be \(-0.4V \sim -0.3V\)
  
  - Differential gain is degraded

\[
A = -g_{m1,2}R_C = -\frac{I/2}{R_C}R_C = -\frac{V_{Rc}}{V_T}
\]

- \( V_{ICM\,max} = V_{CC} - |V_{ECsat}| - V_{EB1} \)
  
  \[= V_{CC} - 0.1 - 0.7 = V_{CC} - 0.8 \]
Input Stage Design (cont.)

- Assume that $V_{RC} = 0.3V$
  - For pnp differential-pair (previous page)
    - $-0.3 \leq V_{ICM} \leq V_{CC} - 0.8$
  - For npn differential-pair (right figure)
    - $0.8 \leq V_{ICM} \leq V_{CC} + 0.3$
- Connecting the two circuits in parallel
  - A rail-to-rail $V_{ICM}$ range
    - $-0.3 \leq V_{ICM} \leq V_{CC} + 0.3$
  - For the overlap region $0.8 \leq V_{ICM} \leq V_{CC} - 0.8$, both pnp and npn circuits are active
    - Higher effective trans-conductance (X2) → higher gain
- Adding a folded-cascode stage can also increase gain
Common-Mode Feedback (CMF)

- Without CMF
  
two mismatched BJT-pairs, i.e. \((Q_9 - Q_{10})\) and \((Q_7 - Q_8)\)
  
  → an increment \(\Delta I\) will be multiplied by large \(R_{out}\)
  
  → large changes at \(v_{o1}\) & \(v_{o2}\)
  
  → one set of BJT-pair saturates

- With CMF
  
  ◆ It ensures \(Q_{7,8}\) remain active
  
  ◆ \(V_{CM}\) is regulated
  
  if \(V_{CM}\uparrow \Rightarrow V_B \uparrow \Rightarrow I_{7,8} \uparrow \Rightarrow V_{CM}\downarrow\)
CMF Circuit Configuration

\[ V_{CM} = \frac{v_{o1} + v_{o2}}{2} \]

\[ v_{o1} = V_{CM} + \frac{v_d}{2} \]

\[ v_{o1} = V_{CM} - \frac{v_d}{2} \]

\( Q_{11} \sim Q_{14} \) act as emitter followers

\[ V_E = V_{CM} + V_{EB11,12} - V_{EB13,14} \]

\[ \approx V_{CM} \]

\[ \Rightarrow V_B = V_E + V_D = V_{CM} + 0.4 \]

\( V_D \): Voltage drop of Schottky barrier diode